Development Tools For Full Digital Power Supply

MICROCHIP

A Leading Provider of Smart, Connected and Secure Embedded Solutions

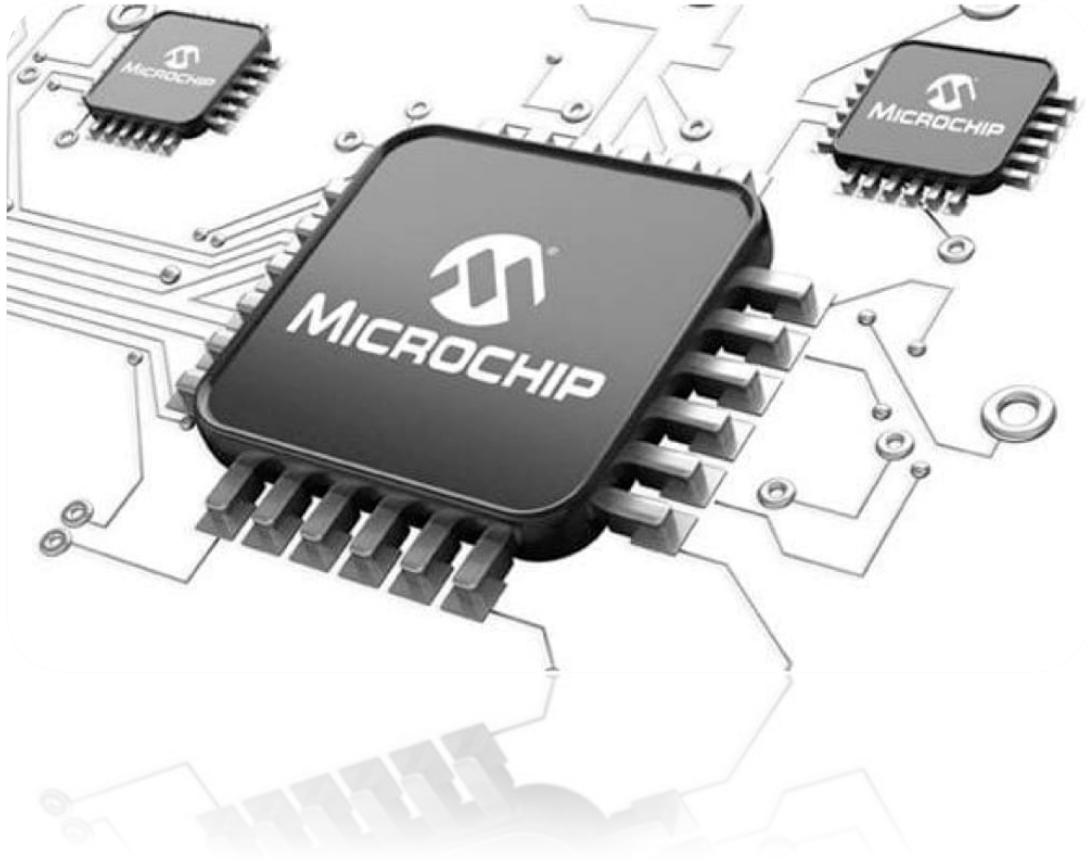
Edward Lee

Dec. 2nd, 2021

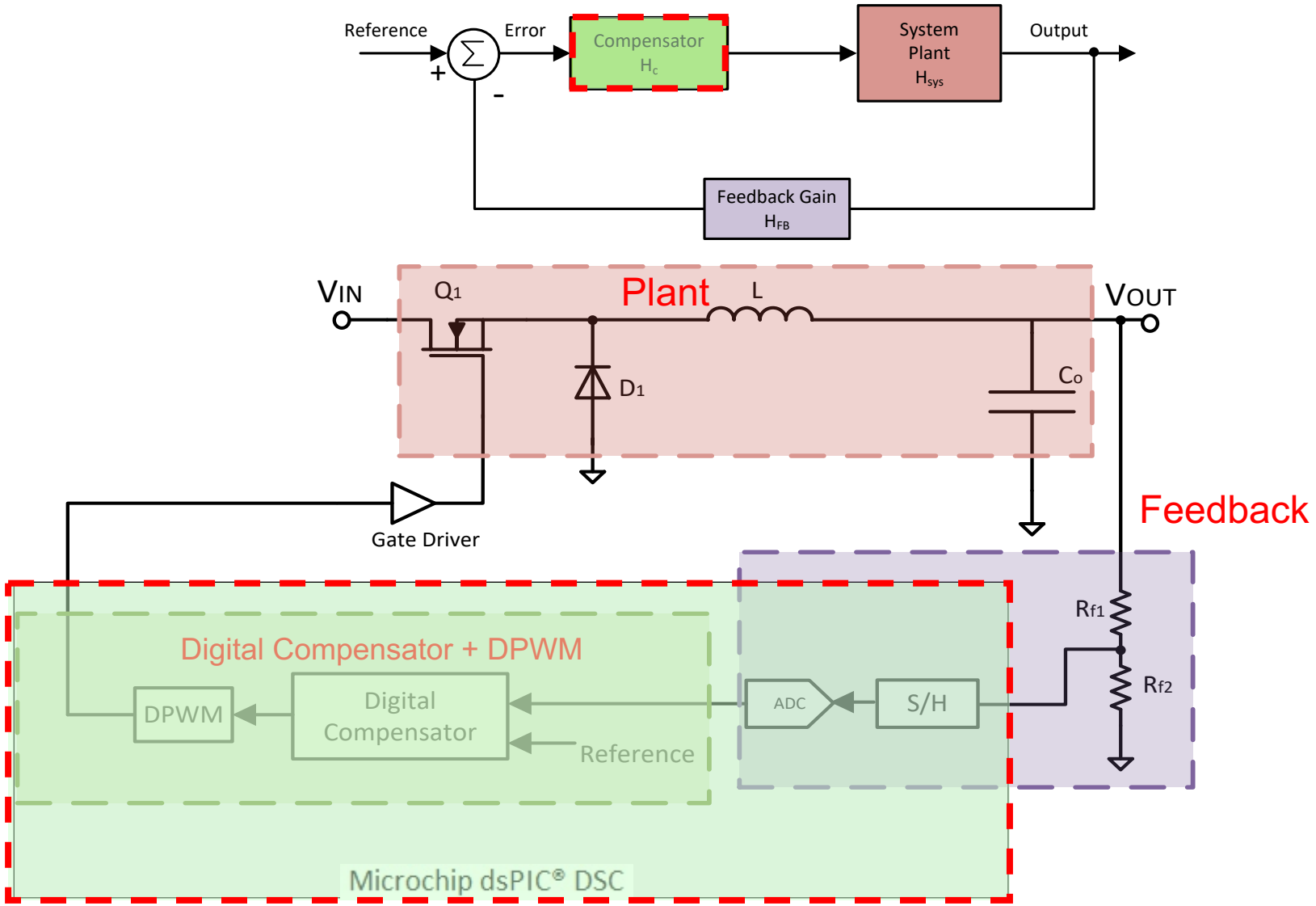
SMART | CONNECTED | SECURE

Agenda

- dsPIC33 vs. Full Digital Power
- Digital Power Development Tools
- Programing
- Digital Power Reference Design
- Other Resources

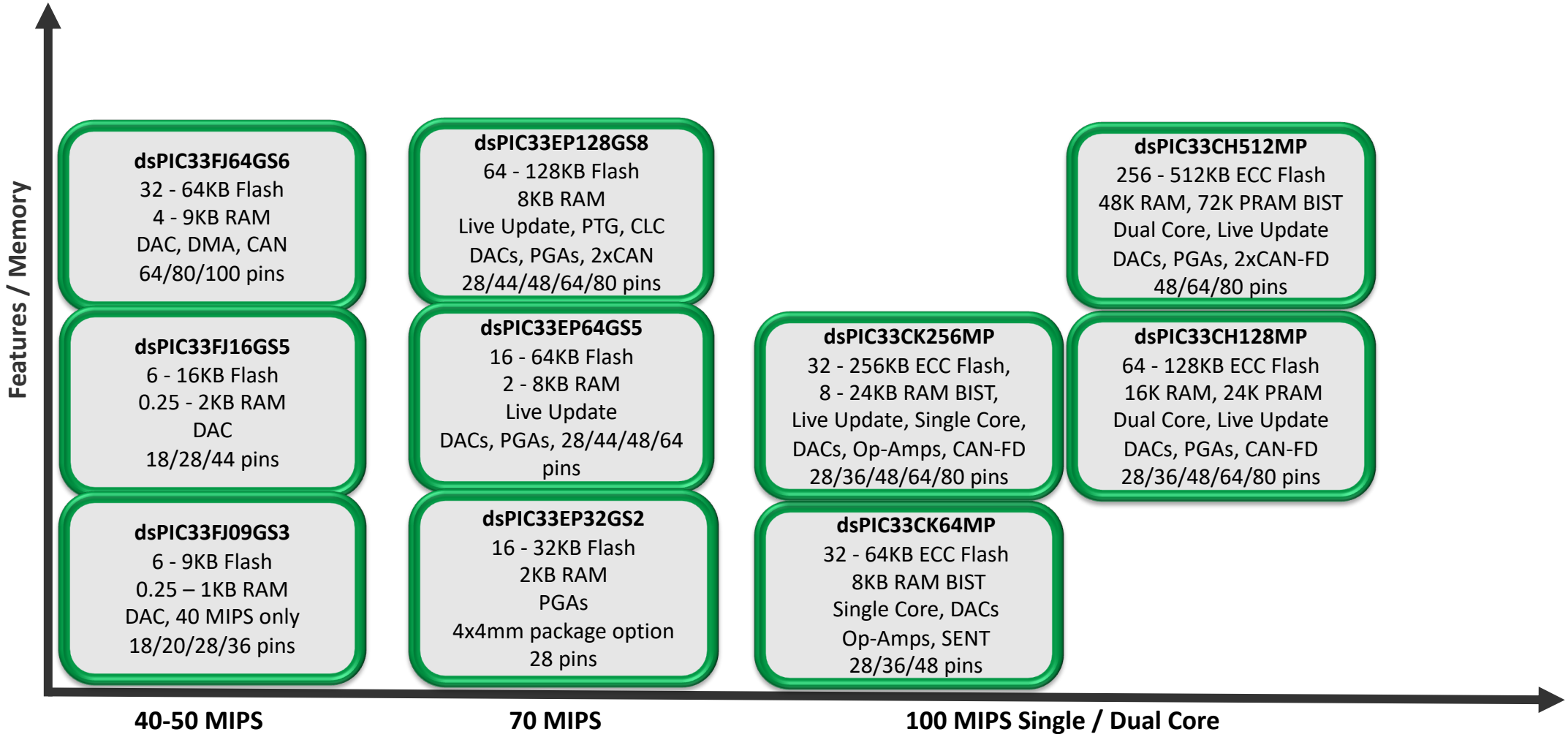


This Is Full Digital Power!



dsPIC33 vs. Full Digital Power

Digital Power Roadmap



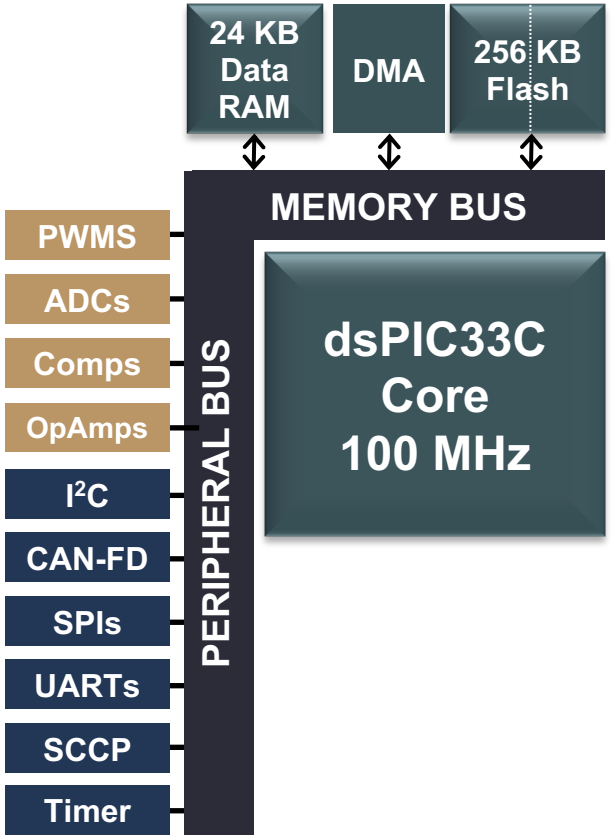
Robustness features on dsPIC33C

- **Internal regulator is Capacitor-less design**
  - No need of an external capacitor, no noise injection from the board
  - Saves space on the board for routing
  - Lower component count, lower cost
  - One extra I/O pin
- **Virtual Pins for Redundancy and Monitoring: Dual core device feature to cross check/monitor**
- **Flash ECC (Error Correcting Code): Flash Error check with 1-bit detection/correction & 2-bit detection**
- **DMT (Deadman Timer) : Instruction cycle counting and could be used as a SW checkpoint**
- **WDT (Watchdog Timer) : For system recovery**
- **CodeGuard™ Security: For code protection schemes**
- **CRC (Cyclic Redundancy Check): For code validation**
- **Two-Speed Start-up: For slowly start up from power on, reduce inrush current**
- **Fail-Safe Clock Monitoring: Clock monitor and switch**
- **Backup FRC (BFRC): Backup for the FRC clock**
- **AEC-Q100 REVG (Grade 0: -40˚C to +150˚C) Compliant: Automotive Qual**

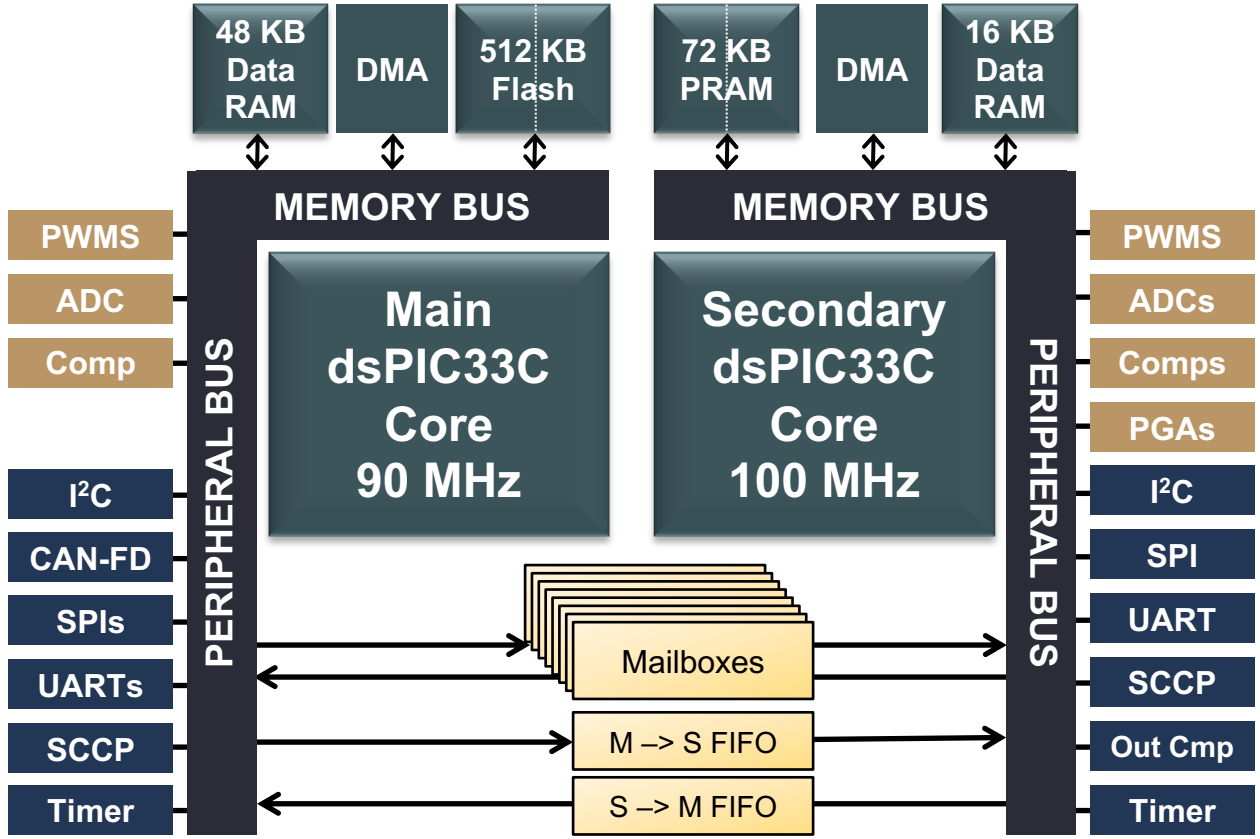
dsPIC33C Family

Single Core dsPIC33CK

250 ps Resolution
285 ns Latency
15 ns Response
10 MHz BW

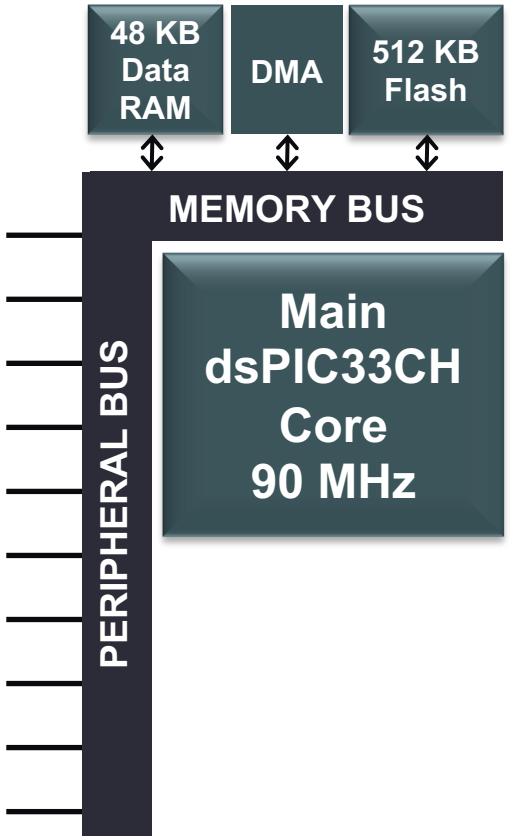


Dual Core dsPIC33CH



MICROCHIP

dsPIC33CH512 MP Main Core



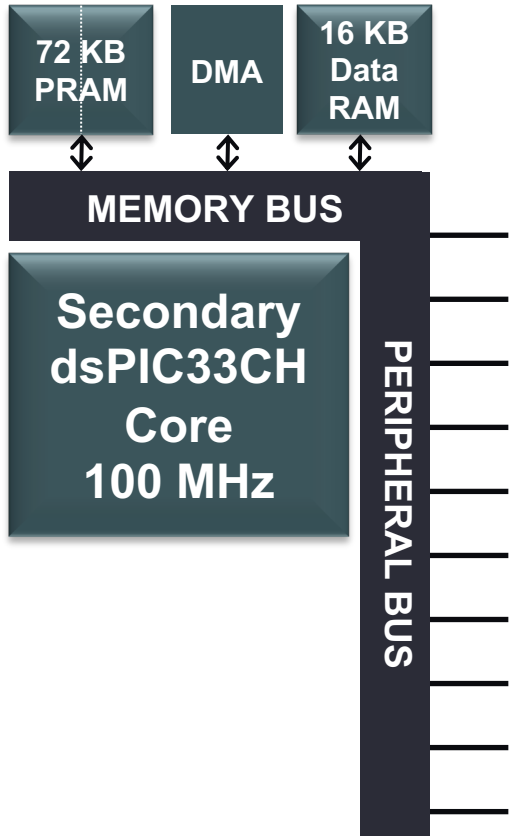
Main Core's Dedicated Peripherals

- 6 General DMA channels
- 2 CAN-FD (with 2 dedicated DMA channels)
- 2 SENT
- 2 SPI with I^2S support
- 2 I^2C with PMBus™ support
- 2 UARTs
- 1 Peripheral Trigger Generator (PTG)
- 4 Configurable Logic Cells (CLCs)
- 1 QEI (Quadrature Encoder Interface)
- 8 SCCPs - 32 bit-timer/Cap/Compare
- 1 CRC Module
- 1 12-bit ADC with up to 18 channels
- 1 Analog Comparator w/ 12-bit DAC
- 1 DAC output buffer (shared across cores)
- 8 PWM Generators
- 64 x 48 bits of OTP Flash

dsPIC33CH512 MP Secondary Core

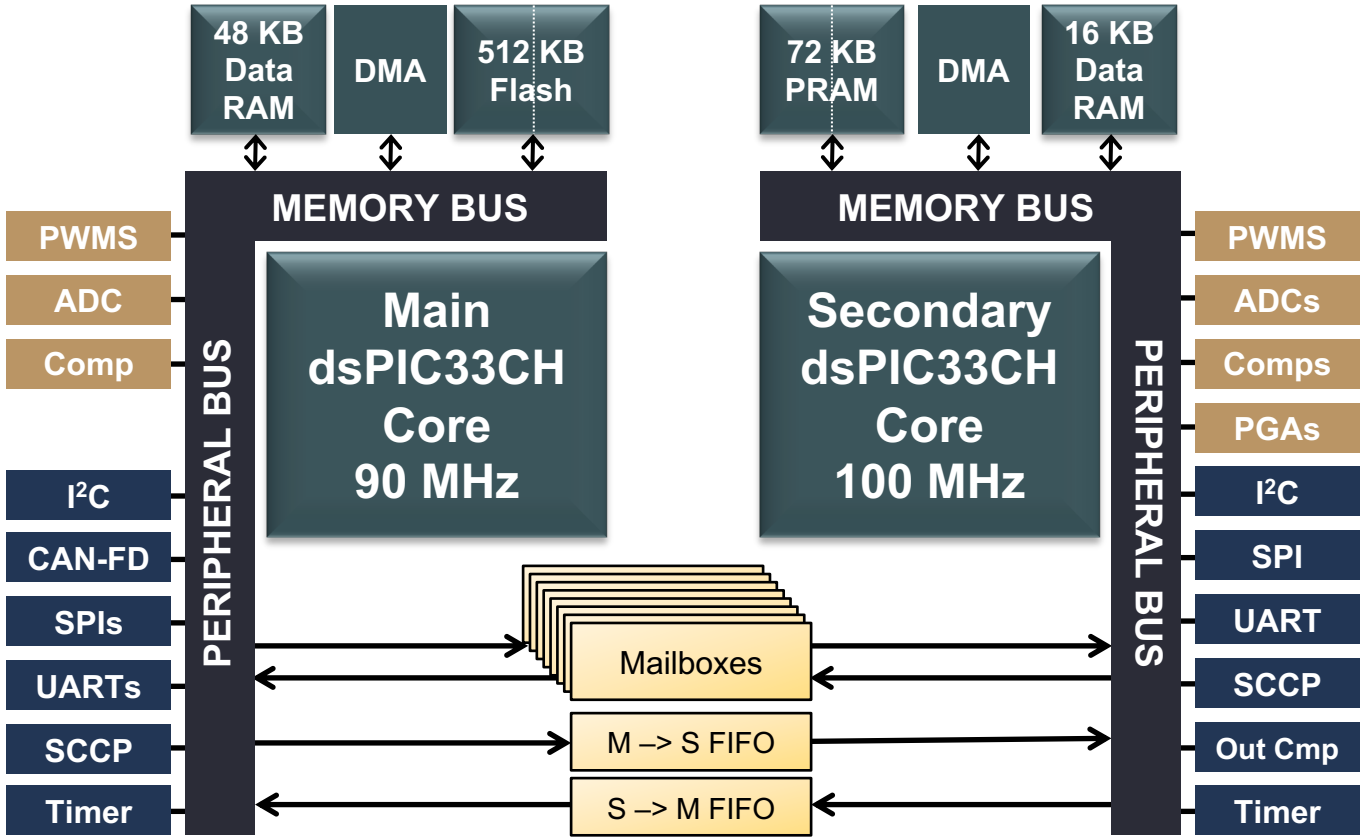
Secondary Core's Dedicated Peripherals

- 3 12-bit ADCs w/ up to 18 channels
- 3 Analog Comparators with 12-bit DACs
- 3 PGAs (can share with main core)
- 8 PWM Generators
- 4 Configurable Logic Cells (CLCs)
- 1 QEI (Quadrature Encoder interfaces)
- 4 SCCPs - 32 bit-timer/Cap/Compare
- 1 16-bit Timer
- 2 Channel DMA
- 1 SPI with I^2S support
- 1 UART
- 1 I^2C with PMBus™ support
- 1 Deadman Timer



Main / Secondary Interface (MSI)

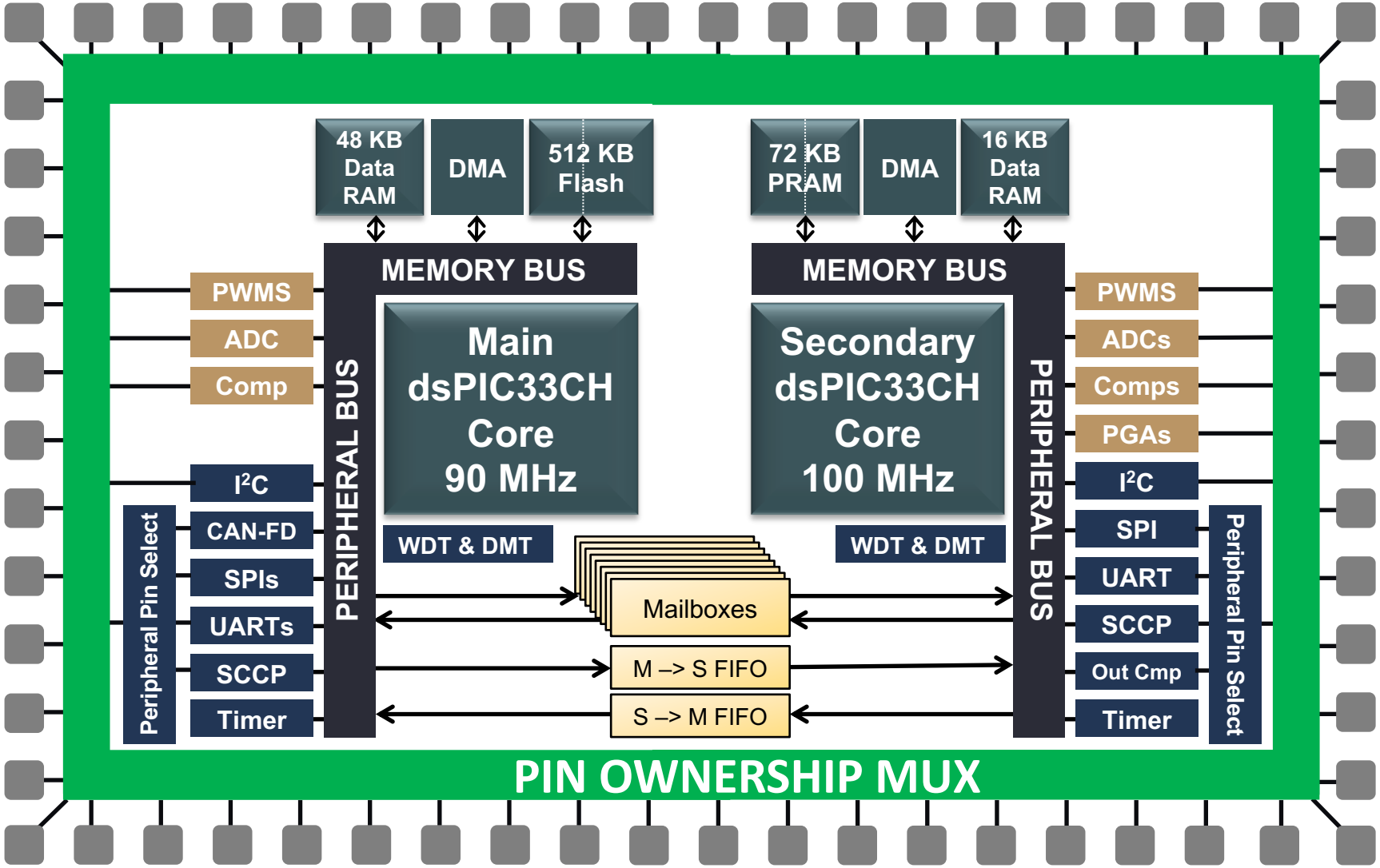
Example: dsPIC33CH512



Configurable direction for all 16 mailboxes
Configurable interrupt operation for mailboxes & FIFOs

dsPIC33CH Family

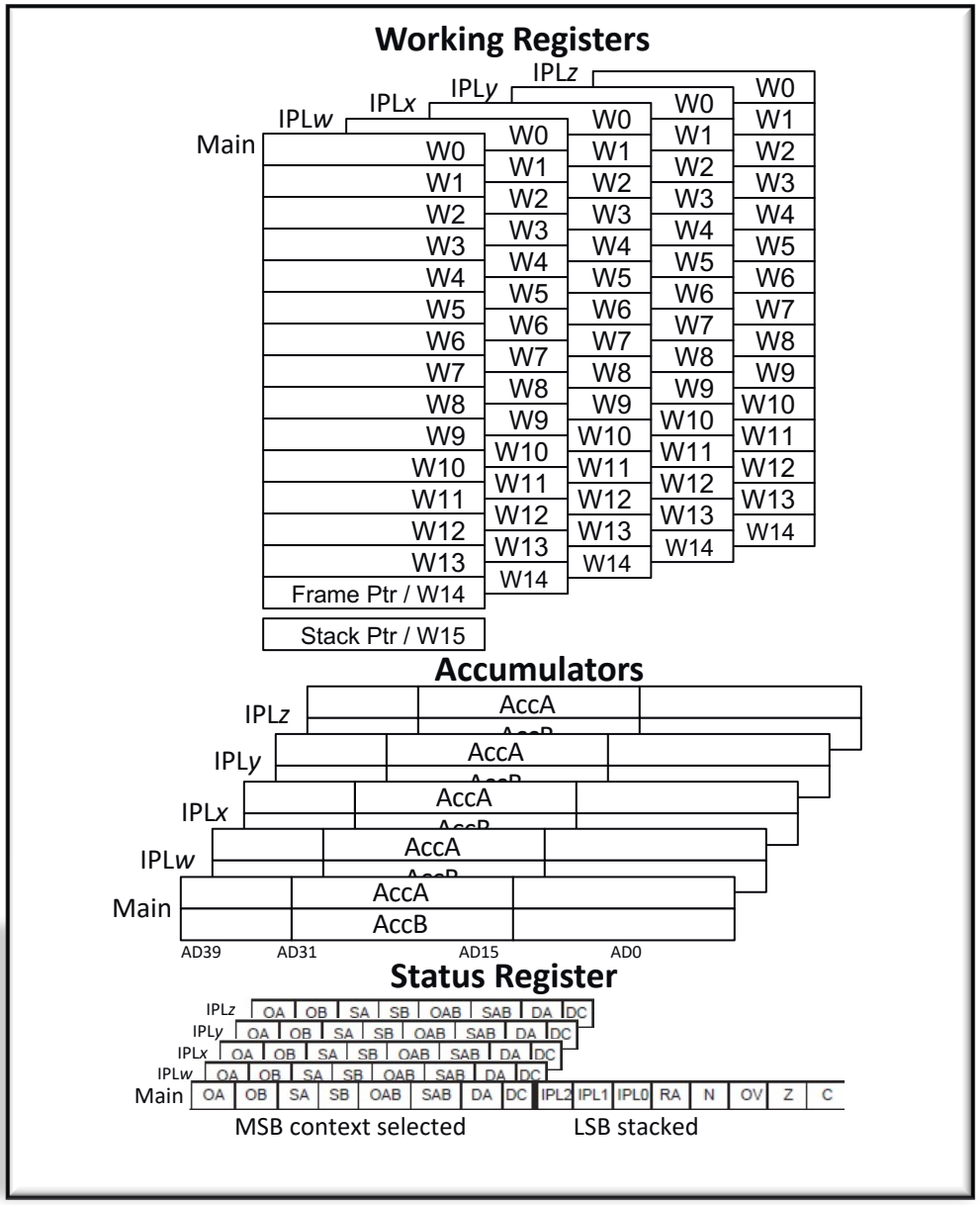
Pin Ownership Mux



dsPIC33C Family

Context-Selected Register Sets

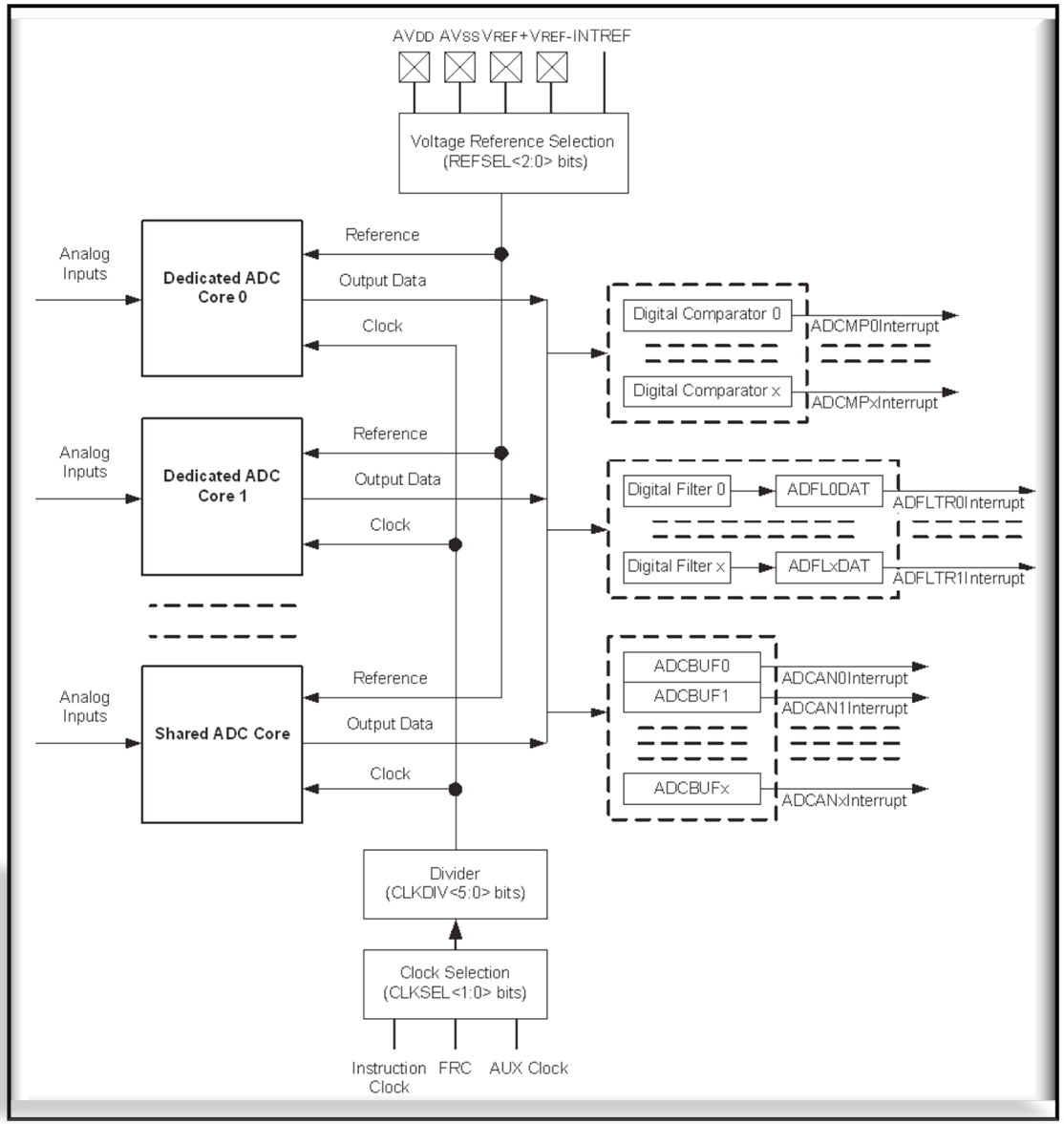
- **Enables nearly instantaneous context switches**
- **Four additional register sets**
  - Each assigned to specific interrupt priority level
  - Persistent data from one interrupt service routine (ISR) invocation to the next
  - Reduces saving and restoring register contents
- **Accelerates compensators up to 50%**
  - Significantly reduces control-loop latencies



dsPIC33C Family

12-Bit ADC

- **285 ns latency**
- **3.5 MSPS per SAR**
- **Up to 24 analog inputs each with a dedicated result register**
- **Multiple and flexible trigger options**
  - PWM Primary and Secondary Trigger
  - Timer Period Match
  - Output Compare event trigger
  - PWM special event trigger
  - PWM Current-Limit event trigger
  - External trigger event from device pin
  - Software trigger
- **Four digital comparators with interrupts:**
  - Multiple comparison options
- **Four oversampling filters with interrupts:**
  - Provides increased resolution

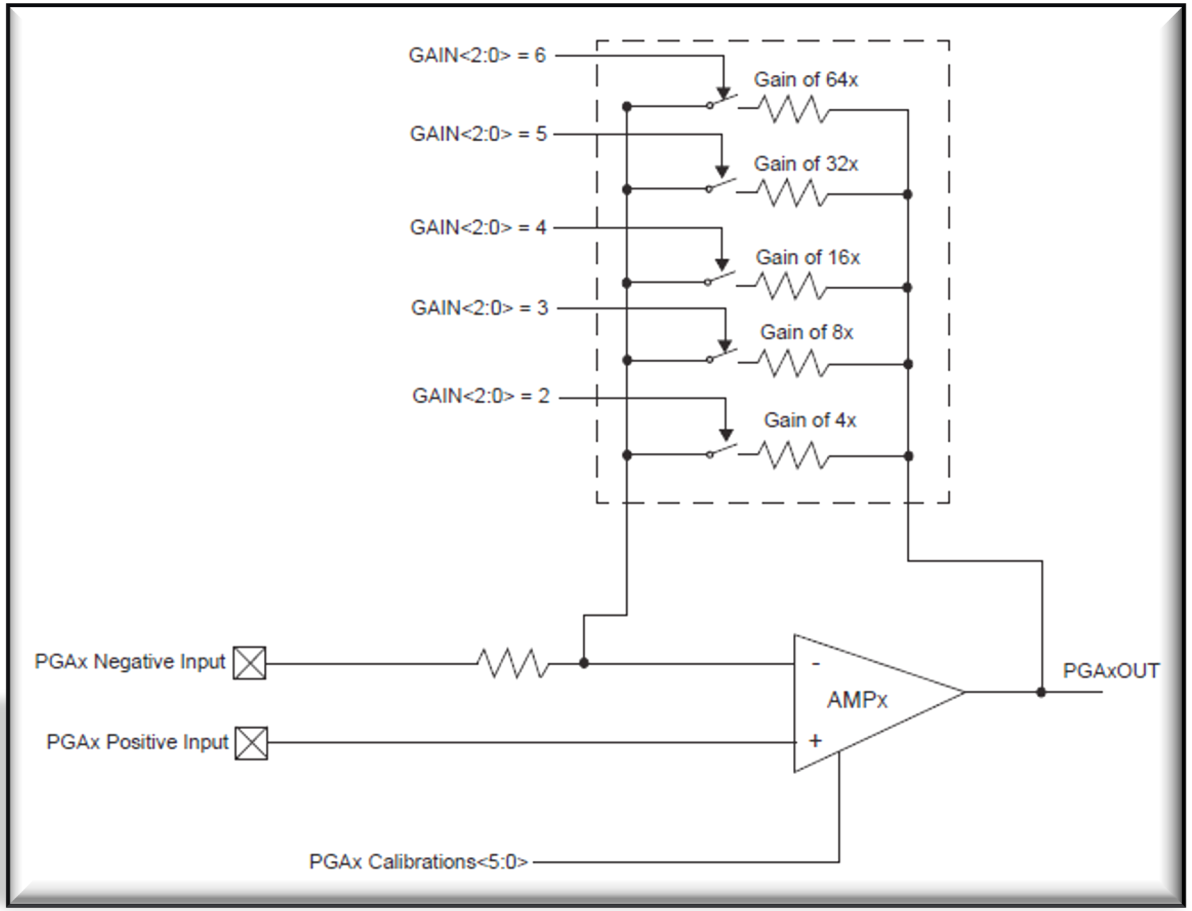


dsPIC33CH Family

Programmable Gain Amps

- Configured by secondary core
- Non-inverting amps with 8 selectable gains
- Output can be read by dedicated S&H circuits
- Output can be input to analog comparators
- Output can be routed to DACOUTx pin

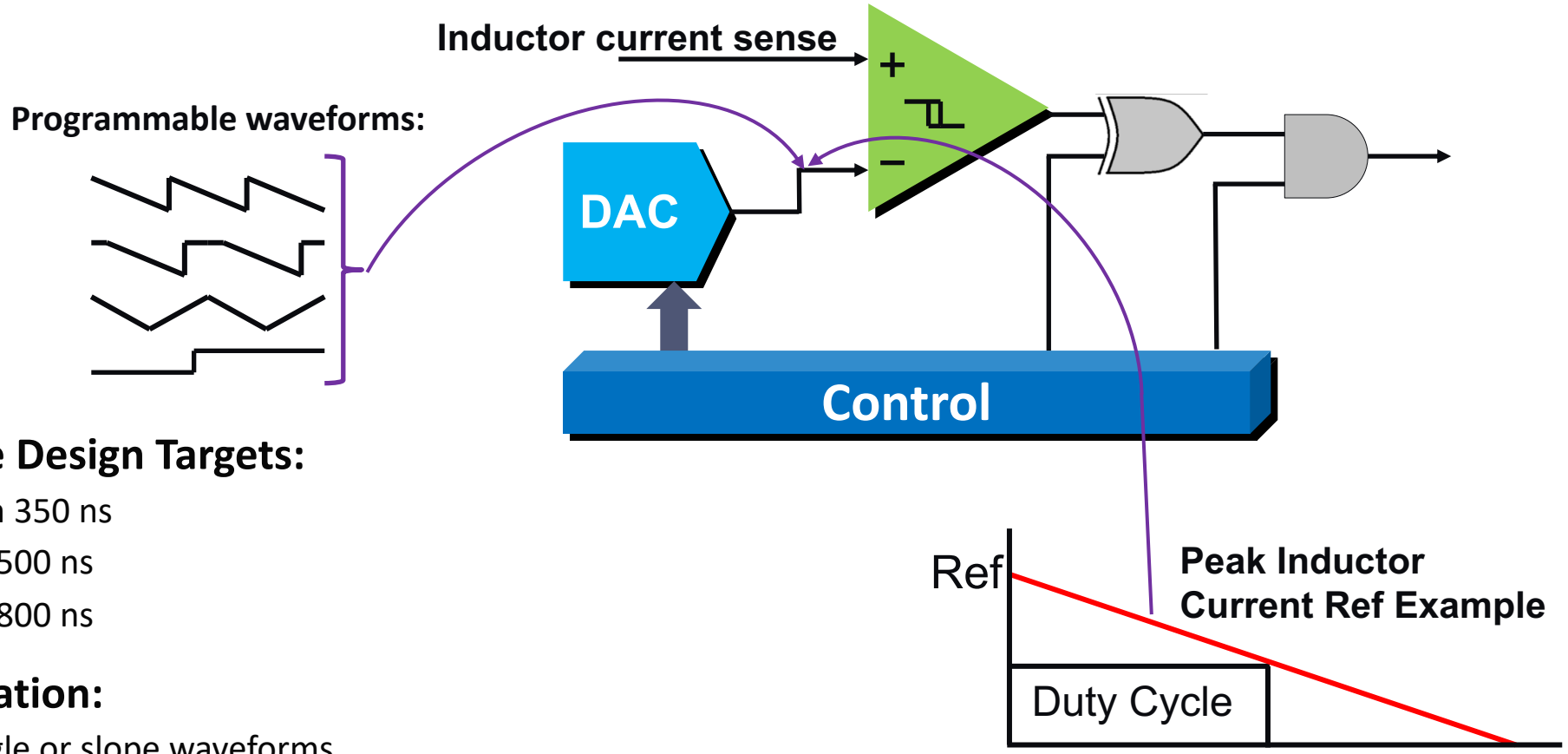
Gain	Typical Bandwidth (-3 dB)
4x	10 MHz
6x	6.7 MHz
8x	5.0 MHz
12x	3.3 MHz
16x	2.5 MHz
24x	1.7 MHz
32x	1.3 MHz
48x	0.8 MHz



dsPIC33C Family

High Speed 12-bit DAC

- **Generates reference voltage waveforms for analog comparators**
  - Can be used for slope compensation in peak current mode topologies



- **2V Step Response Design Targets:**
  - Settle to ±30 mV in 350 ns
  - Settle to ±3 mV in 500 ns
  - Settle to ±1 mV in 800 ns
- **Waveform Generation:**
  - Up to 1 MHz triangle or slope waveforms

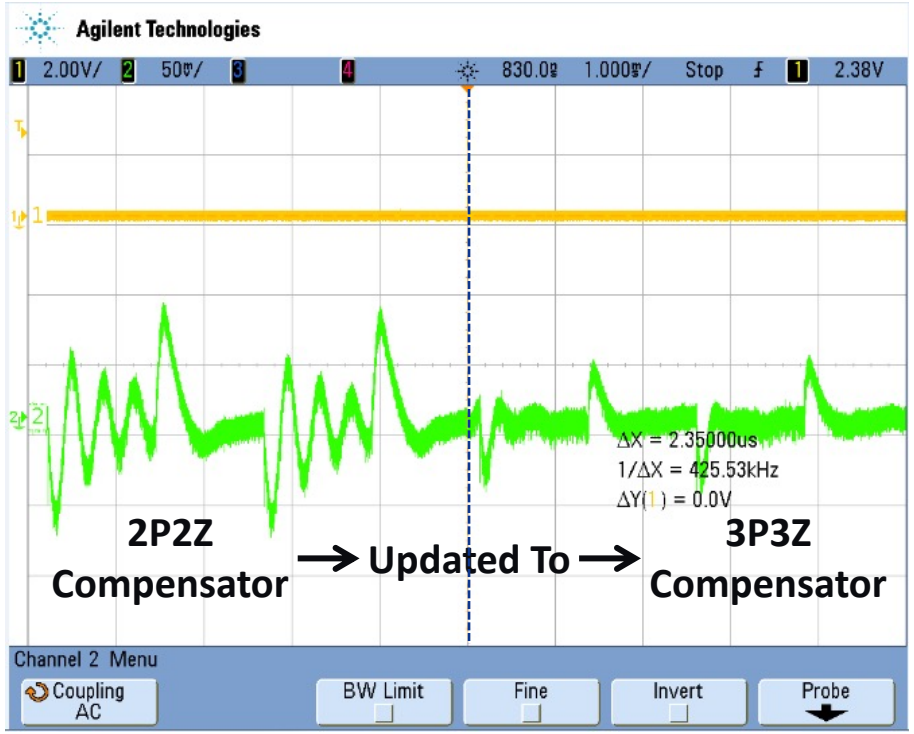
dsPIC33C Family

Live Update

- **Update firmware in an operating power converter while maintaining continuous regulation**

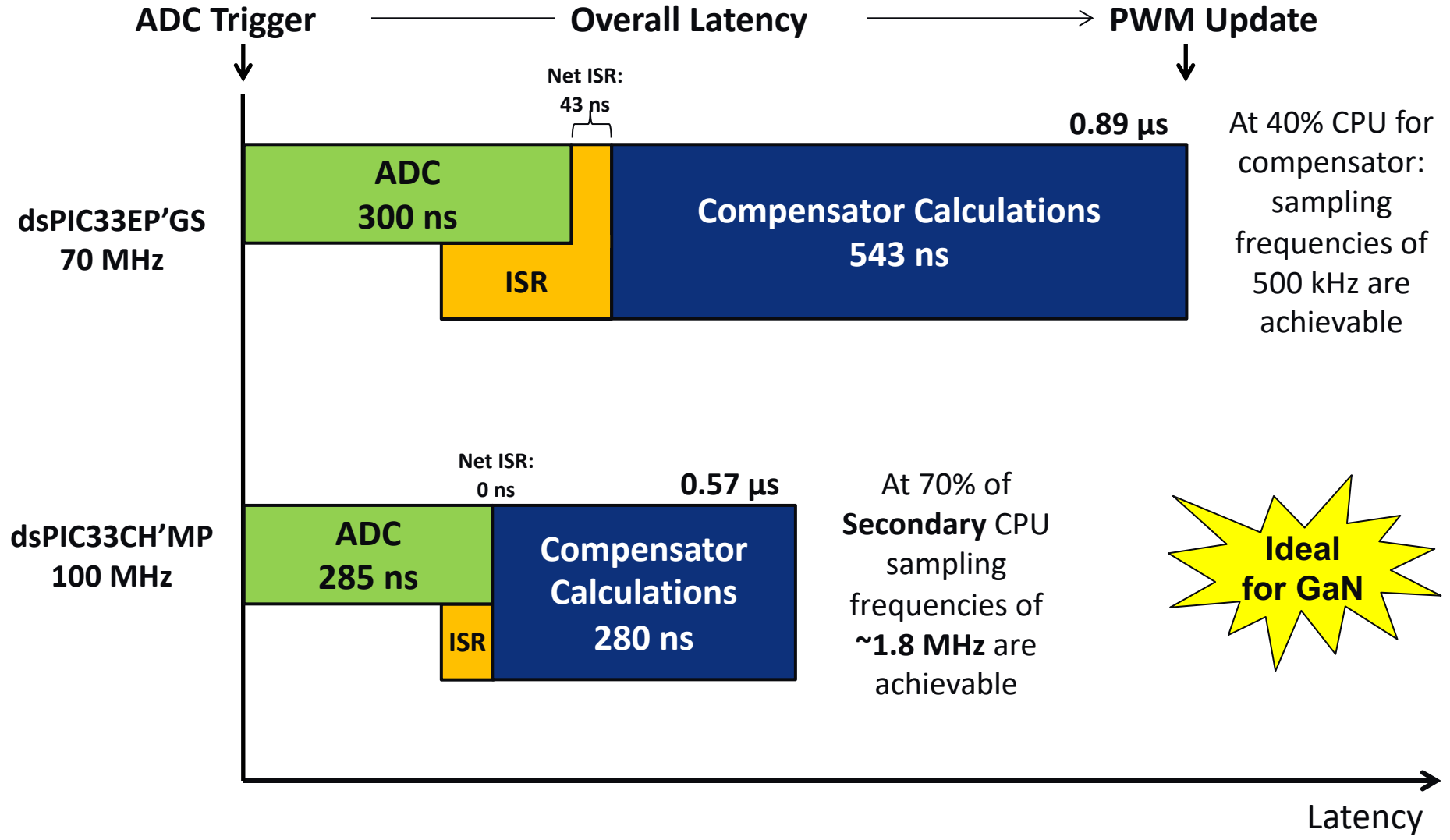
- **dsPIC33C Live Update Features:**
  - Dual Flash partitions (main) & dual RAM partitions (secondary)
    - Update one partition while executing from the other
  - Fast switchover between partitions
    - Transparently fits between compensator updates to PWM
  - Continuous analog comparator fault monitoring
    - PWM output can be truncated due to detected fault in 15 ns (typ) regardless of stage in Live Update process
  - Complete development tools support and example code

Live Update 2P2Z to 3P3Z Demo



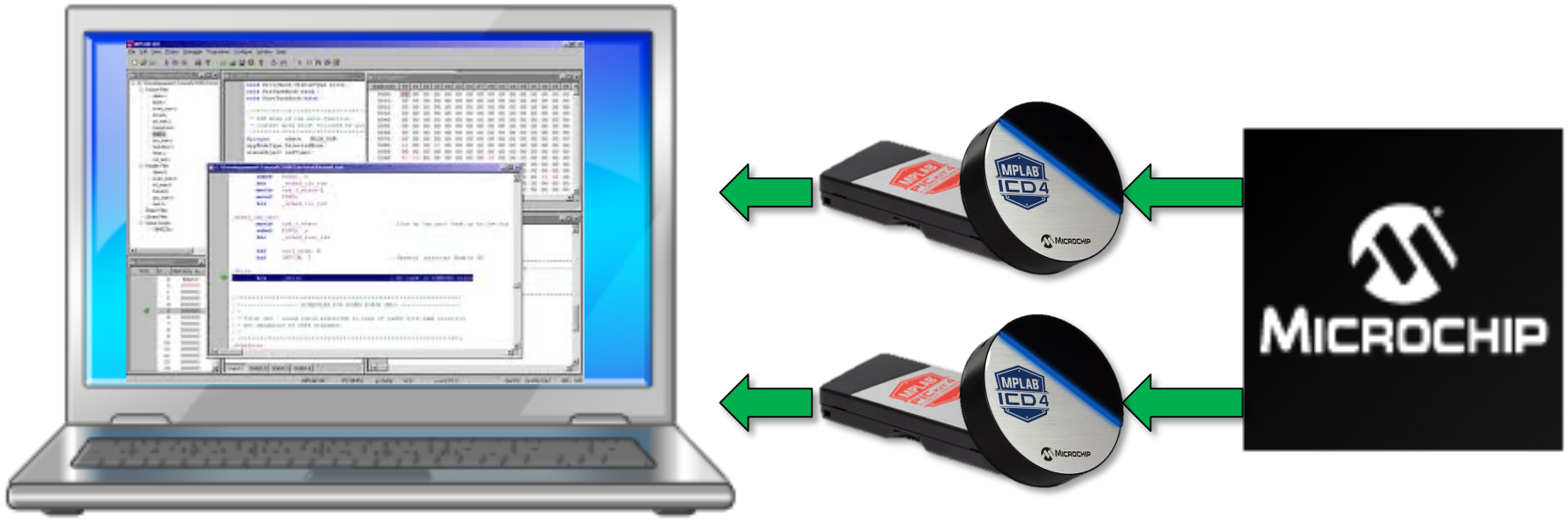
dsPIC33C Performance Example

Digital Power 3P3Z Latency



dsPIC33CH Family

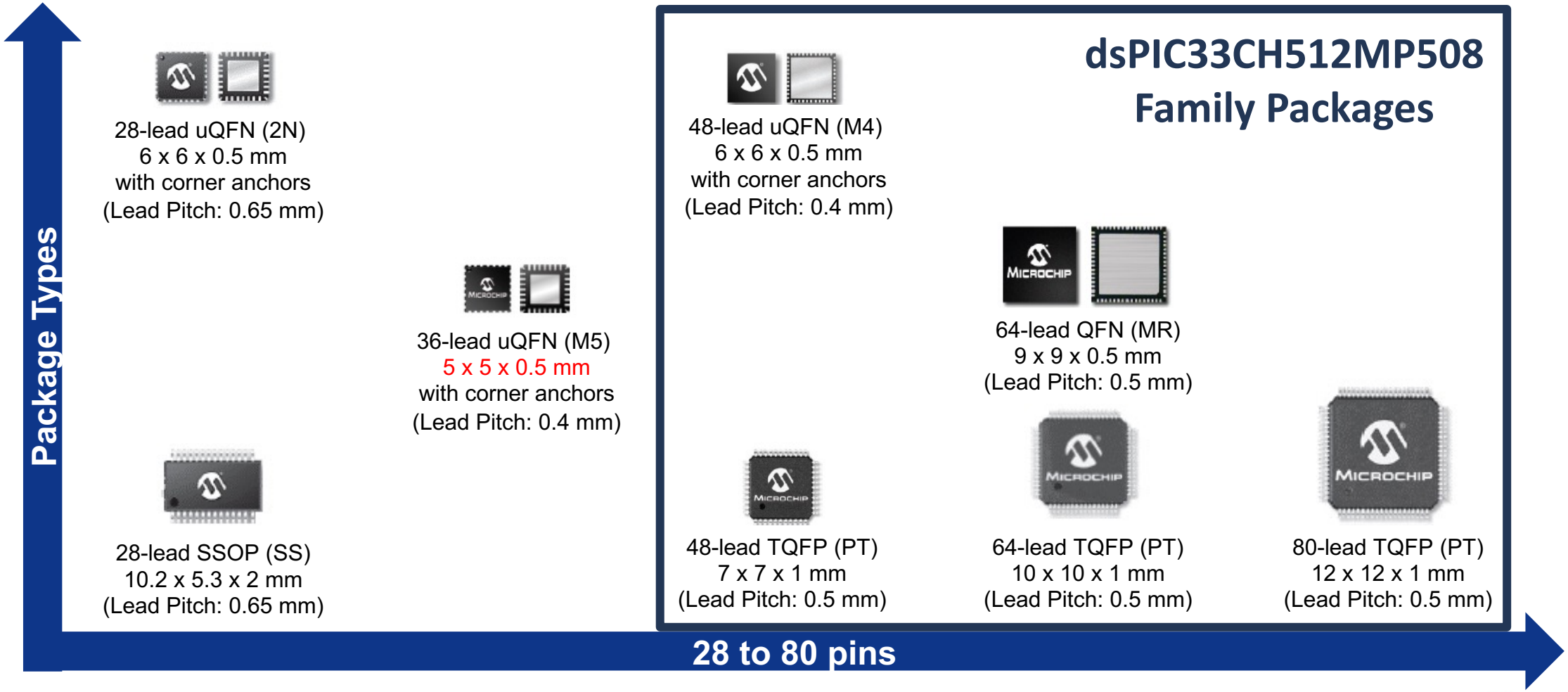
Dual Core Debug



- MPLAB® supports parallel debug sessions
- Main core programs secondary core, hosts image
- Debug is independent
- Changes to secondary core code are placed back into main core's image
- Breakpoints on either core can be configured to halt the other core or leave it running

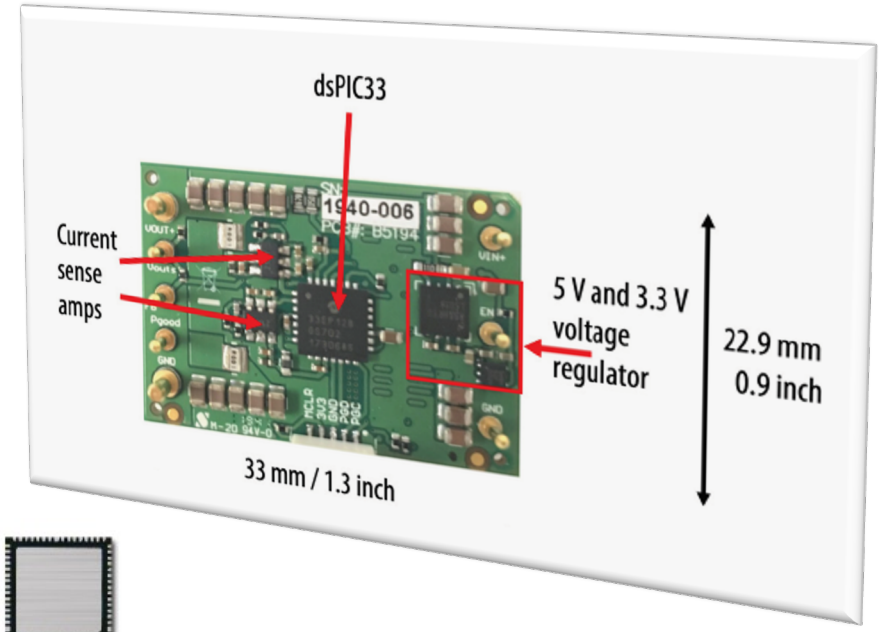
dsPIC33CH Family Packages

Wide range of packages from 28 to 80-pin



dsPIC33CK Family Packages

Wide range of packages from 28 to 80-pin



Package Types

28-lead uQFN (2N)
6 x 6 x 0.5 mm
with corner anchors
(Lead Pitch: 0.65 mm)

48-lead uQFN (M4)
6 x 6 x 0.5 mm
with corner anchors
(Lead Pitch: 0.4 mm)

64-lead QFN (MR)
9 x 9 x 0.5 mm
(Lead Pitch: 0.5 mm)

28-lead uQFN (M6)
4 x 4 x 0.6 mm
with corner anchors
(Lead Pitch: 0.65 mm)

36-lead uQFN (M5)
5 x 5 x 0.5 mm
with corner anchors
(Lead Pitch: 0.4 mm)

28-lead SSOP (SS)
10.2 x 5.3 x 2 mm
(Lead Pitch: 0.65 mm)

48-lead TQFP (PT)
7 x 7 x 1 mm
(Lead Pitch: 0.5 mm)

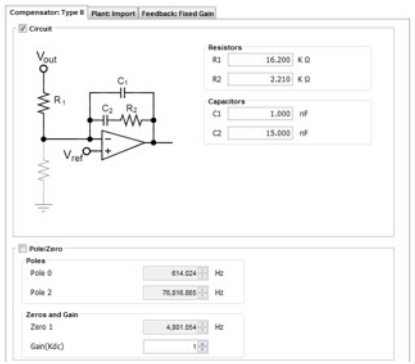
64-lead TQFP (PT)
10 x 10 x 1 mm
(Lead Pitch: 0.5 mm)

80-lead TQFP (PT)
12 x 12 x 1 mm
(Lead Pitch: 0.5 mm)

28 to 80 pins

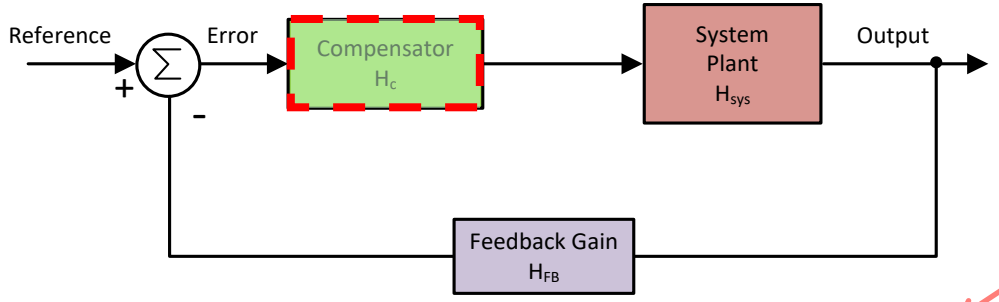
Digital Power Development Tools

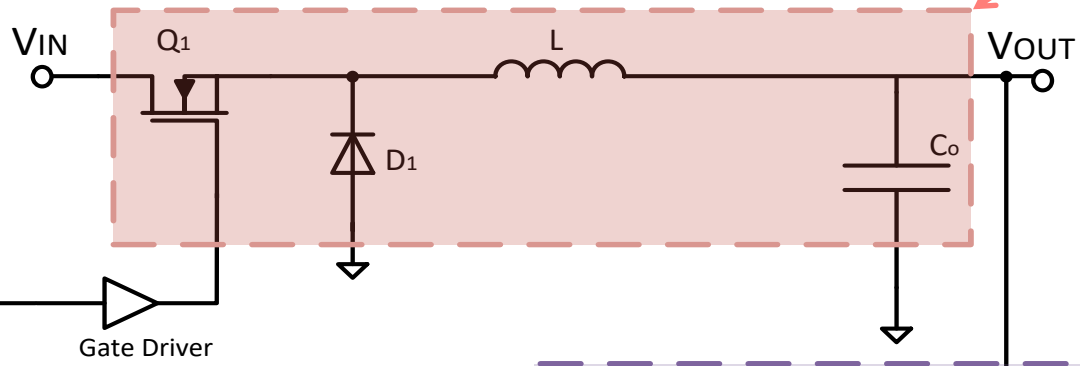
Digital Power Development Suite with DCDT

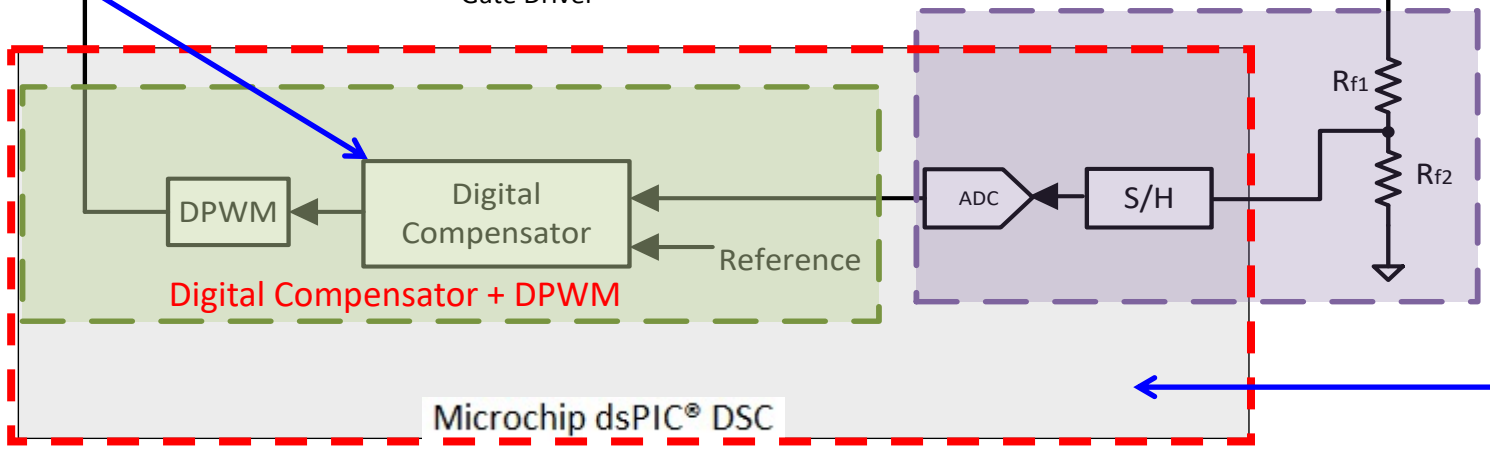


Step #3: DCDT (Coefficients)

Step #4: DCDT SMPS Lib (Compensator)







MPLAB MINDI ANALOG SIMULATOR

Kp Control

Step #2: Getting Plant

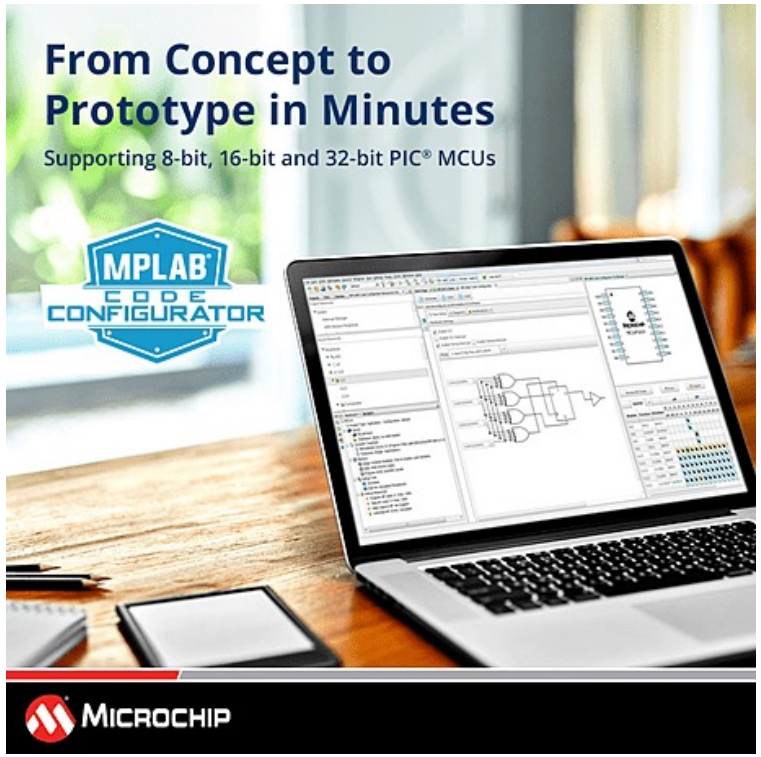
MPLAB CODE CONFIGURATOR

Step #1: MCC (Codebase)

MICROCHIP

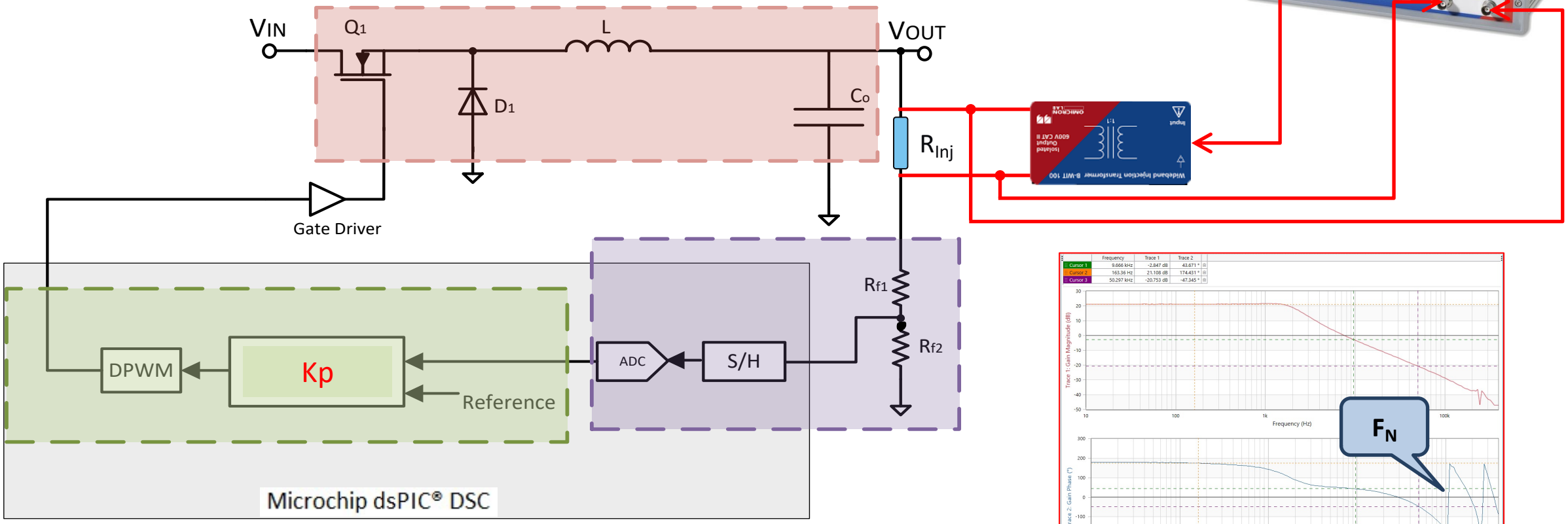
MPLAB® Code Configurator

- **Free Graphical Programming Environment**
- **Intuitive Interface for Quick Start Development**
- **Automated Configuration of Peripherals & Functions**
  - Easy I/O set-up with pin manager
  - Minimized reliance upon product datasheet
  - Reduces overall design effort & time
- **From Novice to Expert…**
  - Accelerates generation of production ready code



- **Quick start software libraries for Dev. Boards and click boards™**
  - Add sensing, control, or communication functionality to your prototype design without the hassle of low-level code development and validation

Kp (P-Term) Control



eRTC Digital Power Workshop

http://elearning.microchip.com.tw/modules/tad_link/index.php?cate_sn=1

eRTC: ePOW001 數位功率因數校正設計與問題探討

eRTC線上課程錄影 | https://www.youtube.com/watch?v=QJKy9OH1PG8&feature=youtu.be

ePOW003 混合型數位電源

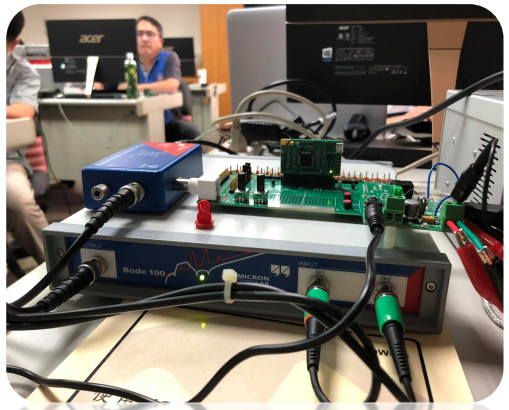
eRTC線上課程錄影 | https://youtu.be/4lO7JoZrUSA

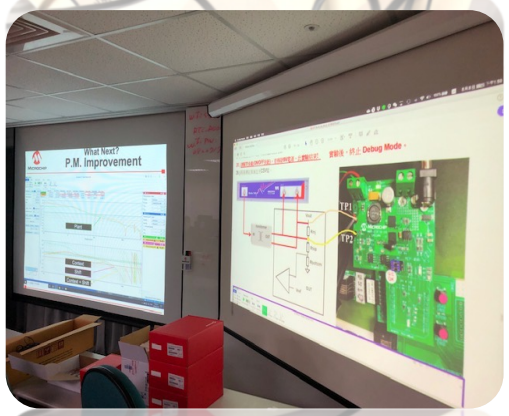
Microchip將電源區分為類比/半數位/全數位電源三類。
此課程主要以半數位電源為主，使用的是PIC16系列晶片，輔以LED Lighting為其中一...

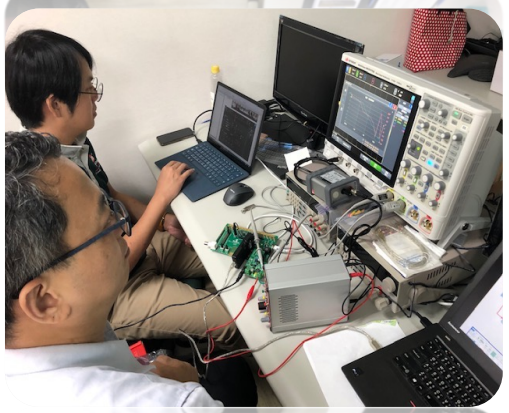
ePOW004 全數位電源

eRTC線上課程錄影 | https://youtu.be/I8T6yhfDFc0

Microchip將電源區分為類比/半數位/全數位電源三類。
此課程主要以全數位電源為主，使用的是dsPIC33系列晶片，輔以MCC + DCDT為主要開工...





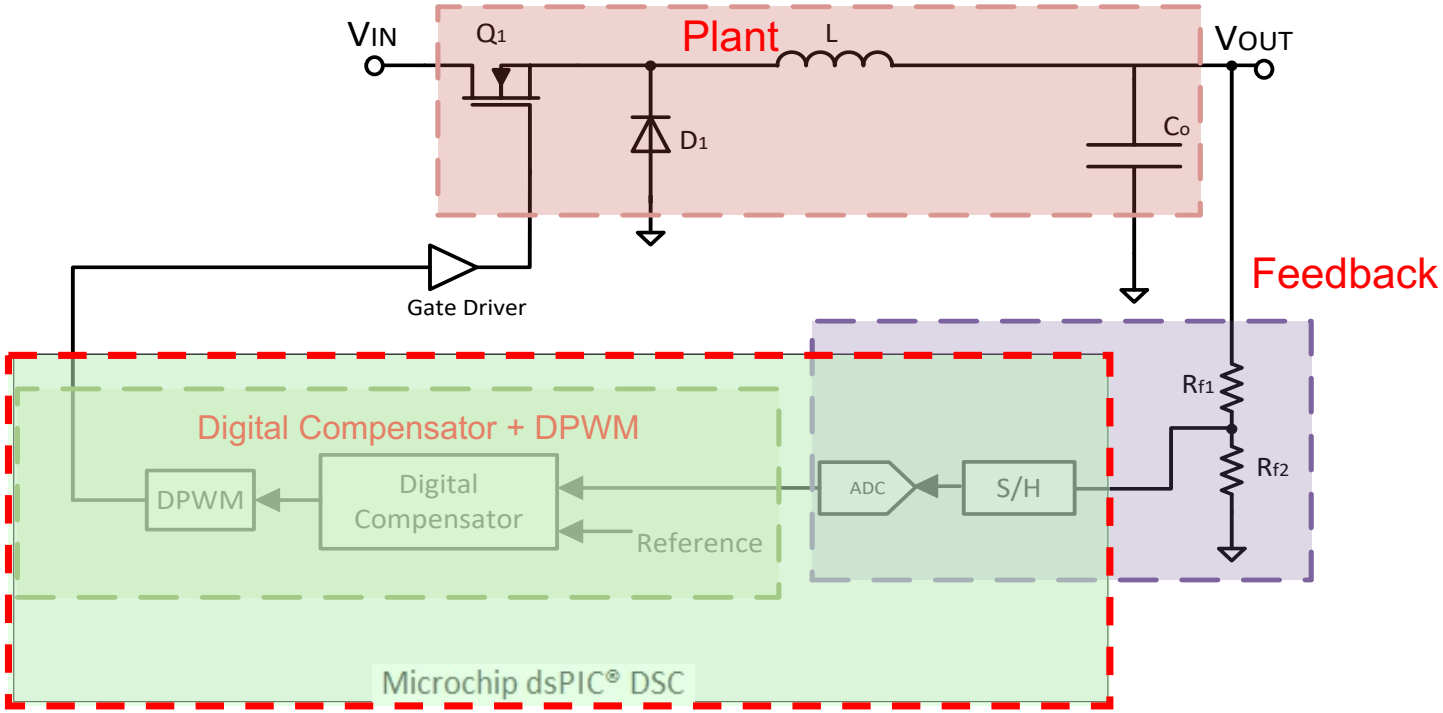


Full Digital Power Implementation

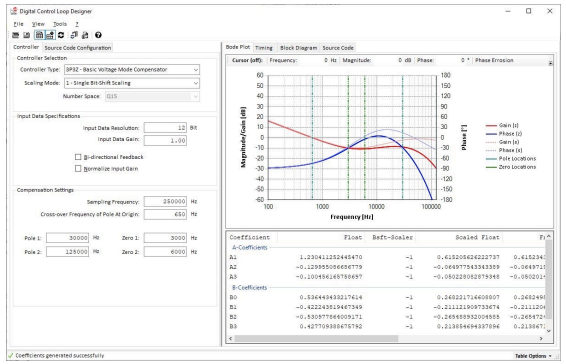
ePOW004

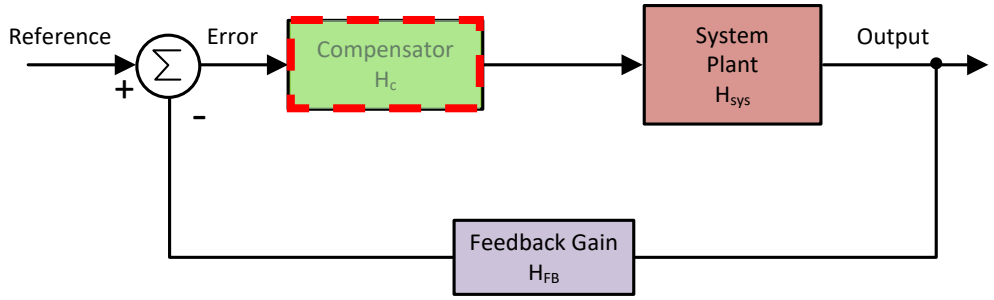
dsPIC全數位電源訓練課程錄影

https://youtu.be/I8T6yhfDFc0

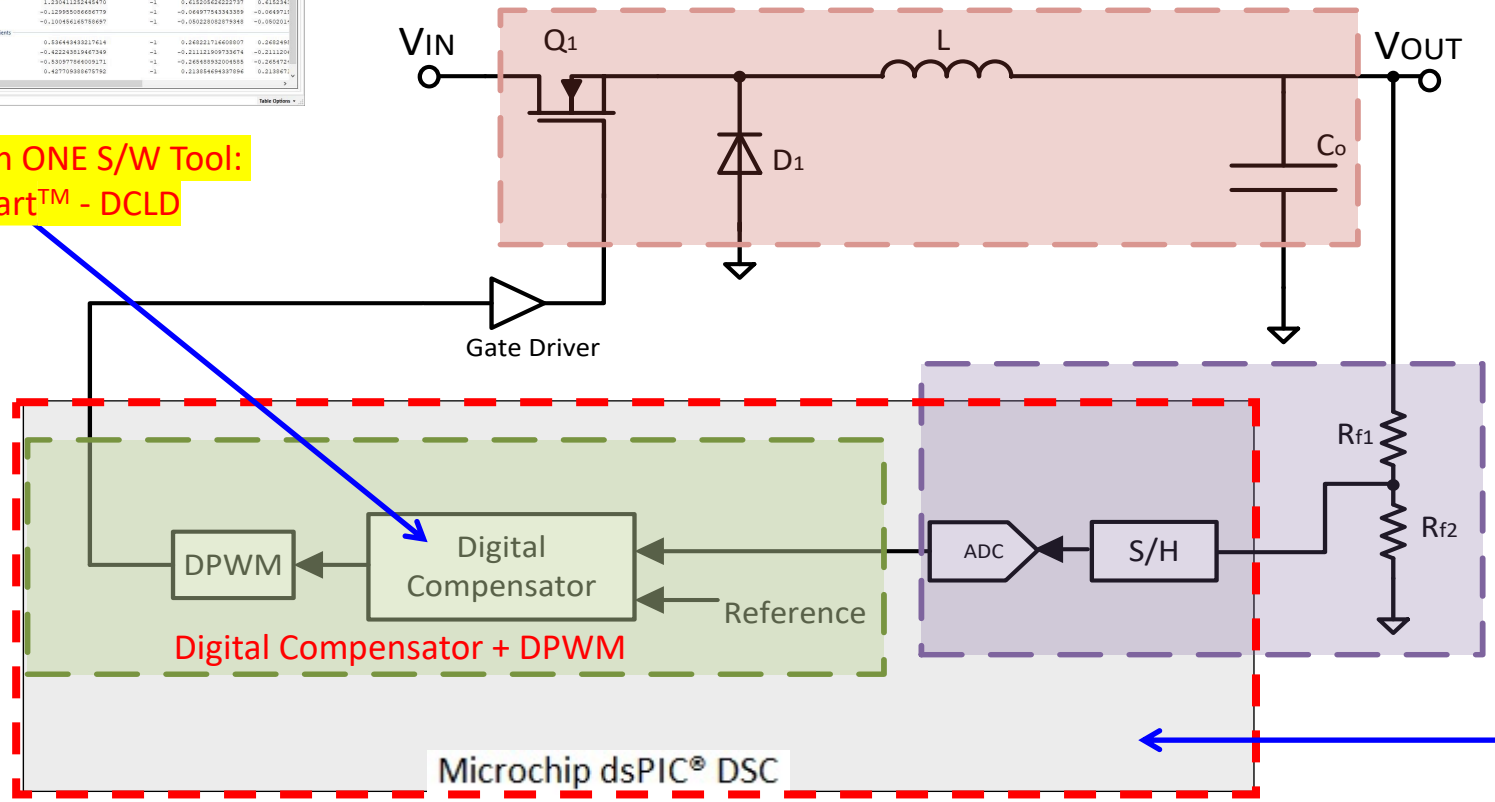


Digital Power Development Suite with DCLD





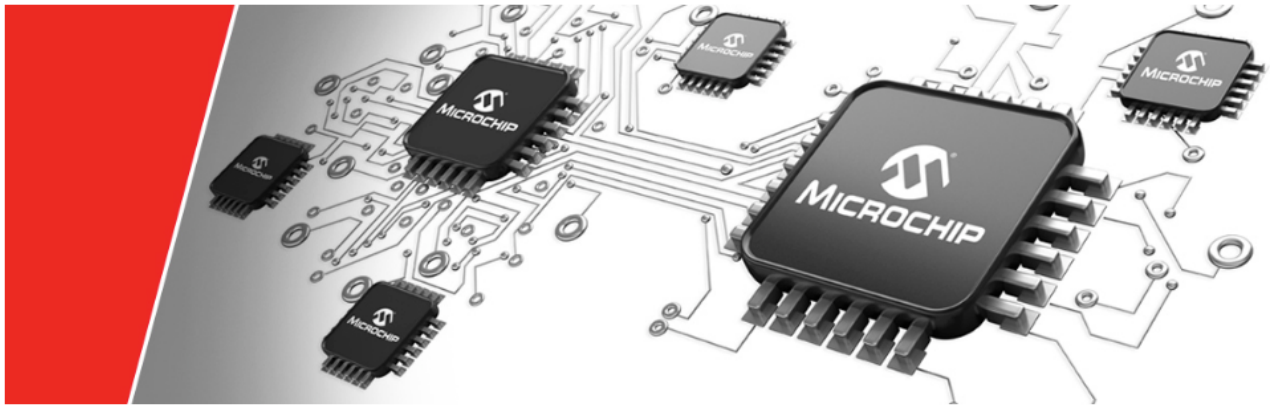
Step #2 ~ #4 in ONE S/W Tool:
PowerSmart™ - DCLD



Step #1: MCC (Codebase)

microchip-pic-avr-tools.github.io

powersmart-dcld



Download | Visit Release Website | View User's Guide

MPLAB® PowerSmart™ SDK
Digital Control Library Designer
Configuration Tool & Code Generator

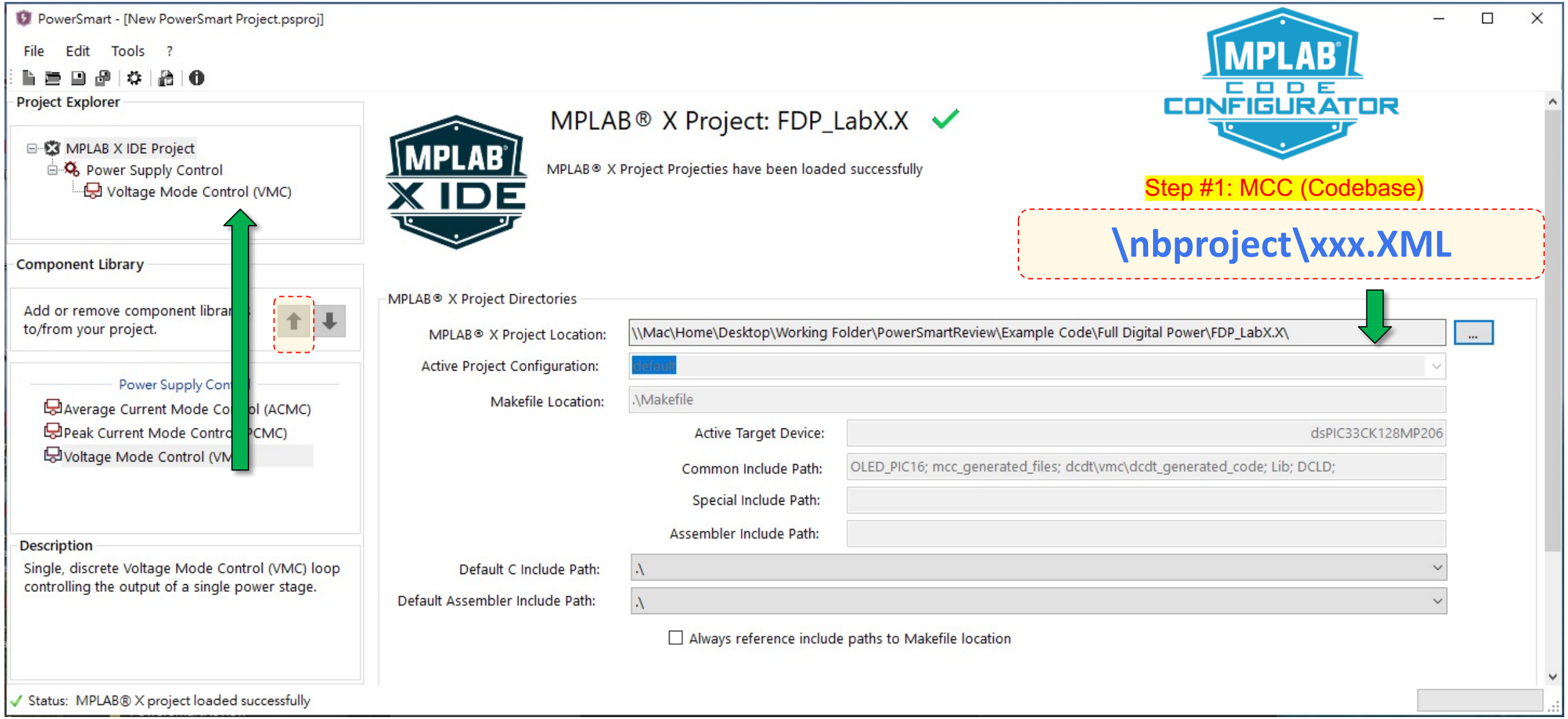
MPLAB® PowerSmart™ SDK for Microchip dsPIC33® Digital Signal Controllers

The MPLAB® PowerSmart™ SDK is a Software Development Kit (SDK) comprised of multiple, individual stand-alone tools for system definition, system modeling, code generation, control system fine tuning and real-time debugging of fully digital control systems for Switched-Mode Power Supplies (SMPS) supporting Microchip Technology's dsPIC® Digital Signal Controllers (DSC).

The major scope of this tool set is the rapid design of a digital power supply control stage rather than the power supply itself. This allows to simplify the design process to models based on interconnected transfer functions. These transfer functions are defined and configured in individual configuration windows. A transfer function can be based on generic Laplace-domain functions, being calculated at runtime or being defined by external data coming from network analyzer measurements or other third-party simulation tools such as MATLAB, SciLab, Simplis/SiMetrix, LTSpice, etc.

DCLD

PowerSmart™ - DCLD Introduction



PowerSmart - [New PowerSmart Project.psproj]

File Edit Tools ?

Project Explorer

MPLAB X IDE
Power Su
Voltag

Component Library

Add or remove con
to/from your proje

Pow
Average Curr
Peak Current
Voltage Mod

Description

Single, discrete Voltage Mode Control (VMC) loop controlling the output of a single power stage.

Status: MPLAB® X project loaded successfully

MPLAB MINDI ANALOG SIMULATOR

Step #2: Getting Plant

Import Transfer Function

Data Series Name: VMC Plant

File Import | Bode Plot

Data Source

Filename: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example Code\Full Dig ...

Series Header Row: 1

Data Start Row: 2

Column Separator: <COMMA>

✓ Data file has been selected.
✓ Data file has been parsed successfully.
✓ Valid name for the new data series has been specified.

Phase Rotation

- (•) No Rotation
- ( ) Rotate by -180°
- ( ) Rotate by +180°

Preview

```
100     21.62018411     166.2357428
102.095159      21.08645356     163.5828554
104.234215      21.64467619     167.2569357
106.418088      21.30840238     164.857718
108.647716      21.19904329     163.6599071
110.924058      21.16797592     167.5429661
113.248094      20.95997998     165.380709
115.620821      21.26479162     164.2172737
```

Import Data

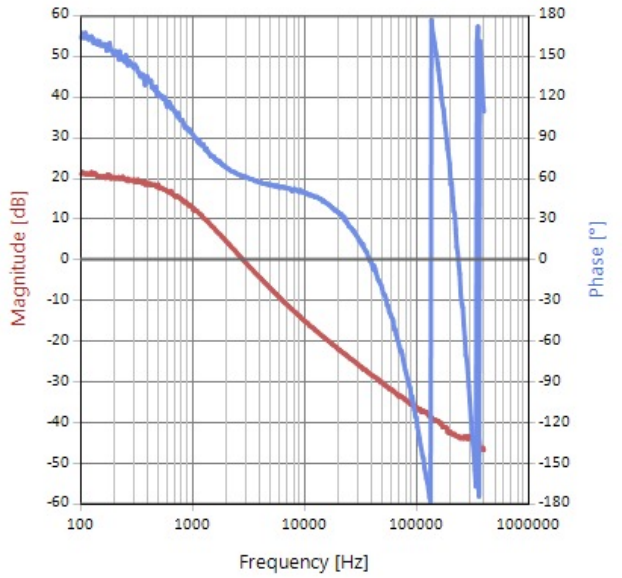
Apply Close

Import Transfer Function

Data Series Name: VMC Plant

File Import | Bode Plot

Frequency: 0 Hz | Magnitude: 0 dB



Bode Plot Settings

Frequency
Start: 100 Hz
Stop: 100k Hz
Points:

Magnitude/Gain
Min: -60 dB
Max: 60 dB
Div: 10 dB

Phase
Min: -180 °
Max: 180 °
Div: 30 °

Show/Hide Data Series

Apply Close

Data Changed:PLANT

PowerSmart Digital Control Library Designer v1.9.14.683 - [\\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example Code\Full Digital Power\FDP_LabX.X\DCLD\New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Development Tools

Use P-Term Loop Controller for Plant Measurements

Nominal Feedback Level: 1237

Nominal Control Output: 0

Fractional: 32765.0

Scaler: 0

Step #2: Getting Plant

Enable Feedback Loop Gain Modulation (AGC)

Add Enable/Disable Adaptive Gain Control (AGC)

Add Observer Function Call before Modulation

Optimize AGC Modulation Factor Accuracy

Add User Extensions

Start of Control Loop
Add Function Parameter

After Reading Source
Add Function Parameter

Before Anti-Windup
Add Function Parameter

Before Writing to Target
Add Function Parameter

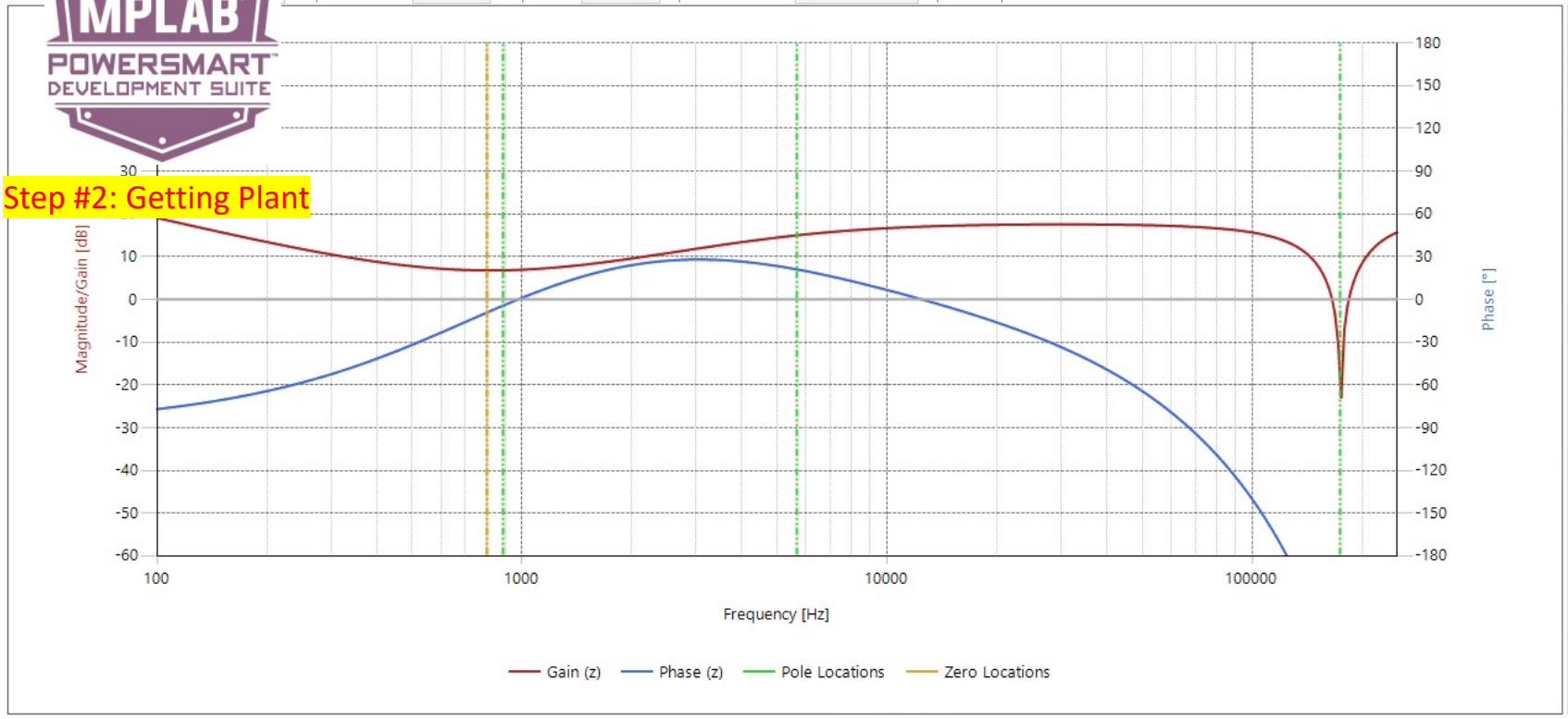
End of Control Loop
Add Function Parameter

Cascade Function Call
Add Function Parameter

Please Note:
Execution time of user functions being called during the control loop execution is not included in the Control Timing Analysis

Freq | ock Diagram | Source Code Output | Info

Hz | Magnitude: 0 dB | Phase: 0 ° | Phase Errosion 0 ° | Reset Scales



Bode Plot Settings

Frequency
Start: 100 Hz
Stop: 250k Hz
Points: 400

Magnitude/Gain
Min: -60 dB
Max: 60 dB
Div: 10 dB

Phase
Min: -180 °
Max: 180 °
Div: 30 °

Options
Unwrap Phase
Show s-Domain
Show Legend

Copy Bode Data

Filter Coefficients

Number Analysis | Settings History

Coefficient	Float	Bsft-Scaler	Scaled Float	Fractional	FP Error	Int	UInt	Hexadecimal	Binary
A-Coefficients									
A1	1.681403575237150	-1	0.840701787618576	0.840728759765625	0.003%	27,549	27,549	0x6B9DFFFF	0b01101011 10011101...
A2	-0.480813159799046	1	-0.961626319598093	-0.961608886718750	-0.002%	-31,510	34,026	0x84EA0001	0b10000100 11101010...
A3	-0.200590415438105	2	-0.802361661752421	-0.802337646484375	-0.003%	-26,291	39,245	0x994D0002	0b10011001 01001101...
B-Coefficients									
B0	23.106724903141200	-5	0.722085153223164	0.722106933593750	0.003%	23,662	23,662	0x5C6EFFFB	0b01011100 01101110...
B1	-22.446475281837800	-5	-0.701452352557432	-0.701446533203125	-0.001%	-22,985	42,551	0xA637FFFB	0b10100110 00110111...
B2	-23.102008423801800	-5	-0.721937763243806	-0.721923828125000	-0.002%	-23,656	41,880	0xA398FFFB	0b10100011 10011000...
B3	22.451191761177300	-5	0.701599742536789	0.701629638671875	0.004%	22,991	22,991	0x59CFFFFB	0b01011001 11001111...

Coefficients generated successfully

Refresh Period: 1129 ms Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Up

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 1 - Single Bit-Shift Scaling

Number Space: Q15

Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 0.199203

Feedback Offset Compensation/Bi-directional Feedback

Enable Singal Rectification Control

Compensation Filter Settings

Sampling Frequency: 350k Hz

Cross-over Frequency of Pole At Origin: 886.82 Hz

Pole 1: 5.652k Hz Zero 1: 801.57 Hz

Pole 2: 175k Hz Zero 2: 801.57 Hz

Frequency

Cursor (

Number

Coeffi

A-Coef

A1

A2

A3

B-Coef

B0

B1

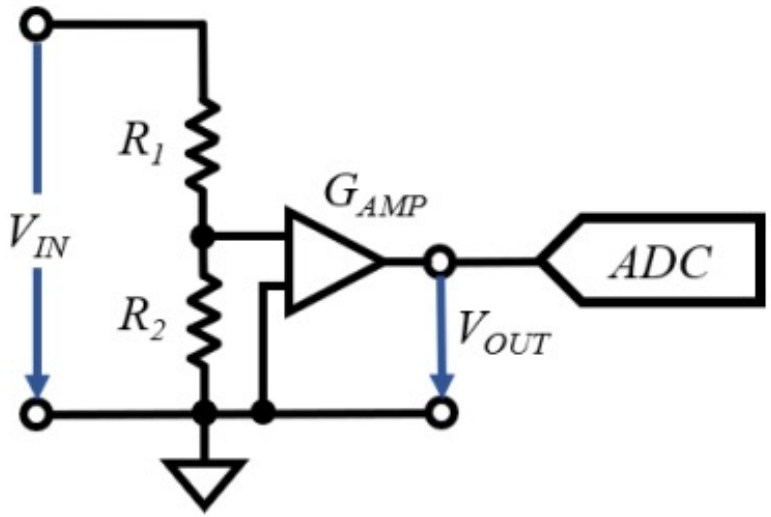
B2

B3

Input Gain Calculator

Voltage Feedback | Shunt Amplifier | Current Transformer | Digital Source

Circuit



Input Scaling

ADC Reference: 3.3 V

ADC Resolution: 12 Bit

Minimum: 0

Maximum: 4095

Differential (signed)

Calculation

Maximum Sense Voltage: 16.566 V

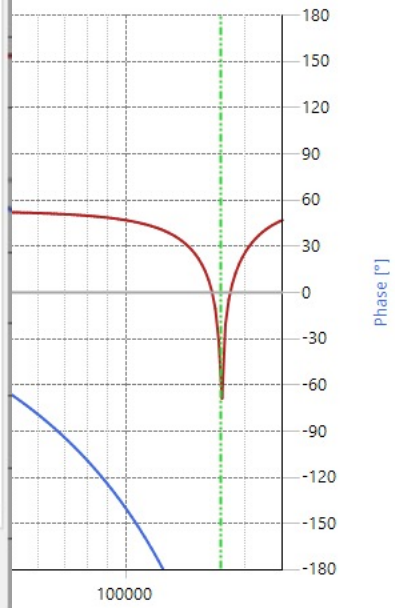
R1: 4.02k Ω

R2: 1.0k Ω

Amplifier Gain: 1.000 V/V

Signal Gain: 0.199203 V/V

OK | Cancel



Bode Plot Settings

Frequency

Start: 100 Hz

Stop: 250k Hz

Points: 400

Magnitude/Gain

Min: -60 dB

Max: 60 dB

Div: 10 dB

Phase

Min: -180 °

Max: 180 °

Div: 30 °

Options

Unwrap Phase

Show s-Domain

Show Legend

Copy Bode Data

Int	UInt	Hexadecimal	Binary
722	1,722	0x06BA	0b00000110 10111010
492	65,044	0xFE14	0b11111110 00010100
205	65,331	0xFF33	0b11111111 00110011
662	23,662	0x5C6E	0b01011100 01101110
985	42,551	0xA637	0b10100110 00110111
656	41,880	0xA398	0b10100011 10011000
991	22,991	0x59CF	0b01011001 11001111

Coefficients generated successfully

Refresh Period: 2477 ms Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 1 - Single Bit-Shift Scaling

Number Space: Q15

☑ Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 0.199203

☐ Feedback Offset Compensation/Bi-directional Feedback

☐ Enable Singal Rectification Control

Compensation Filter Settings

Sampling Frequency: 350k Hz

Cross-over Frequency of Pole At Origin: 886.82 Hz

Pole 1: 5.652k Hz Zero 1: 801.57 Hz

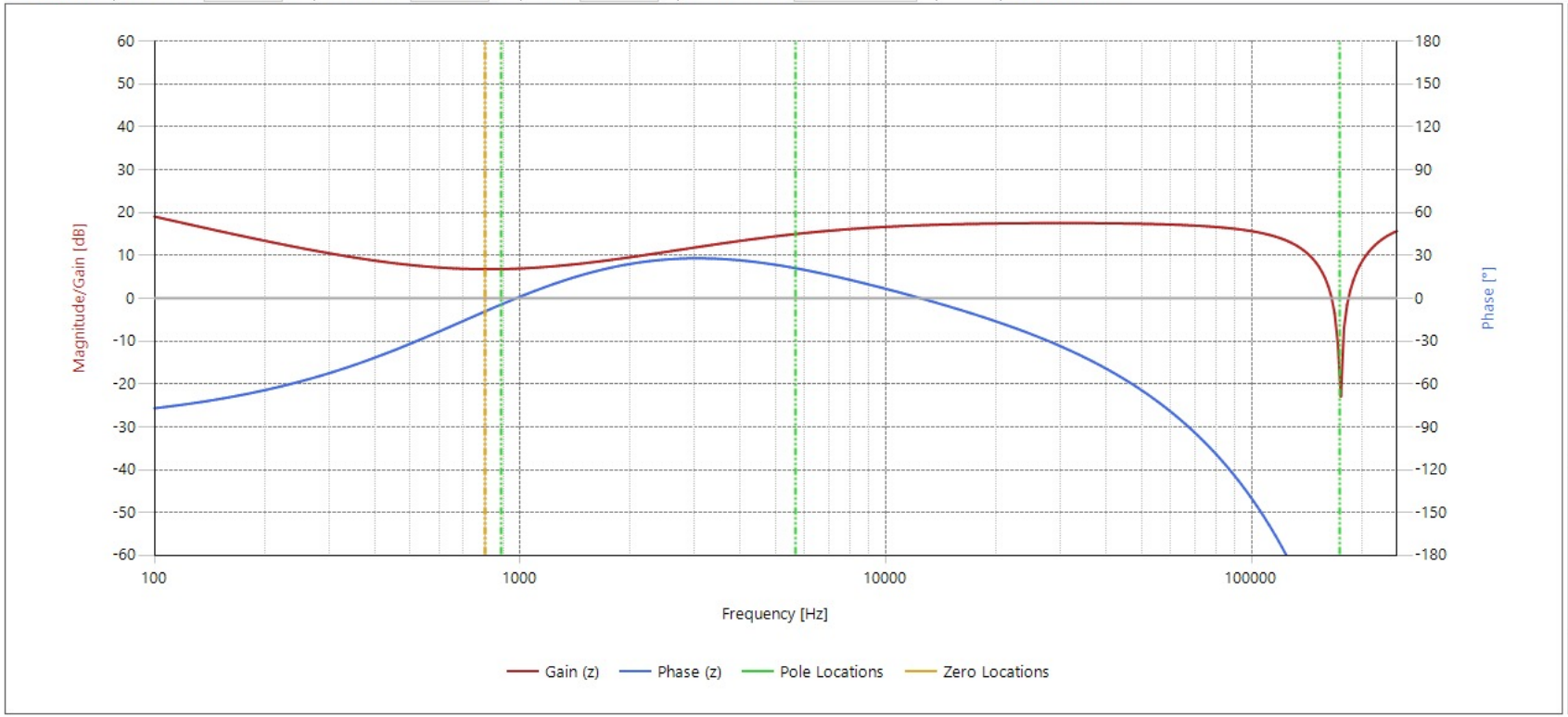
Pole 2: 175k Hz Zero 2: 801.57 Hz

MPLAB® POWERSMART™ DEVELOPMENT SUITE

Step #3: DCLD (Coefficients)

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Cursor (off): Frequency: 0 Hz Magnitude: 0 dB Phase: 0 ° Phase Errosion 0 ° Reset Scales



Bode Plot Settings

Frequency

Start: 100 Hz

Stop: 250k Hz

Points: 400

Magnitude/Gain

Min: -60 dB

Max: 60 dB

Div: 10 dB

Phase

Min: -180 °

Max: 180 °

Div: 30 °

Options

☑ Unwrap Phase

☐ Show s-Domain

☑ Show Legend

Copy Bode Data

Filter Coefficients

Number Analysis | Settings History

Coefficient	Float	Bsft-Scaler	Scaled Float	Fractional	FP Error	Int	UInt	Hexadecimal	Binary
A-Coefficients									
A1	1.681403575237150	-5	0.052543861726161	0.052551269531250	0.014%	1,722	1,722	0x06BA	0b00000110 10111010
A2	-0.480813159799046	-5	-0.015025411243720	-0.015014648437500	-0.072%	-492	65,044	0xFE14	0b11111110 00010100
A3	-0.200590415438105	-5	-0.006268450482441	-0.006256103515625	-0.197%	-205	65,331	0xFF33	0b11111111 00110011
B-Coefficients									
B0	23.106724903141200	-5	0.722085153223164	0.722106933593750	0.003%	23,662	23,662	0x5C6E	0b01011100 01101110
B1	-22.446475281837800	-5	-0.701452352557432	-0.701446533203125	-0.001%	-22,985	42,551	0xA637	0b10100110 00110111
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B3	22.451191761177300	-5	0.701599742536789	0.701629638671875	0.004%	22,991	22,991	0x59CF	0b01011001 11001111

✓ Coefficients generated successfully

Refresh Period: 2477 ms Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 4 - Fast Floating Point Coefficient Scaling

Number Space: Q15

☑ Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 0.199203

☐ Feedback Offset Compensation/Bi-directional Feedback

☐ Enable Singal Rectification Control

Compensation Filter Settings

Sampling Frequency: 350k Hz

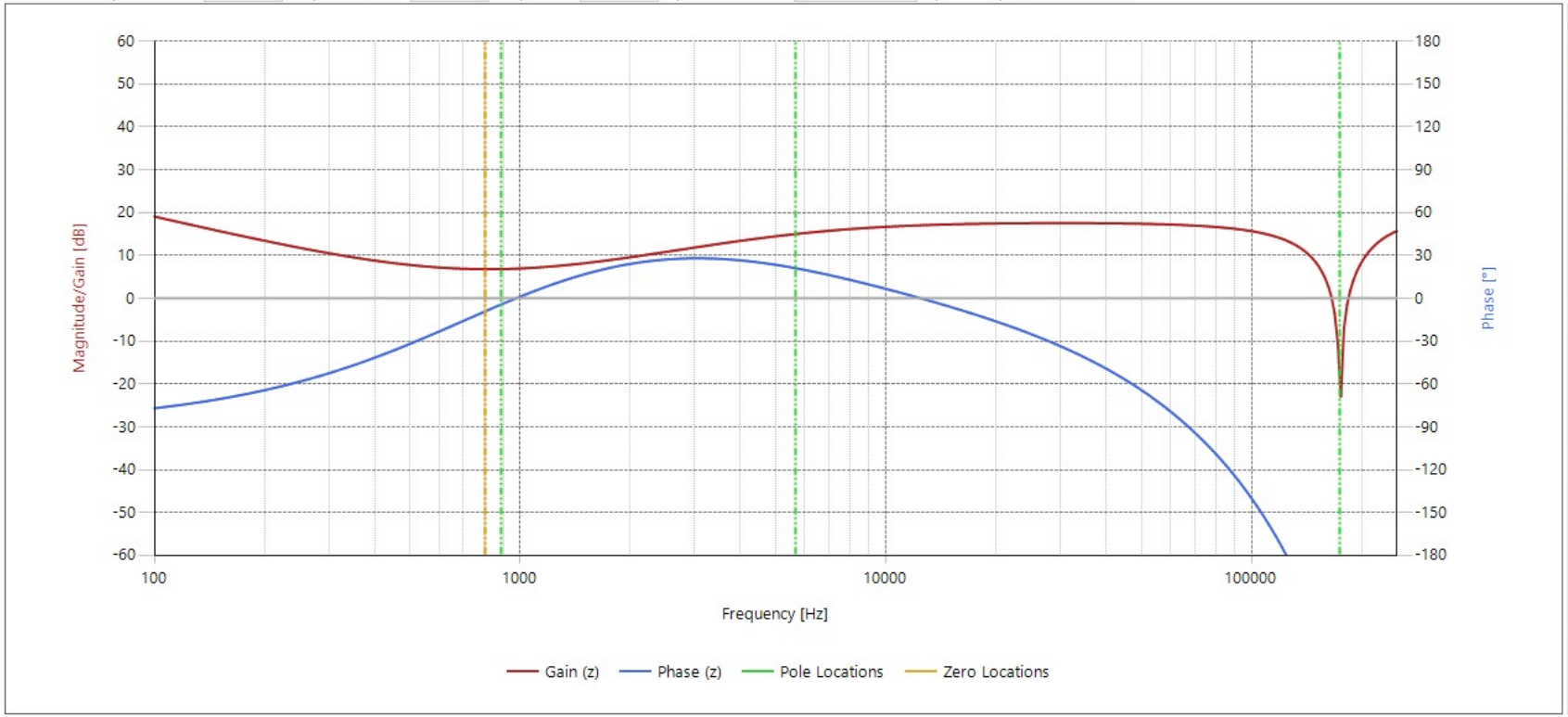
Cross-over Frequency of Pole At Origin: 886.82 Hz

Pole 1: 5.652k Hz Zero 1: 801.57 Hz

Pole 2: 175k Hz Zero 2: 801.57 Hz

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Cursor (off): Frequency: 0 Hz Magnitude: 0 dB Phase: 0 ° Phase Errosion 0 ° Reset Scales



Bode Plot Settings

Frequency

Start: 100 Hz

Stop: 250k Hz

Points: 400

Magnitude/Gain

Min: -60 dB

Max: 60 dB

Div: 10 dB

Phase

Min: -180 °

Max: 180 °

Div: 30 °

Options

☑ Unwrap Phase

☐ Show s-Domain

☑ Show Legend

Copy Bode Data

Filter Coefficients

Number Analysis | Settings History

Coefficient	Float	Bsft-Scaler	Scaled Float	Fractional	FP Error	Int	UInt	Hexadecimal	Binary
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A2	-0.480813159799046	1	-0.961626319598093	-0.961608886718750	-0.002%	-31,510	34,026	0x84EA0001	0b10000100 11101010...
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B2	-23.102008423801800	-5	-0.721937763243806	-0.721923828125000	-0.002%	-23,656	41,880	0xA398FFFB	0b10100011 10011000...
B3	22.451191761177300	-5	0.701599742536789	0.701629638671875	0.004%	22,991	22,991	0x59CFFFFB	0b01011001 11001111...

✓ Coefficients generated successfully

Refresh Period: 4380 ms Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 4 - Fast Floating Point Coefficient Scaling

Number Space: Q15

☑ Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 0.199203

☐ Feedback Offset Compensation/Bi-directional Feedback

☐ Enable Singal Rectification Control

Compensation Filter Settings

Sampling Frequency: 350k Hz

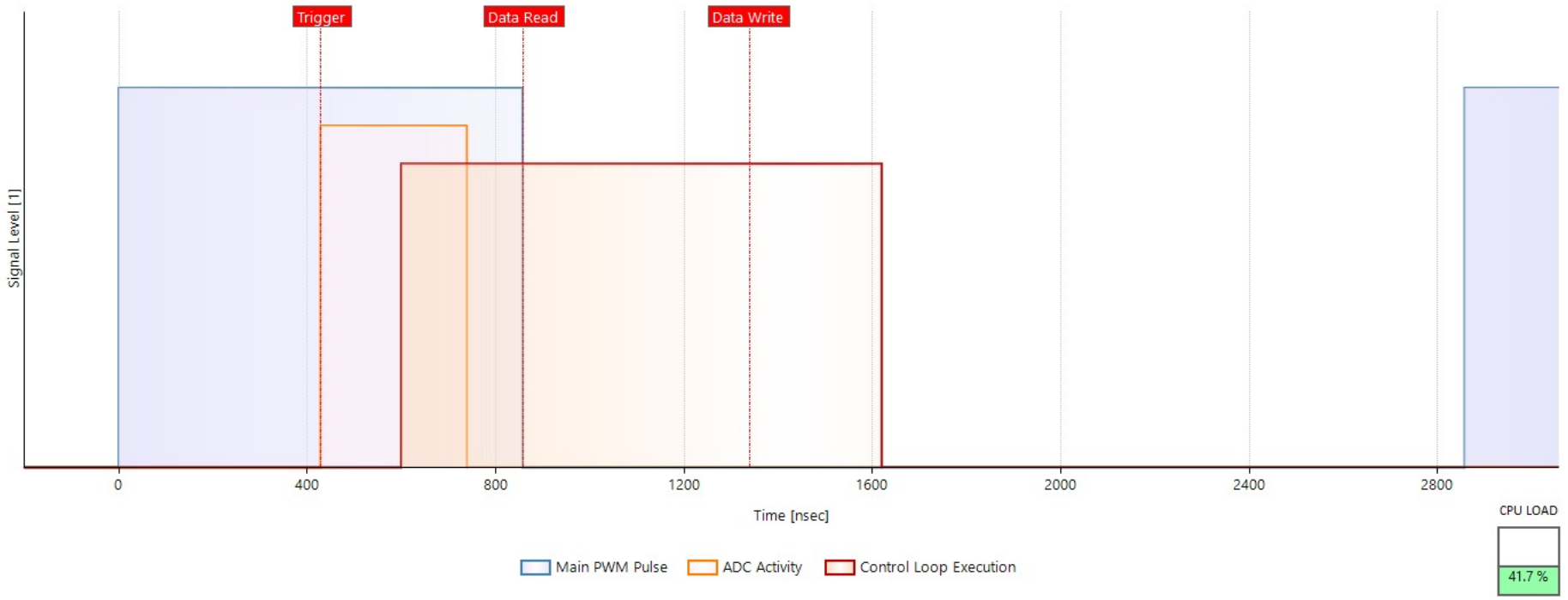
Cross-over Frequency of Pole At Origin: 886.82 Hz

Pole 1: 5.652k Hz Zero 1: 801.57 Hz

Pole 2: 175k Hz Zero 2: 801.57 Hz

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Cursor (off): Absolute: 0 nsec | Relative to ADC S&H Event: nsec 0 | Relative To Falling Edge: 0 nsec | Trigger at: 50% On-Time



Execution Timing

Control Loop Call Event: 0 - PWM Interrupt Trigger

CPU Clock: 100 MHz

PWM Frequency: 350 kHz

Duty Cycle: 30 %

ADC Latency: 310 nsec

Control Interupt Latency: 171 nsec

User Trigger Delay: 0 nsec

Total Number of Instructions:	105	
Normalized Runtime Instruction Cycles:	102	
Instruction Cycles until DATA READ:	26	
Instruction Cycles until DATA WRITEBACK:	74	
Execution Period (Loop Trigger to Exit Control Ro...	1.191	µsec
Data Capture Delay (ADC Trigger to DATA READ):	0.431	µsec
Response Delay (ADC Trigger to DATA WRITEBACK):	0.911	µsec
Relatie CPU Load:	41.7	%

✓ Saving File:

Refresh Period: 4380 ms Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

Controller Selection

Controller Type: 3P3Z - Basic Voltage Mode Compensator

Scaling Mode: 4 - Fast Floating Point Coefficient Scaling

Number Space: Q15

Normalize Input Gain

Total Input Data Length (Resolution): 12 Bit

Input Signal Gain: 0.199203

Feedback Offset Compensation/Bi-directional Feedback

Enable Singal Rectification Control

Compensation Filter Settings

Sampling Frequency: 350k Hz

Cross-over Frequency of Pole At Origin: 886.82 Hz

Pole 1: 5.652k Hz Zero 1: 801.57 Hz

Pole 2: 175k Hz Zero 2: 801.57 Hz

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Assembly Source File | API C-Source File | API C-Header File | NPNZ16b Library Header File | NPNZ16b Library Include File | Example Code

Controller Configuration Template

Include unused settings | Copy to Clipboard

Step #4: Compensator

```
/* ************************************************************************
 * 3p3z Controller Configuration Code Example
 * ************************************************************************
 *
 * The following code example covers all user-defined configurations of the
 * control object 'VCOMP' required to run the recently configured controller.
 *
 * Please note:
 * This is no executable code and serves only as template for the integration into
 * a proprietary firmware project. You can copy & paste this entire code example
 * to your code project by clicking the 'Copy to Clipboard' above or pick specific
 * section by selecting a text section and pressing <CTRL>+'C'.
 *
 * Once code has been copied to user code, each setting has to be configured by
 * replacing the placeholders <[data type]> in each code line by your individual
 * configuration values.
 *
 * This code example only lists configurations of features which have been selected
 * in this tool. Enabling/disabling code generation options may also change the
 * contents of this code example. Unused options are EXCLUDED from this code example.
 *
 * ************************************************************************/

// Standard Include Files
#include <stdint.h>                         // include standard integer data types
#include <stdbool.h>                        // include standard boolean data types
#include <stddef.h>                         // include standard definition data types

// 3p3z Controller Include Files
#include "VCOMP.h"                          // include 'VCOMP' controller header file

volatile uint16_t VCOMP_ControlObject_Initialize(void)
{
    volatile uint16_t retval = 0;           // Auxiliary variable for function call verification (initially set to ZERO = false)

    /* Controller Input and Output Ports Configuration */

    // Configure Controller Primary Input Port
```

Output

```
>WRITEBACK delay: 1057.14285714286 ns
>timing chart update completed successfully (60 ms)
>CPU clock setting: 100 MHz
>Execution period: 1020 ns
>DATA READ delay: 260 ns
>WRITEBACK delay: 740 ns
>timing chart update completed successfully (43 ms)
```

Saving File:

Refresh Period: 4380 ms | Table Options

PowerSmart Digital Control Library Designer v1.9.14.683 - [\\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example Code\Full Digital Power\FDP_LabX.X\DCLD\New PowerSmart Project.psproj]

File View Tools ?

Save | Coefficients | Bode Settings | Timing | Refresh Charts | Configuration | Update Code | Export Files | Help

MPLAB® X Project: \\Mac\Home\Desktop\Working Folder\PowerSmartReview\Example C

Controller | Source Code Configuration | Advanced

File & Function Label

Name Prefix: VCOMP

Context Management

- Save/Restore Shadow Registers
- Save/Restore MAC Working Registers
- Save/Restore Accumulators
  - Save/Restore Accumulator A
  - Save/Restore Accumulator B
- Save/Restore DSP Core Configuration
- Save/Restore Core Status Register

Used Resources: WREG 0,1,2,3,4,5,6,8,10/ACC AB

Basic Feature Extensions

- Store/Reload Result Accumulator
- Add DSP Core Configuration
- Add Enable/Disable Feature
  - Always read from source when disabled
- Add Error Normalization
- Add Automatic Placement of Primary ADC Trigger A
- Add Automatic Placement of Secondary ADC Trigger B

Automated Data Interface

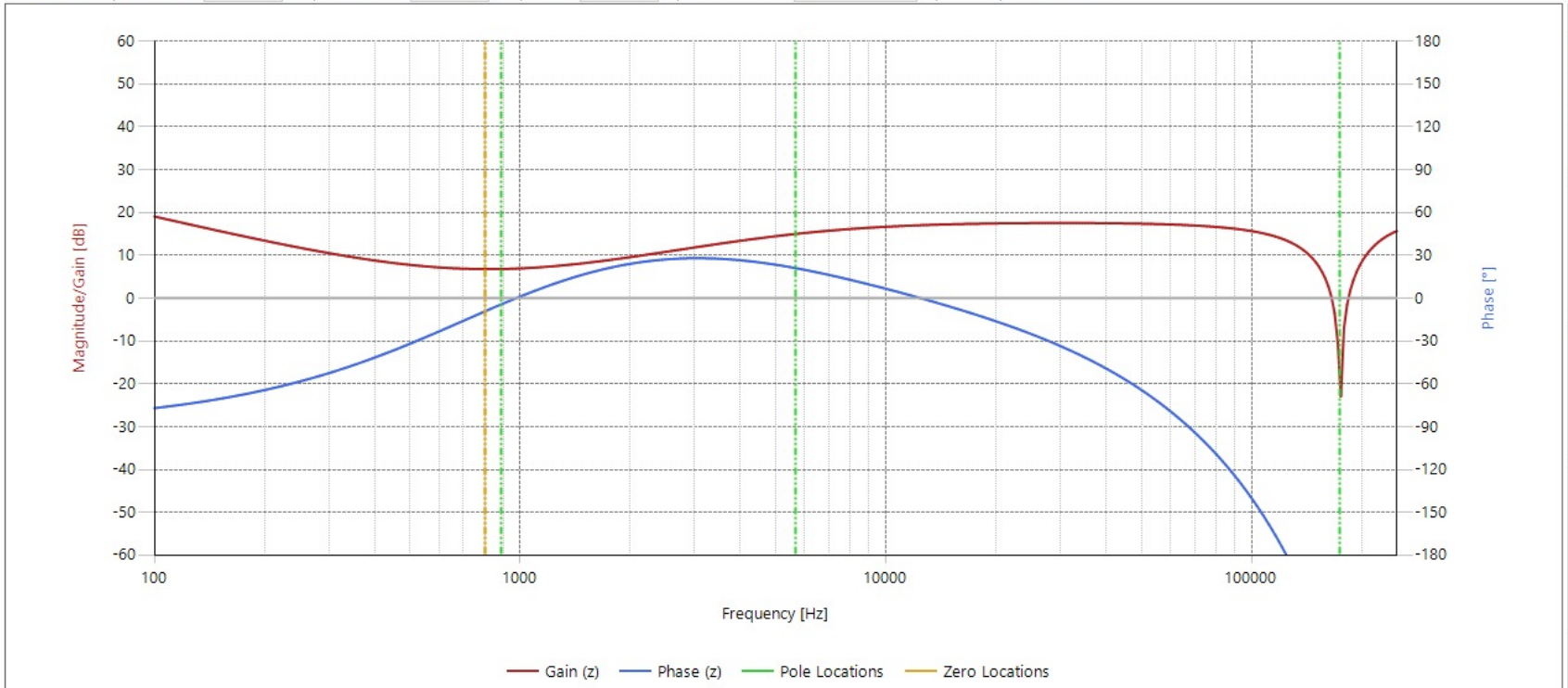
Data Provider Sources

Anti-Windup

- Limit Control Loop Output to Positive Numbers
  - Anti Windup Limiter Number Range: -32768...32767
- Clamp Control Output Maximum
  - Generate Upper Saturation Status Flag Bit
- Clamp Control Output Minimum
  - Force Values below Minimum Threshold to Zero
  - Generate Lower Saturation Status Flag Bit

Frequency Domain | Time Domain | Block Diagram | Source Code Output | Info

Cursor (off): Frequency: 0 Hz Magnitude: 0 dB Phase: 0 ° Phase Erosion 0 ° Reset Scales



Bode Plot Settings

Frequency
- Start: 100 Hz
- Stop: 250k Hz
- Points: 400

Magnitude/Gain
- Min: -60 dB
- Max: 60 dB
- Div: 10 dB

Phase
- Min: -180 °
- Max: 180 °
- Div: 30 °

Options
- Unwrap Phase
- Show s-Domain
- Show Legend

Copy Bode Data

Filter Coefficients

Number Analysis | Settings History

Coefficient	Float	Bsft-Scaler	Scaled Float	Fractional	FP Error	Int	UInt	Hexadecimal	Binary
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A2	-0.480813159799046	1	-0.961626319598093	-0.961608886718750	-0.002%	-31,510	34,026	0x84EA0001	0b10000100 11101010...
A3	-0.200590415438105	2	-0.802361661752421	-0.802337646484375	-0.003%	-26,291	39,245	0x994D0002	0b10011001 01001101...
B-Coefficients									
B0	23.106724903141200	-5	0.722085153223164	0.722106933593750	0.003%	23,662	23,662	0x5C6EFFFB	0b01011100 01101110...
B1	-22.446475281837800	-5	-0.701452352557432	-0.701446533203125	-0.001%	-22,985	42,551	0xA637FFFB	0b10100110 00110111...
B2	-23.102008423801800	-5	-0.721937763243806	-0.721923828125000	-0.002%	-23,656	41,880	0xA398FFFB	0b10100011 10011000...
B3	22.451191761177300	-5	0.701599742536789	0.701629638671875	0.004%	22,991	22,991	0x59CFFFFB	0b01011001 11001111...

Coefficients generated successfully

Refresh Period: 1129 ms Table Options

Weibinar* - Bode Analyzer Suite

File | Home | Measurement | View | Cursor

Add Cursor | Add Delta Cursor | Stability margin calculation | Select trace: PowerSmart-D... | Track margins | Find margins | Cursor 1 Phase margin: 54.579 ° | Cursor 2 Gain margin: 9.608 dB | Cursor 3 Stability margin: 0.587 | Link cursors | Cursor distance: Decade (10) | Cursor A: New cursor | Cursor B: New cursor

Cursors | Cursor Calculation | Linked cursors

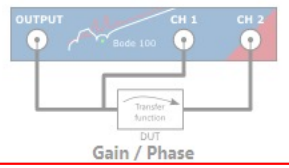
Frequency Sweep Fixed

Start frequency: 100 Hz
Stop frequency: 400 kHz
Center: 200.05 kHz
Span: 399.9 kHz
Get from zoom
Sweep: Linear / Logarithmic
Number of points: 401

Level: Constant / Variable
Source level: -10 dBm

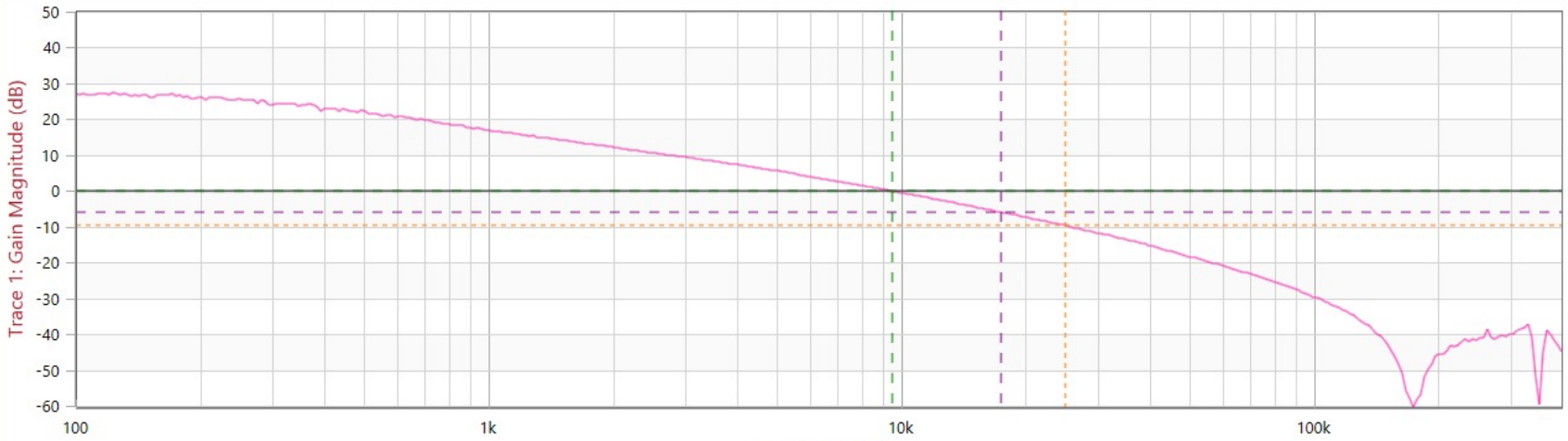
Attenuator: Receiver 1: 0 dB | Receiver 2: 0 dB

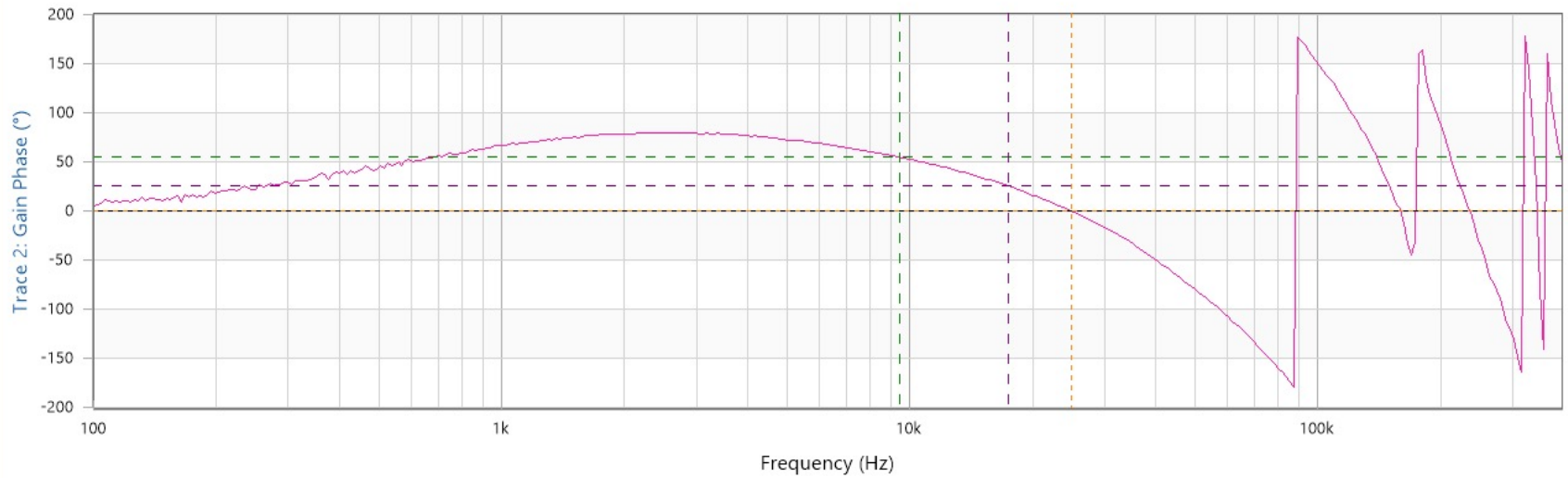
Receiver bandwidth: 30 Hz



Gain / Phase

	Frequency	PowerSmart-D...	PowerSmart-D...
Cursor 1	9.482 kHz	0 dB	54.579 °
Cursor 2	24.962 kHz	-9.608 dB	0 °
Cursor 3	17.47 kHz	-5.948 dB	25.432 °





Trace 1
Measurement: Gain
Display: Memory
Format: Magnitude (dB)
Y_{max}: 50 dB
Y_{min}: -60 dB

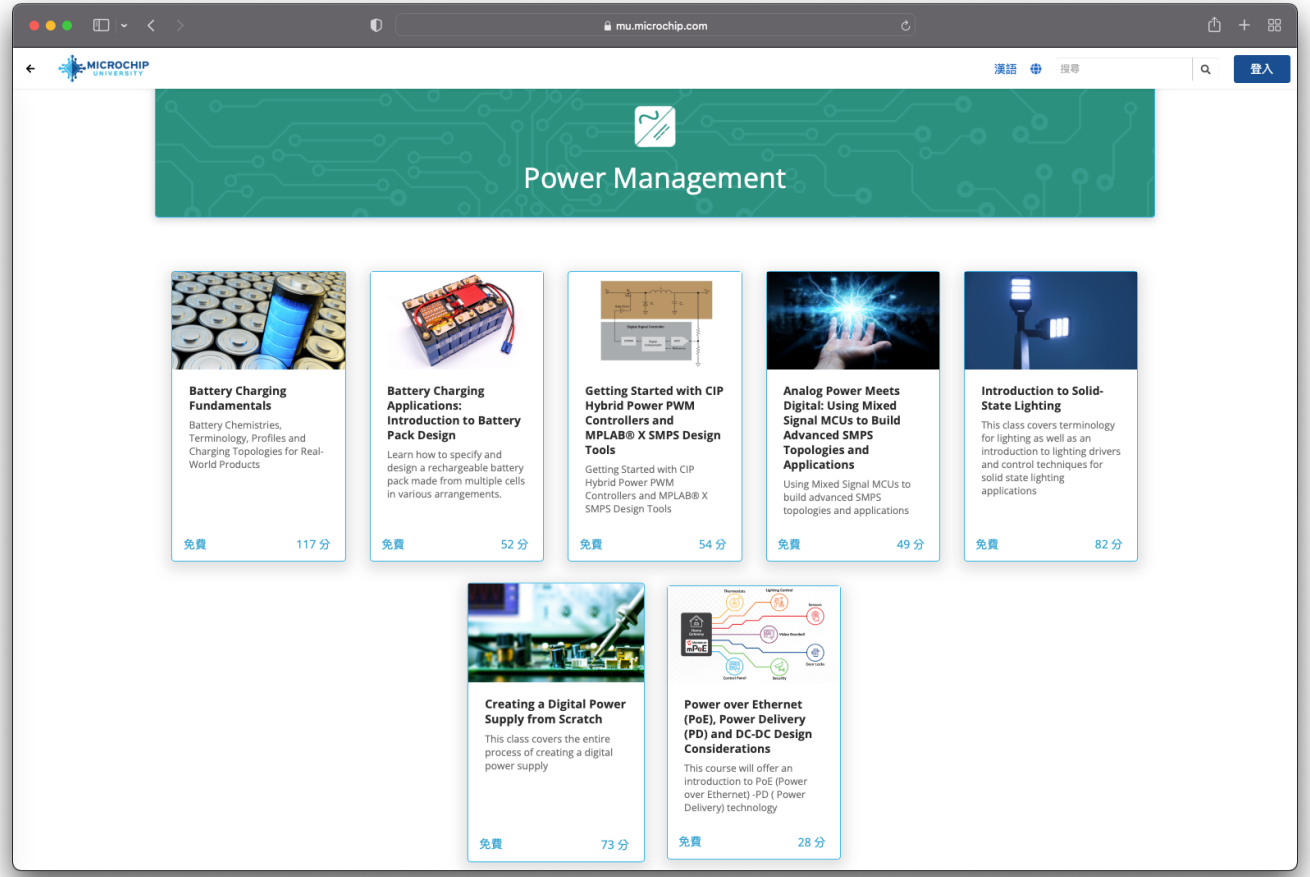
Trace 2
Measurement: Gain
Display: Memory
Format: Phase (°)
Unwrap phase
Y_{max}: 200 °
Y_{min}: -200 °

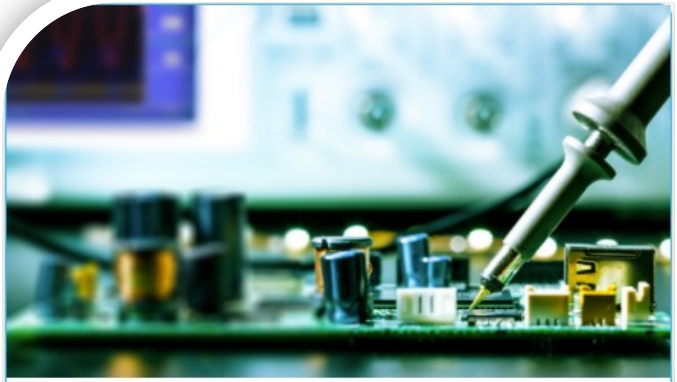
PowerSmart-DCLD (Mode 4)

Measurement → new memory

Training Courses For Power Management

- **Microchip University – Power Management**
  - https://mu.microchip.com/page/power-management





Creating a Digital Power Supply from Scratch

This class covers the entire process of creating a digital power supply

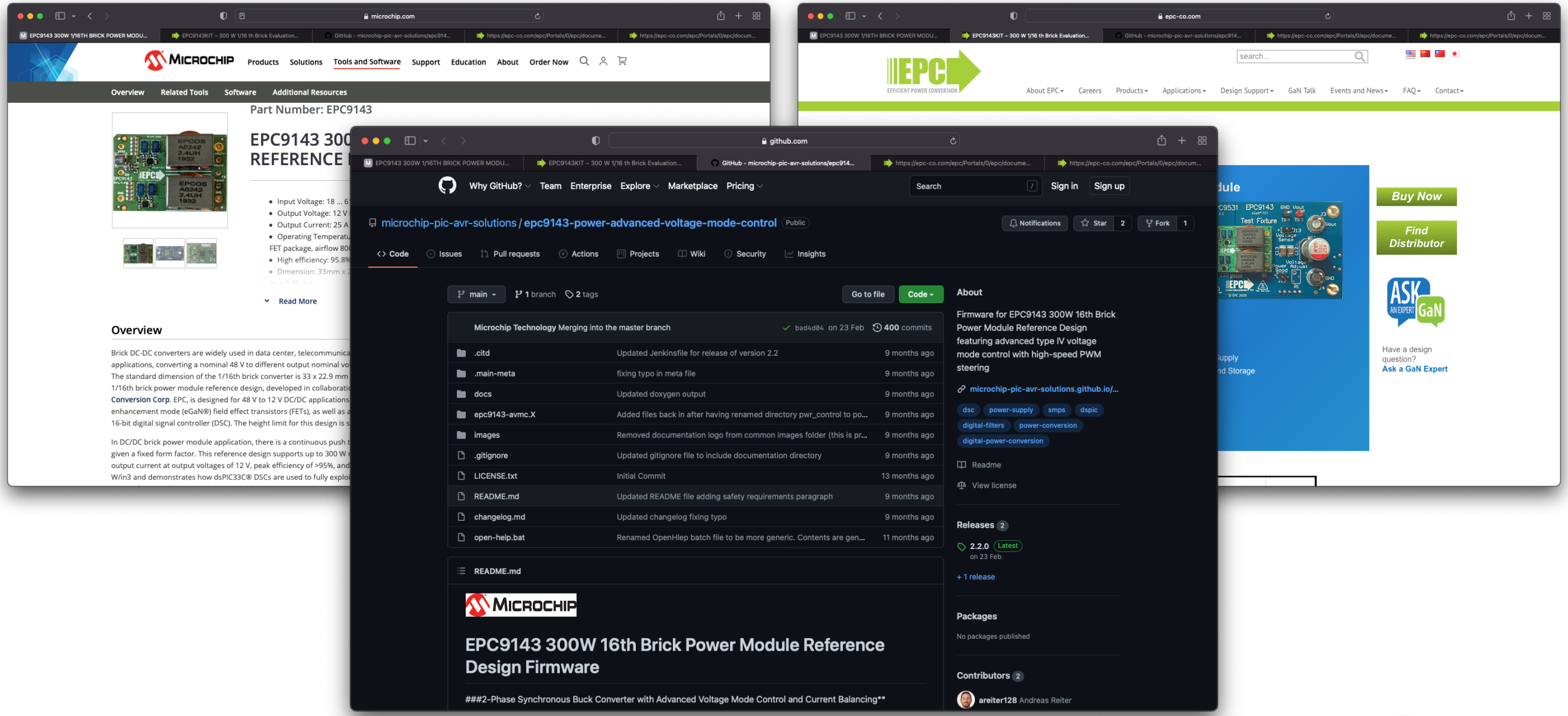
MPLAB® POWERSMART™ DEVELOPMENT SUITE Is HERE!!

免費 73 分

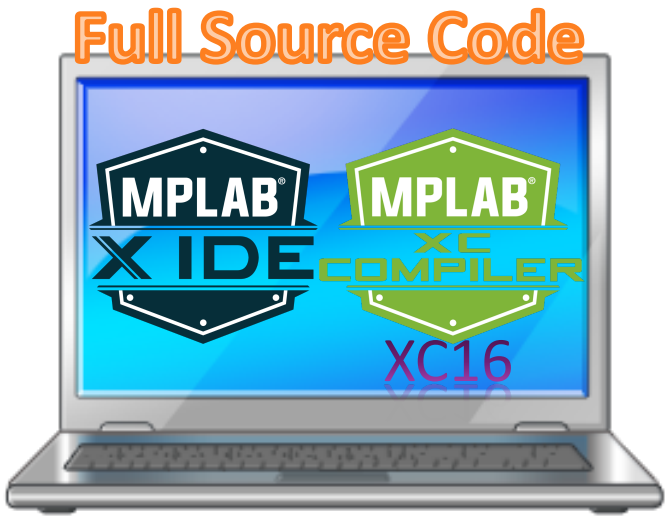
More Resources Regarding PowerSmart™

Programing

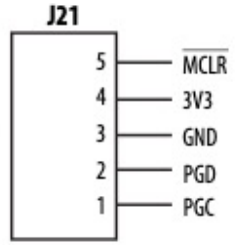
Searching F/W On Microchip or EPC Website

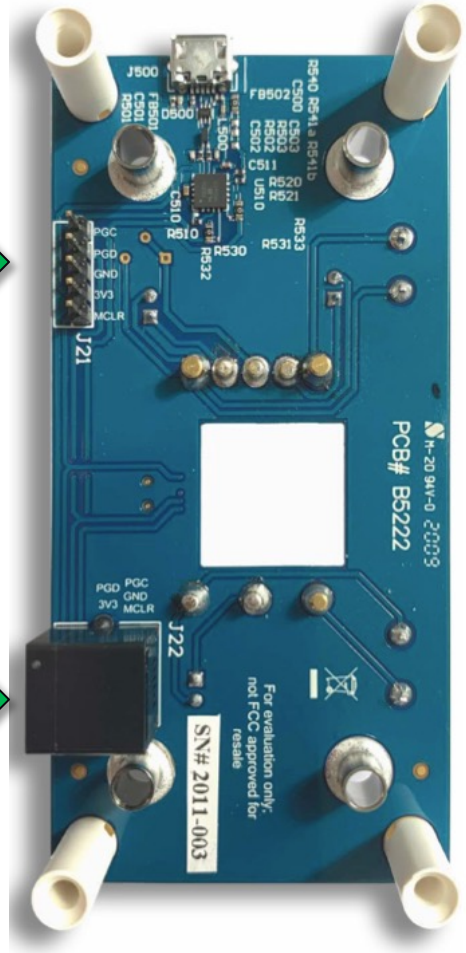


Connections



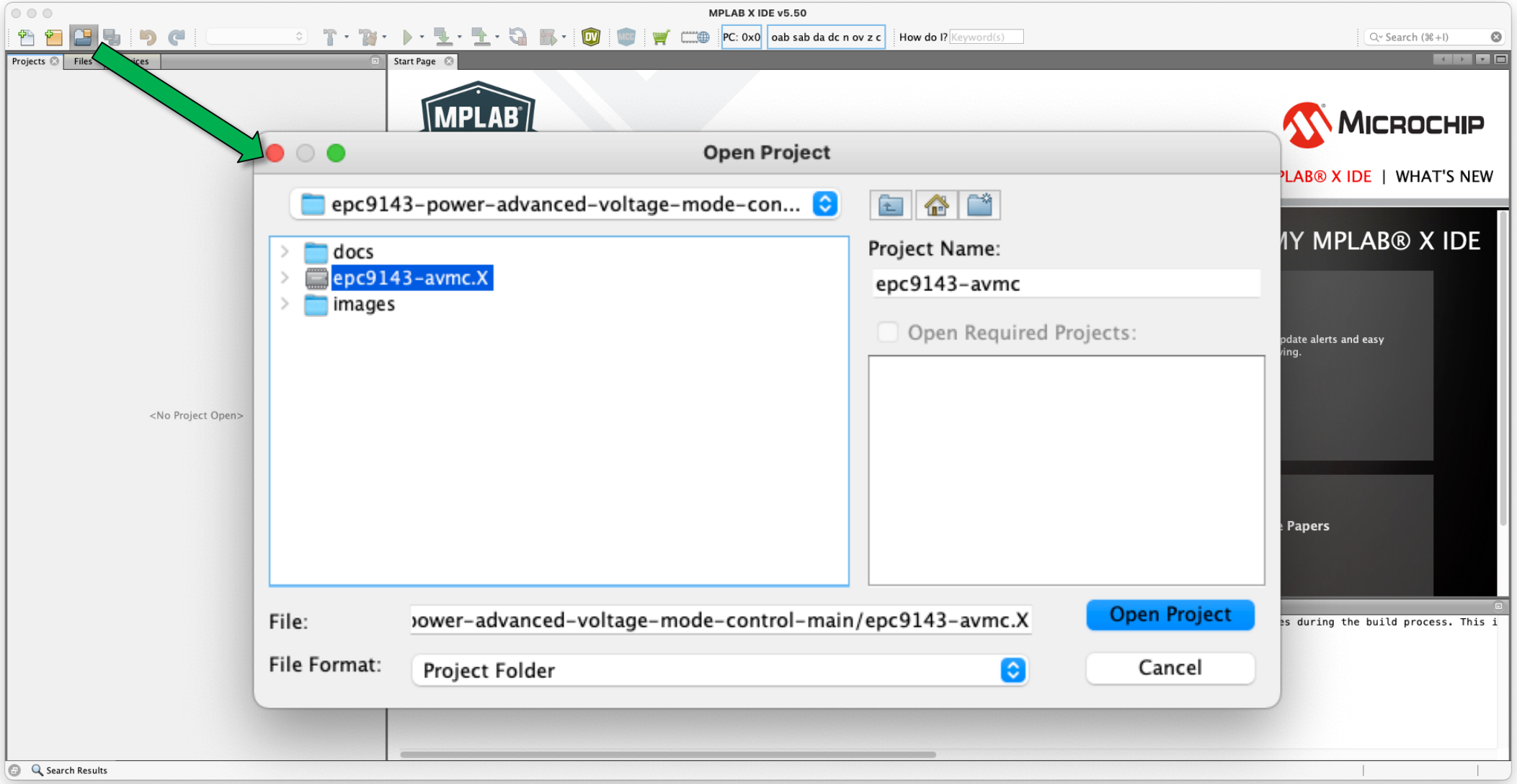
In-Circuit Debugger





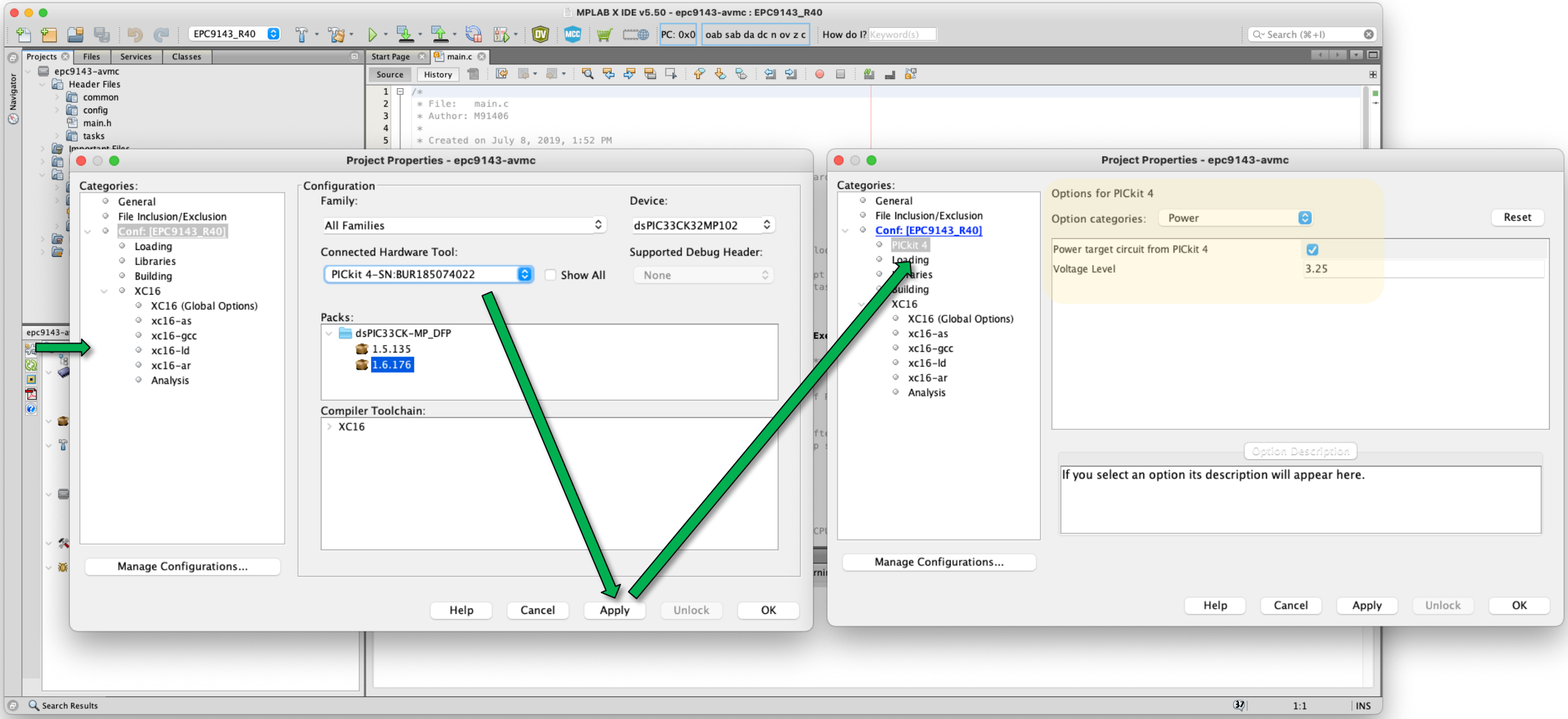
MICROCHIP

Coding & Programing With MPLAB X IDE

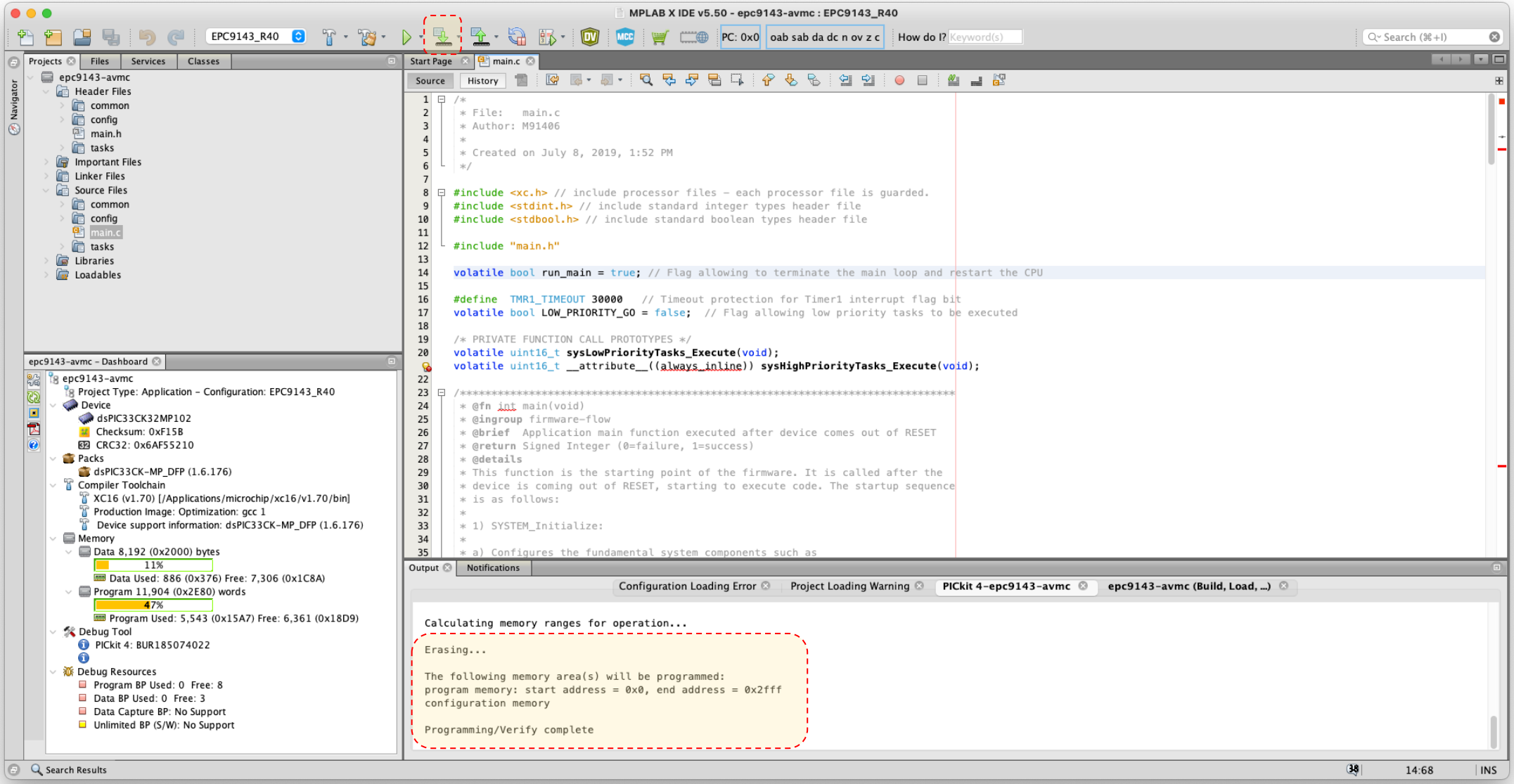


MICROCHIP

Coding & Programing With MPLAB X IDE



Coding & Programing With MPLAB X IDE



Digital Power Reference Design

Vienna PFC Reference Design

The primary stage of a High-speed EV Charger

- 30 kW Vienna rectifier topology
- 98.5 % peak efficiency
- 3-phase 380/400 VAC, 50 Hz/60 Hz input voltage
- <5 % current THD at half and full loads
- Microchip 700 V, 15 mOhm SiC MOSFETs mounted on AVVID MaxClip heat sinks to reduce communication loop inductance and voltage spikes across devices
- PCB design according to IEC standards, with consideration for safety, current stress, mechanical stress, and noise immunity
- dsPIC33CH controller with verified open-source software using 3-level modulation for digital control

Matching 30 kW LLC charger in development

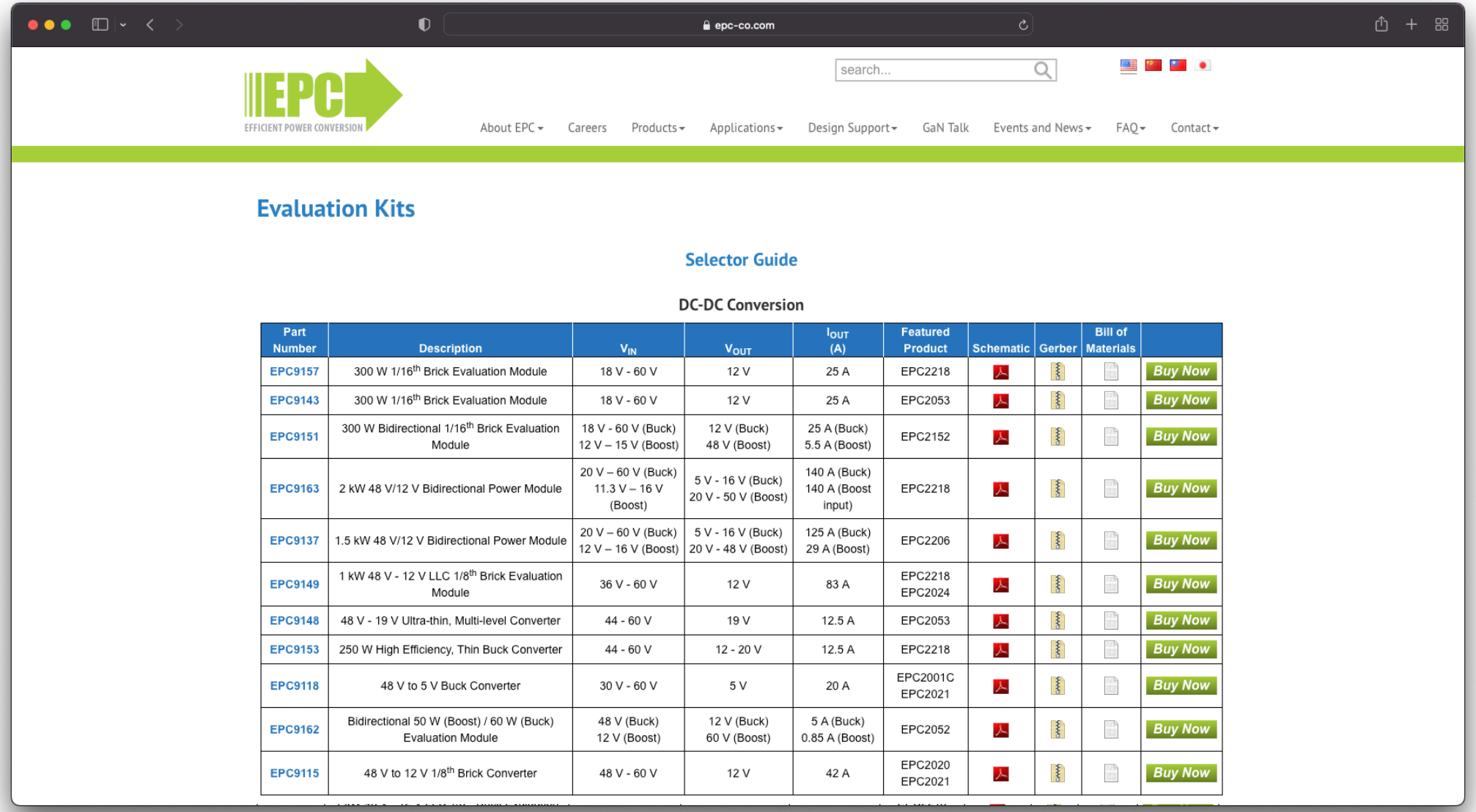
Transphorm's 4 kW Bridgeless Totem-Pole PFC

dsPIC33CK and Transphorm's SuperGaN™

- **> 99% peak efficiency**
- **< 2% THDv with < 3% THDi noise distortion**
- **> 0.99 PF**
- **Zero Load / High Load startup ability**

Test Setup and Conditions	
Evaluation Kit	TDTTP4000W066C-KIT
Operating frequency	66 kHz
Input voltage	85 Vac to 265 Vac
Output voltage	385 Vdc ±5%
Digital power PIM	dsPIC33CK256MP506
GaN device	TP65H035G4WS
Gate resistor	30Ω
Gate ferrite bead	200Ω @ 100 MHz

EPC Evaluation Kits With dsPIC33



Evaluation Kits

Selector Guide

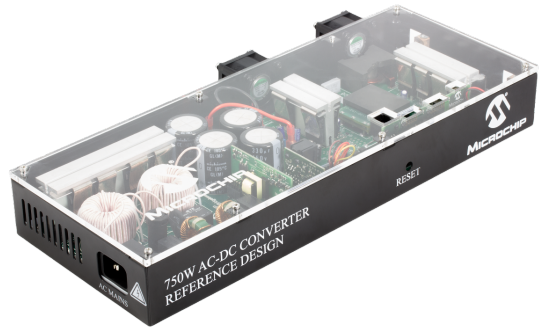
DC-DC Conversion

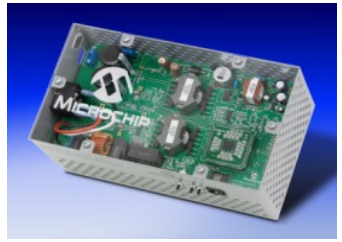
Part Number	Description	V_{IN}	V_{OUT}	I_{OUT} (A)	Featured Product	Schematic	Gerber	Bill of Materials	
EPC9157	300 W 1/16th Brick Evaluation Module	18 V - 60 V	12 V	25 A	EPC2218				Buy Now
EPC9143	300 W 1/16th Brick Evaluation Module	18 V - 60 V	12 V	25 A	EPC2053				Buy Now
EPC9151	300 W Bidirectional 1/16th Brick Evaluation Module	18 V - 60 V (Buck) 12 V – 15 V (Boost)	12 V (Buck) 48 V (Boost)	25 A (Buck) 5.5 A (Boost)	EPC2152				Buy Now
EPC9163	2 kW 48 V/12 V Bidirectional Power Module	20 V – 60 V (Buck) 11.3 V – 16 V (Boost)	5 V - 16 V (Buck) 20 V - 50 V (Boost)	140 A (Buck) 140 A (Boost input)	EPC2218				Buy Now
EPC9137	1.5 kW 48 V/12 V Bidirectional Power Module	20 V – 60 V (Buck) 12 V – 16 V (Boost)	5 V - 16 V (Buck) 20 V - 48 V (Boost)	125 A (Buck) 29 A (Boost)	EPC2206				Buy Now
EPC9149	1 kW 48 V - 12 V LLC 1/8th Brick Evaluation Module	36 V - 60 V	12 V	83 A	EPC2218 EPC2024				Buy Now
EPC9148	48 V - 19 V Ultra-thin, Multi-level Converter	44 - 60 V	19 V	12.5 A	EPC2053				Buy Now
EPC9153	250 W High Efficiency, Thin Buck Converter	44 - 60 V	12 - 20 V	12.5 A	EPC2218				Buy Now
EPC9118	48 V to 5 V Buck Converter	30 V - 60 V	5 V	20 A	EPC2001C EPC2021				Buy Now
EPC9162	Bidirectional 50 W (Boost) / 60 W (Buck) Evaluation Module	48 V (Buck) 12 V (Boost)	12 V (Buck) 60 V (Boost)	5 A (Buck) 0.85 A (Boost)	EPC2052				Buy Now
EPC9115	48 V to 12 V 1/8th Brick Converter	48 V - 60 V	12 V	42 A	EPC2020 EPC2021				Buy Now

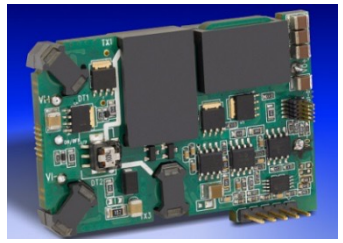
Royalty-Free* Reference Designs

Available Today

- **750W AC/DC Supply**
  - *Semi-Bridgeless PFC*
  - *Zero Voltage Switching Full-Bridge with Peak Current Mode Control using Digital Slope Compensation and Synchronous Rectification*
- **720W Platinum-rated AC/DC Supply**
  - *IPFC + interleaved 2-switch forward conv with SR*
  - *Adaptive algorithms to achieve > 94% efficiency*
- **Enhanced Solar Micro Inverter**
  - *250W panel input, grid-tied output*
  - *MPPT to achieve 94.5% efficiency (peak)*
- **1 KW Pure Sine Wave UPS**
  - *Offline UPS system*
  - *Push-pull converter & full-bridge inverter*
- **Interleaved Power Factor Correction**
  - *Two phase interleaved PFC*
  - *Up to 400VDC output, 350W sustained*
- **DC/DC LLC Resonant Converter**
  - *Zero Voltage Switching on half-bridge conv*
  - *Zero Current Switching on synch rectifier. >95% eff*
- **Quarter Brick DC/DC Converter**
  - *Phase-shifted full-bridge topology*
  - *Planar magnetics and non-linear control for efficiency*







*Royalty-free when used in accordance with Microchip's licensing agreement

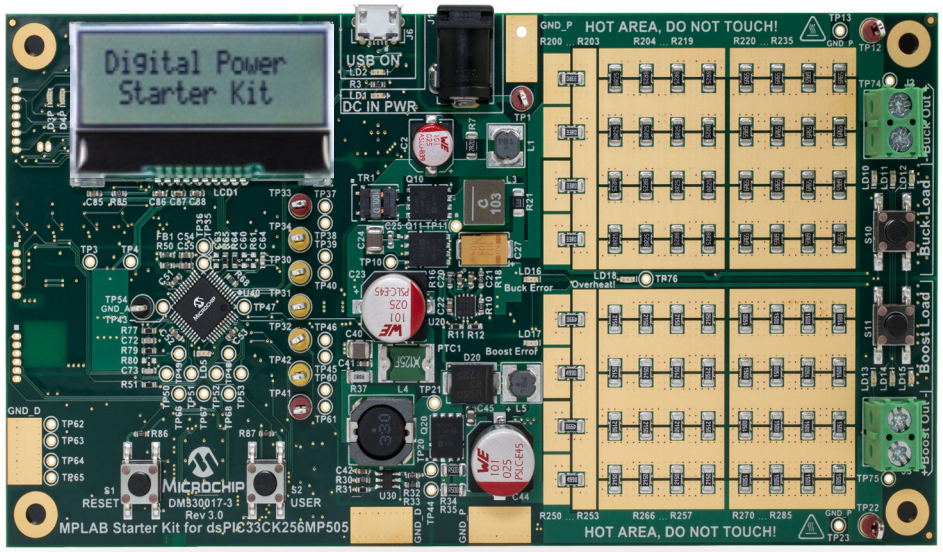
MPLAB® Starter Kit for Digital Power -3

Features:

- dsPIC33CK256MP based
- Independent buck and boost DC/DC converters
- LCD display, status LEDs, temperature sensors
- Configurable resistive loads
- PKOB-4 On-board debugging / programming via USB

Package Contents:

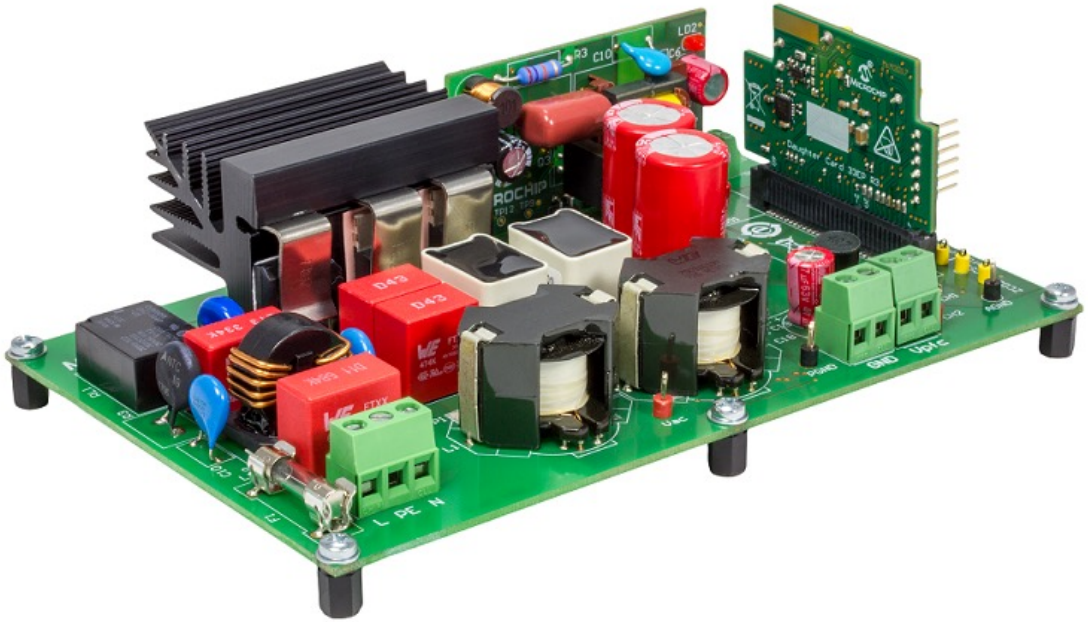
- Board (~ 5” x 2.5”)
- Mini USB cable
- 9V Power Supply
- Info Sheet with schematic



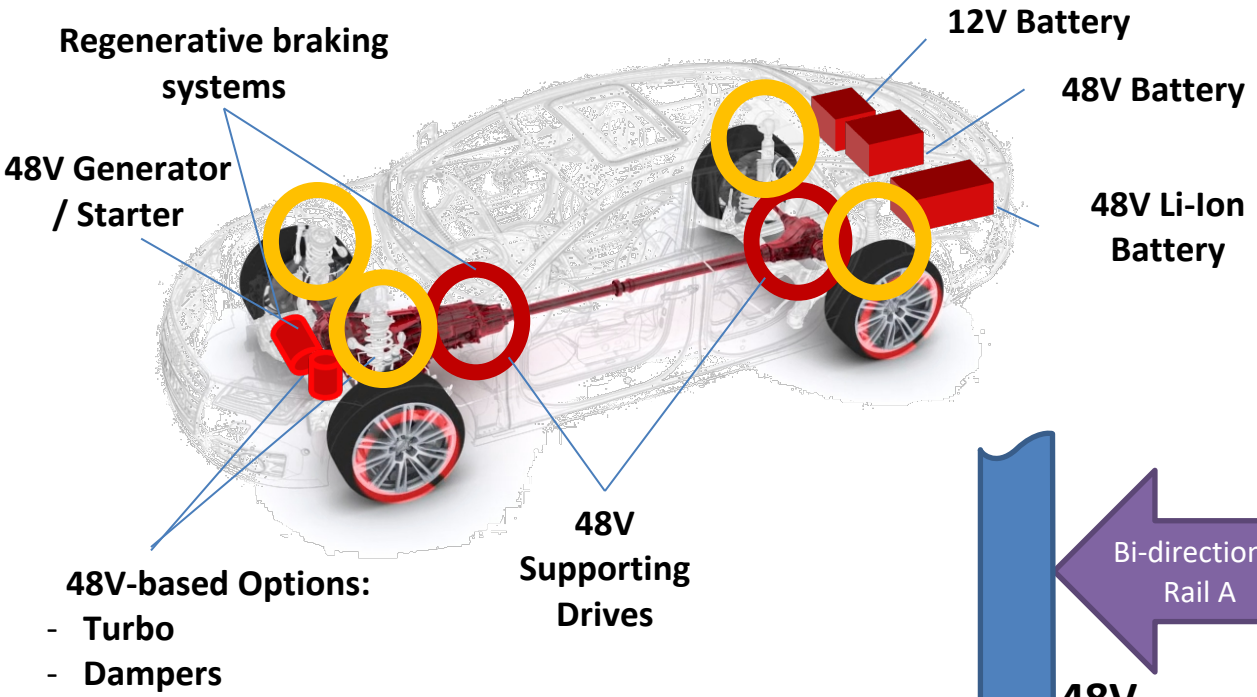
Part # DM330017-3

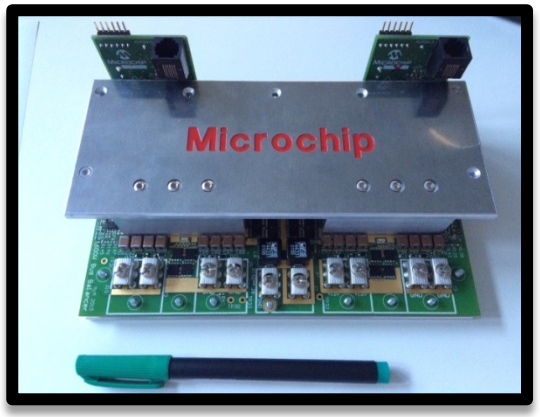
LV PFC Development Board

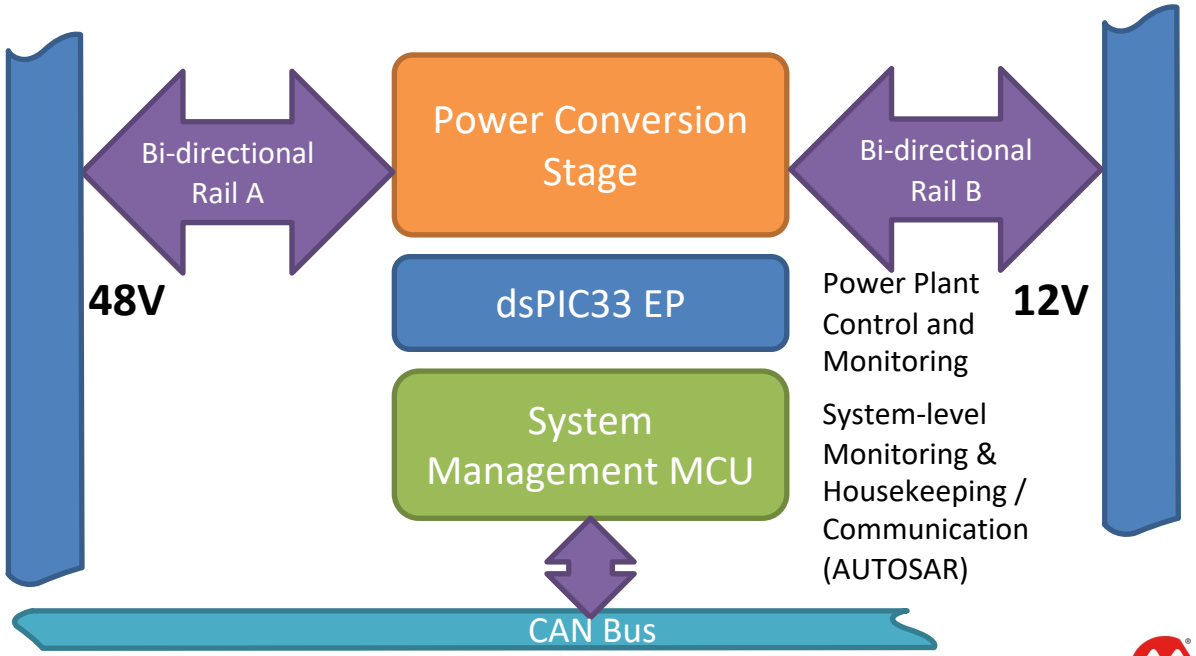
- **Low Voltage PFC**
  - Vin: 12 - 24V AC
  - Vout: 31 - 42V DC
  - ~50W Max
- **Topology**
  - Single phase or
    Interleaved dual phase
  - Firmware for:
    - Continuous Conduction Mode
    - Critical Conduction Mode (a.k.a. Transition Mode or Boundary Mode)
- **Uses DP PIM controller modules**
- **Companion DC/DC Interleaved LLC Development Board In Development**
- **Part # DV330101**



Automotive Bidirectional DC/DC Bus Converter







May The *Power* Be With You