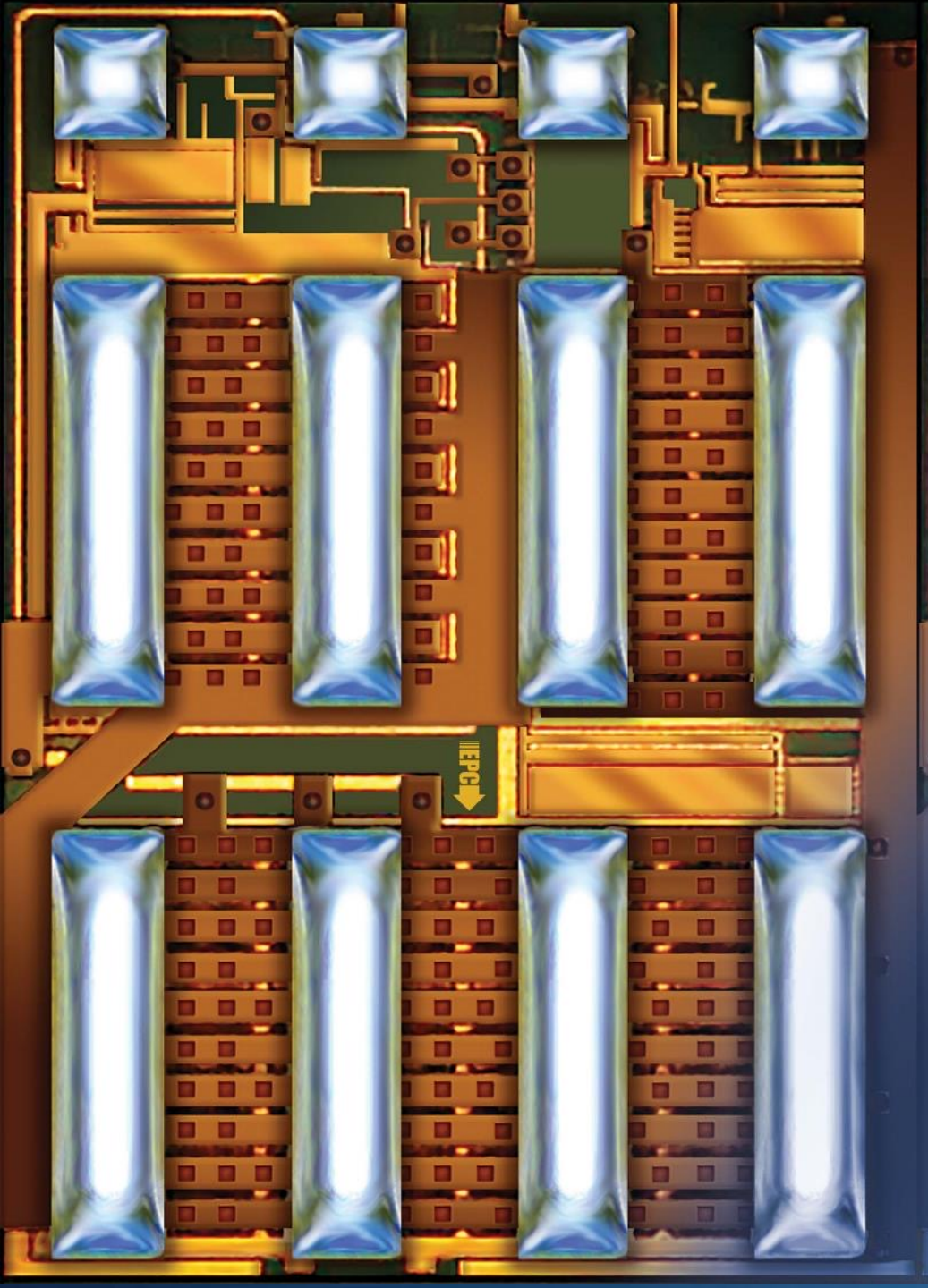
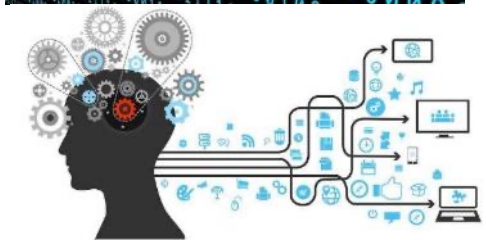


A 1 kW eGaN FET-based LLC Resonant Converter in a ⅛th Power Brick Size

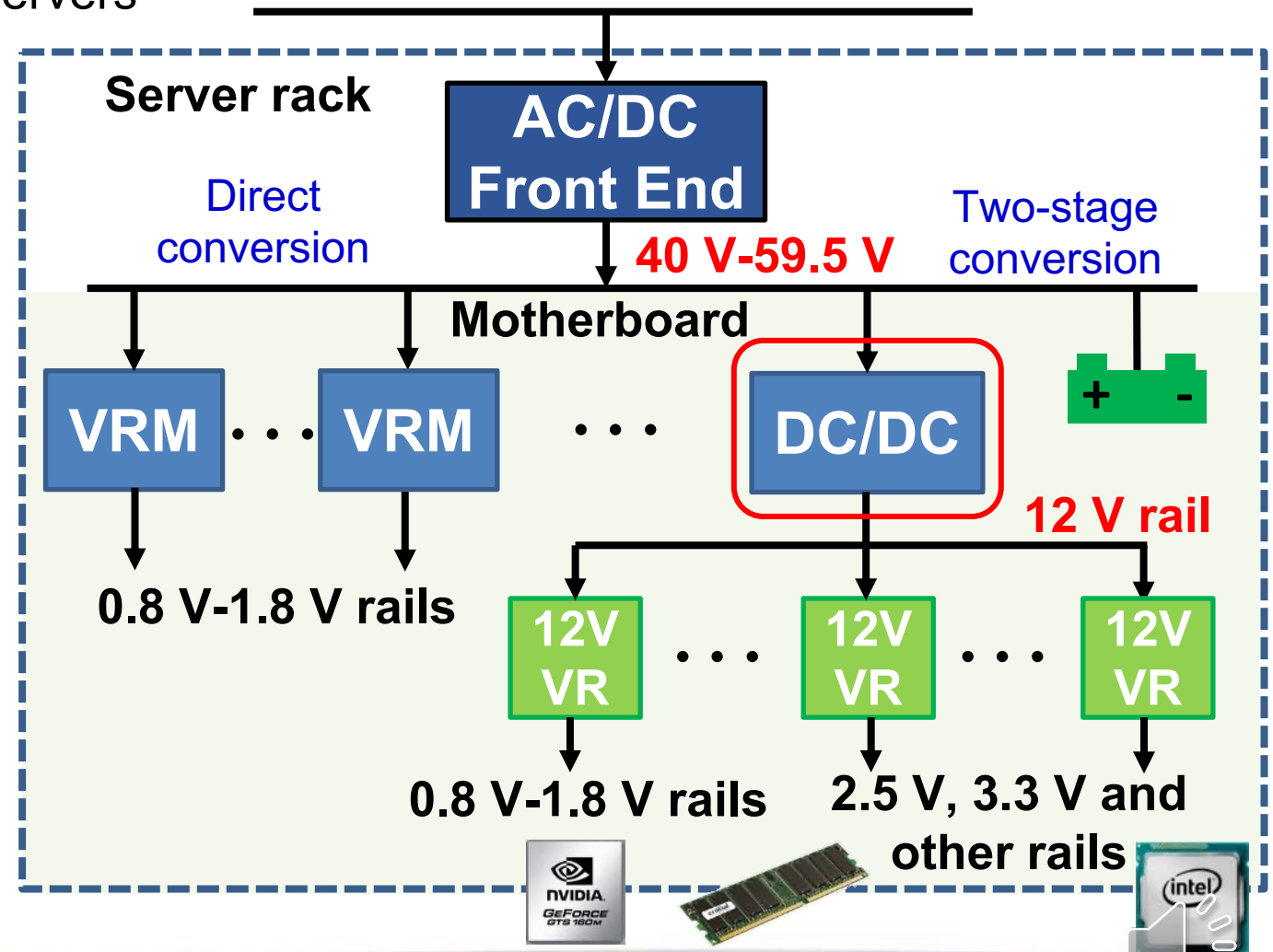
EFFICIENT POWER CONVERSION

Market Trends Leading to 48V Rack Power Architecture

AI adoption, 5G, Big Data, Cloud Servers



- High power demand
- Higher power per board
- Higher component density
- Migration to on board 48V
- Premium for density

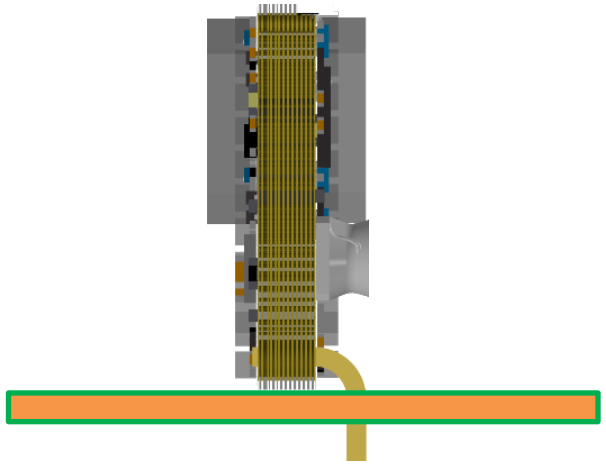


Specifications

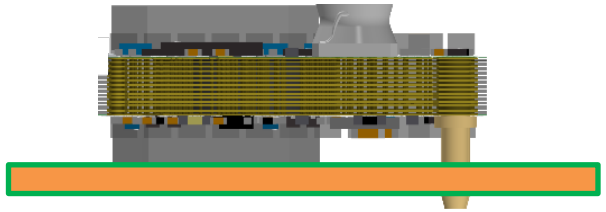
Specification	Min.	Nom.	Max.	Units
Input Voltage	36	48	60	Volts
Output Voltage	9	12	15	Volts
Output Power		1000		Watt
Switching frequency		1		MHz
Total thickness			*10	mm
Cooling Air-Flow			400	LFM
Size (X & Y)			‡58.4 x 22.9	mm

‡ Standard DOSA ⅛th Brick converter size
* Excluding heatsink

- Horizontal or Vertical mount using pins

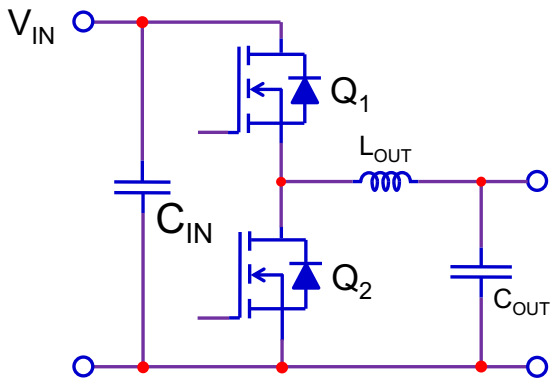


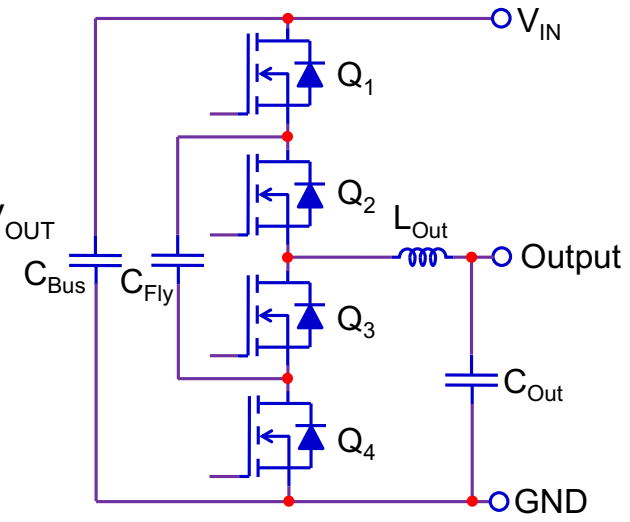
Vertical mount

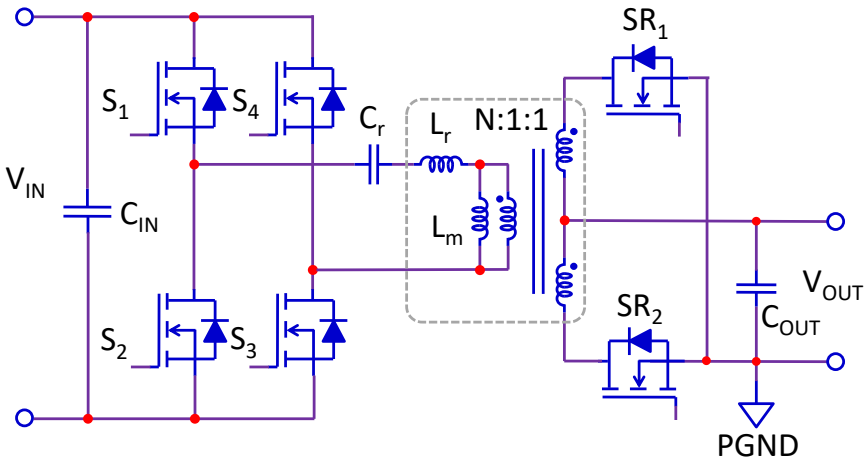


Horizontal mount

Topology Down Selection





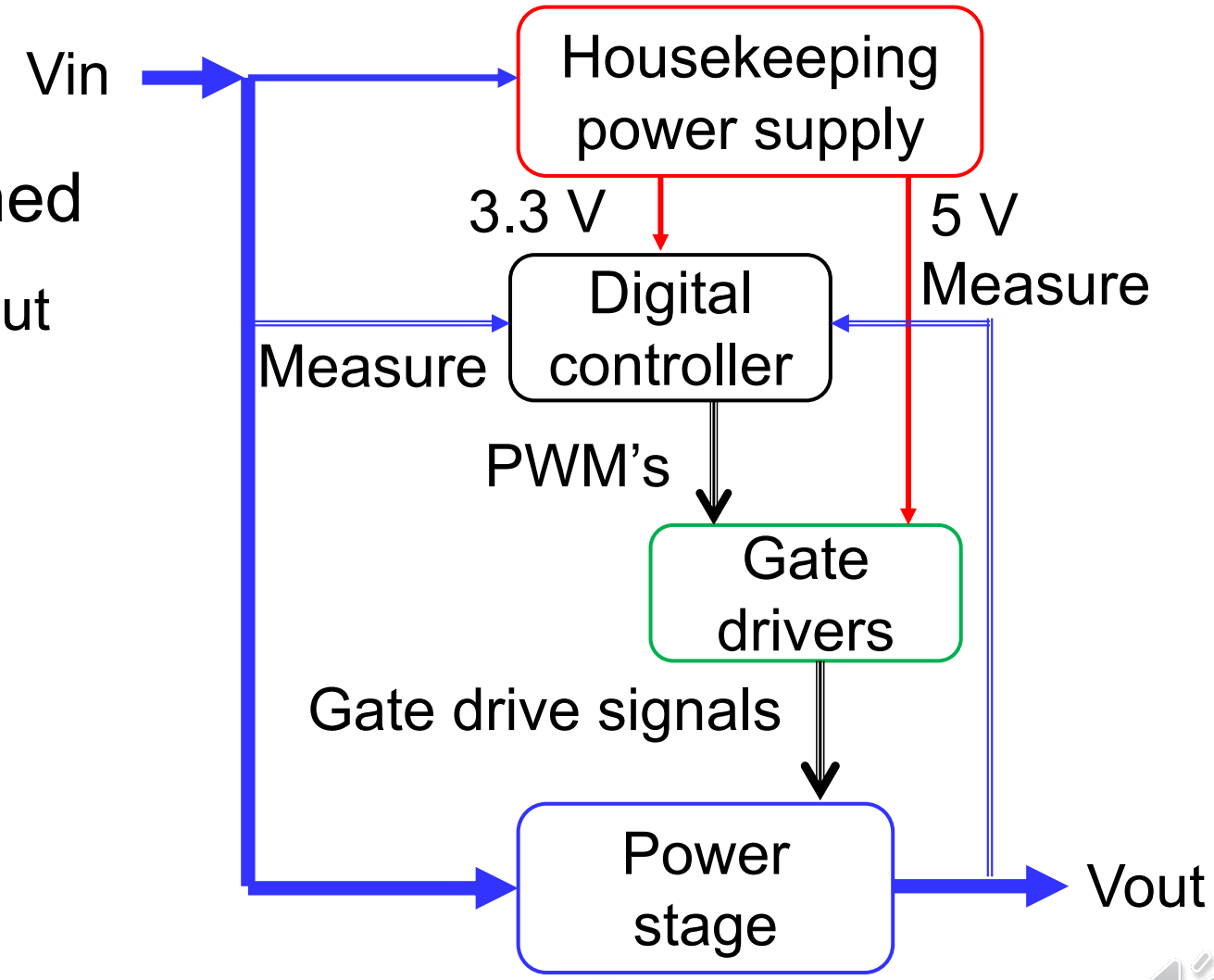


Topology	Buck Converter	Switched Capacitor	LLC converter
Load regulation	Full regulation	Fixed even-ratio with large high-current droop	Fixed ratio, low droop
Power density	Medium	Medium	High
Efficiency	≈ 97%	≈ 98%	≈ 98%
Load power	< 300 W	< 600 W	> 300 W
Complexity	Simple	High	Medium

Module Design

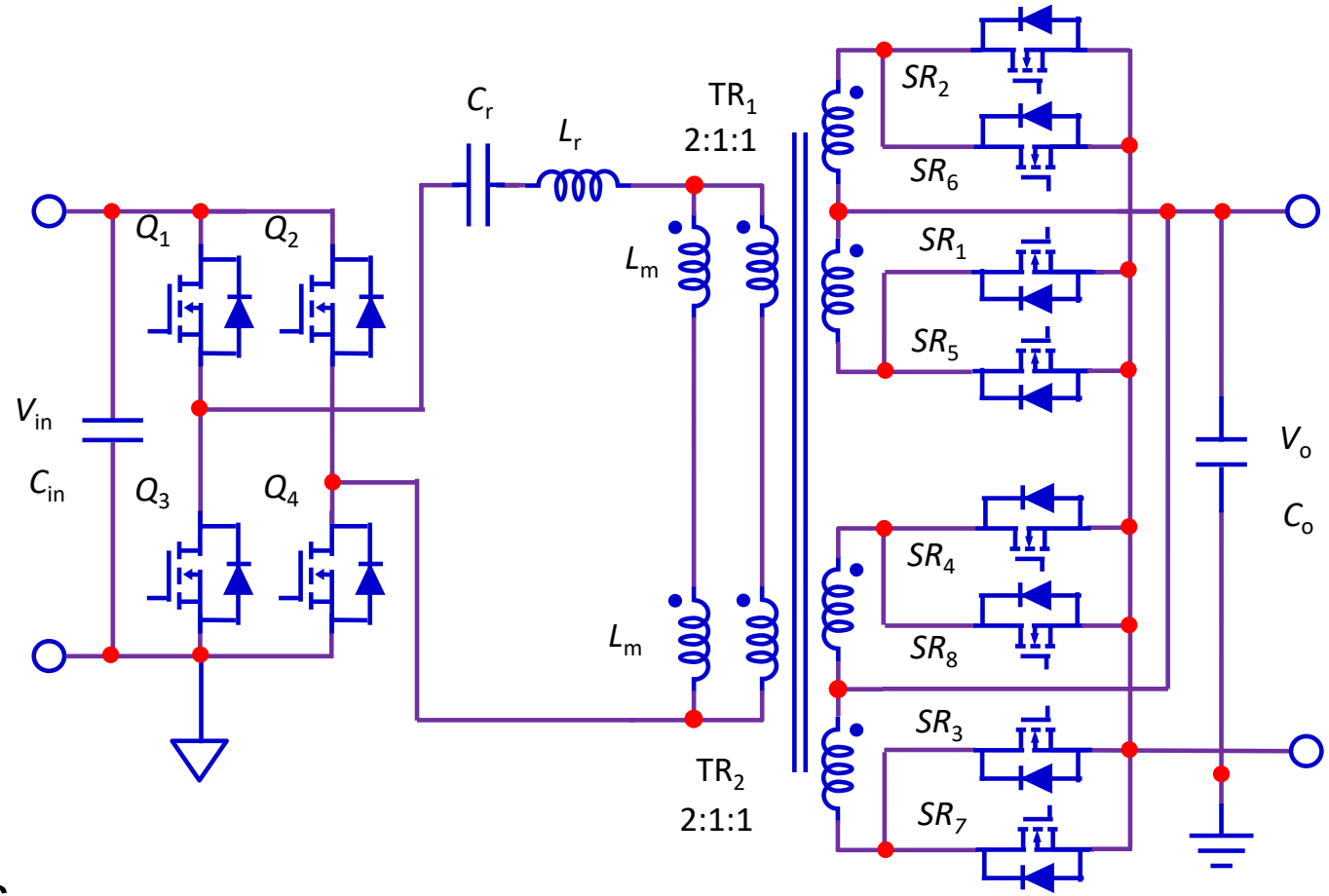
System Overview

- System needs to be self contained
  - Gate power derived from 48 V input
  - 3.3 V power derived from 5 V
- Digital controller
  - Voltage feedback control
  - Precise timing



LLC Resonant Topology

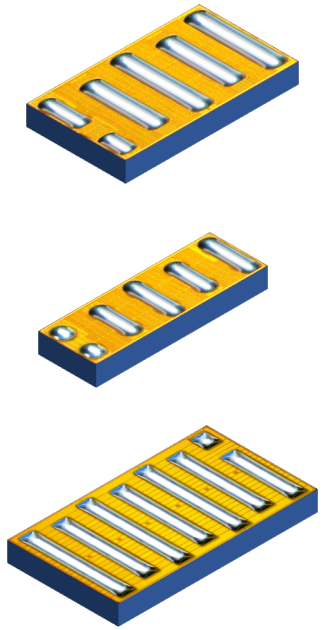
- Full bridge primary
  - Lower primary current
  - No DC voltage across resonant capacitor
  - Leakage inductance used for resonance
  - Magnetizing inductance used for ZVS
- Dual rectifier secondary
  - High Current
  - Parallel FETs
  - Dual center tap common ground FETs

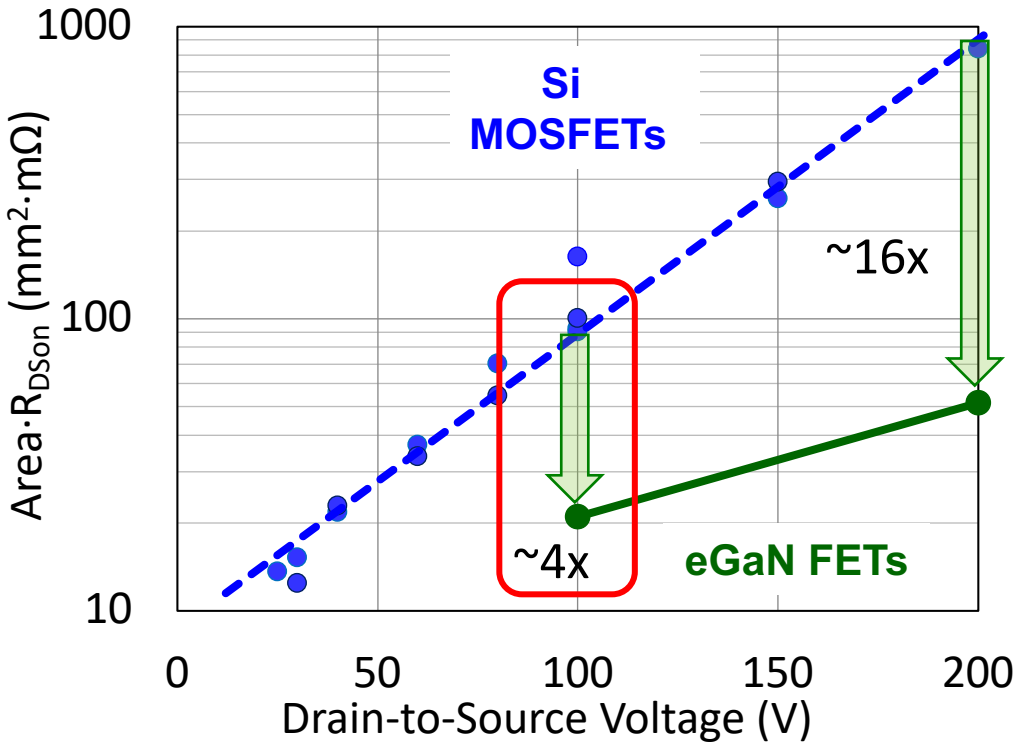


GaN vs Silicon in 48 V

With respect to MOSFETs:

- Reduced FOM ~ 4 times
- Lower Q_G ~ 5 -10 times
- Lower R_{DSon} at V_{GS} = 5 V
- Lower Q_{OSS}
- Lower Q_{GD}
- Zero Q_{RR}
- Smaller

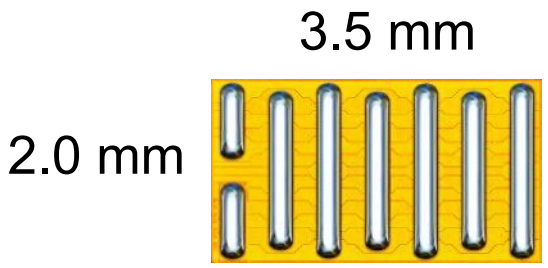




Devices Selected

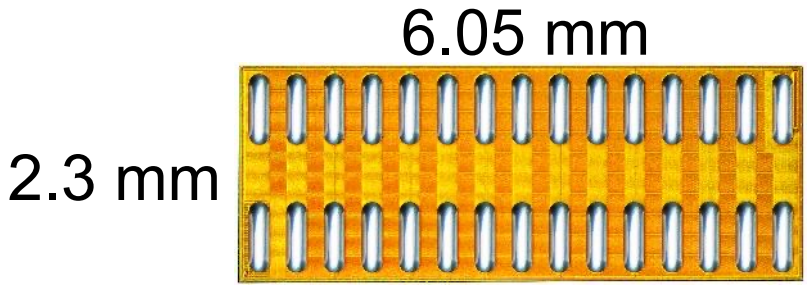
Primary Side

Parameter	EPC2218
$V_{ds,max}$	100 V
$R_{ds,on}$	2.4 mΩ
Q_{oss}	46 nC
Q_G	10.5 nC
$R_{\theta,jc}$ $R_{\theta,jb}$	0.5 °C/W 1.4 °C/W

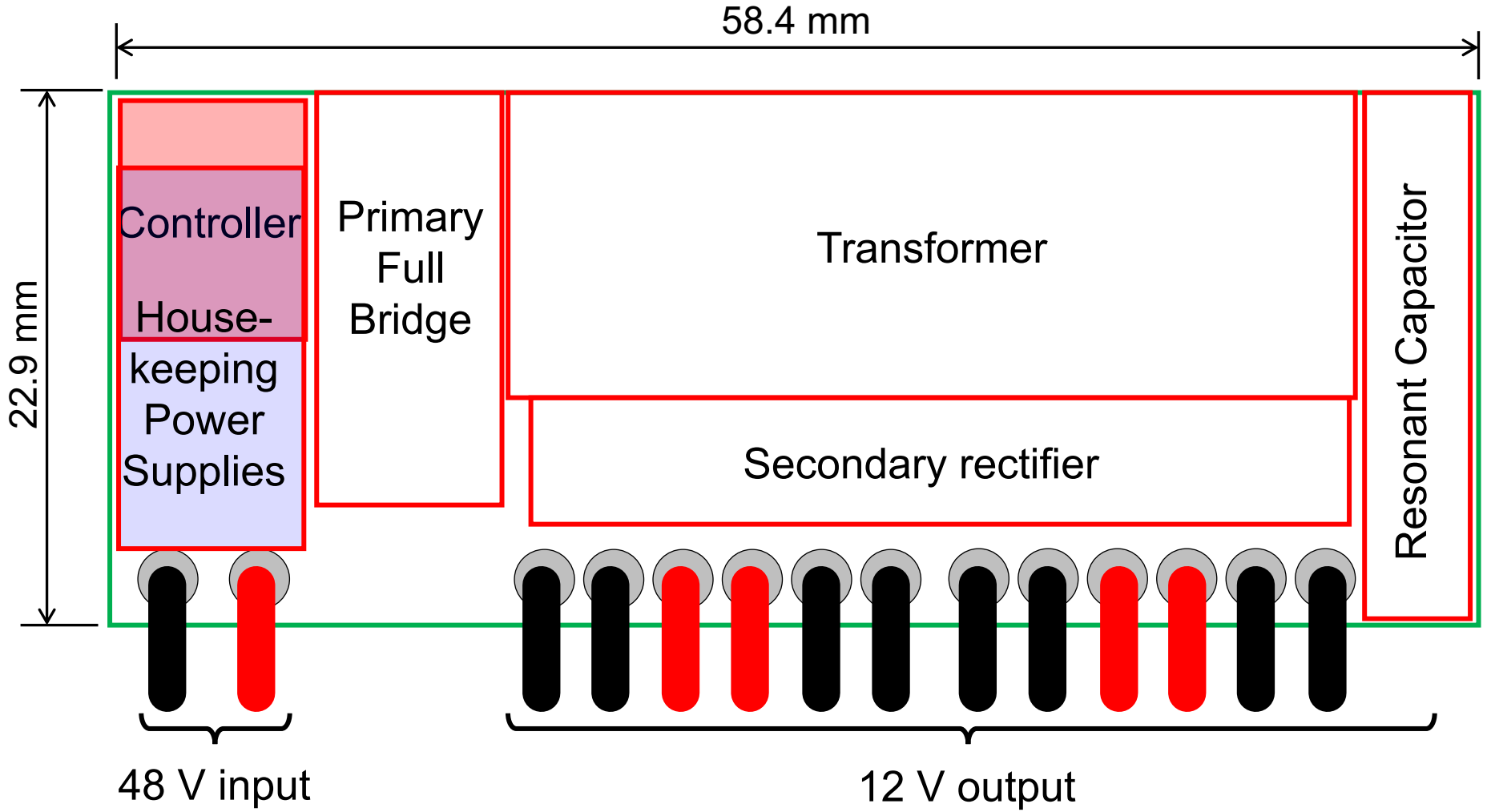


Secondary Side

Parameter	EPC2024
$V_{ds,max}$	40 V
$R_{ds,on}$ at 4.5 V_{GS}	1.2 mΩ
Q_{oss}	45 nC
Q_G	18 nC
$R_{\theta,jc}$ $R_{\theta,jb}$	0.4 °C/W 1.1 °C/W

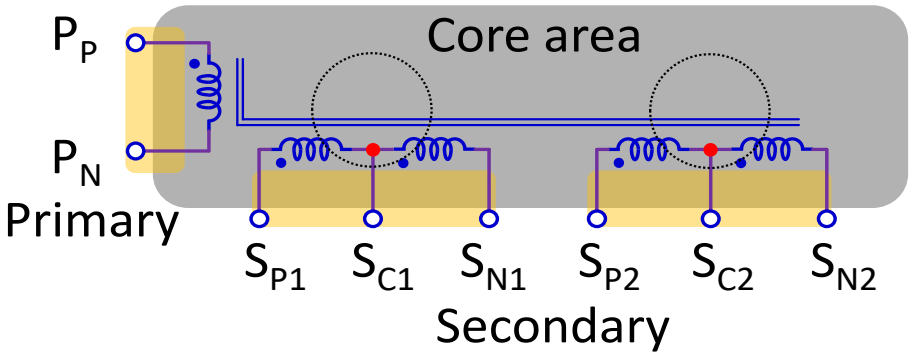


Design Planning

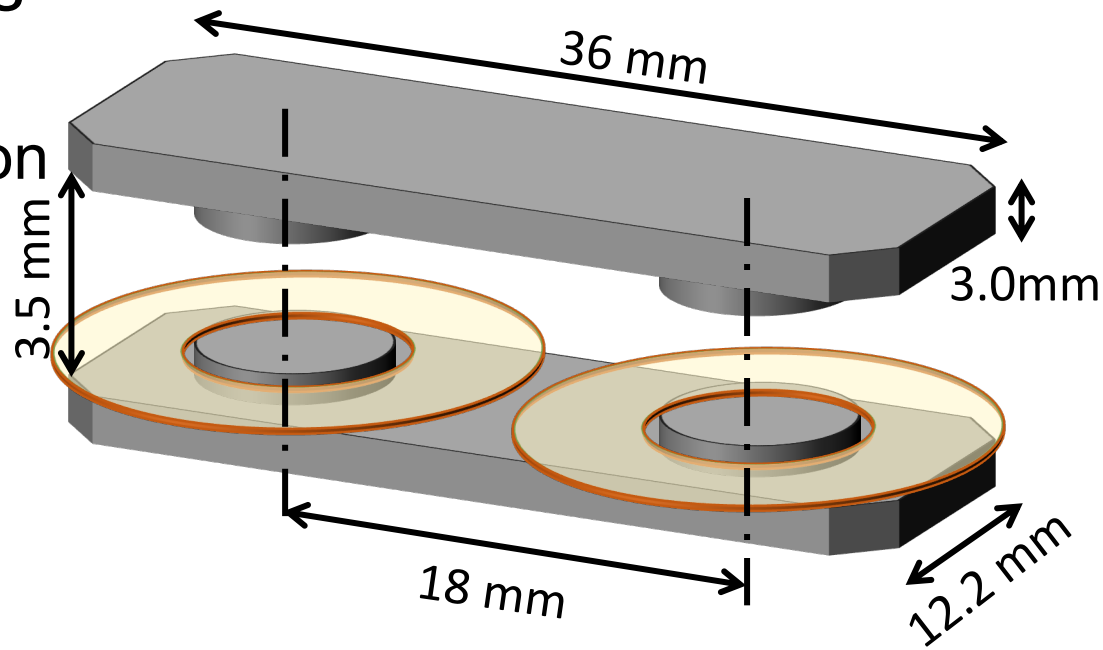


Transformer Design Overview

- 3 oz Copper thickness windings
- Interleaved windings for min. loss
- Minimize power path losses
  - Primary side connection
  - Secondary bottom connection



Transformer connection points

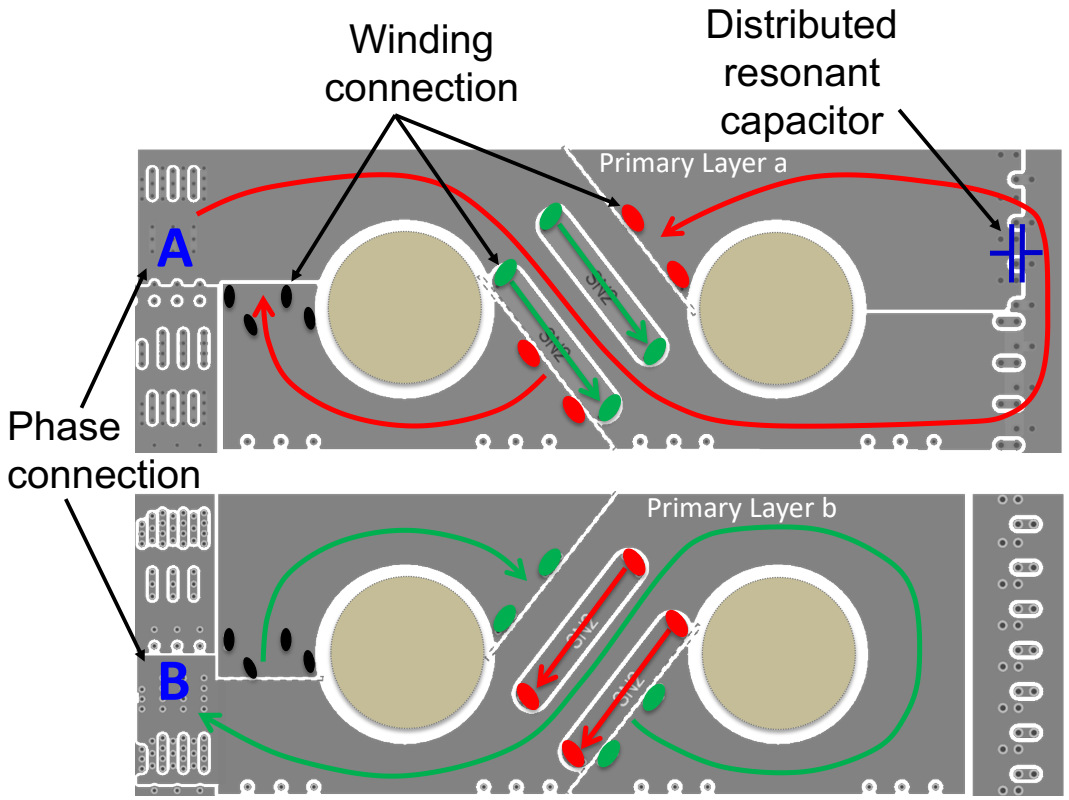


Layer Stackup

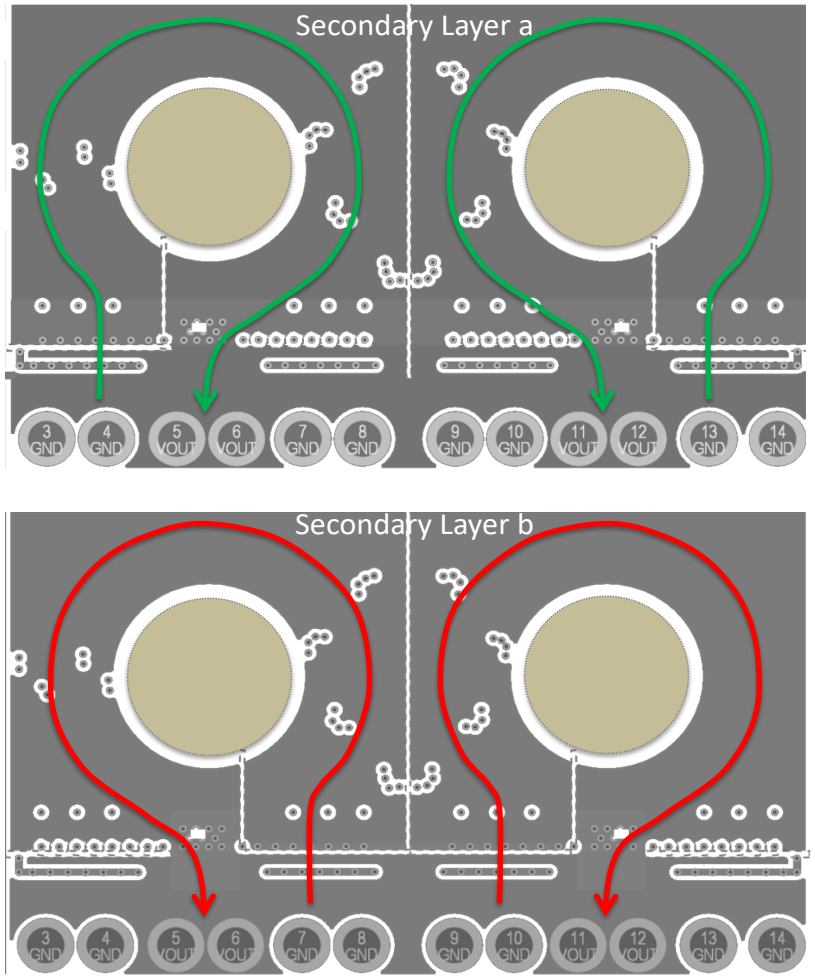
1		Shield
		2 Sec-
Pri	3	
		4 Sec+
		5 Sec+
Pri	6	
		7 Sec-
		8 Sec-
Pri	9	
		10 Sec+
		11 Sec+
Pri	12	
		13 Sec-
14		Shield

Transformer Winding Details

- Primary winding cross-over
- Short secondary connections



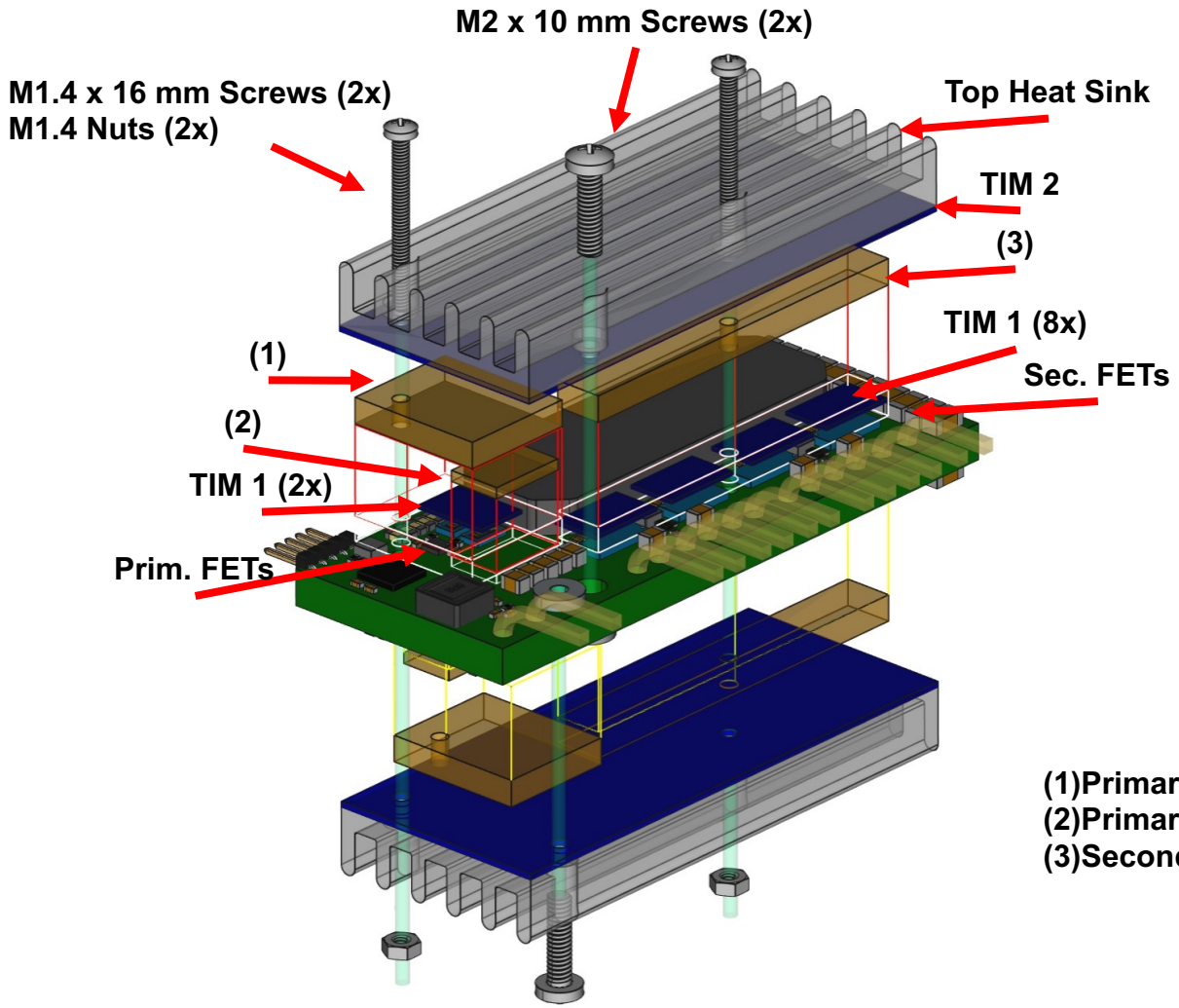
Primary winding design



Secondary winding design

Thermal Solution Approach

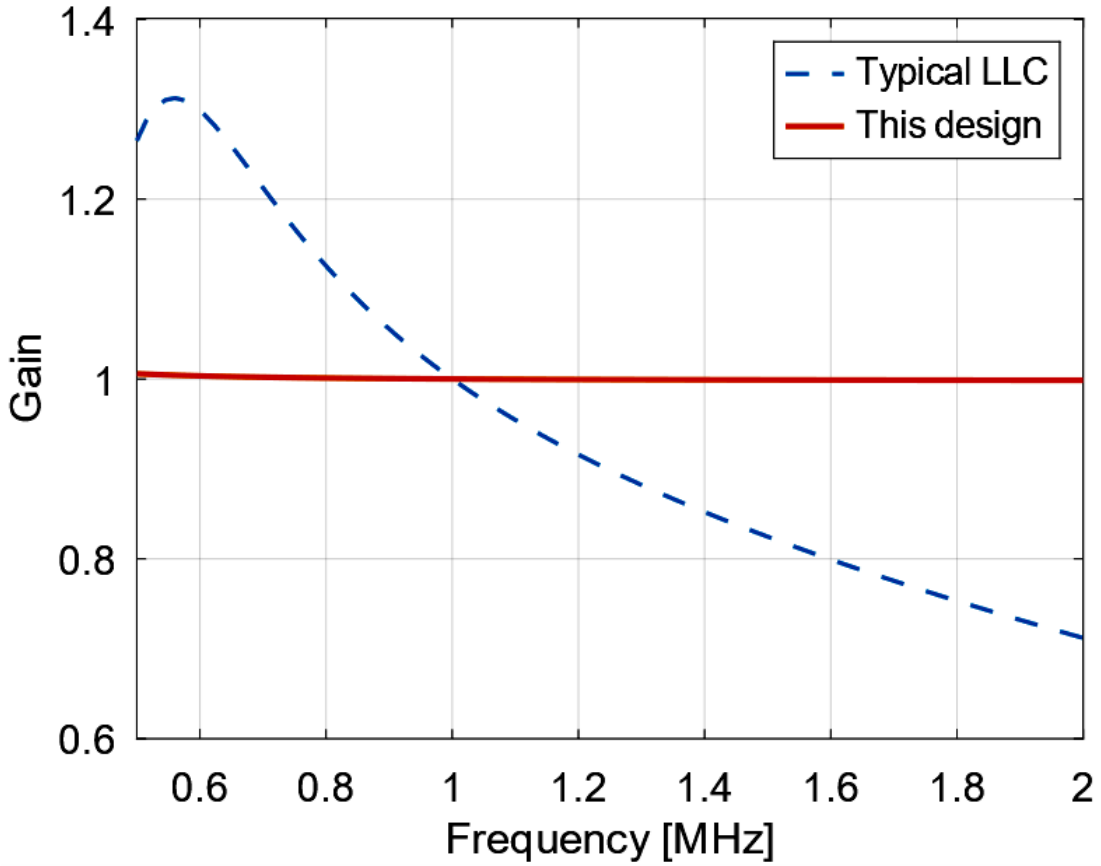
- Customized heat spreaders
- TIM used for improving thermal conductivity
  - T-Global: A1780- 500 µm for FETs (TIM 1)
    - High thermal conductivity (17.8 W/m.K)
    - Compressible (2:1)
    - Isolation
  - T-Global: A6300 used for Heat Sink (TIM 2) (6.2 W/m.K)



(1)Primary Heat Spreader (2x)
(2)Primary Heat Spreader Seat (2x)
(3)Secondary Heat Spreader (2x)

Control Requirements

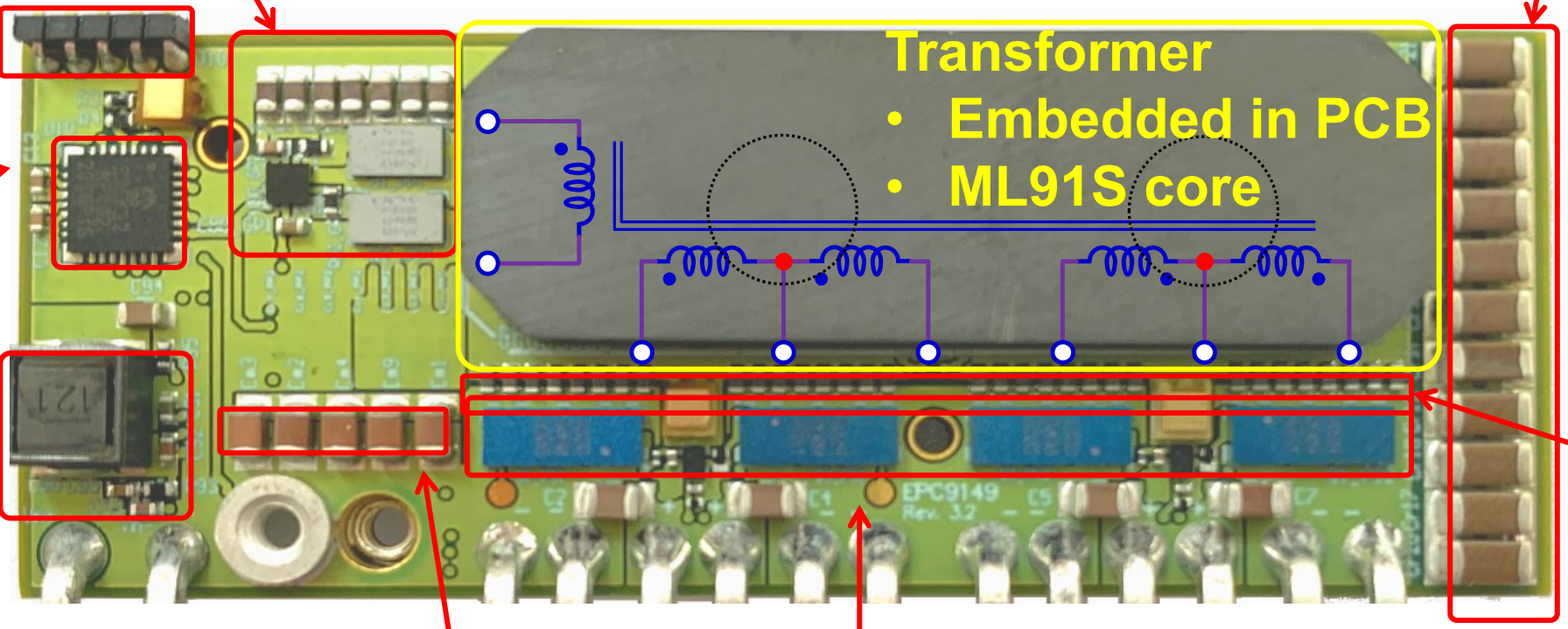
- Resonant inductance, transformer leakage, very small ~ 8nH. Frequency modulation not possible
  - Startup current limit achieved using PWM ramp up – 2% – 50%
- Over-temperature protection



Voltage conversion ratios of a typical LLC converter compared to this design.

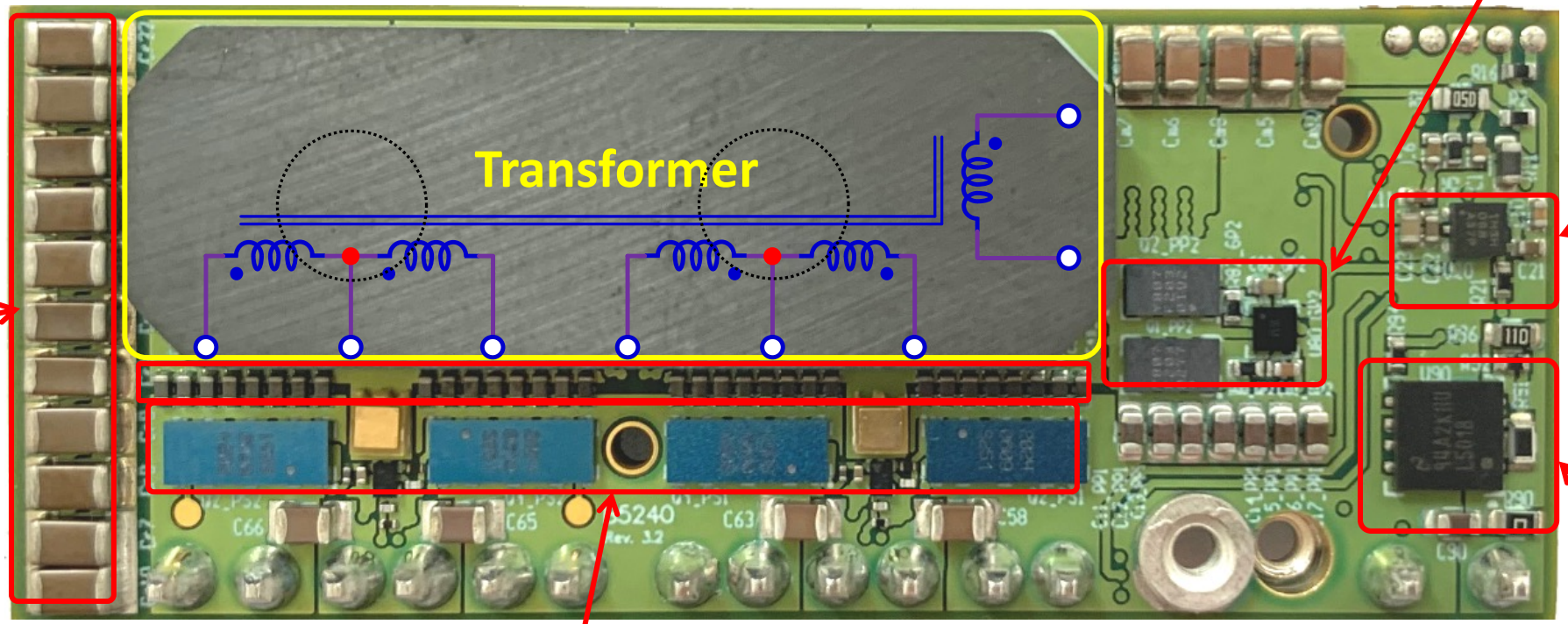
Experimental Validation

Experimental Unit Overview - Top



Function Blocks Overview – Bottom

EPC9149



Primary HB 2

3.3 V House-Keeping PSU

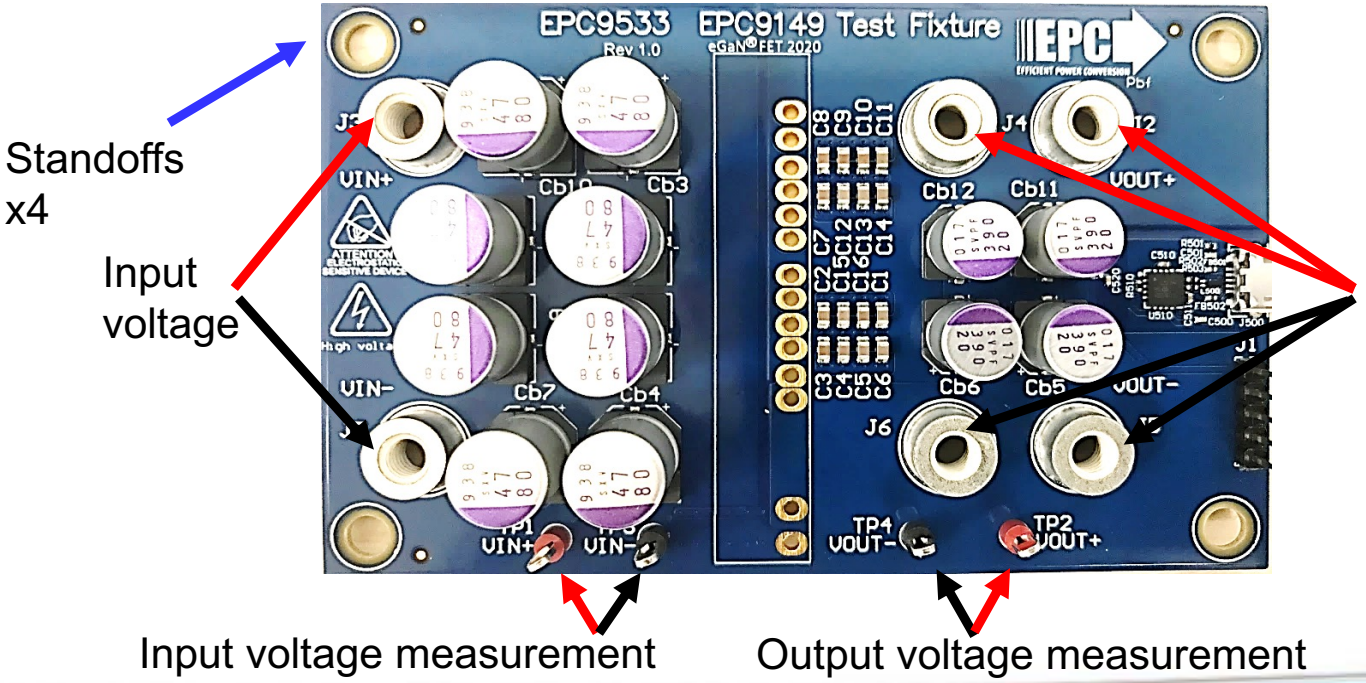
Resonant Capacitor Bank

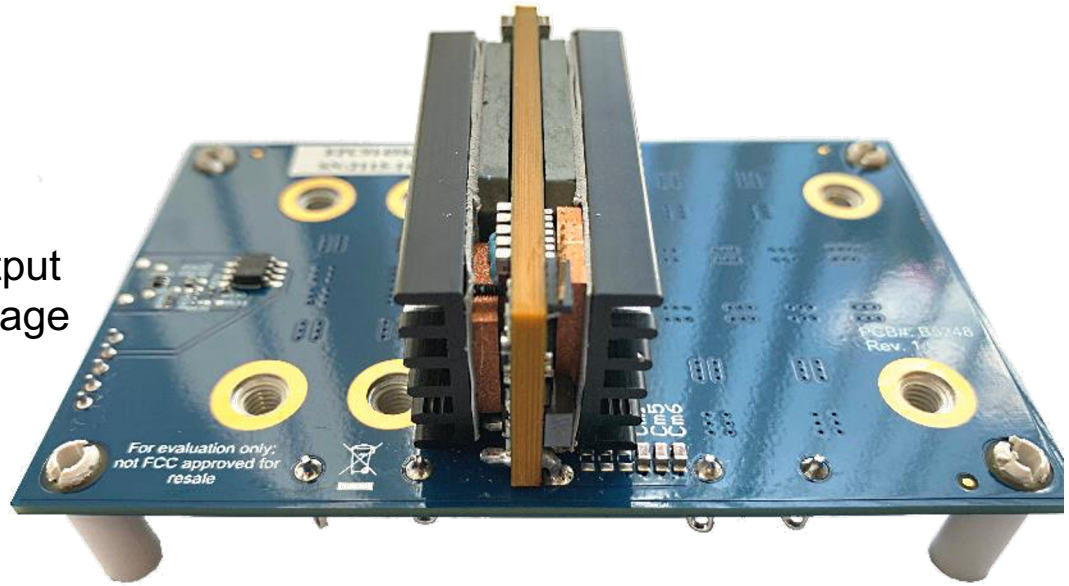
HV House-Keeping PSU

Rectifier

Motherboard & Connections

- Input and output connections,
- Kelvin measurement:
  - Input and output Voltage
- The LLC module is soldered on the motherboard.



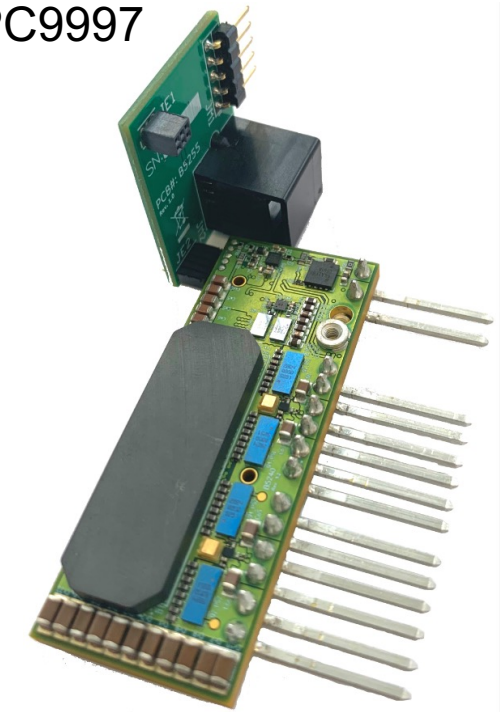


Programming the controller

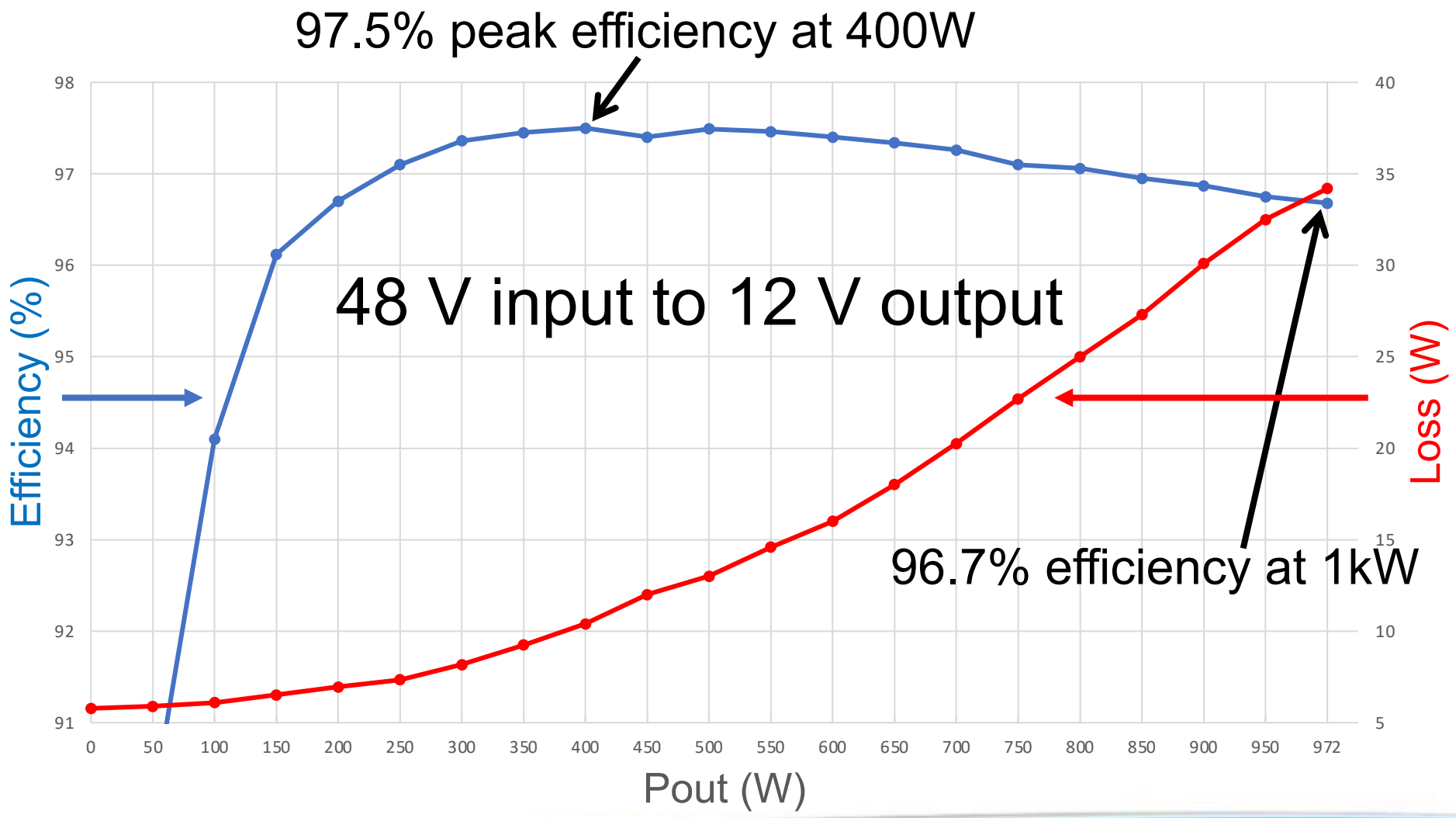
- RJ11 to ICSP adapter and EPC9997 can be used to interface the programmer and the main board.

Microchip adapter 02-10310-R1

EPC9997

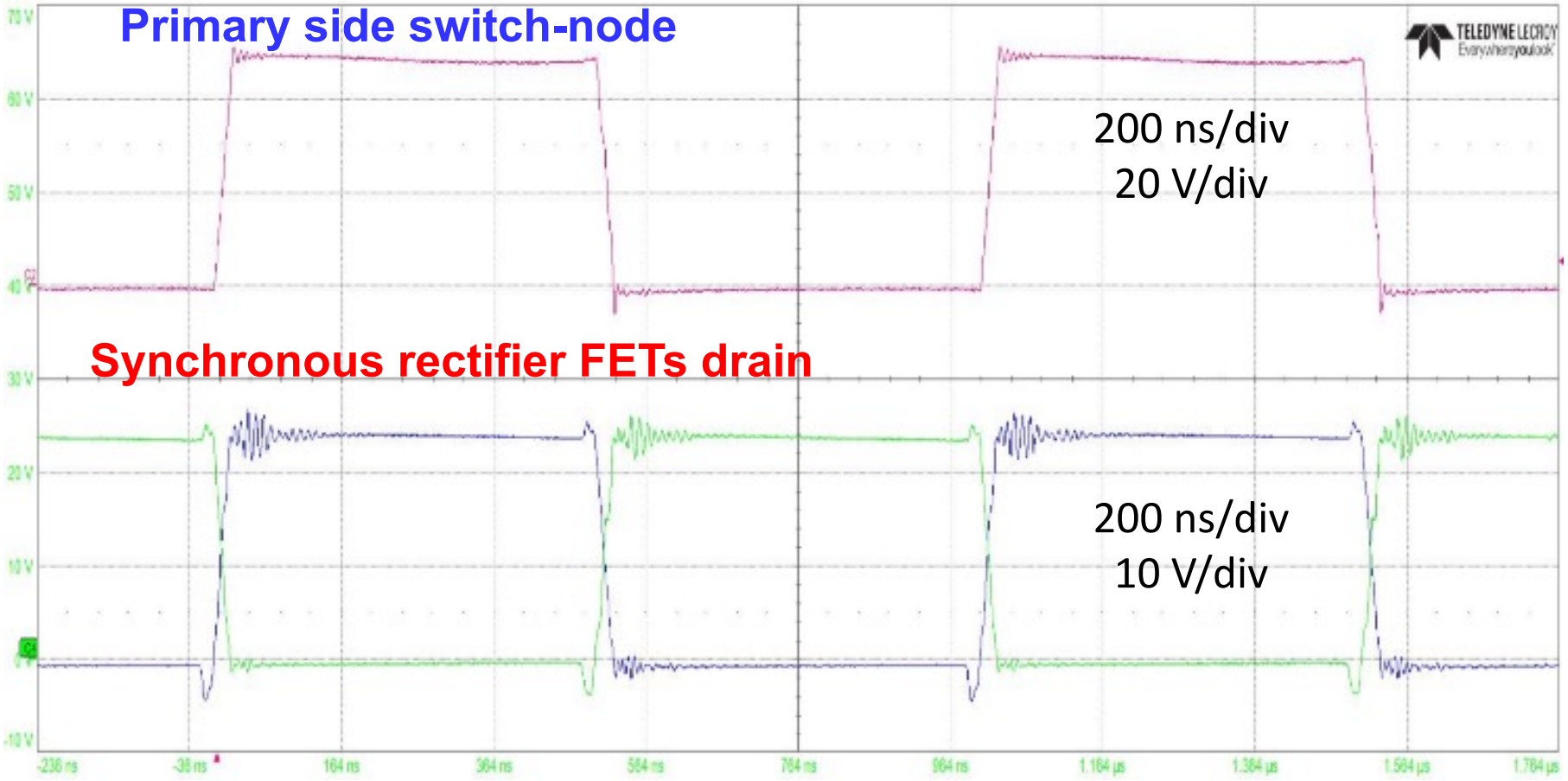


Experimental - Efficiency & Loss

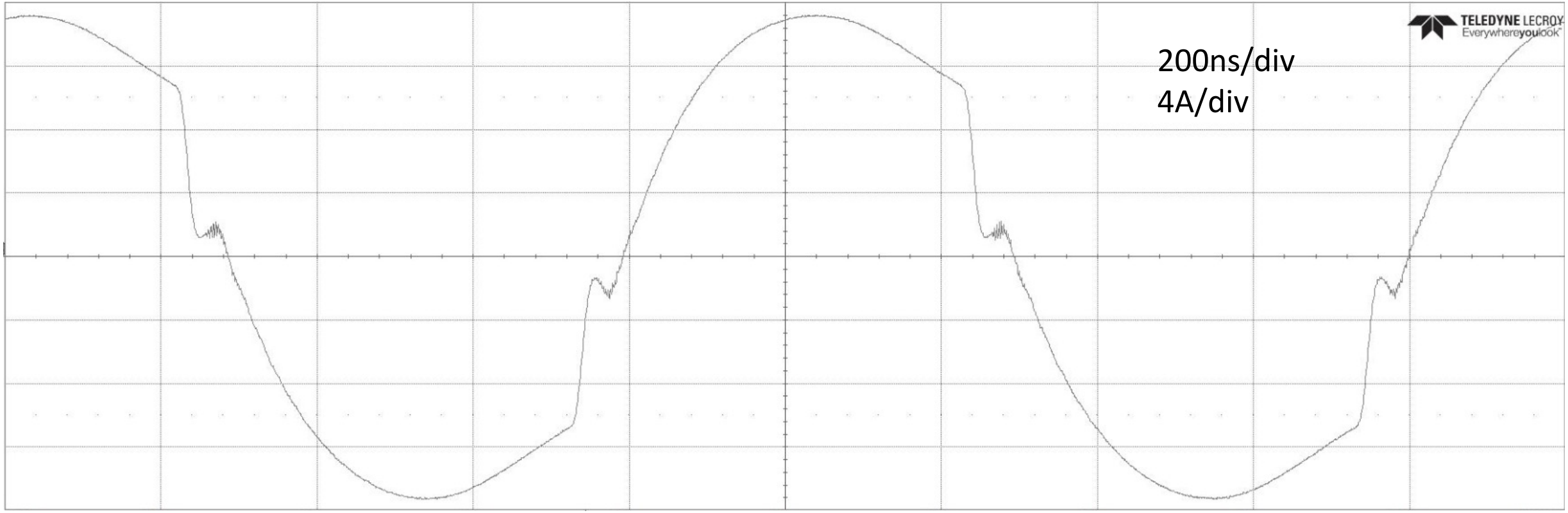


Switching Waveforms

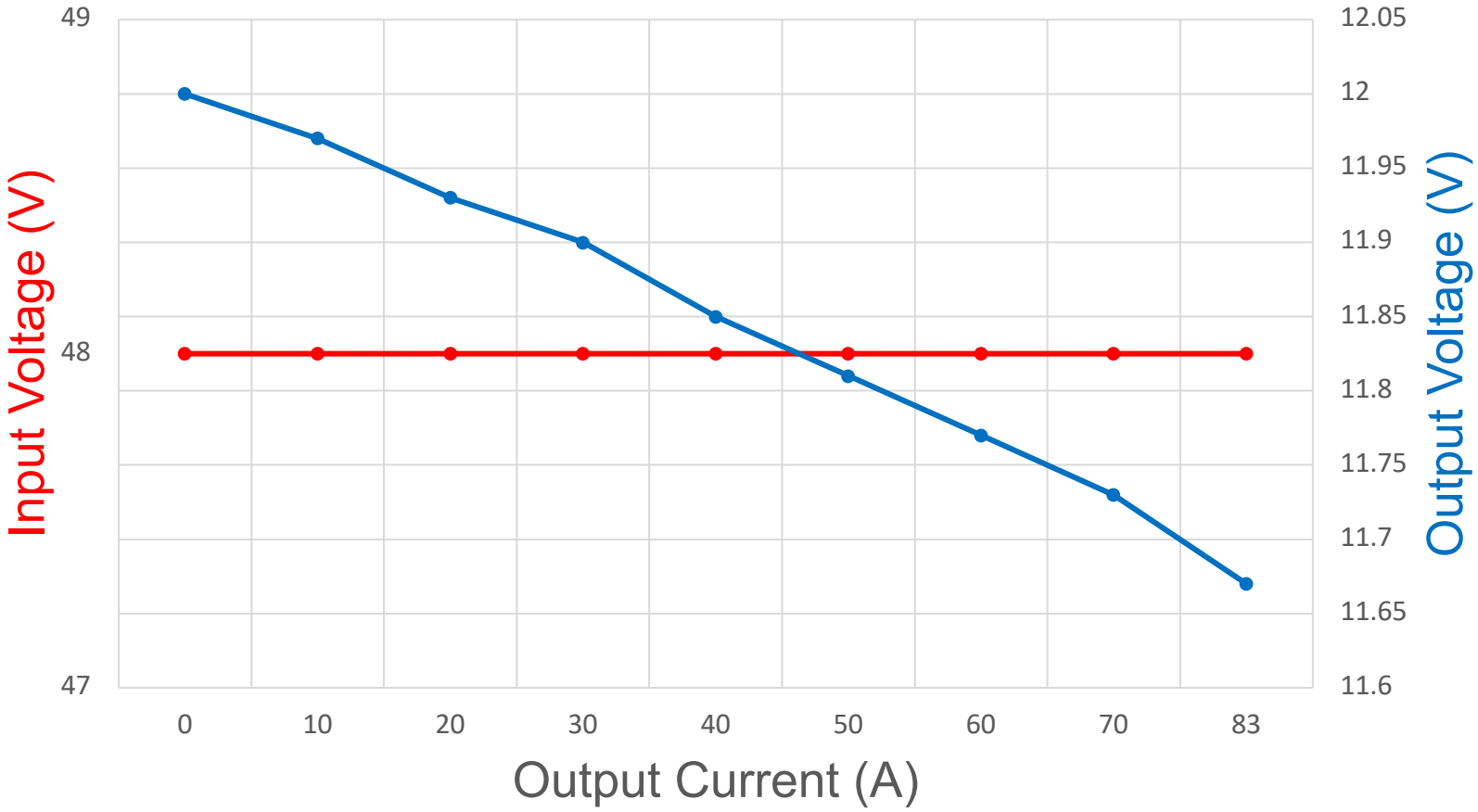
48 V input to 12 V output at 1kW



Primary Current



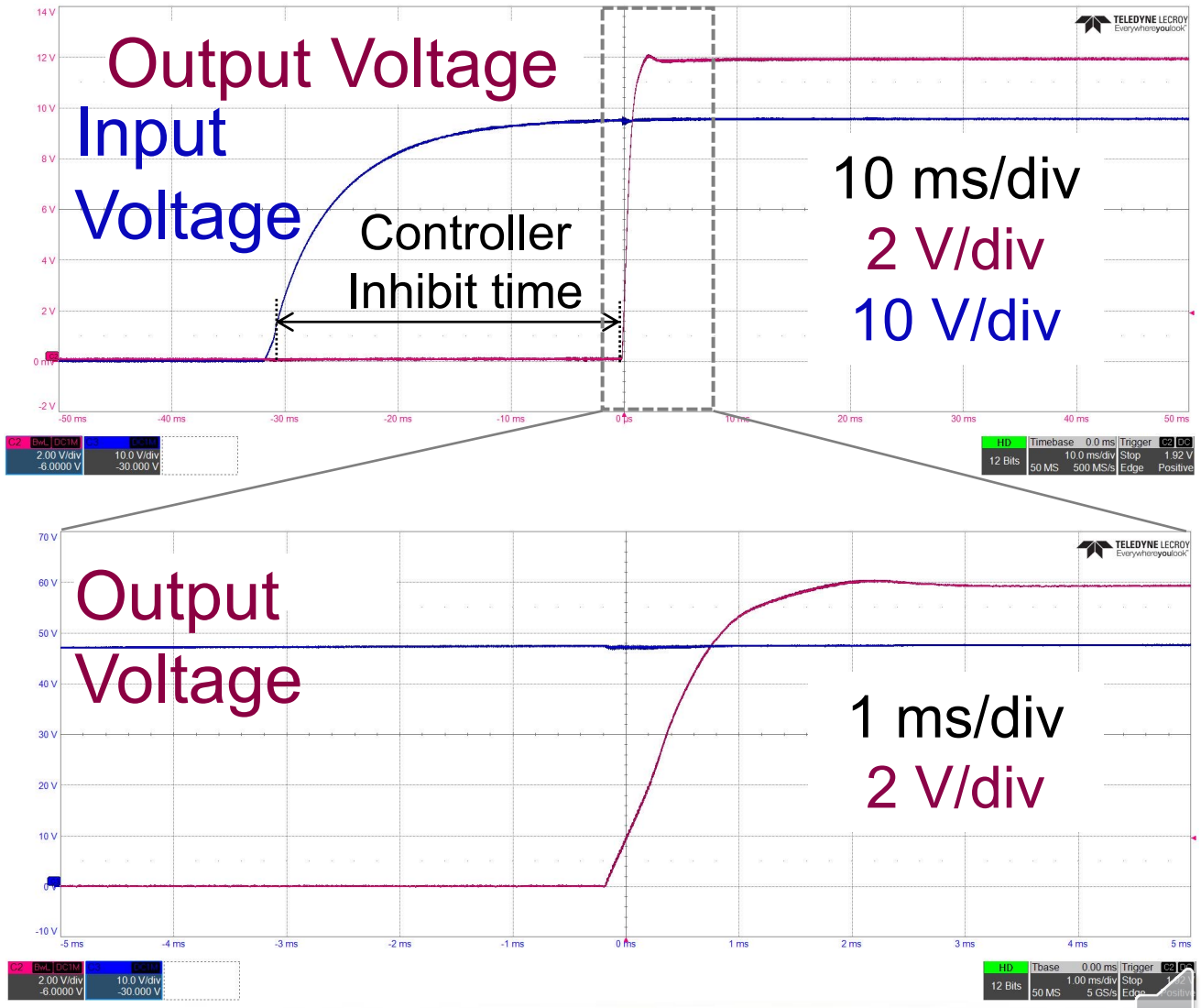
Measured Output Voltage Droop



Output voltage droop vs output current

Experimental – Startup

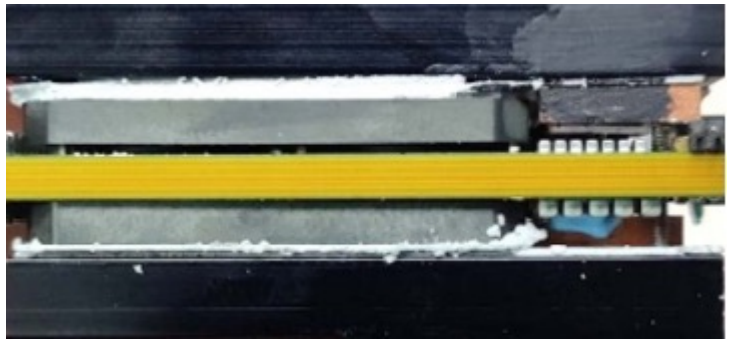
- Soft startup implemented:
  - Avoid inrush current and excessive voltage stress
  - Duty cycle ramp up
- Start into resistive load (144mΩ)

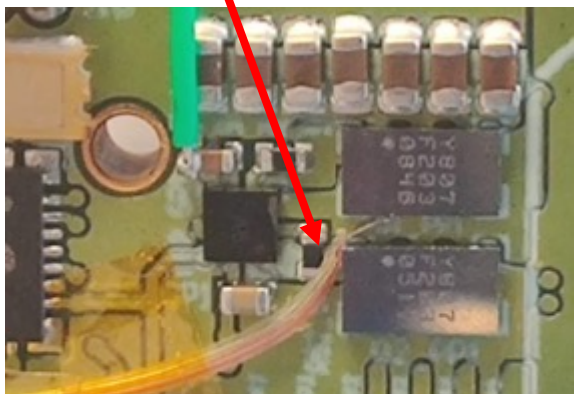


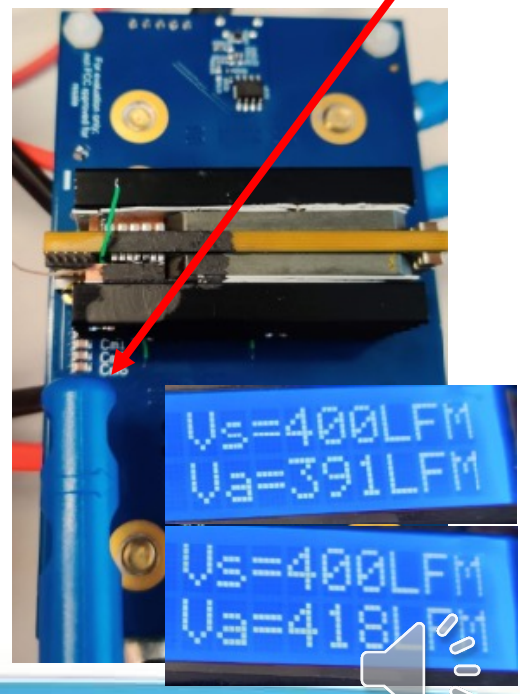
Thermal Testing Setup

- FET die temperature measured using K-type thermocouple
- IR camera used to measure external temperature of board, HSp, and heatsink
- Forced convection cooled at 400 LFM
- Device operated at full load 83A

Top view of final assembled structure

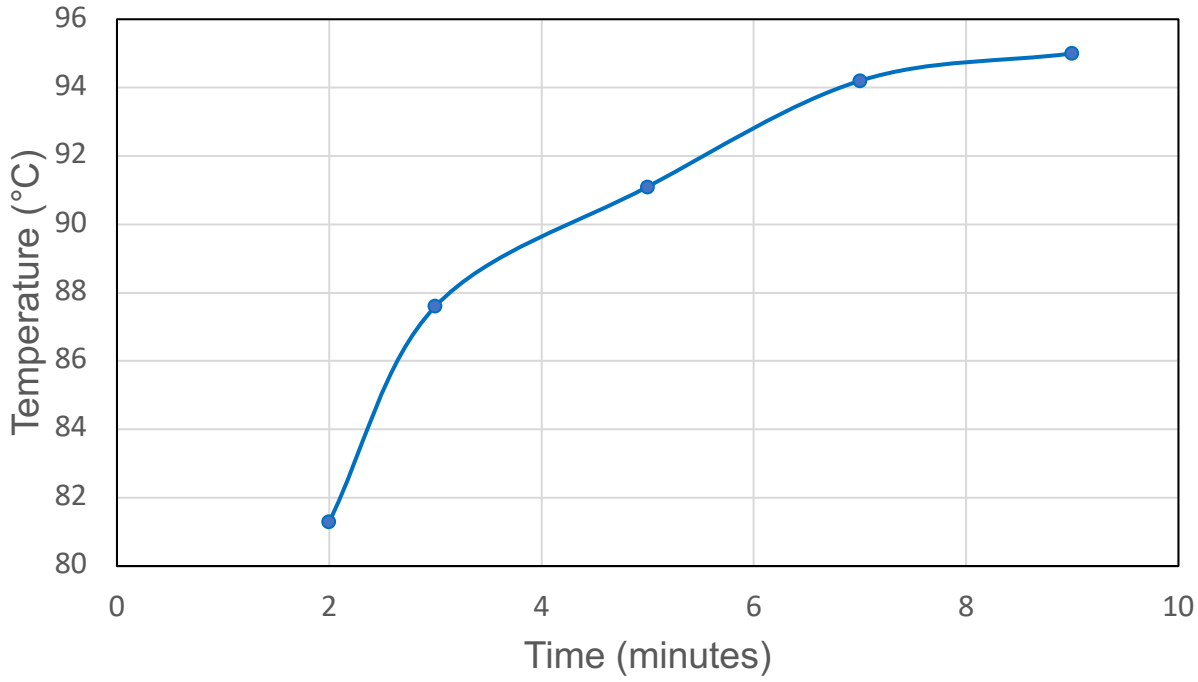




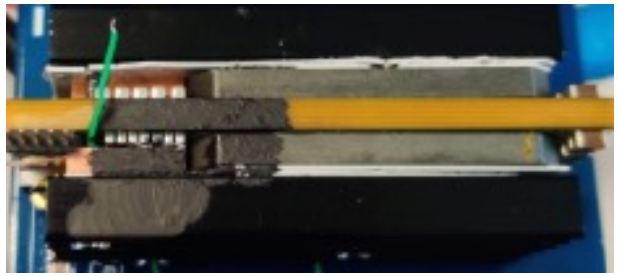


Thermal Results

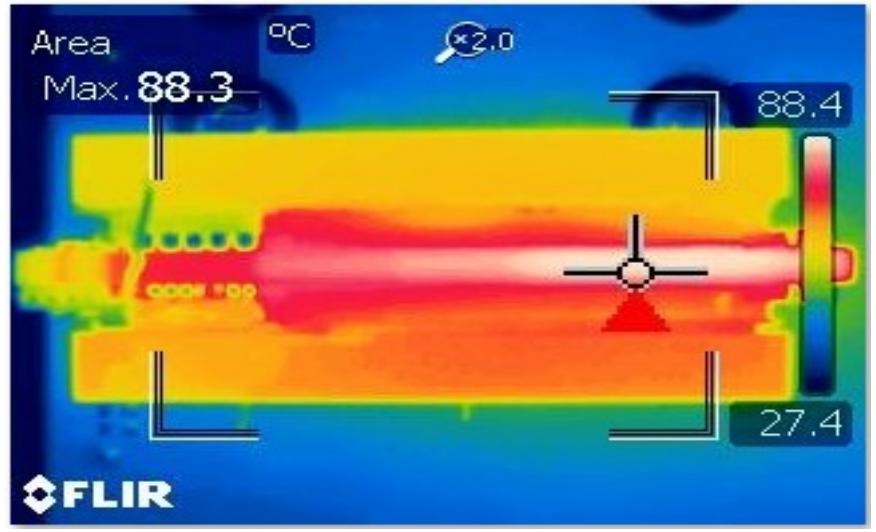
- Steady state in 10 minutes
- 70 °C primary FETs rise



Board standard image



Air-Flow

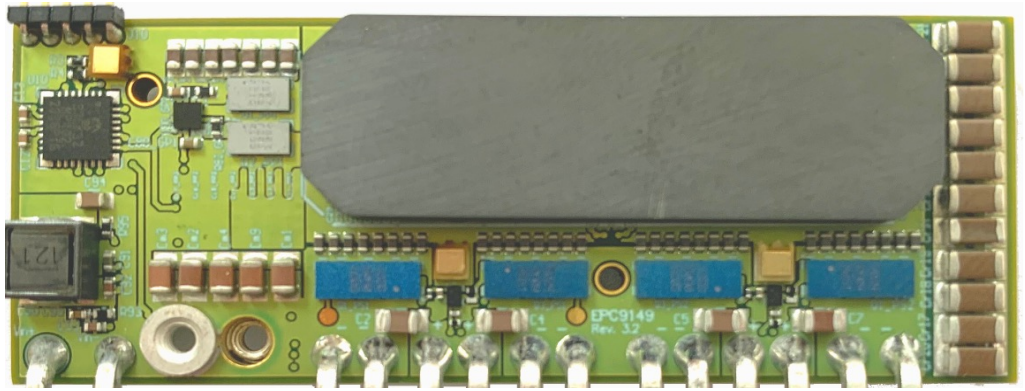


Board thermal image

48 V_{IN}, 12 V_{OUT}, 1 kW, 400 LFM, T_{Amb} = 25°C

Conclusion

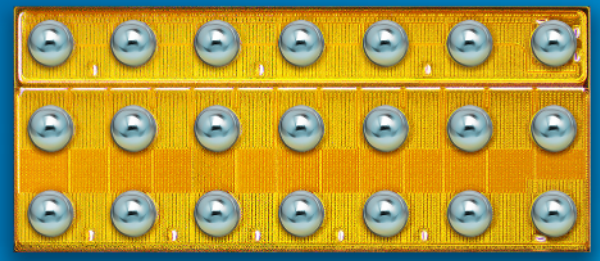
- 1 kW LLC design
  - 58.4 x 22.9 x 10 mm volume
  - Uses conventional PCB technology
- eGaN FETs
  - Achieves high efficiency
  - Enable high power density (1226 W/in^3)



EFFICIENT POWER CONVERSION

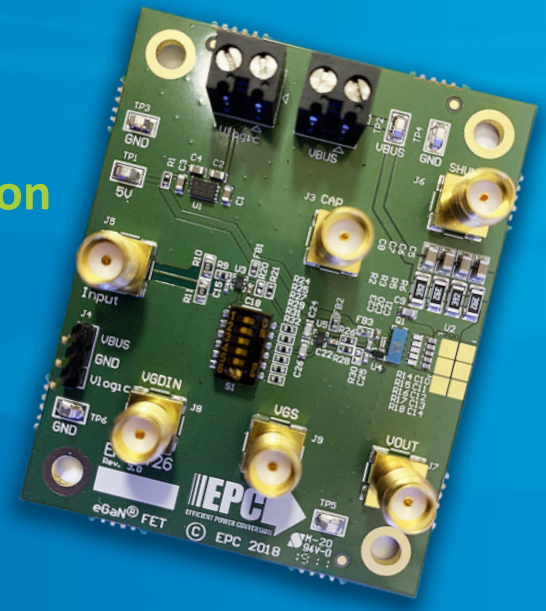
How To GaN Video Series

3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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Microchip Solution On EPC9149 LLC Converter

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Edward Lee

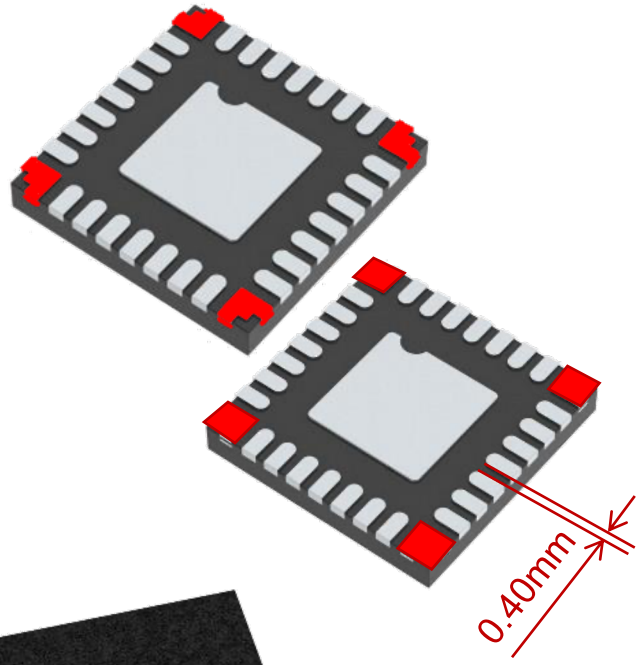
Dec. 2nd, 2021

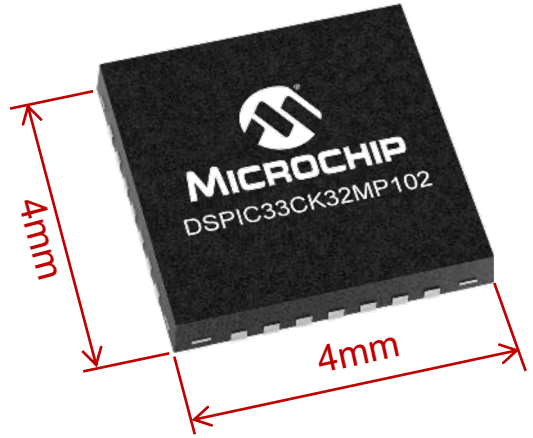
SMART | CONNECTED | SECURE

Controller Overview

EPC9149 LLC Converter

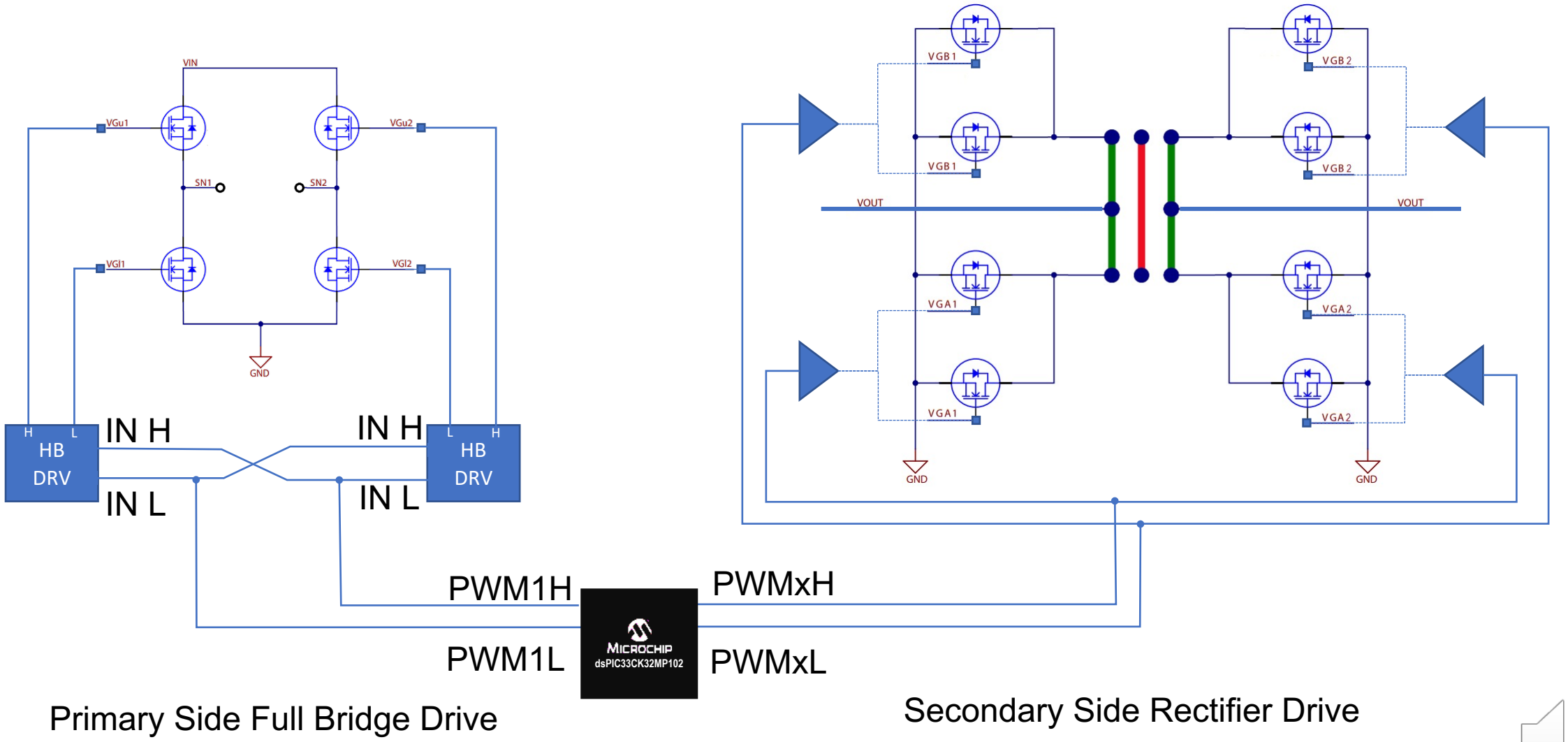
- **Choice of controller dsPIC33CK32MP102T-I/M6**
  - Very small at 4x4 mm
  - 250ps PWM resolution for precise ZVS timing
  - Low power consumption
  - Built in Op-Amps for analog feedback circuit reduction
- **Controller used for**
  - Maintaining ZVS
  - De-embed gate drive propagation mismatch
  - Power flow direction
  - Startup PWM
  - Operations monitoring
  - Over temperature protection
  - Communications





PWM Drive Simplification

EPC9149 LLC Converter



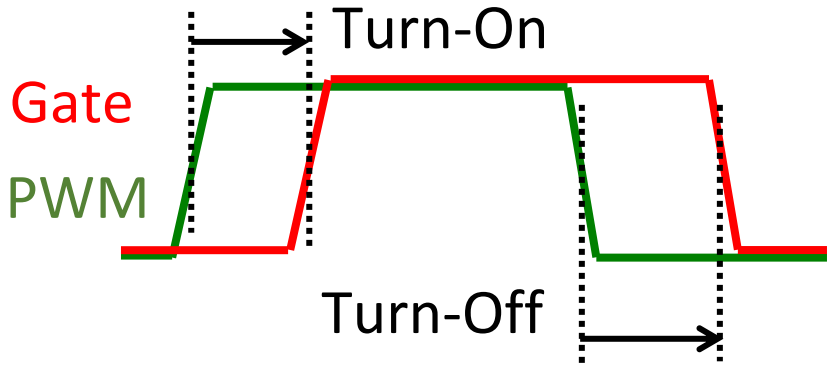
Primary Side Full Bridge Drive

Secondary Side Rectifier Drive

Key PWM Adjustment Settings

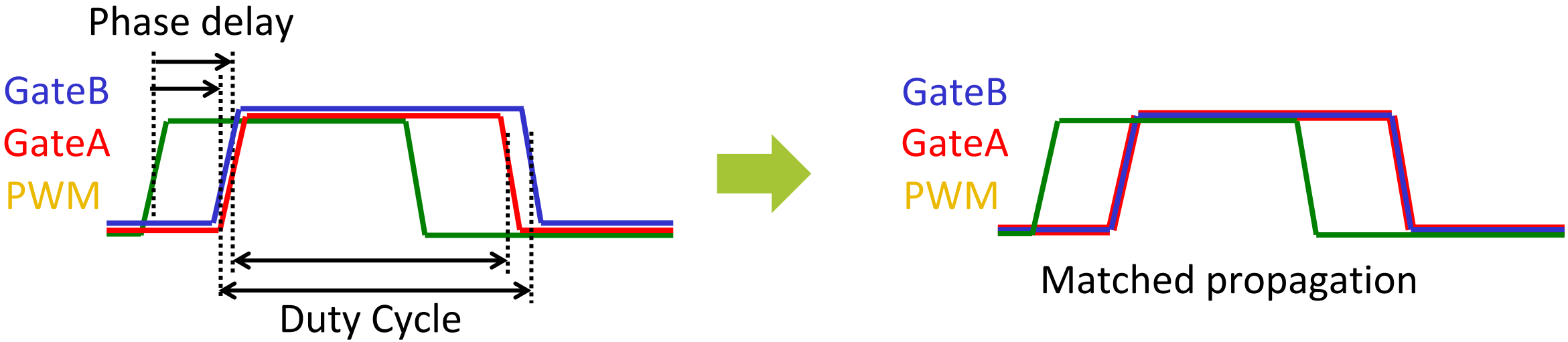
EPC9149 LLC Converter

- **Correcting gate driver propagation delay mismatches**
  - Within gate driver mismatch
  - Between gate driver's mismatch
  - Between gate driver types mismatch (Pri-Sec)
- **Propagation mismatch**
  - Generates DC offset
  - Asymmetrical current and even harmonic generation
- **Settings**
  - Optimal timing for ZVS
  - Optimal operating frequency
    - Overcomes discrete capacitor values



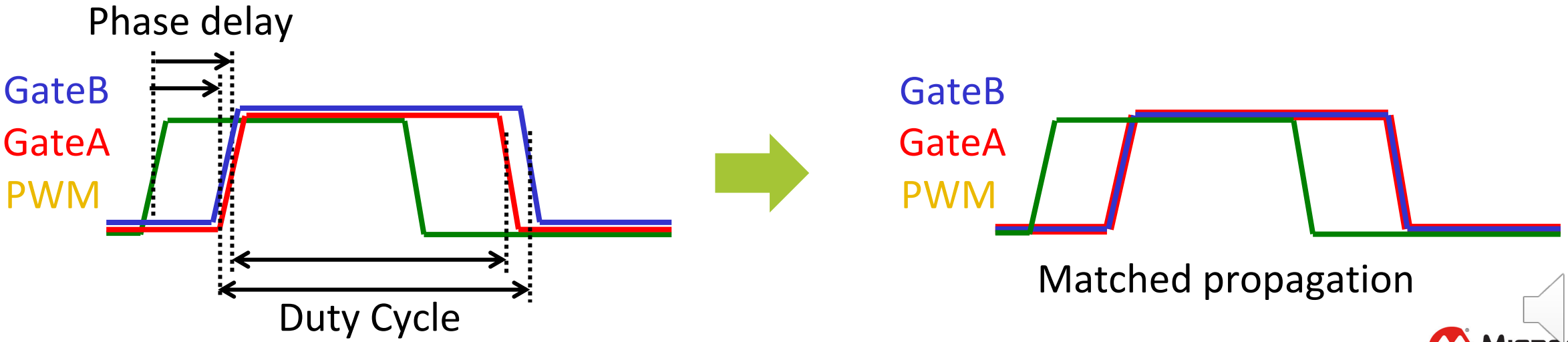
Primary Side Timing

- **Phase delay – compensates driver to driver mismatch**
- **Duty cycle – compensates within a HB driver mismatch**
- **Dead-time – Sets ZVS (all 4 FETs will have same value)**



Secondary Side Timing

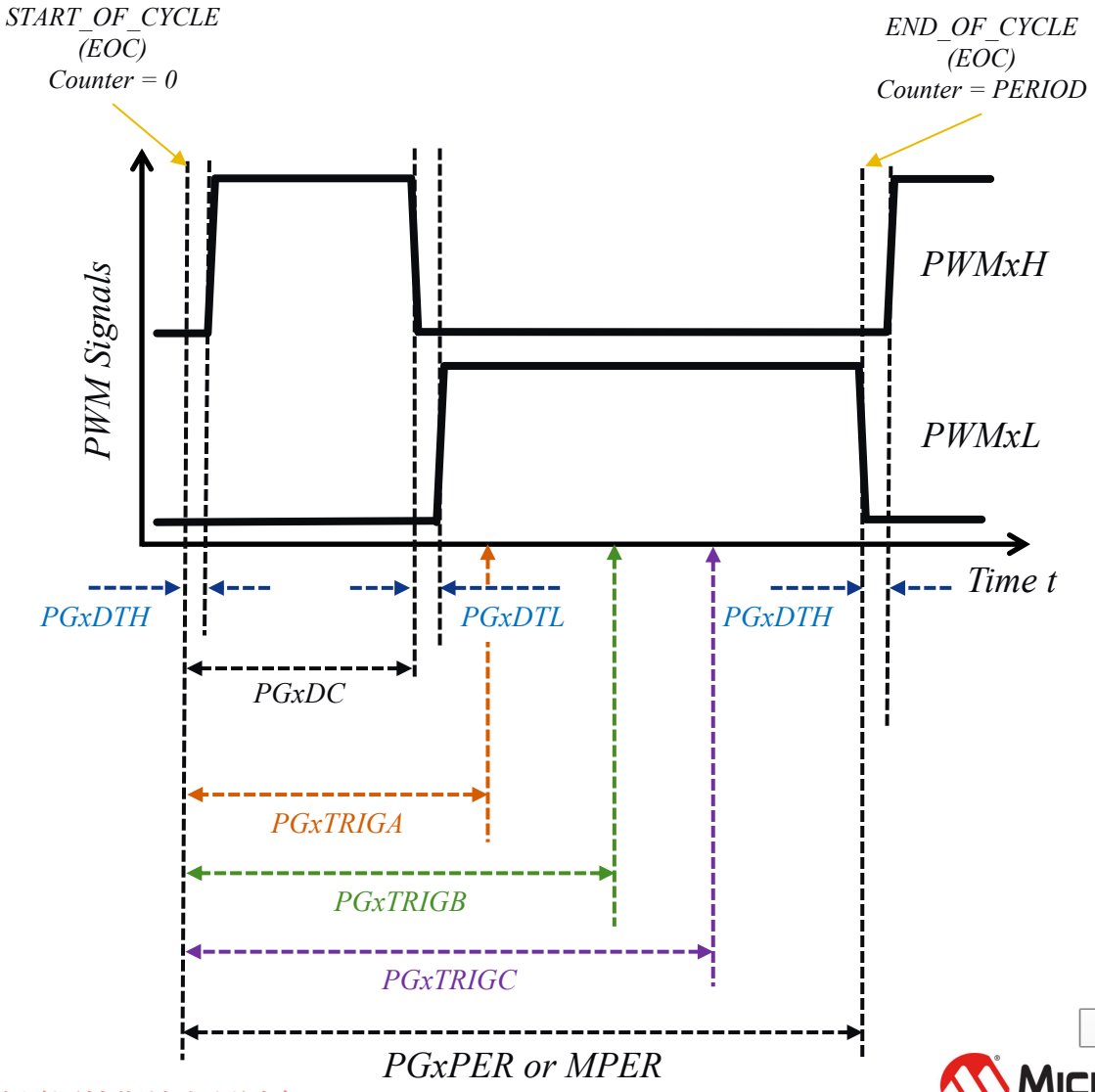
- **Phase delay**
  - Compensates between primary and secondary drivers
- **Duty cycle**
  - Corrects gate driver mismatch
  - Sets correct timing of secondary



PWM Logic Programmability

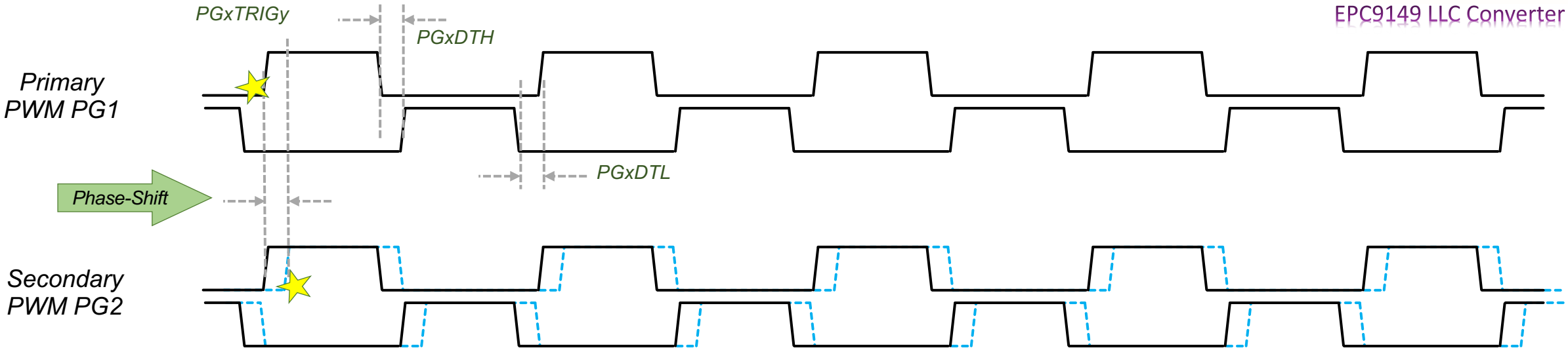
EPC9149 LLC Converter

- **Each PWM generator offers three triggers:**
  - PGxTRIGA:
    - Enhanced trigger options (can be delayed and shifted across multiple PWM cycles)
    - Available as ADC trigger
    - Available for PWM synchronization
  - PGxTRIGB:
    - Generated each cycle (fixed)
    - Available as ADC trigger
    - Available for PWM synchronization
  - PGxTRIGC:
    - Generated each cycle (fixed)
    - Available as ADC trigger
    - Available for PWM synchronization
- **Each trigger can be placed across the cycle independently with 250 ps placement resolution**



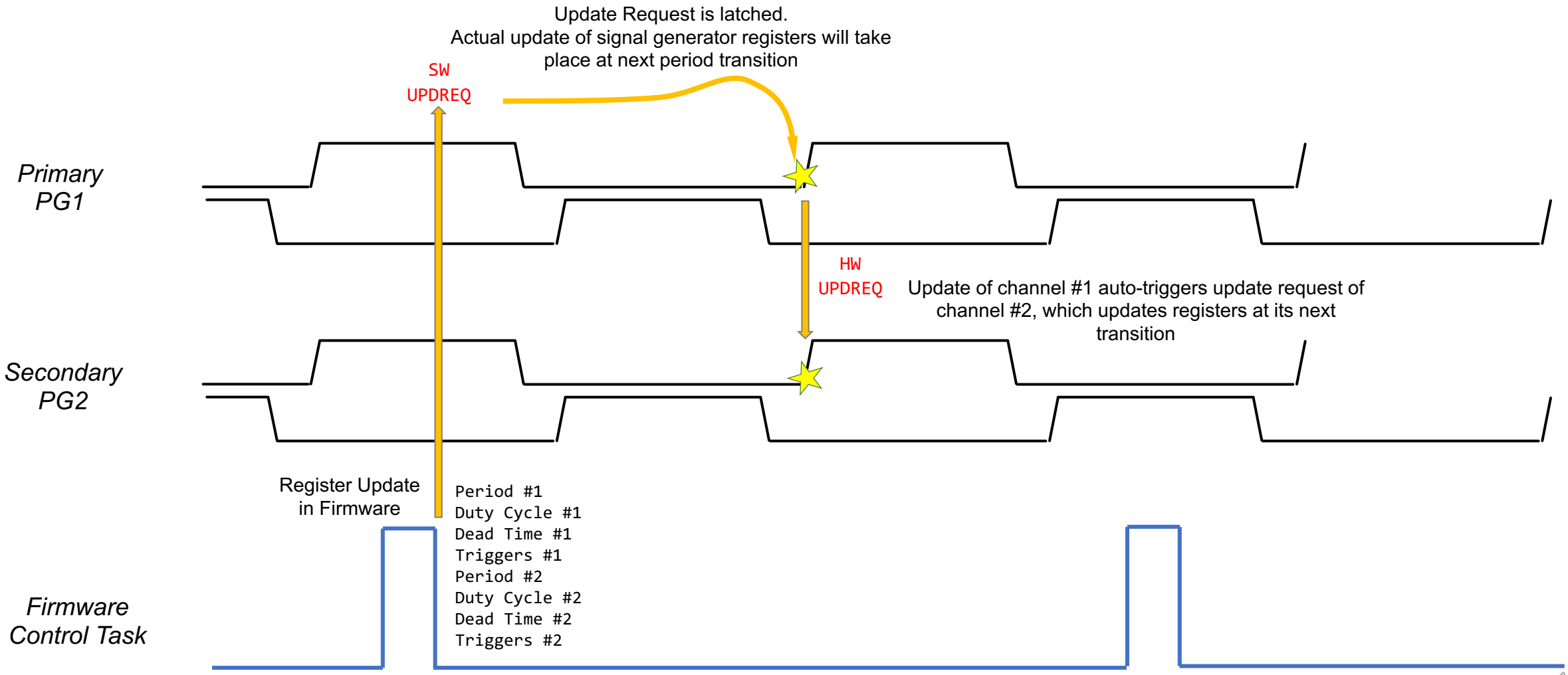
PWM Daisy Chain Configuration

EPC9149 LLC Converter



- **Start-of-Cycle (SOC) of PWM channel PG2 is synchronized by PWM channel PG1 its trigger placed within its period at PGxTRIGy**
- **Each PWM channel remains fully configurable for individual duty cycles, dead times, periods, triggers etc.**
- **Frequency changes are applied to both channels simultaneously due to the synchronization trigger. All other properties, however, must be set by updating all desired registers independently**

Daisy chain update



Control Implementation

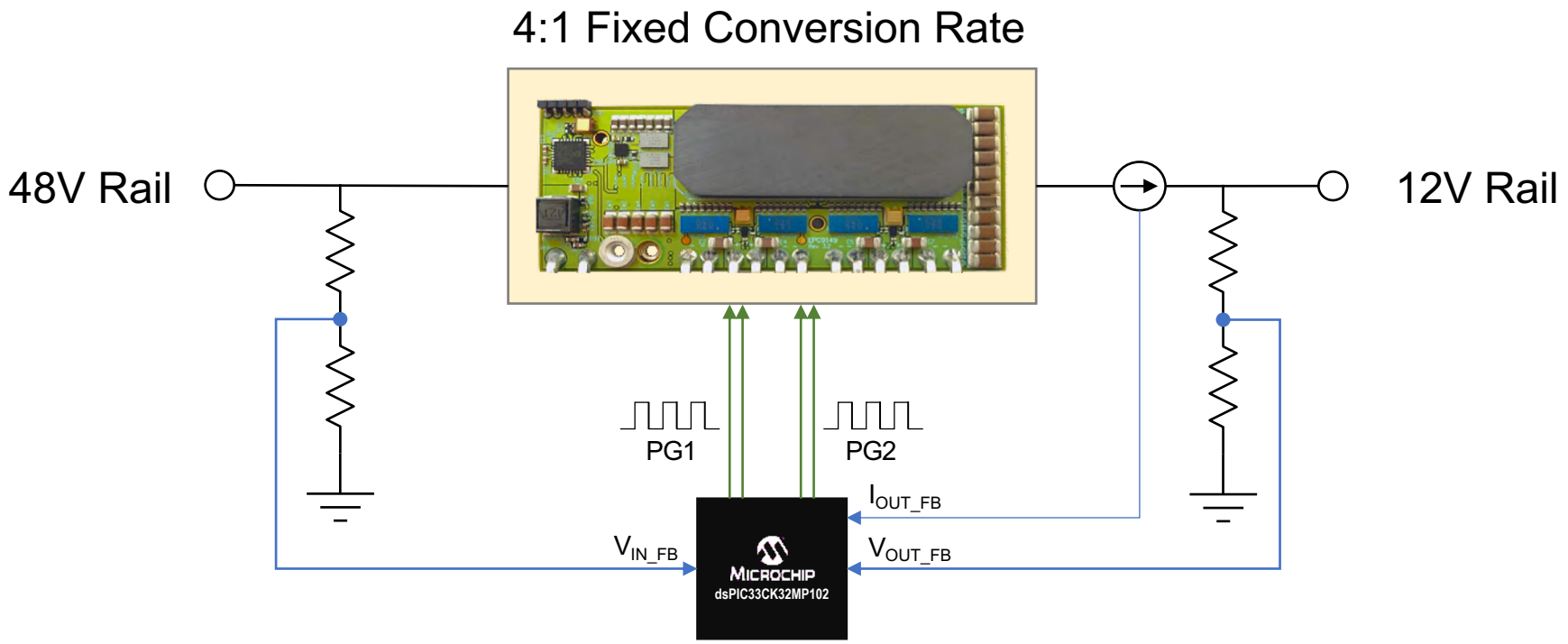
EPC9149 LLC Converter

Operating Frequency Control:

- 4:1 conversion rate kept constant by VIN to VOUT comparison
- Continuous voltage monitoring of input and output voltage (UVLO, OVLO, OVP)

Duty-Cycle Startup Procedure:

- Timer-controlled voltage ramp start-up keeping voltage growth monotonous
- Optimized pulse generation during duty cycle modulation for reduced component stress

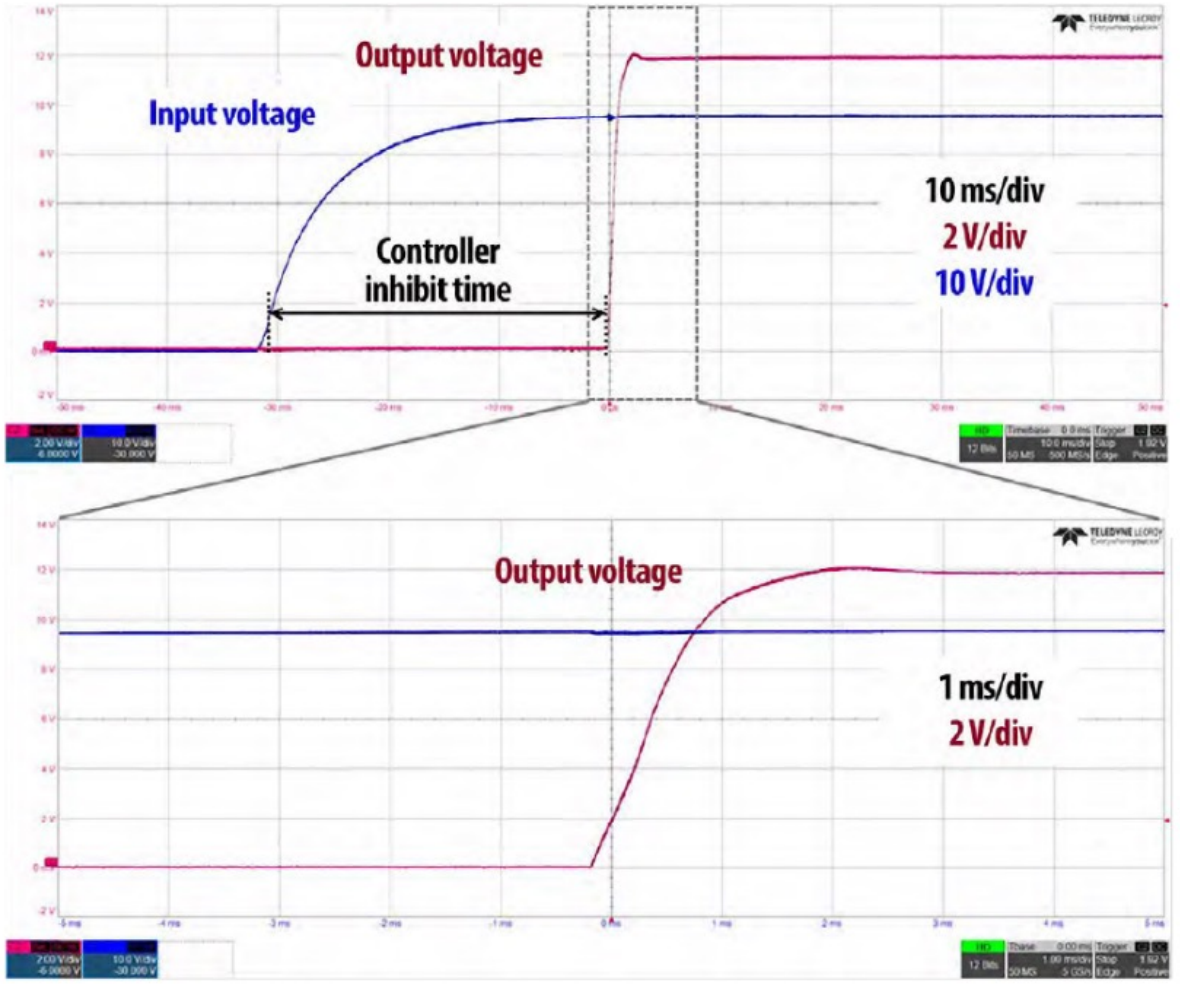


Bi-directional capable

Startup

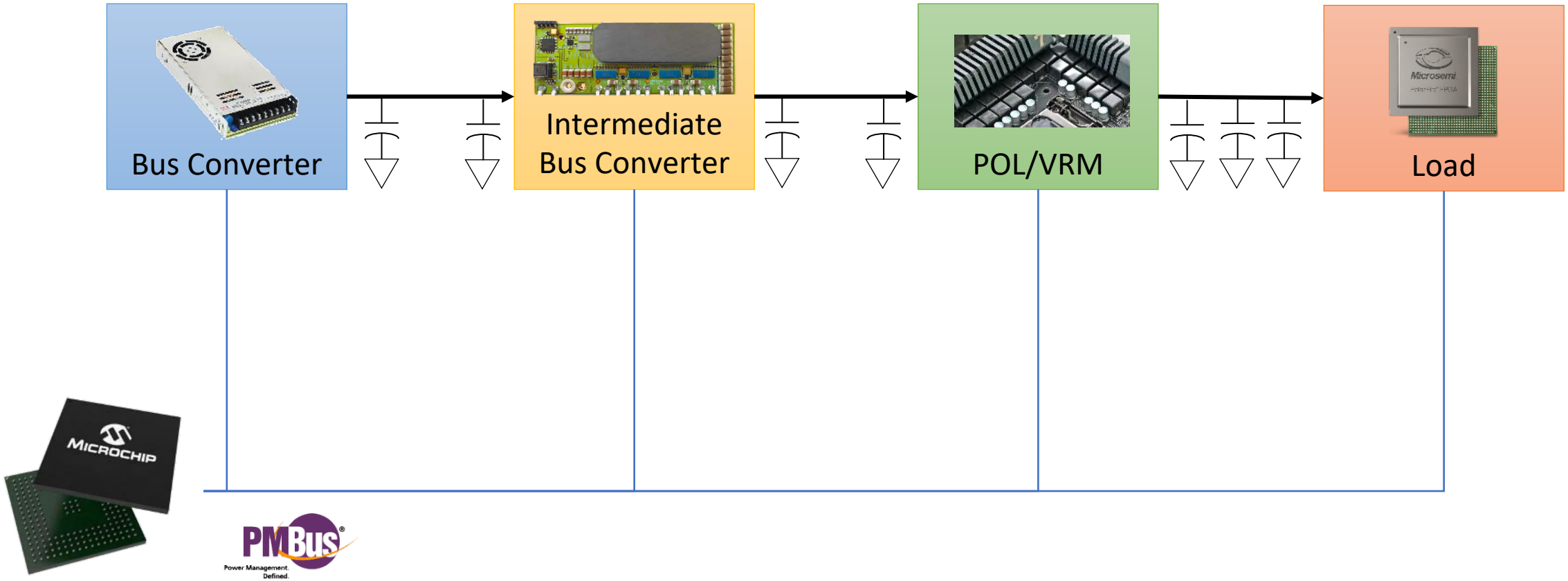
EPC9149 LLC Converter

- Programmable output voltage ramp timing for advanced sequencing
- Monotonous startup
- Component stress reduction by optimized pulse generation based on voltage level and load current feedback



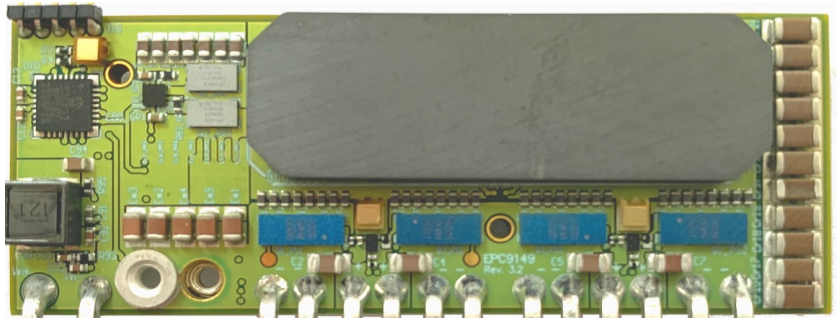
PDN System Design Considerations

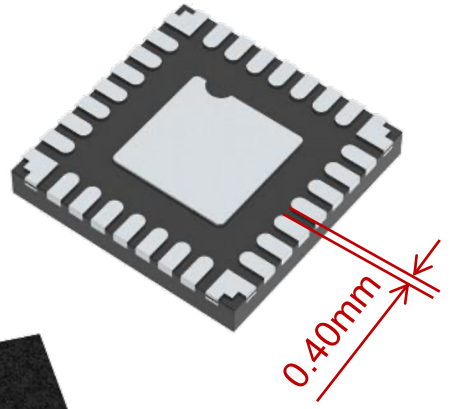
EPC9149 LLC Converter

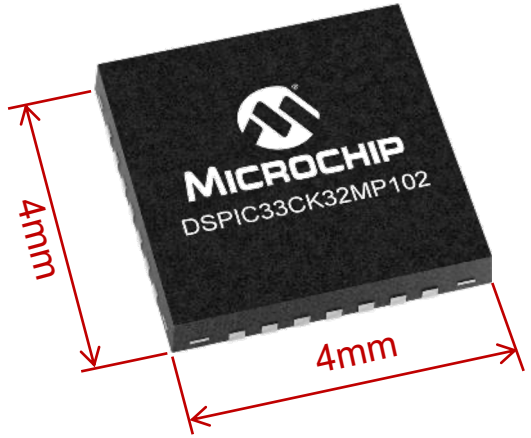


Summary

- **1 kW LLC design**
  - 58.4 x 22.9 x 10 mm volume
- **eGaN FETs**
  - Achieves high efficiency
  - Enable high power density (1226 W/in3)
- **Propagation mismatches**
- **dsPIC33C**
  - PWM Logic Programmability
  - 250ps PWM resolution for precise ZVS timing
  - Very small at 4x4 mm







May The *Power* Be With You