實驗板程式範例:

- APP_CPLD1_MCU 範例: <u>https://www.microchip.com.tw/modules/tad_uploader/index.php?op=dlfile&cfs</u> <u>n=271&cat_sn=39&name=cpld.zip</u>
- APP_CPLD1_ATF1502 範例:
 https://www.microchip.com.tw/modules/tad_uploader/index.php?op=dlfile&cfs n=272&cat_sn=39&name=atf1502.zip

示範影片:

- 開發軟體安裝說明影片:<u>https://youtu.be/Dv3imDQrVos</u>
- CPLD 燒錄範例影片: <u>https://youtu.be/syg608gLVYs</u>
- CPLD 開發範例影片: <u>https://youtu.be/F1s_vNdrERM</u>

使用工具:

PCB : Microchip Taiwan office APP-CPLD01

CPLD part number : ATF1502ASV

開發環境: WinCUPL v5.30.3, https://www.microchip.com/en-us/products/fpgasand-plds/spld-cplds/pld-design-resources

燒錄器:ATDH1150USB

燒錄軟體: ATMISP V7.3

MCU: PIC16F18446

開發環境: MPLAB X IDE V6.15

PIC16F1xxxx_DFP: 1.25.389

Compiler : XC8 v2.46

燒錄器:PICkit4

, WinCUPL

範例程式功能簡介:

以 CPLD 做一個 10 進位的計數器, CPLD 的 pin 19, 22, 25 & 28 輸出點亮 LED, 輸入 訊號為 clock, dir(counter 計數方向, 加 or 減), clr(清除輸出) & ena(輸出致能),這些 輸入訊號分別是由 MCU 的 RC0(pin 16), RC1(pin 15), RC2(pin 14) & RC3(pin 7)輸出 來完成.

安裝開發環境&燒錄軟體:

先從 Microchip 網站下載此兩軟體, WinCUPL v5.30.3 & ATMISP V7.3, 先儲存在硬碟 後,解壓縮此兩軟體,然後安裝此兩軟體,在安裝過程中,只需按 Next or Yes 按鍵即可 順利安裝此兩個軟體. WinCUPL 預設安裝路徑 C:\Wincupl, ATMISP 安裝在 C:\ATMISP7.

燒錄程序:若想先試試看 CPLD 的工作狀況,則可先做燒錄的動作

- 1. APP-CPLD01 jump 設定: P1 & P2: 2&3 pin 短路, J1, J3, J4, J5 & J7:空接, J2 & J6:短路
- 2. 將燒錄器 ATDH1150USB 先連接到電腦的 USB 埠
- 3. 開啟 ATMISP
- 4. 設定燒錄程序的 project, File → New → 1 → OK

Create New Devic	e Chain X				
Enter number of devices					
1					
ОК	Cancel				

5. Device Name 選擇 ATF1502ASV, JTAG Instruction 選擇 Program/Verify, JEDEC File 選擇 COUNT10_B.jed, →OK

Device Property	×
Device Name	
ATF1502ASV	Device #1
JTAG Instruction	Instruction Width
Program/Verify	10
JEDEC File	
D:\data\ATF1502\COUNT10_B.jed	Browse
OK Reset	

6. 從 USB 埠連接電源至 APP-CPLD01 USB1, 並且將燒錄器 ATDH1150USB 連接至 APP-CPLD01 的 JTAG ISP Header, 接線如下圖



7. 按 Run 按键, 稍等一點時間即可看到以下畫面, 表示燒錄成功

CTMISP ATMISP	– 🗆 X
File Edit View Options Help	
D 😅 🖬 % 🖻 🖻 🚭 🥐	
Device Chain Hierarchy Untitled Device Name: ATF1502ASV JTAG Instruction: Program/Verify Instruction Width: 10 DCODE: YES JEDEC File: D:\data\ATF1502\COUNT10_B.jed	Hardware Setting # of Dev. Port Setting Cable Type 1 USB ATDH1150USB SVF File Name Write SVF file Write SVF file Use state reset SVF Version TCK period (us) Revision D 1
Iog: erasing device #1. log: programming device #1. log: verifying device #1: OK log: JTAG instructions finished successfully.	Run Exit
Ready	

8. 目前支援 Microchip SPLD/CPLD 的台灣本地廠商分別是研儀 LABTOOL-48UXP, 崇貿 SG8000, 岱鐠 NuProg-E2

有關 MCU 的開發&燒錄請參考 Microchip MCU 的相關資料,在此不再贅述,為此 demo board 上的 MCU 燒錄檔案名稱為 CPLD.X.production.hex

接下來我們就要討論如何開發 CPLD 的程式

- 1. 開啟 WinCUPL
- 2. File → New → Project, 然後輸入以下資訊,然後按 OK

Design Properties

Name:	Count10_B	OK
PartNo:	ATF1502ASV	Cancel
Date:	2024/4/24	
Revision:	01	
Designer:	Richard Hsu	
Company:	Microchip Taiwan office	
Assembly:	None	
Location:		
Device:	f1502isptqfp44	

3. 選填輸入 pin 數量, 因 demo board 輸入訊號有四個,故輸入 4, →OK

INPUT PINS	×
How many input pins are there	ОК
	Cancel
4	

4. 選填輸出 pin 數量, 因 demo board 輸入訊號有五個,故輸入 5, →OK

OUTPUT PINS	×
How many output pins are there	ОК
	Cancel
5	

5. 此程式中沒有用到 pinnode, 故保留為 0, →OK

PINNODES	×
How many pinnodess are there	OK Cancel
٥	

6. 至此 project 表頭就建立好了

```
Name Count10_B;
PartNo ATF1502ASV ;
Date 2024/4/24;
Revision 01 ;
Designer Richard Hsu ;
Company Microchip Taiwan office ;
Assembly None ;
Location ;
Device f1502isptqfp44 ;
/* ***************** INPUT PINS *****************************/
PIN =
                                                                   */
                               ; /*
                                ; /*
PIN
      =
                                                                   */
PIN
      =
                                ; /*
                                                                    */
                                ; /*
                                                                    */
PIN
      =
/* ***************** OUTPUT PINS ******************************/
PIN =
                               ; /*
                                                                    */
                               ; /*
PIN
      =
                                                                    */
                                ; /*
PIN
      =
                                                                    */
                                ; /*
PIN
                                                                   */
      =
PIN
      =
                                ; /*
                                                                   */
```

7. 現在就依線路圖將輸出入 pin 定義寫入

```
/** Inputs **/
Pin 37 = clk;
Pin 39 = clr;
Pin 38 = dir;
Pin 40 = !ena;
/** Outputs **/
Pin 28 = Q0;
Pin 25 = Q1;
Pin 25 = Q1;
Pin 22 = Q2;
Pin 19 = Q3;
Pin 18 = carry;
```

8. 接下來輸入程式本體

/** Declarations and Intermediate Variable Definitions **/				
field count = [0301;	/* declare counter bit field */		
Sdefine S0 'b'0	000	/* define counter states */		
Sdefine S1 'b'0	001	,,		
Sdefine S2 'b'0	010			
Sdefine S2 'b'0	011			
Sdefine S4 'b'0	100			
Sdefine S5 'b'0	101			
Sdefine S6 'b'0	110			
Sdefine S7 'b'0	111			
Sdefine S8 'b'10	000			
Sdefine S9 'b'10	001			
count.ck = clk;				
count.oe = ena;				
field mode = [c]	lr,dir];	/* declare mode control field */		
up = mode:0;		/* define count up mode */		
down = mode:1;		/* define count down mode */		
clear = mode:[2	3];	/* define count clear mode */		
/** Logic Equat:	ions **/			
Sequenced count	{	<pre>/* free running counter */</pre>		
present 30	if up	next S1;		
	if down	next S9:		
	if clear	next S0;		
	if down	out carry;		
present S1	if up	next S2;		
	if down	next S0;		
	if clear	next S0;		
present S2	if up	next S3;		
	if down	next S1;		
	if clear	next S0;		
present S3	if up	next S4;		
	if down	next S2;		
	if clear	next S0;		
present S4	if up	next S5;		
	if down	next S3;		
	if clear	next S0;		
present S5	if up	next S6;		
	if down	next S4;		
	if clear	next S0;		
present S6	if up	next S7;		
	if down	next S5;		
	if clear	next S0;		
present S7	if up	next S8;		
	if down	next S6;		
	if clear	next S0;		
present S8	if up	next S9:		
	if down	next S7:		
	if clear	next SO:		
present S9	if up	next SO:		
	if down	next S8:		
	if clear	next S0;		
l.	if up	out carry: /* assert carry output */		
D.				

- 9. 儲存此 project, File → Save As, 請自行選擇檔案名稱 & 儲存路徑, 選擇 project 的副檔名為.pld, 然後選擇 Save.
- 10. 接下來要建立 simulation file, File → New → Text File
- 11. 首先 copy Project file 的表頭至此新檔案

```
Name Countl0_B ;

PartNo ATF1502ASV ;

Date 2024/4/24 ;

Revision 01 ;

Designer Richard Hsu ;

Company Microchip Taiwan office ;

Assembly None ;

Location ;

Device f1502isptqfp44 ;
```

12. 輸入訊號的排列順序,如以下例子

ORDER: clk, clr, dir, !ena, %2, Q3..Q0, %1, carry;

13. 再輸入各訊號之間的 high or low 關係,如以下例子

VECT	DRS:				
C100	"0"	L	1*	synchronous clear to	state 0 */
C000	"1"	L	1*	count up to state 1	*/
C000	"2"	L	1*	count up to state 2	*/
C000	"3"	L	1*	count up to state 3	*/
C000	"4"	L	1*	count up to state 4	*/
C000	"5"	L	1*	count up to state 5	*/
C000	"6"	L	1*	count up to state 6	*/
C000	"7"	L	1*	count up to state 7	*/
C000	"8"	L	1*	count up to state 8	*/
C000	"9"	H	1*	count up to state 9 -	carry */
C000	"0"	L	1*	count up to state 0	*/
C010	"9"	L	1*	count down to state 9	*/
C010	"8"	L	1*	count down to state 8	*/
C010	"7"	L	1*	count down to state 7	*/
C010	"6"	L	1*	count down to state 6	*/
C010	"5"	L	1*	count down to state 5	*/
C010	"4"	L	1*	count down to state 4	*/
C010	"3"	L	1*	count down to state 3	*/
C010	"2"	L	1*	count down to state 2	*/
C010	"1"	L	1*	count down to state 1	*/
C010	"0"	H	1*	count down to state 0	- carry*/
C0012	ZZZZ	L	1* 1	est tri-state	*/
C000	"2"	L	1*	count up to state 2	*/
C100	"0"	L	1*	synchronous clear to	state 0 */

- 14. 儲存此 simulation file, File → Save As, 請將檔案與 project 儲存在同一路徑,並且 使用相同的檔案名稱,但附檔案選擇.si, 然後選擇 Save.
- 15. 至此,整個 project 已經完整建立
- 16. 接下來,我們要 compile & simulate 整個程式,看是否有錯誤,並產生燒錄檔案.jed
- 17. Options→Compiler →General,請勾選"JEDEC name = PLD name" & "View Simulation Results", → Apply → OK.

Output Files	Minimization	Optimization
General	Library	
🔲 Secure Device		
🔲 Deactivate Unused	IOR Terms	
🔽 Simulate		
🔲 One-hot-bit State M	lachine	
JEDEC name = PLI	D name	
View Simulation Re	sults	

18. Compile & simulation, Run \rightarrow Device Dependent Compile

Run	Utilities	Window	Help	
	Device De	pendent Co	ompile	F9
	Device Inc	Ctrl+F9		
	F7			
	Device Inc	lependent	Simulate	Ctrl+F7

19. 可以看到以下 compile 訊息

	Compilation	\times	
1	Status:	Compilation successful!	OK
	Information:	Total Time: 1 secs	
	Warnings:	60	
k	Errors:	0	

Messages	
Module: cuplx	
Module: cupla	
Module: cupib	
Module: cupim	
Module: cupic	
Module: find1502	
Module: vsima	
total time: 1 secs	

20. 按 OK 後就會看到 simulation 的結果



21. 此時燒錄檔案.jed 也產生了,可用此檔案燒錄到 ATF1502ASV

