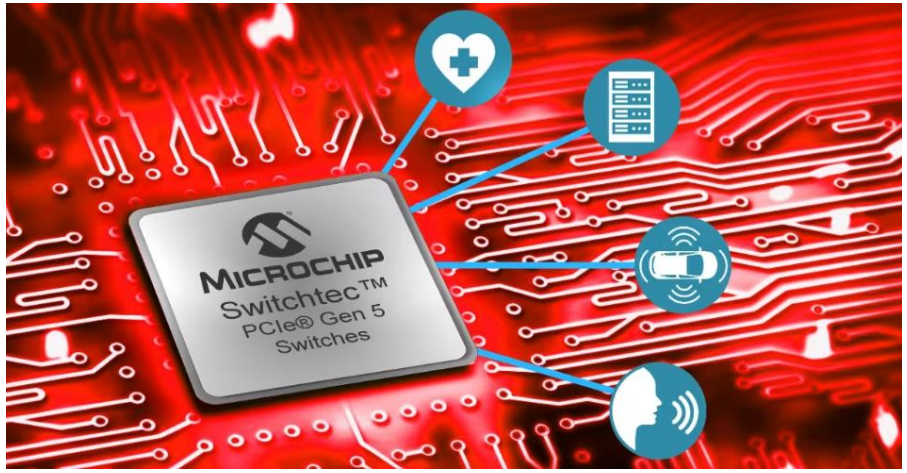
高速資料傳輸的利器
PCIe 無所不在

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

Kevin Huang May 2024

Agenda

- PCIe Applications
- What is PCIe?
- Microchip PCIe Solutions
- PCIe over Cable Demo

Agenda

- **PCIe Applications**
- What is PCIe?
- Microchip PCIe Solutions
- PCIe over Cable Demo

PCIe® is Everywhere

PCIe® technology is pervasive in systems such as CPUs, GPUs, NICs, SSDs, FPGA, and other multiple end points that require low latency, high performance interconnect for diverse applications.

AI/ML

Cloud Infrastructure
Enterprise Storage

Cloud Gaming

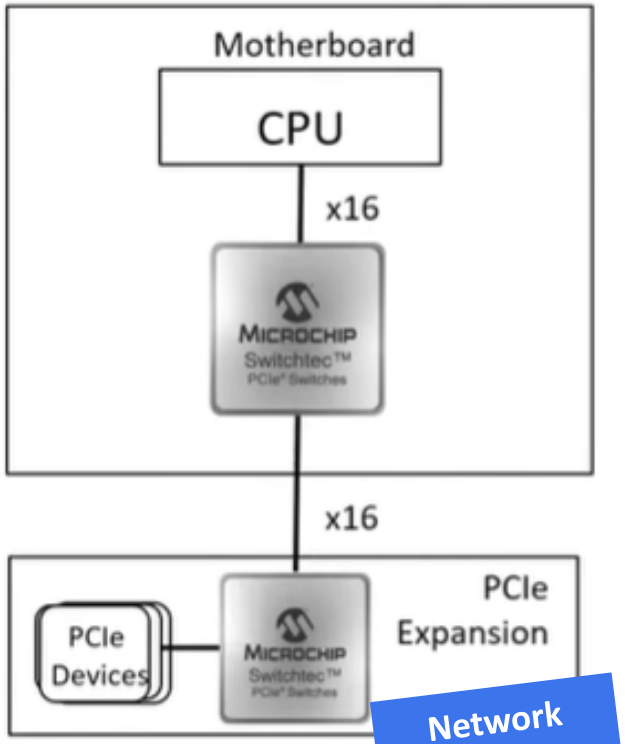
Military Systems

Telecommunications
System

Automotive
Self-Driving Cars

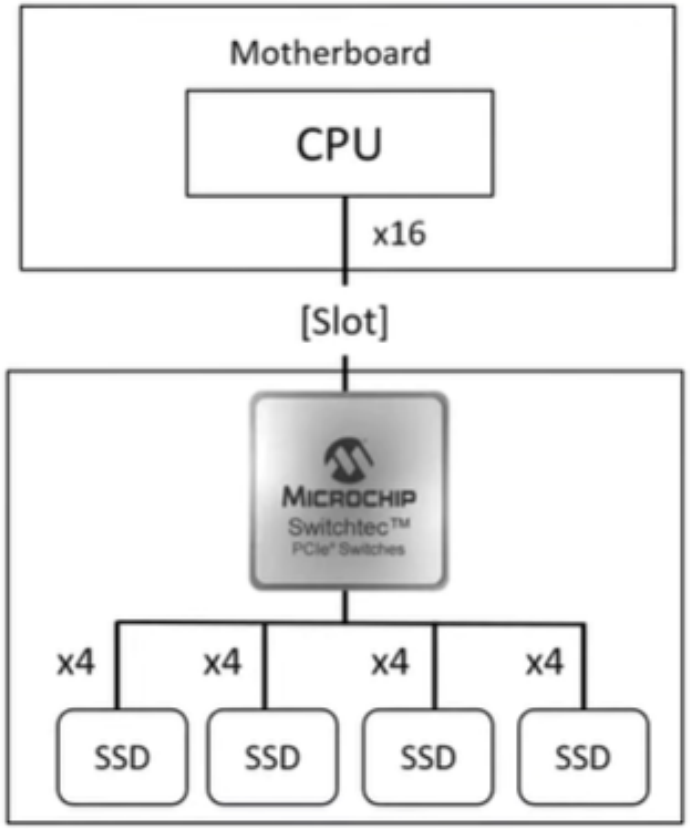
PCIe Fanout Switch Applications

PCIe® Expansion Use Case



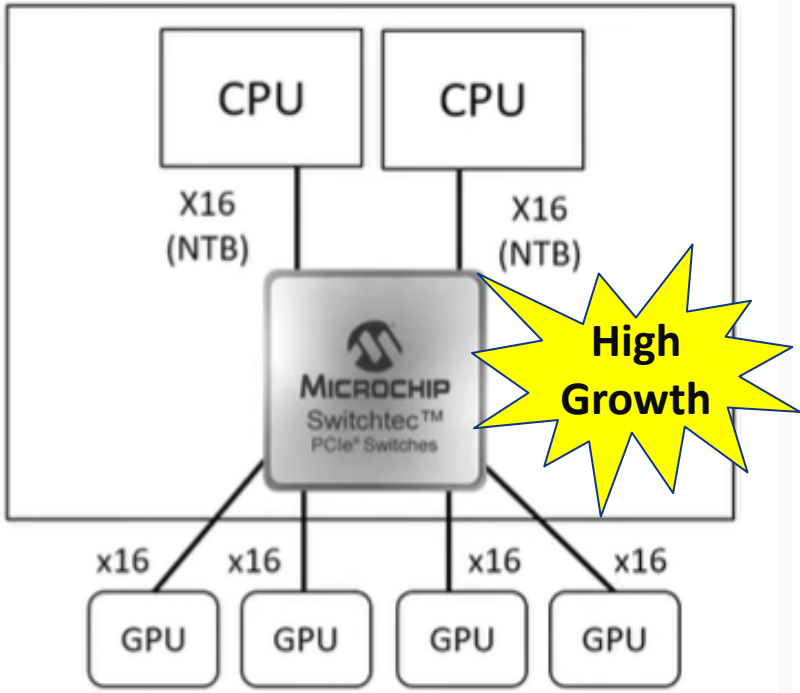
- Telecommun
- Data communications
- Defense systems
- Radar System

Server Use Case



- Embedded Systems
- PCIe Expansion
- Video Broadcasting
- DVR

Machine Learning / AI Use Case



- Servers
- GPU workstations
- Machine Learning / AI
- Cloud Infrastructure
- Storage systems

MICROCHIP

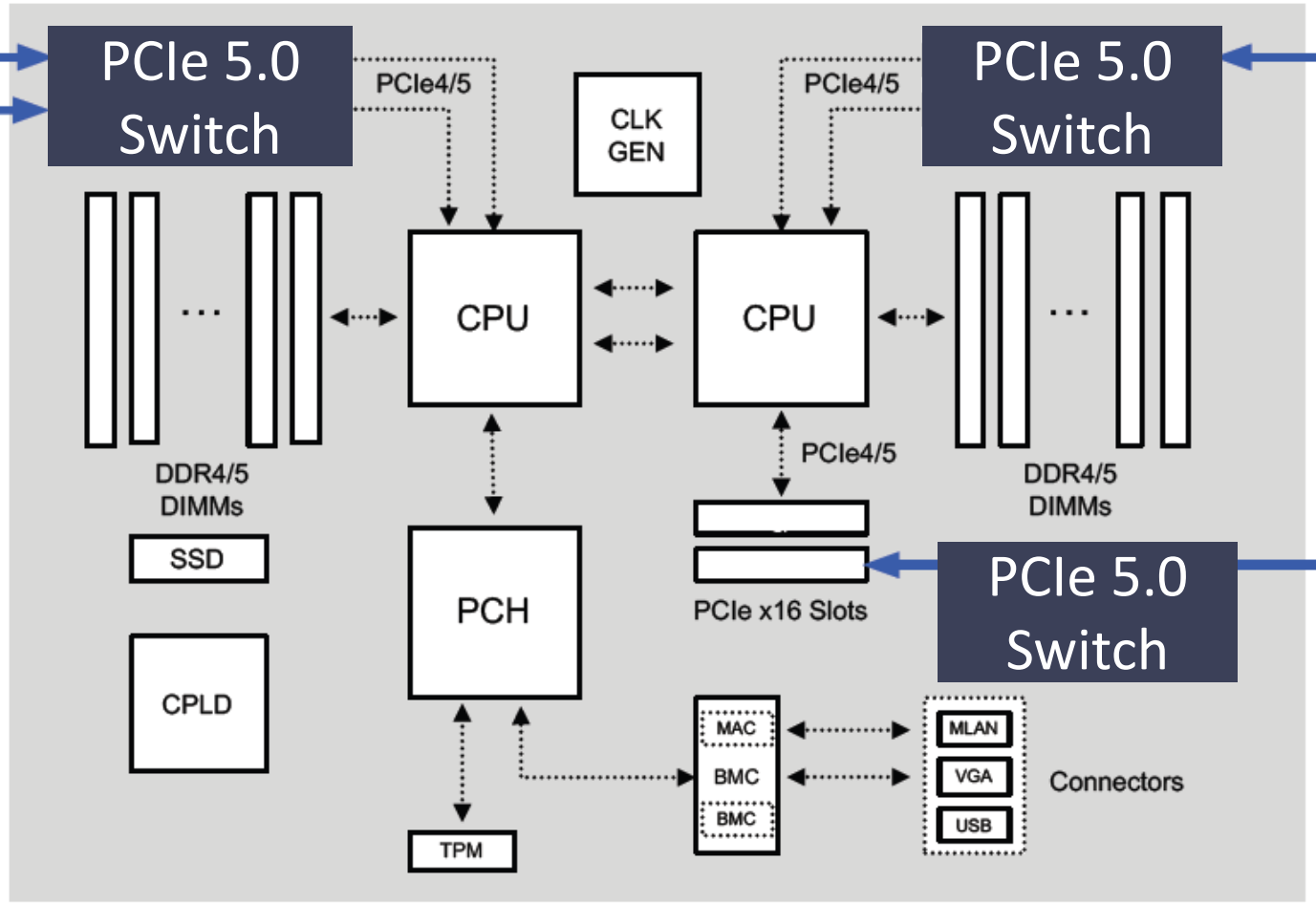
PCIe Switch Application Market Segments .1

- Server systems:
  - PCIe switches are commonly used in server systems to increase the number of PCIe devices that can be connected to the system. This can include network adapters, storage controllers, and GPUs
- Data centers:
  - PCIe fan out switches can be used in data centers to help manage the flow of data between multiple PCIe devices, which can help improve overall system performance and reduce latency.
- Cloud computing:
  - PCIe switches are also used in cloud computing environments to connect multiple virtual machines to a single physical PCIe device, such as a GPU, to improve the efficiency of the cloud computing environment.

Data Center Typical Application with PCIe Switches

NIC/SmartNIC

PCIe-FC Host Bus Adapter
(HBA)
(Storage Area Networks)



GPU/AI Accelerator
(Direct Attach Storage)

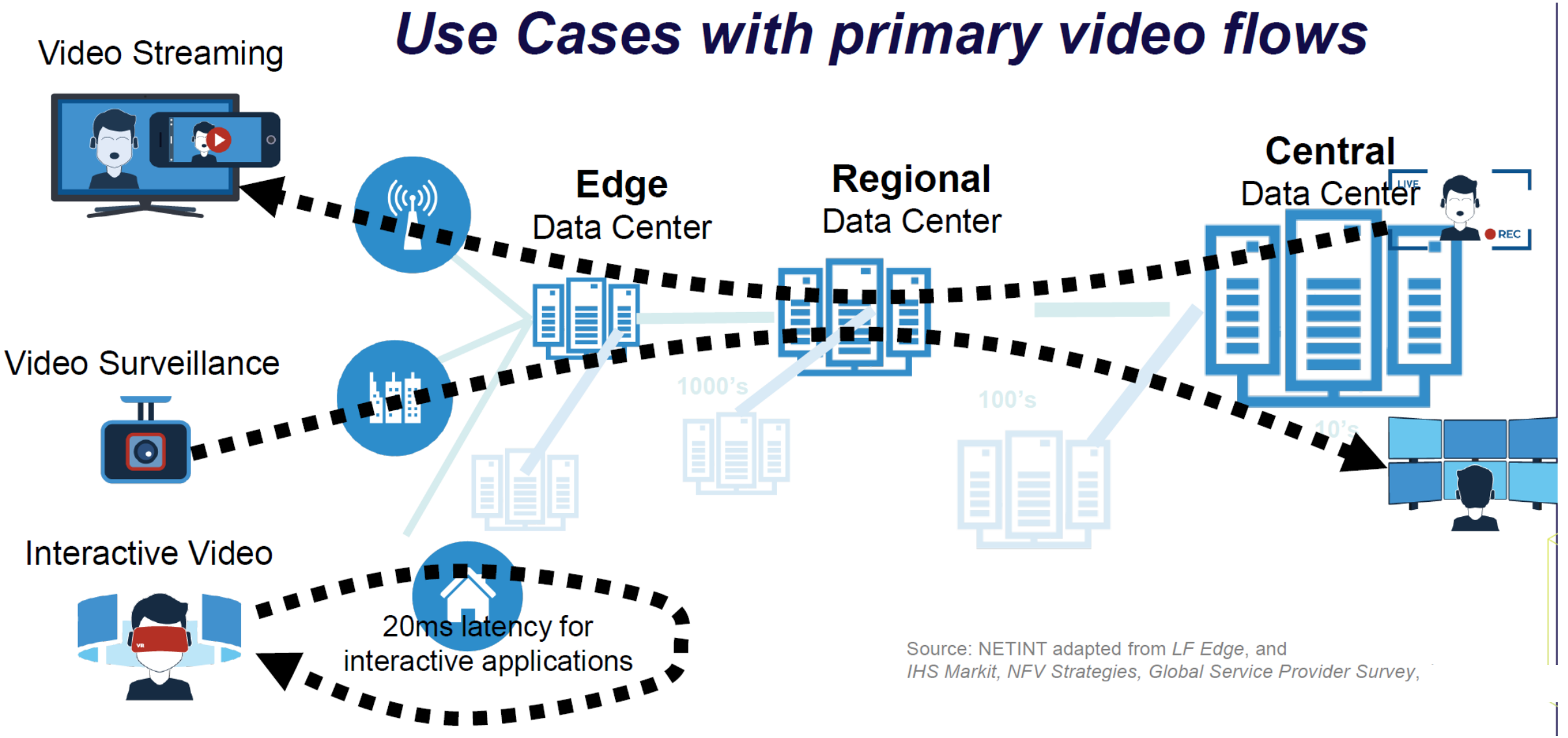
U.2 MVMe SSD
(Direct Attach Storage)

PCIe Switch Application Market Segments .2

- **Media and entertainment:**
  - PCIe switches are used with video processing/codec to facilitate data transfer from the edge to the cloud
- **Gaming systems:**
  - PCIe switches can be used in gaming systems to connect multiple GPUs or other high-performance devices to a single PCIe slot, which can help improve gaming performance and reduce latency
- **Industrial and embedded systems:**
  - PCIe switches are often used in industrial and embedded systems where space and power consumption are critical factors. They can help reduce the number of PCIe slots needed, which can help save space and power

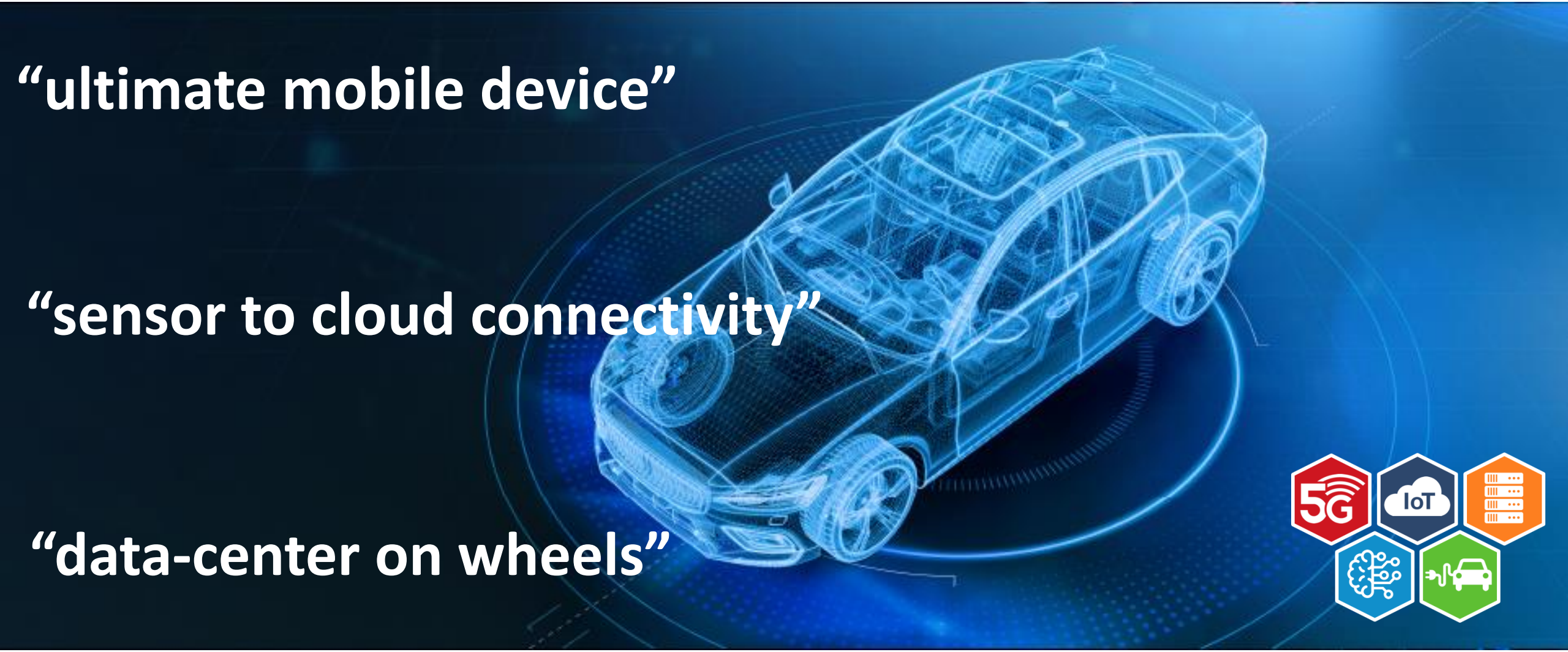
Video Edge Storage and the Video Cloud

Use Cases with primary video flows

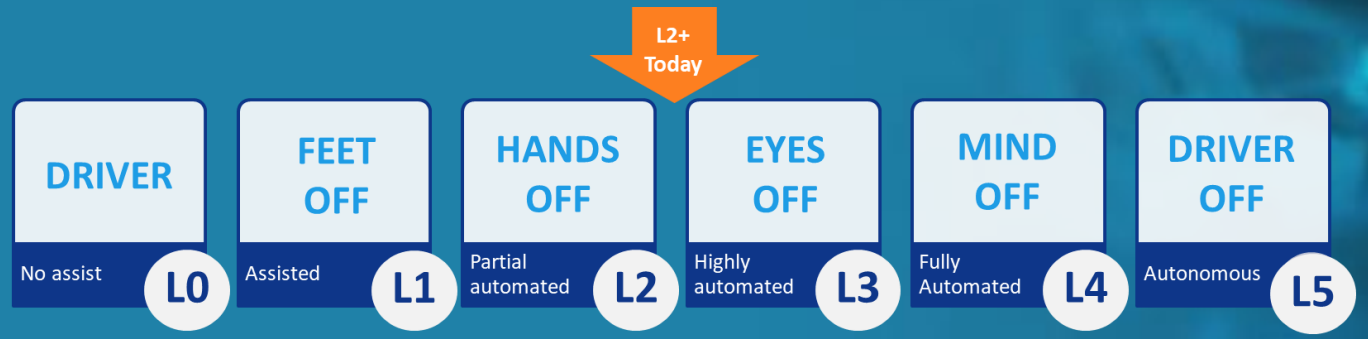


Source: NETINT adapted from *LF Edge*, and
IHS Markit, NFV Strategies, Global Service Provider Survey,

Future of Automotive



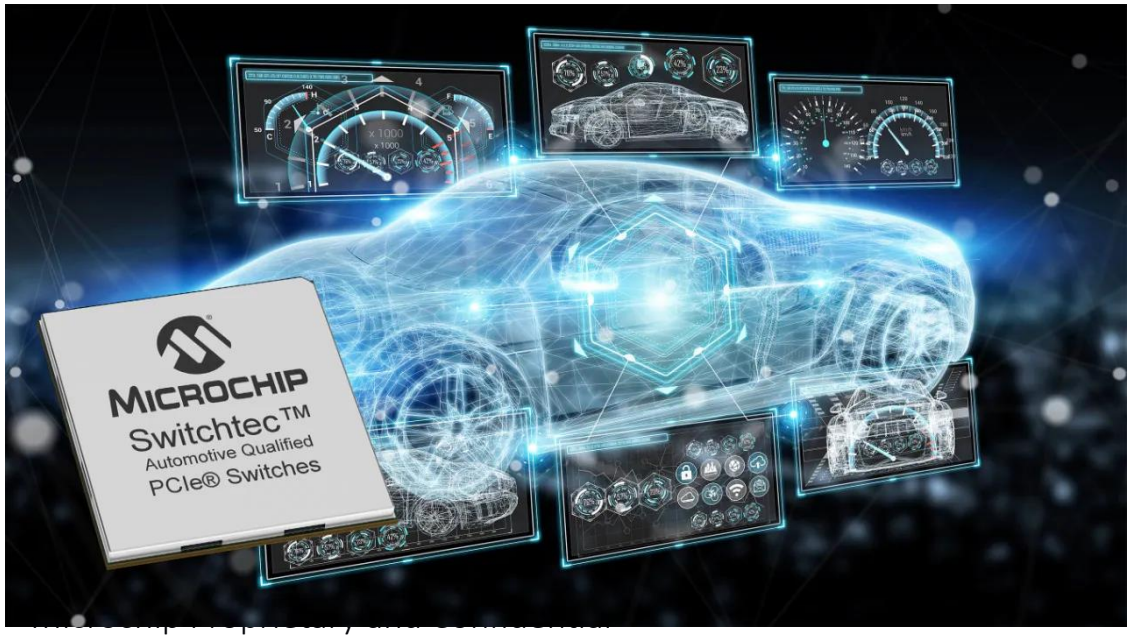
Autonomous Mobility Drives Big Data



- Camera/sensor data
- ECU interconnectivity
- Redundant safety networks
- Cloud connectivity
- Data logging

Why PCIe For Automotive?

- It is a natural I/O bus that is already available in most SoCs, controllers, & CPUs.
- Open standard with a large ecosystems and multiple vendors.
- Point-to-Point architecture
- Supports chip-to-chip, backplanes, short cables and optical communication topologies.
- Extremely low latency compared to other protocols.
- Scalable bandwidth



Agenda

- PCIe Applications
- **What is PCIe?**
- Microchip PCIe Solutions
- PCIe over Cable Demo

PCI-SIG - Organizing Body

- **PCI-SIG = Peripheral Component Interconnect Special Interest Group**
- Industry organization specifying
  - Peripheral Component Interconnect (PCI),
  - PCI-X
  - PCI Express (PCIe)
- Based in Beaverton, Oregon
- Formed 1992
- Specifications are available to members of the organization
  https://pcisig.com/specifications

Spec History: PCIe Speed Comparison

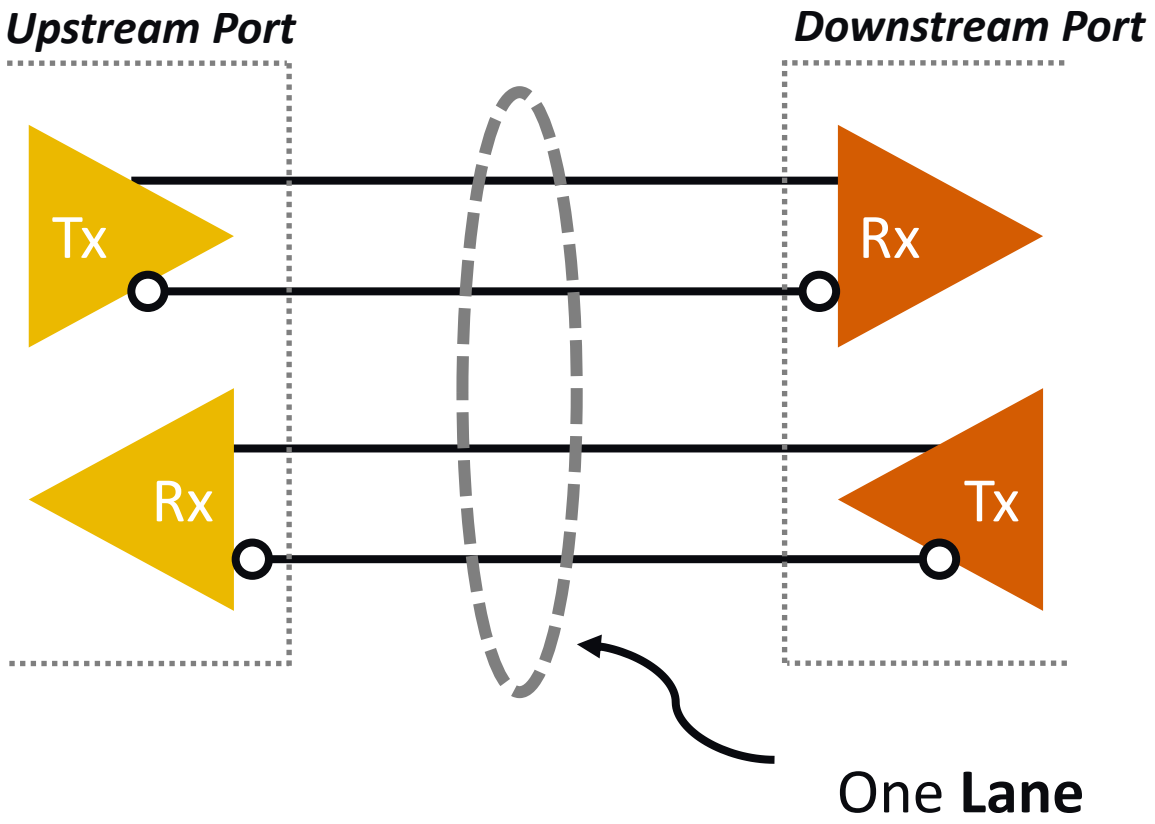
PCIe Generation	Encoding	Transfer Speed (GT/s)	X1 Throughput (GB/s)	X4 Throughput (GB/s)	X8 Throughput (GB/s)	X16 Throughput (GB/s)
Gen 1	8b/10b	**2.5**	0.25	1	2	4
Gen 2	8b/10b	**5**	.5	2	4	8
Gen 3	128b/130b	**8**	~1	~4	~8	~16
Gen 4	128b/130b	**16**	~2	~8	~16	~32
Gen 5	128b/130b	**32**	~4	~16	~32	~64

PCIe Future Timeline

Specification in Progress	Draft 0.3	Draft 0.5	Draft 0.7	Draft 0.71	Draft 0.9	Final 1.0
16 GT/s NRZ **PCI Express 4.0 Base Electrical Chapter**			Workgroup vote on April 7		Workgroup approved on March 30, 2017	WG approved on Sept. 28, 2017
32 GT/s NRZ **PCI Express 5.0 Base Electrical Chapter**	WG approved 5/11/17	WG approved on 10/3/17	WG approved on 03/29/18		WG approved on 09/27/18	WG approved on 05/23/19
64 GT/s PAM4 **PCI Express 6.0 Base Electrical Chapter**	WG approved 9/12/19	WG approved 12/12/19	WG Approved 10/08/20	WG Approved 06/24/21	WG Approved 09/30/21	WG Approved 12/16/21
128 GT/s PAM4 **PCI Express 7.0 Base Electrical Chapter**	WG approved 03/23/23	Dec 2023	Mar 2025		Sep 2025	Dec 2025

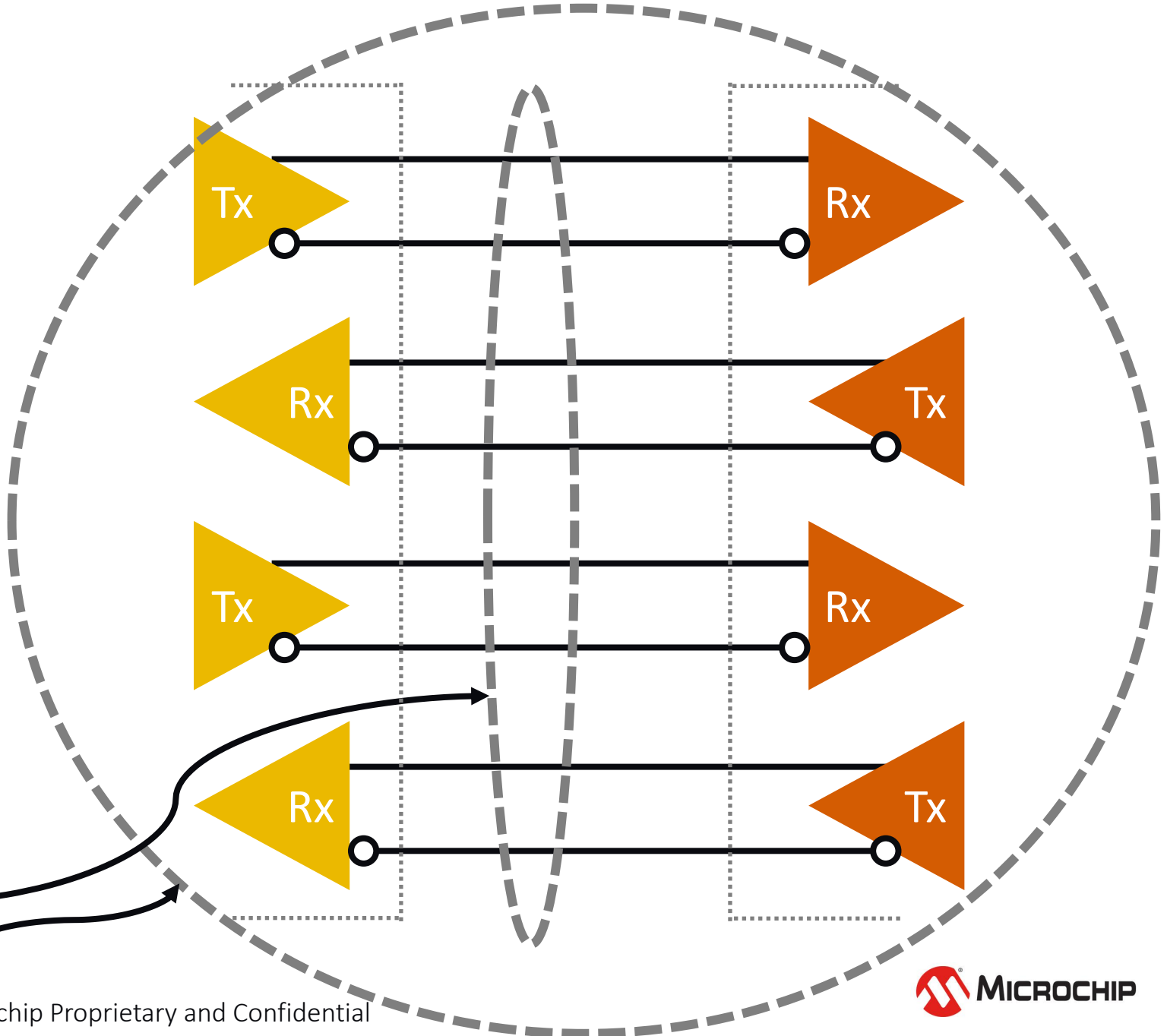
PCIe Elements

- A **lane** includes a differential transmitter and a differential receiver, 4 wires per lane.
- A **lane** is full-duplex (Also regarded as dual-simplex)
  - Dual-Simplex connection, transfers in both direction simultaneously
- Symmetric: A port has the same number of lanes in each direction (RX & TX)



PCIe Elements

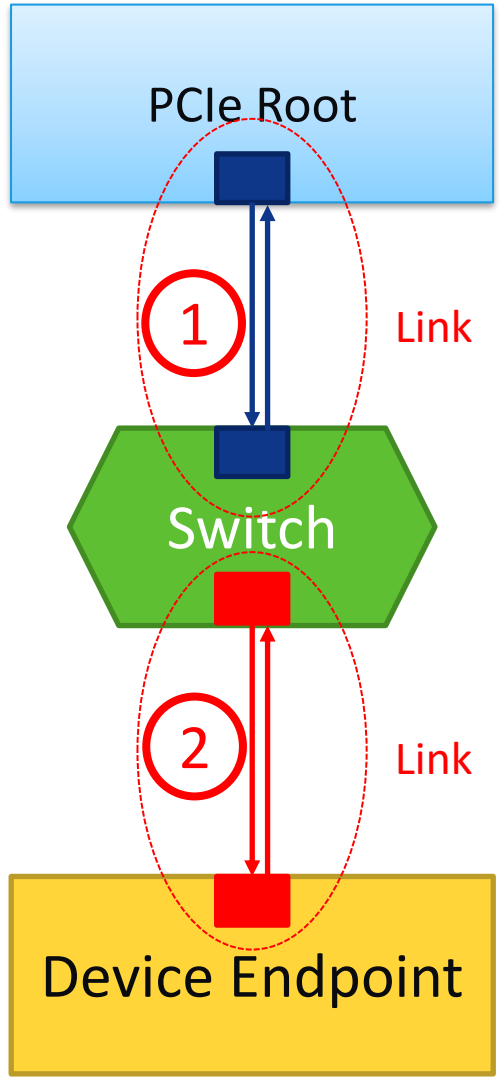
- A **link** consists of 1 to 32 **lanes** which connect two devices within in a PCIe hierarchy
- All **lanes** within a **link** operate at the same speed
- Lane count doubles, then bandwidth doubles.



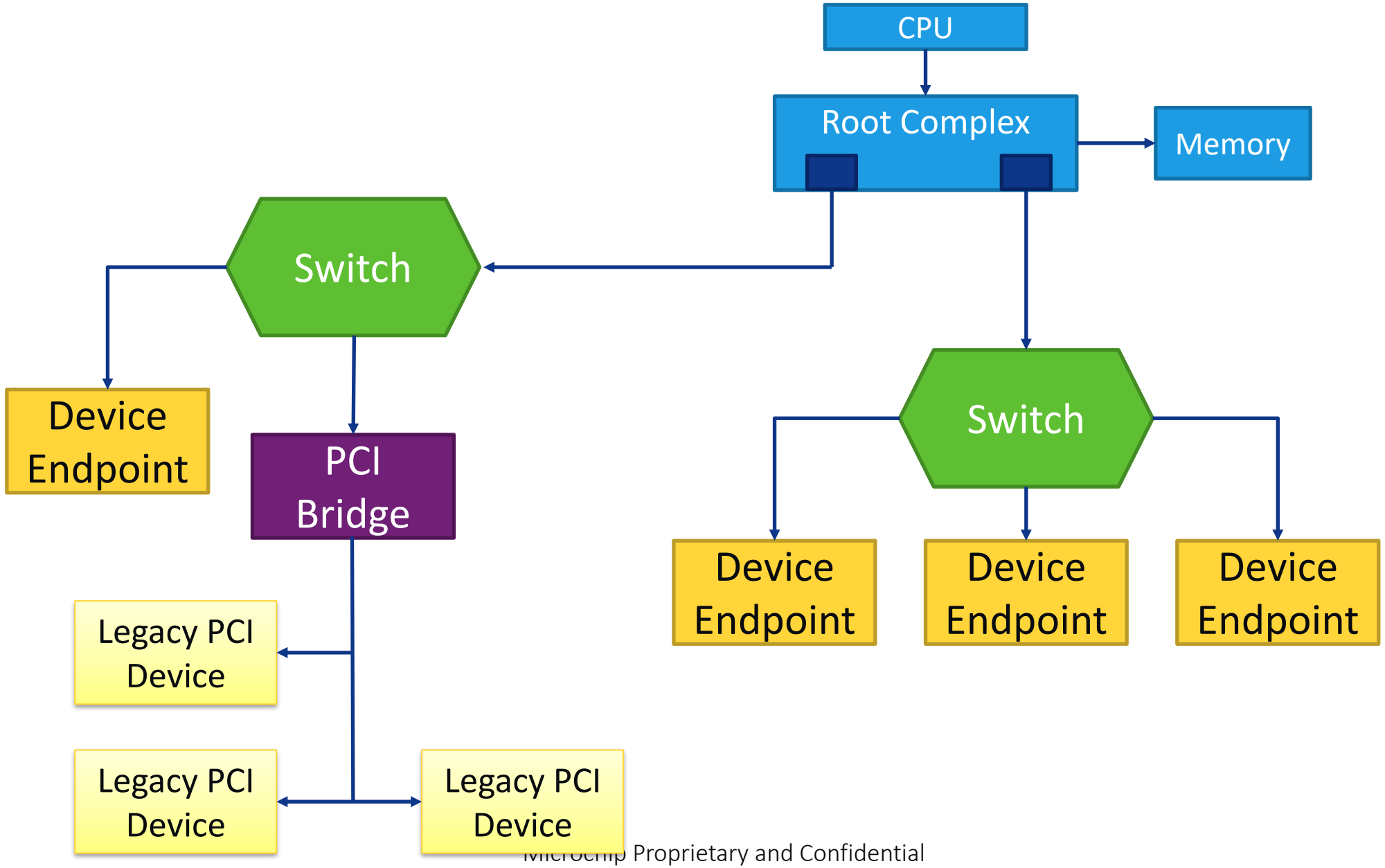
PCIe Systems

PCIe Port Terminology:

- Must be viewed from each ‘link perspective’
- Link: PHY-to-PHY Connection
- Link width can be x1, x2, x4, x8, x12, x16, x32 lanes (Bifurcation)
- Link Speed can be different at point 1 and 2.

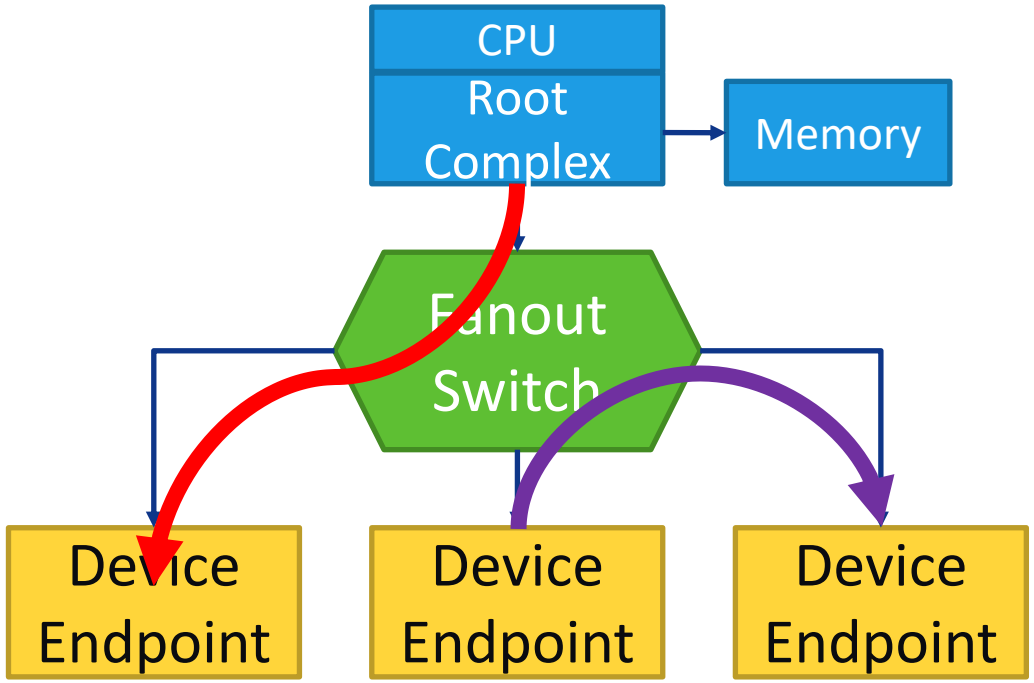


PCIe System Hierarchy Example



System Component: PCIe Fanout Switches

- **PCIe switches have:**
  - One upstream port that connects in the direction of the host
  - 1+ downstream ports that connect to the devices or additional switches
  - Switching logic that routes the data packets between the ports
    - Peer-to-Peer

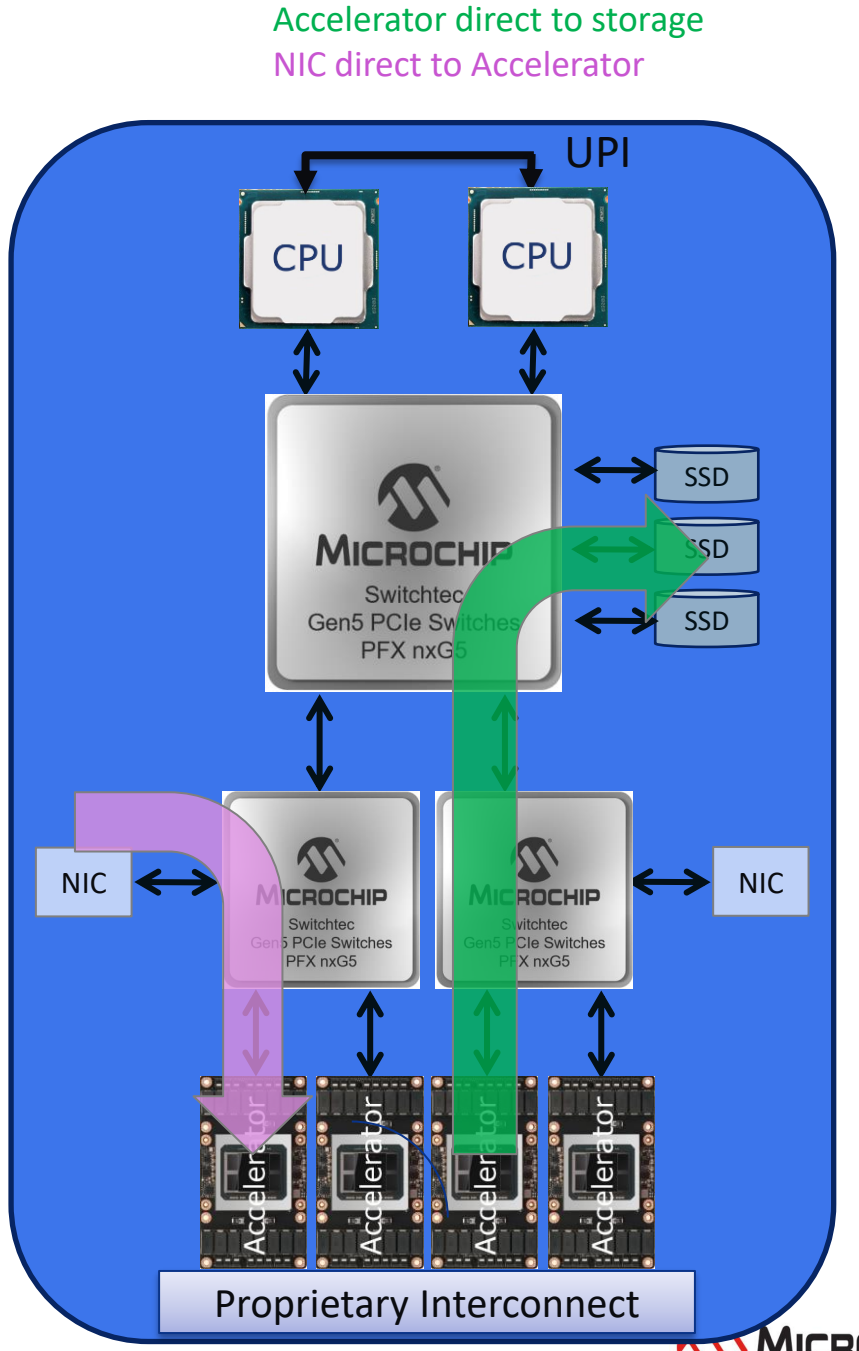


Peer to Peer Applications

- **Accelerator direct to storage use model**
  - NVMe SSDs
  - NVRAM Drive
  - JBOF
  - NVMe RAID Controller
  - SAS Controller

- **Network (Infiniband, Ethernet, etc) direct to Accelerator is typically close to the Accelerators**

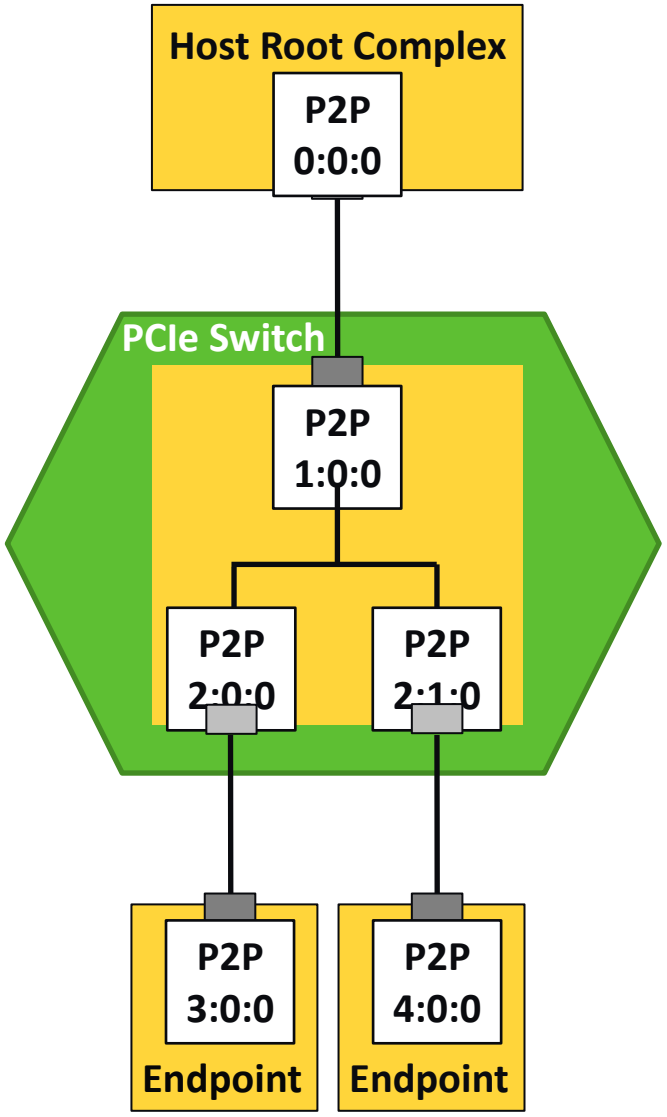
- **Switch DMA could be used for:**
  - Host to Host communications
  - Deposit to NVRAM Drive
  - Deposit to NVMe Controller Memory Buffer (CMB)
  - Accelerator to Accelerator



PCIe Switch with Single-Root

PCIe Enumeration

- **PCIe fanout switches are a network of bridges**
- **Enumeration: FW/SW must go out and discover what devices and functions exist in their system.**
  - **depth-first search** algorithm to discover all BDFs.
  - (Bus: Dev. Funcs) in the system **starting with 0:0.0** and searching from there.



PCIe BDF ID

- **PCIe enumeration/hierarchy limits**
  - **256** Buses per Root Complex
  - **32** Devices per Bus
  - **8** Functions per Device

Root complex assigns and programs each device with a **Bus** # and **Device** # in its Configuration space.

“BDF” ID

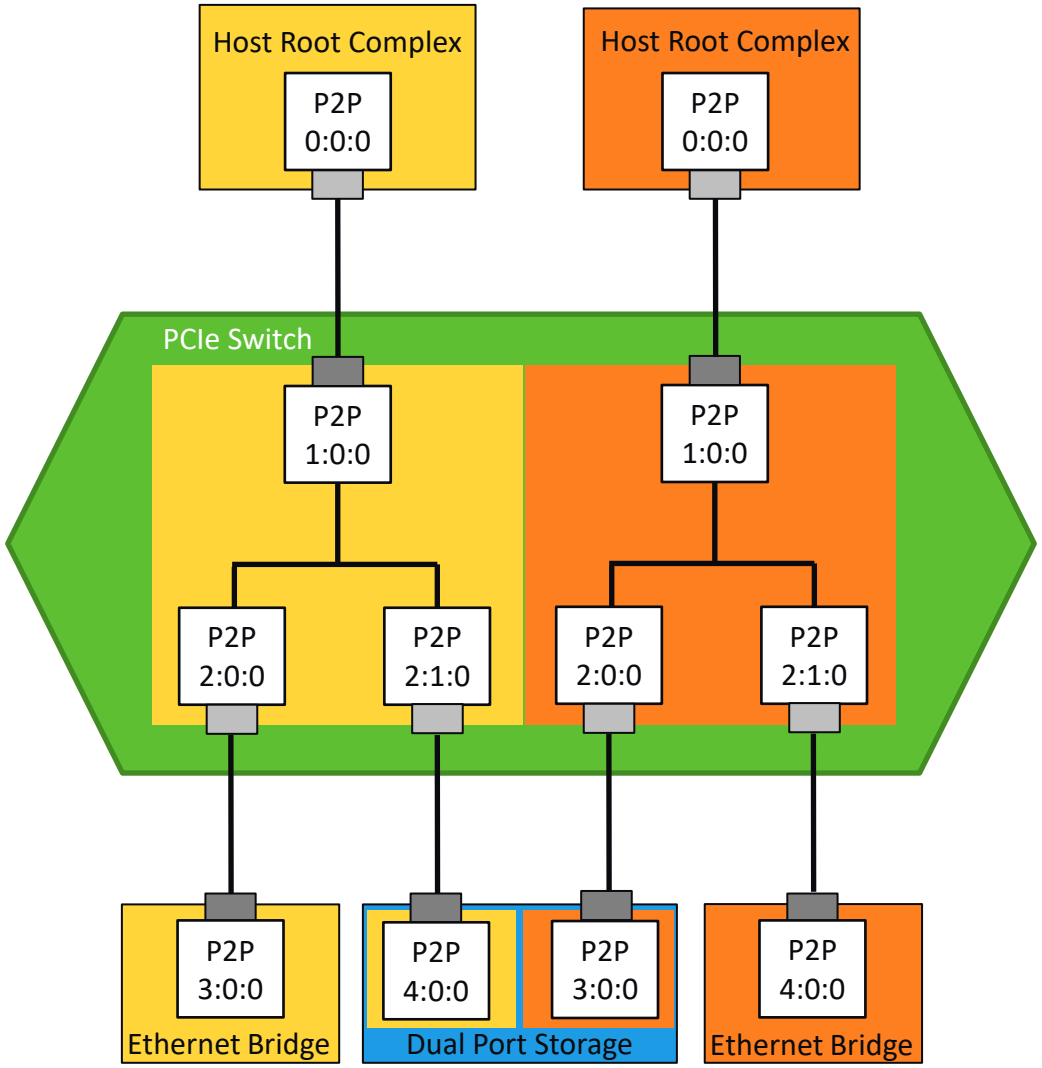
- After enumeration, all PCIe functions in the hierarchy **have a unique “BDF” ID** – you can recognize these in Linux ***lspci*** output:

```
BB:DD.F <Device_class>: <Vendor_name> <Function_name>
```

PCIe Switch with Multi-Root

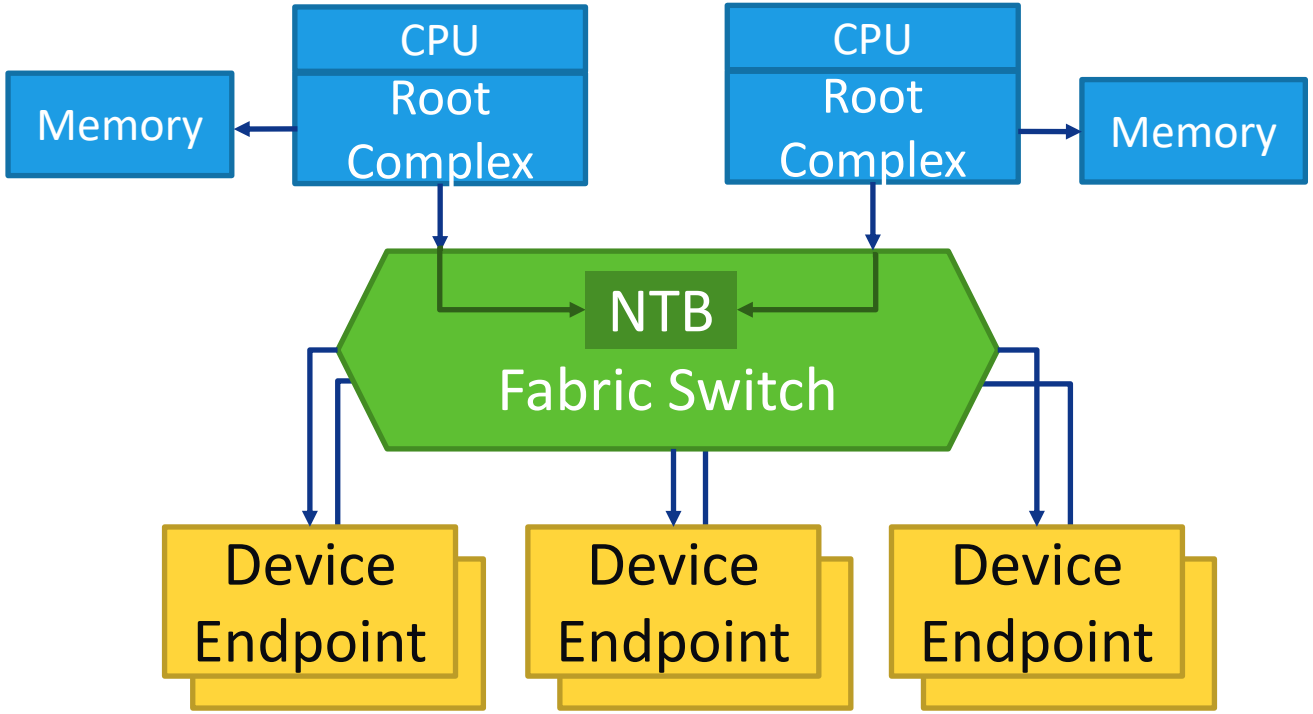
PCIe® Virtual Switch Partitions (VSP)

- Divide PCIe switch into Virtual Switch Partitions.
- Each partition:
  - Has its own root complex
  - Is a closed system with individual enumeration and partition reset schemes
- Provides isolated memory address islands
- Dual port storage devices give transparent access to two hosts



System Component: PCIe Fanout NTB Switches

- **What about Multi-Root applications with switches?**
  - Switches can also allow host-to-host communication & device sharing between RCs.
  - This is enabled via a feature called **NTB**: **N**on-**T**ransparent **B**ridging.
  - **Requires NTB support in switch, NTB memory window configuration, and NTB-specific software on participating components to function**



Not in PCIe Spec

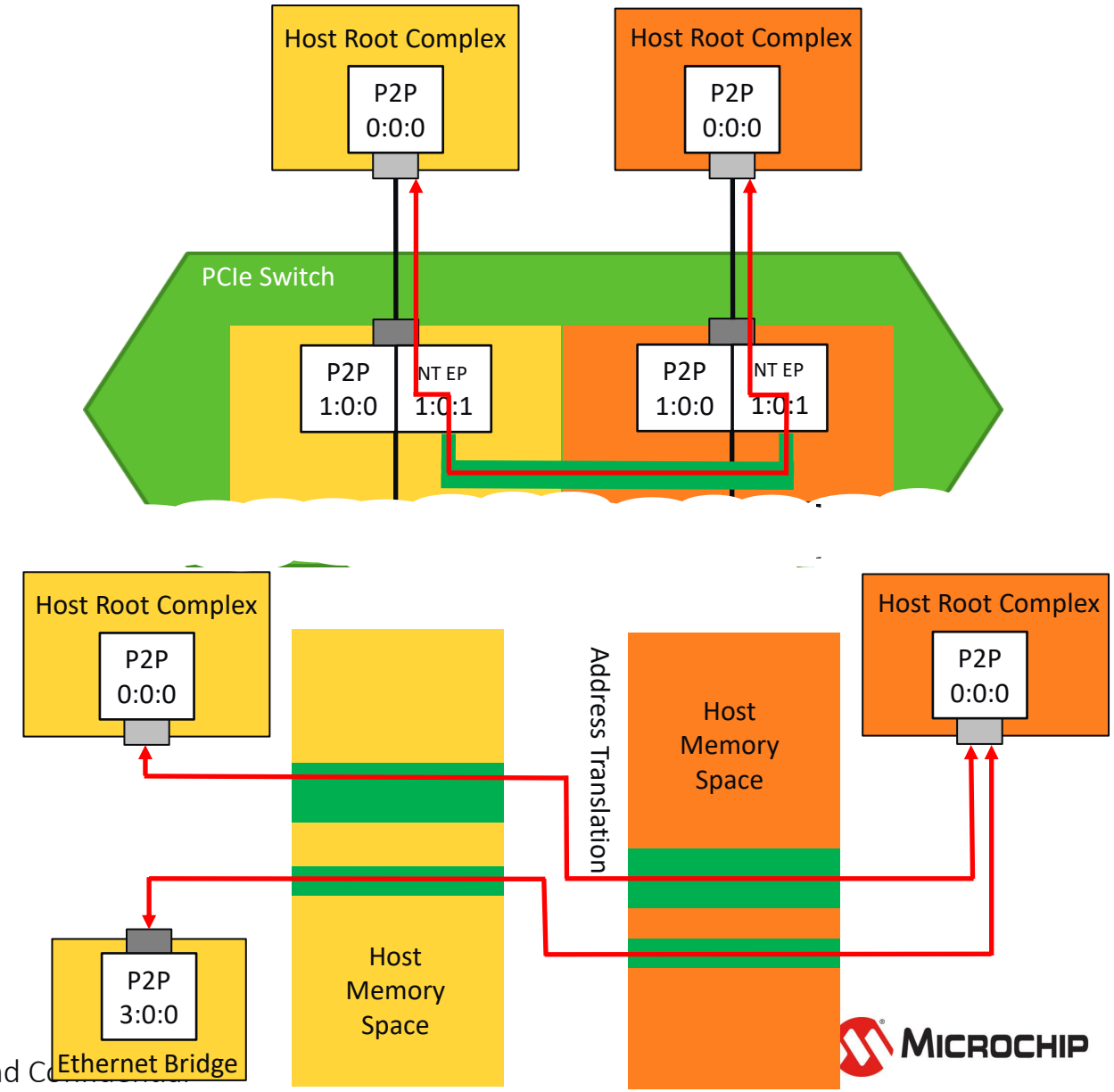
PCIe Switches with Non Transparent Bridging

- **“Transparent” – Root complex enumerates and can access any PCIe components in the hierarchy beneath.**

- **“Non-transparent” – The PCIe components a given root complex wants to access, exist in a hierarchy under a different root complex.**
  - In NTB-enabled switches, we call the hierarchies as “partitions” and configure rules for how RC in one partition can access RCs/devices in other partitions.
  - This involves hand-crafted memory address translation rules in the NTB hardware of the switch.

PCIe® Non-Transparent Bridging (NTB)

- Bridges PCIe domains
- NT End Point (NT EP) function is enumerated in each NT enabled partition
- Utilizes Non – Transparent Endpoints to facilitate communication between switch partitions
- Addresses and IDs mapped across partitions
- Host-to-host communication
- Not defined in PCIe spec



Agenda

- PCIe Applications
- What is PCIe?
- **Microchip PCIe Solutions**
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PCIe Roadmap Positioning

PERFOMANCE
Lanes / Ports & Features

Peripheral Expansion Bridging, SBC, IPC

Bridgeport

- 4-6 Lane PCIe Gen3
- USB2/USB3, GPIO
- 2.5G Ethernet
- PCIe passthrough

Aberdeen

- PCIe Gen 1
- Single Port Bridge
- 1Gbps Ethernet

High Performance Edge, Embedded Compute switching

Stamford

- **16 Lane PCIe Gen4**
- 5-7 Port Switch
- Cross-Link port
- 4x NTB (hosts)
- DMA

Trident / Harpoon

- PCIe Gen 4 / 5
- **28 to 100 lanes**
- Up to 52 ports
- Up to 48 NTB (hosts)
- Adv. SW Fabric

Cloud Computing, Data Center, Compute,

Seamless scalability

BANDWIDTH / SPEED

MICROCHIP

PCIe Leadership & Investment

Industry's First Automotive-Qualified Gen 4 PCIe® Switches Enable Autonomous Driving Ecosystem

Switchtec™ Gen 4 PCIe switches provide low-latency, low-power and high-performance connectivity for ADAS designs.

Facebook Twitter LinkedIn Email Share

CHANDLER, Ariz., February 21, 2022 — High-speed, low-latency connectivity solutions for distributed, heterogenous compute systems are a fundamental element in next-generation autonomous driving applications. Microchip Technology Inc. **(Nasdaq: MCHP)** is announcing the market's first **Gen 4 automotive-qualified PCIe® switches.** These Switchtec™ PFX, PSX and PAX switch solutions provide cutting-edge compute interconnect capabilities for Advanced Driver Assistance Systems (ADAS).

"Our automotive-qualified portfolio of Switchtec Gen 4 switches provides the lowest latency and high bandwidth required to link the CPU and accelerator building blocks used in ADAS applications," says Krishna Mallampati, associate director of marketing and applications for Microchip's data center solutions business unit. "We are delighted to see the culmination of several years of collaboration with key technology partners and to bring these solutions to market."

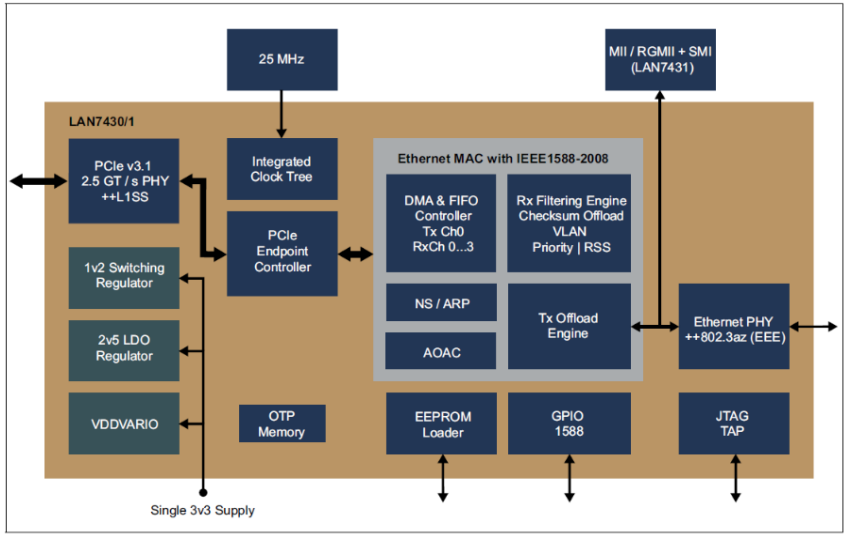
- 1st Automotive PCIe switch to market
- 1st Automotive Ethernet to market
- 1st Automotive USB to market

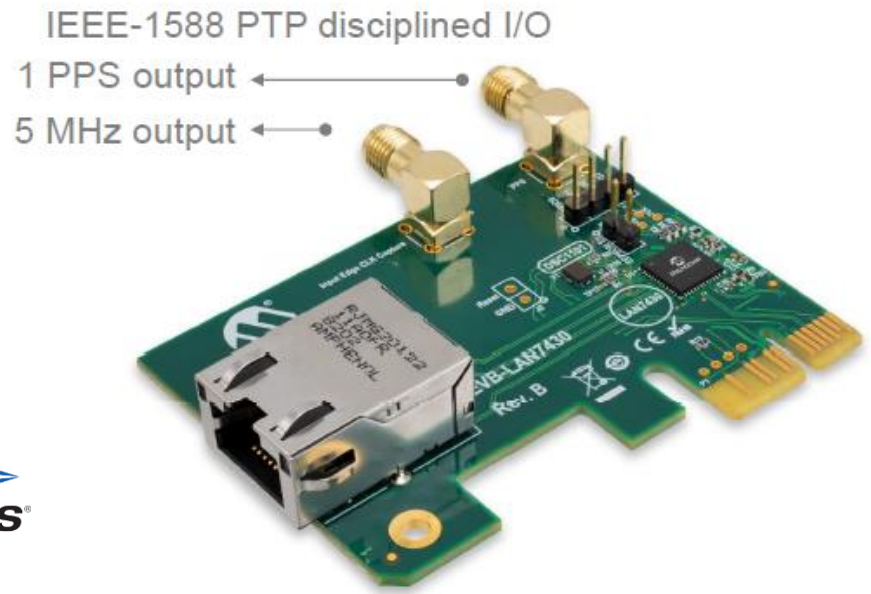
MICROCHIP

LAN7431 PCIe Gen3 to Gigabit Ethernet Bridge

Features

- Single-chip, PCIe 3.1 @ 2.5GT/s to 10/100/1000 Ethernet controller
- PCIe Low Power Sub States LPSS L1.1 (snooze) & L1.2 (off)
- IEEE 1588-2008 Programmable Time Compare output (Eg: 1PPS)
- IEEE 1588-2008 Capture input
- JTAG via integrated 1149.1 compliant TAP
- Accessible GPIO
- Linux, Android, MSFT Windows and QNX driver packages
- Interface to external PHY via RGMII or MII
- AEC-Q100 Grade 2 (-40 to +105C) support
- 72-pin SQFN (9 x 9 mm, 0.5mm pitch)





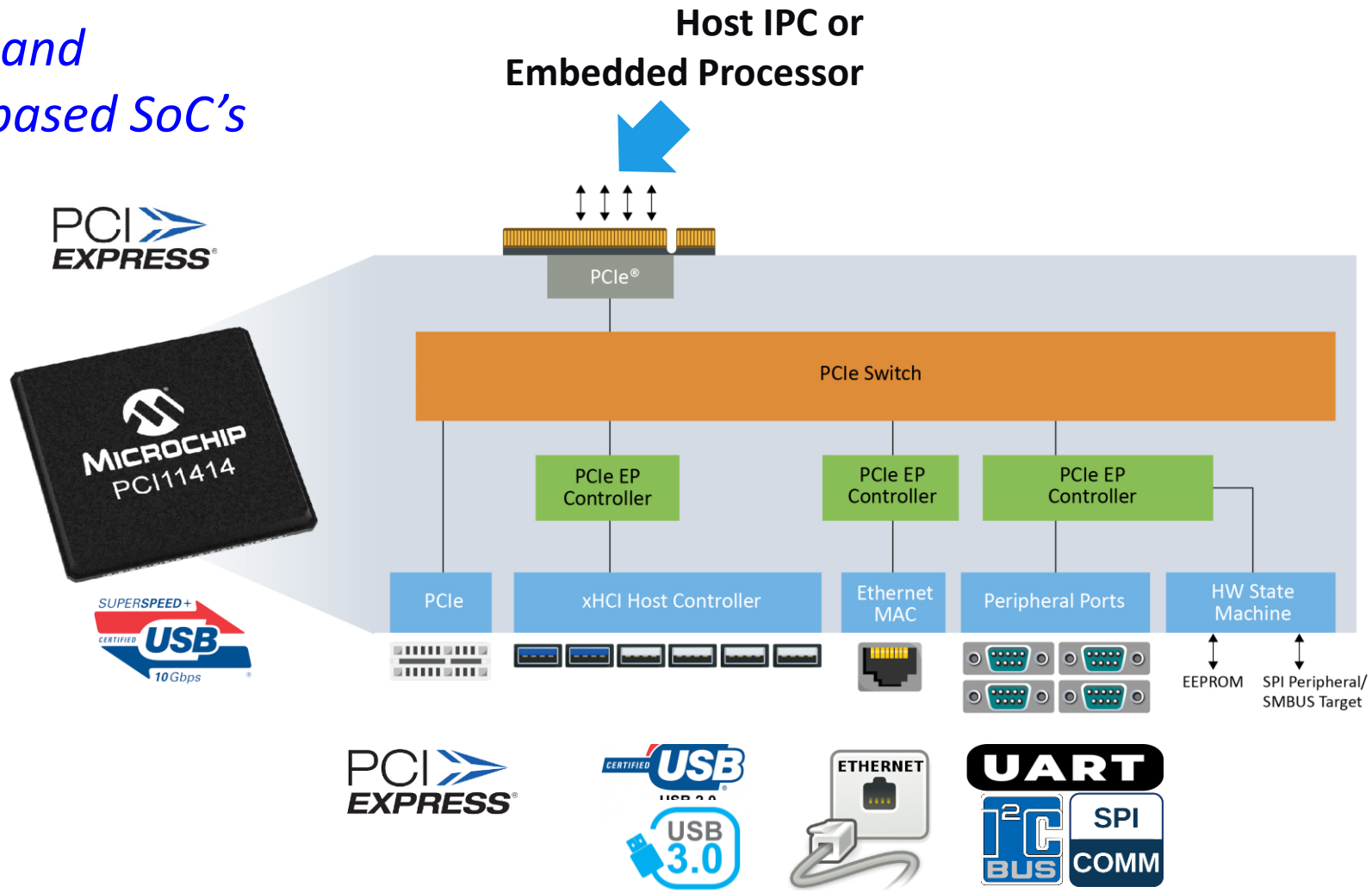
PCI EXPRESS

Bridgeport PCIe Expander Device

Enables embedded connectivity and peripheral abstraction for PCIe-based SoC's

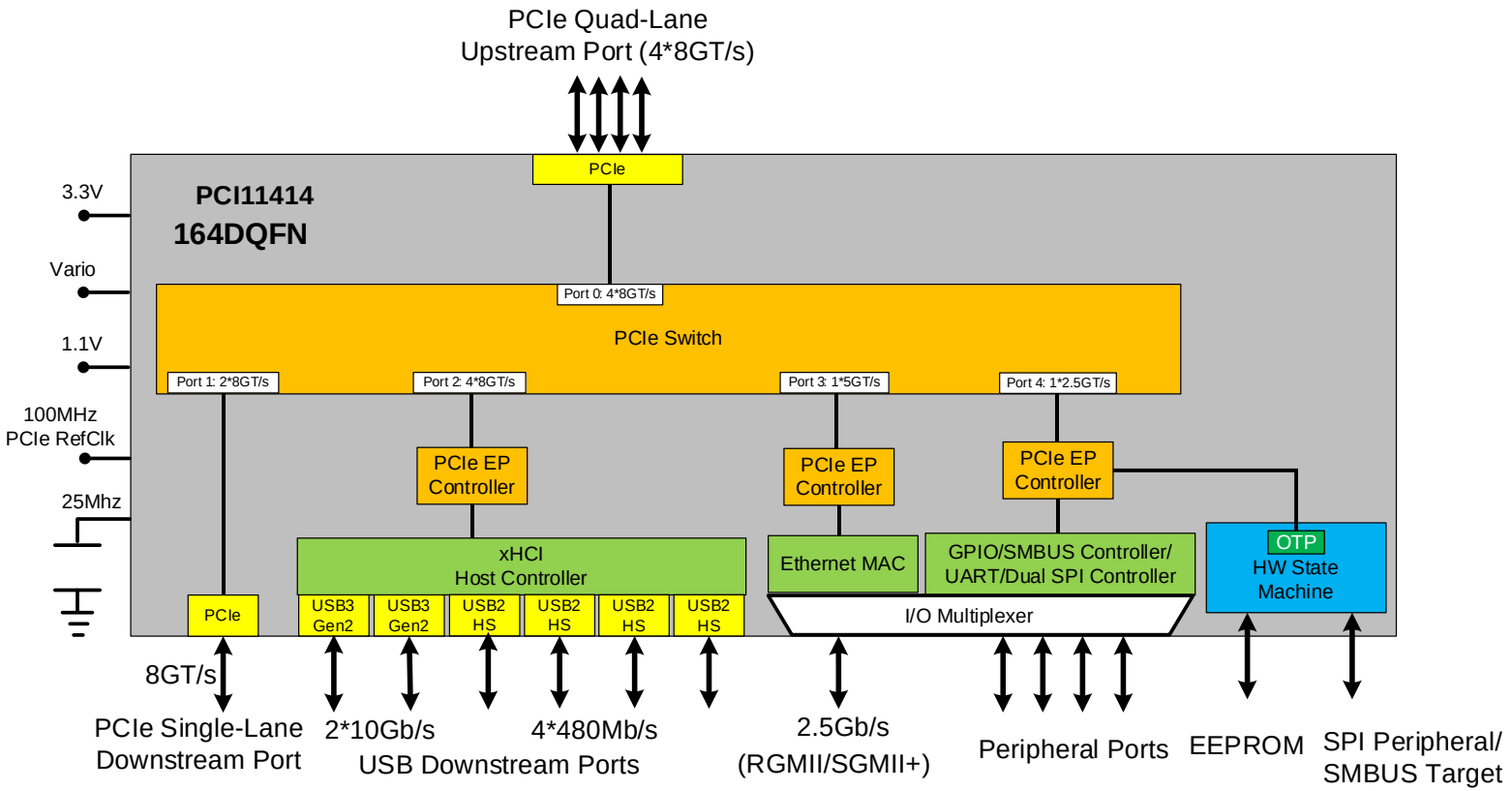
Features

- PCIe link to common processor platforms
- Providing standard interfaces
  - PCIe Fanout switching
  - Ethernet networking – 2.5G, 1G
  - USB HOST supporting USB3.2Gen2 & USB2
  - UARTS, GPIO, SPI
  - SD Express



Bridgeport Product Family

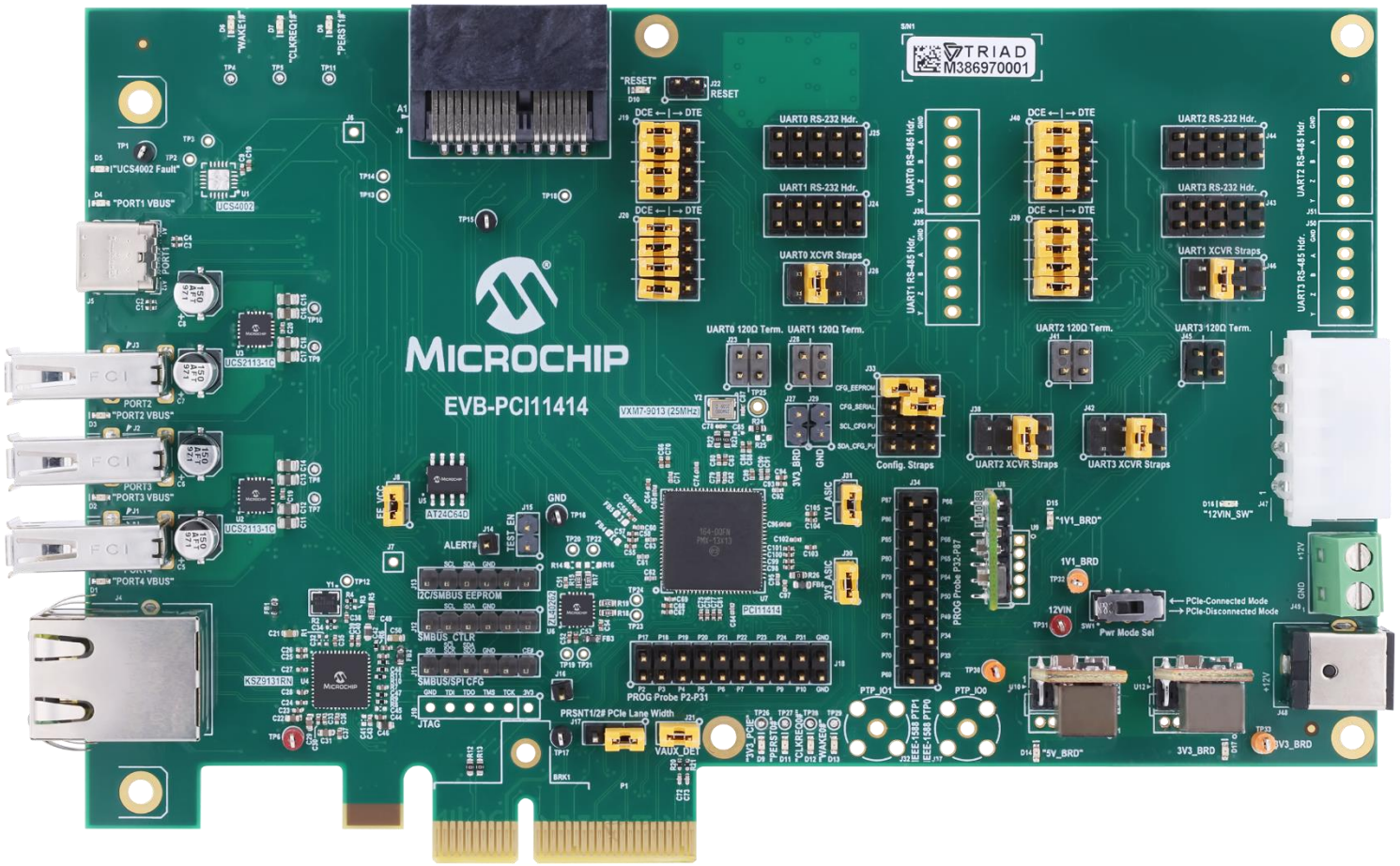
Bridgeport CPN Feature Table	Device	Feature							
		PCIe			USB Host		Networking	UARTs	GPIO
		Upstream	Downstream		3.2Gen2	LS/FS/HS			
		Port 0	Port 1	Port 2	Port 0, 1	Port 2, 3	MAC		
PCIe Switch – USB Host, Networking, Quad UART, GPIO	**PCI11414**	●	●		●	●	●	●	●
PCIe Switch – 1 Downstream Port, USB Host	**PCI11400**	●	●		●	●		○	●
PCIe Switch – 1 Downstream Port, Networking	**PCI11010**	●	●				●	○	●
PCIe Switch – 1 Downstream Port, M.2 Buildout	**PCI11101**	●	●		●			●	●
PCIe Switch – 2 Downstream Port	**PCI12000**	●	●	●				○	●



- **Industry Standard Packaging**
  AEC-Q100 & Automotive Grade 2 (+105degC)
  Commercial & Industrial (+85degC)
  72QFN / 100QFN / 132DRQFN / 164DRQFN
- **PCIe 3.1 (8GT/s)**
  Single/Dual/Quad lanes
  Low Power Sub States
  SD Express
- **Networking**
  2.5G / 1G / 100Mb / 10Mb
- **USB Host Controller**
  Type C support
  10Gb Single Lane XHCI Host
- **Serial interfaces & GPIO**
  RS232/RS485 (Auto direction), SPI, I2C

Evaluation Platform

EVB-PCI11414



- **Industry Standard Packaging**
  - Commercial & Industrial (+85degC)
  - 164DRQFN 0.5mm Pitch , 13mm x 13mm
- **PCIe 3.1 (8GT/s)**
  - Single/Dual/Quad lanes upstream
  - Singe lane downstream
- **USB 3.2Gen2 10G XHCI Host Controller**
  - USB Type C & 3x USB type A
- **Ethernet 2.5G MAC**
  - Shown here with KSZ9131 GigE PHY
  - MAC PTP GPIO via SMA connectors
- **Serial interfaces & GPIO**
  - Quad RS232/RS485 (Auto direction)
  - Dual SPI, I2C, GPIO
  - 10bT1S /10SPE / IEEE802.3cg via SPI

MICROCHIP

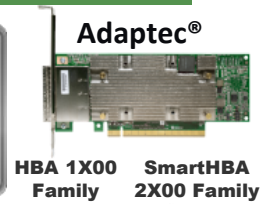
Microchip Data Center Solutions Segments

Storage & Compute Infrastructure

Server OxM & Hyperscale

Storage System OxM

IOCs & HBAs



HBA 1X00 Family | SmartHBA 2X00 Family

ROCs & RAID Adapters

SmartRAID 3X00 Family

SAS Expanders

SAS Expander Cards

CXL™/PCIe® Switch & Fabrics

+ Automotive variants

Tachyon IO Controllers

Custom Adapters

Hyperscale, SSDs, Storage & Server OxM

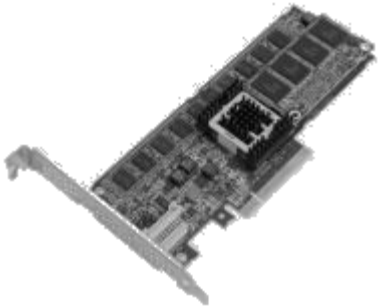
Storage End Point Solutions

Flashtec® SSD Controllers

Performance

Mainstream

Flashtec® NVRAM Drives



Server OxM, Hyperscale, HPC

Memory Infrastructure

Smart Memory Controllers

OMI

Expansion

CXL

Expansion

Pooling

MICROCHIP

Microchip Embedded PCIe Switch Roadmap

2016 ~ 2018	2024/1	2024/9

Production

Saratoga Gen3 PCIe Switches

- Scalable up to 48 ports, 48 NTBs, 24 virtual switches
- Flexible Bifurcation x2, x4, x8, x16
- Error Containment
- Reliability / Quality – 5th generation SERDES
- Advanced Diagnostics and Debug
- 96/48, 80/40, 64/32, 48/24, 32/16, 24/12 lane/port variants
- Architectural variants: PFX, PSX, PFX-L and PFX-I
- **Non-automotive derivatives only**

Trident Gen4 PCIe Switches

- Superset of Gen3 PFX features (no port mirror)
- 110ns pin-to-pin latency
- Error Containment (Hot- and Surprise-Plug)
- Advanced Diagnostics and Debug
- End-to-end Data Integrity
- NVMe-MI support
- High-performance Cut Through DMA
- Secure boot
- 100/52, 84/44, 68/36, 52/28, 36/20, 28/16 lane/port variants
- Architectural variants: PFX, PSX, and PAX
- **AEC Q-100 qualified derivatives**

Production

Bridgeport Gen3 PCIe Bridges

- Flexible family of devices
- USB Host Controller Endpoint
- Up to six USB2/USB3 ports
- 2.5G Ethernet Endpoint
- PCIe pass-through to 1 or 2 ports
- **AEC Q-100 qualified derivatives**

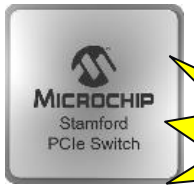
NEW

Production

Harpoon Gen5 PCIe Switches

- PFX:
  - Superset of Gen4 PFX features
  - Enhanced Diagnostics and Debug
  - Architectural variants: PFX, PSX and PAX
- PSX:
  - SDK enables customization
- PAX
  - PCIe and GPGPU Fabric support
  - Multi-host SR-IOV Sharing support
  - PAX SDK enables customization

Production Commercial: Q1 2024
Production AEC Q-100: Q2 2025



Coming

Development

Stamford Gen4 PCIe Switch

- Gen4 16 GT/s
- 12 to 32 lanes
- NTB support
- Compatible with Trident PFX feature set
- **Automotive Functional Safety, ASIL-B**
- **AEC Q-100 qualified derivatives**

Sampling Q3 2024

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Switchtec PCIe Gen 3 Switch Product Family

PFX

High Reliability and Flexible PCIe Fanout Switch

- Scalable up to 48 ports, 48 NTBs, 24 virtual switches
- Flexible Bifurcation (x2, x4, x8, x16)
- Error Containment (Hot- and Surprise-Plug)
- Reliability / Quality – 5th generation SERDES
- Advanced Diagnostics and Debug
- Low Power
- End-to-end Data Integrity
- 96-, 80-, 64-, 48-, 32-, 24-lane variants

PSX

Programmable PCIe Storage Switch

- Superset of PFX, pin-compatible
- SoC Architecture / SDK enables customization and differentiated solutions (e.g. internal root complex, error containment)
- Enterprise- class, field-proven, enclosure mgmt processor (SDK)
- 96-, 80-, 64-, 48-, 32-, 24-lane variants

PAX

PCIe Advanced Fabric Switch

- Pin-compatible to PSX and PFX
- PCIe Fabric support
- Multi-host I/O Sharing support
- 96-, 80-, 64-, 48-, 32-, 24-lane variants

Pin-compatible across 96-, 80-, 64-lane, and across 48- 32-, and 24-lane switches

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Switchtec PCIe Gen 3 Switch Product Family

PFX-L

PFX-L Fanout-Lite PCIe Switch

- Subset of PFX features, footprint-compatible
- Up to 24 ports, 2 NTBs, 6 virtual switches
- x4, x8, x16 port bifurcation
- Advanced diagnostics and debug w/ chiplink gen/analyzer
- End-to-end data integrity
- 96-, 80-, 64-, 48-, 32-, 24-lane variants

PFX-I

High Reliability and Flexible PCIe Extended Temperature Industrial Fanout Switch

- Scalable up to 48 ports, 48 NTBs, 24 virtual switches
- Flexible Bifurcation (x2, x4, x8, x16)
- Error Containment (Hot- and Surprise-Plug)
- Reliability / Quality – 5th generation SERDES
- Advanced Diagnostics and Debug
- Low Power
- End-to-end Data Integrity
- 96-, 80-, 64-, 48-, 32-, 24-lane variants
- PFX-I is pin compatible with the same** feature set as PFX, and supports extended industrial temperature ranges -40C (Ta) to +105C (Tj)
- **PFX-I doesn't support Adaptive Voltage Scaling (AVS). AVS is a way to reduce power consumption by lowering the voltage supply

Pin-compatible across 96-, 80-, 64-lane, and across 48- 32-, and 24-lane switches

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Trident PCIe Gen4 Switch Product Family

PFX

PFX Gen4 Fanout PCIe Switch

- Superset of Gen3 PFX features (except no Port Mirroring)
- PCIe Gen4 Switch Scalable up to 52 ports, 48 NTBs, 26 virtual switches
- **110ns pin-to-pin latency**
- Error Containment (Hot- and Surprise-Plug)
- Advanced Diagnostics and Debug
- End-to-end Data Integrity
- **High-performance CutThrough DMA**
- **Secure boot**

PSX

PSX Gen4 Programmable PCIe Switch

- Superset of Gen4 PFX
- SDK enables customization and differentiated solutions
- Enterprise- class, field-proven, enclosure mgmt processor
- NVMe-MI support
- High-performance CutThrough DMA
- Secure boot

PAX

PAX Gen4 Advanced Fabric PCIe Switch

- PCIe and GPGPU Fabric support
- Multi-host SR-IOV Sharing support
- High-performance CutThrough DMA and Fabric DMA
- PAX SDK enables customization and differentiated solutions
- Secure boot

Pin-compatible across 100-, 84-, 68-lane, across 52- 36-, and 28-lane switches, and across product families PFX, PSX and PAX

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Switchtec™ Automotive Qualified Switch Portfolio

PFX-A

- Scalable up to 52 lanes, 28 ports, 26 NTBs
- 110 ns pin-to-pin latency
- Error Containment (Hot- and Surprise-Plug)
- End-to-end Data Integrity
- Secure Boot
- 29 mm × 29 mm

Part Number	Description
PM43028B1-F3EI	PFX-A 28xG4, 28-lane Gen 4 Fanout Automotive PCIe® Switch
PM43036B1-F3EI	PFX-A 36xG4, 36-lane Gen 4 Fanout Automotive PCIe Switch
PM43052B1-F3EI	PFX-A 52xG4, 52-lane Gen 4 Fanout Automotive PCIe Switch

PSX-A

Includes PFX attributes and,

- SDK customizable / differentiated solutions
- Enclosure management processor
- NVMe-MI support
- High-performance Cut-Through DMA
- 29 mm × 29 mm

Part Number	Description
PM44028B1-F3EI	PSX-A 28xG4, 28-lane Gen 4 Programmable Automotive PCIe® Switch
PM44036B1-F3EI	PSX-A 36xG4, 36-lane Gen 4 Programmable Automotive PCIe Switch
PM44052B1-F3EI	PSX-A 52xG4, 52-lane Gen 4 Programmable Automotive PCIe Switch

PAX-A

Includes PFX, PSX attributes and

- PCIe® and GPGPU Fabric support
- Multi-host Sharing of SR-IOV Endpoint
- 29 mm × 29 mm

Part Number	Description
PM45028B1-F3EI	PAX-A 28xG4, 28-lane Gen 4 Advanced Fabric Automotive PCIe® Switch
PM45036B1-F3EI	PAX-A 36xG4, 36-lane Gen 4 Advanced Fabric Automotive PCIe Switch
PM45052B1-F3EI	PAX-A 52xG4, 52-lane Gen 4 Advanced Fabric Automotive PCIe Switch

PFX/PSX/PAX Gen5 PCIe Switches

High-Reliability, Low Latency PCIe Switches

Key Features

- **PCIe Gen5 fanout switches**
  - 100-, 84-, 68-lane PCIe switches, 40x40mm pkg, 1mm ball pitch
  - 52-, 36-, and 28-lane PCIe switches, 31x31mm pkg, 1mm ball pitch
  - Flexible port bifurcation: x1*, x2, x4, x8, x16; Upstream/Downstream/NTB
- **Clocking**
  - SRIS, SRNS, Common clocking with SSC, SRIS clocking modes, SSC Clock Skewing
  - Up to 6 Host REFCLK inputs, 7 REFCLK outputs
- **Error Containment, DPC, CTS, Hot-Plug, Surprise Plug Support**
- **PCIe Multicast, multiple overlays per port**
- **Diagnostics/Debug – Physical to TLP layer**
- **Secure boot image authentication**
- **Peripheral Interfaces**
  - TWI, SPI, UARTs, SGPIO, GPIO
  - 100M/**GE** (on 100-, 84-lane, 68-lane devices only)
- **High Performance CutThrough DMA engines**
  - 120 GB/sec for 4KB transfer size and 175 GB/sec for 1MB transfer size, 64 DMA channels

- PSX: customer-programmable
  - SoC with Dual-Core 1GHz MIPS
  - SDK, programmable PCIe Control Plane and encl. mgmt
- PAX: advanced fabric PCIe switch
  - Multi-host SR-IOV sharing
  - PCIe Fabric Support
  - Fabric DMA
- **Additional new features for Gen5**
  - **Enhanced on-chip PCIe analyzer for debugging TLPs per port and Ordered Sets per lane**
  - **Enhanced LTSSM monitor for advanced triggering**
  - **Automatic port bifurcation (Rev B)**

* x1 natively on four lanes

ChipLink on Harpoon Gen 5

☑ Ease of Configuration

- Rapid device setup with presets for common use cases
- GUI-based device configuration and topology viewer

☑ Functional Debug

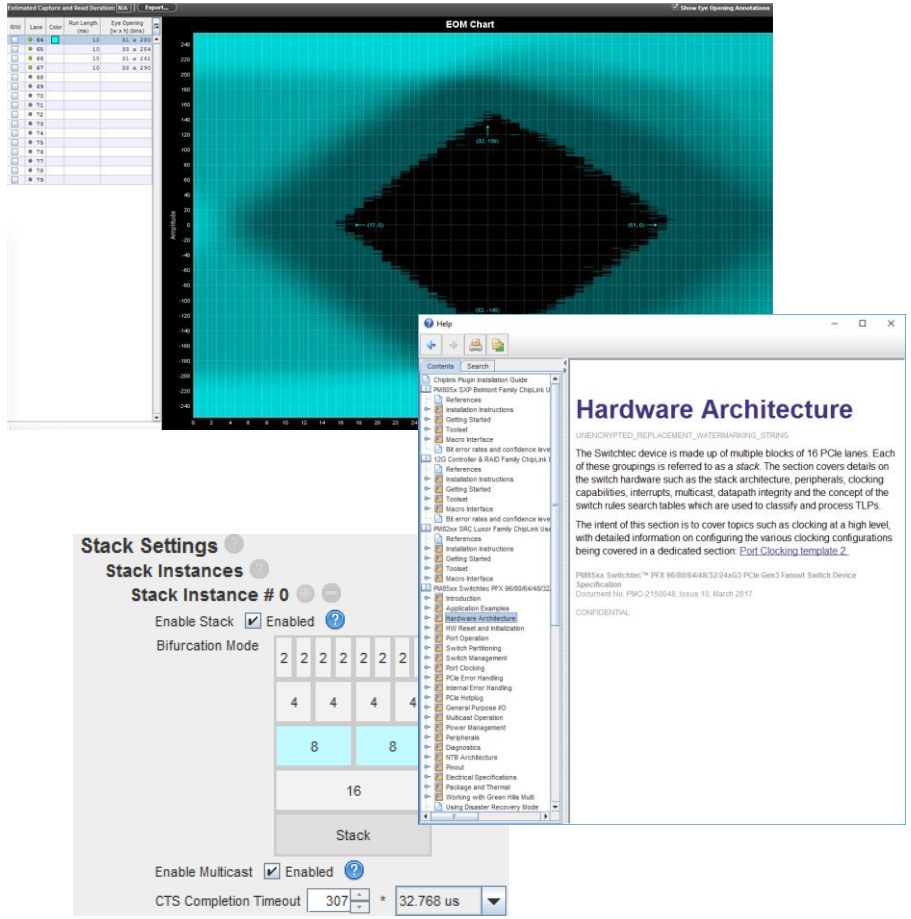
- Pattern generators and analyzers
- New OS Analyzer
- New TLP Analyzer: improved triggers and TLP capture
- New LTSSM Monitor: improved trigger flexibility and entry tables
- Performance and Error Counters

☑ Signal Integrity Analysis

- Eye Capture, Signal Integrity Analyzer
- One-click forensic captures

☑ Complete Access to Device Documentation

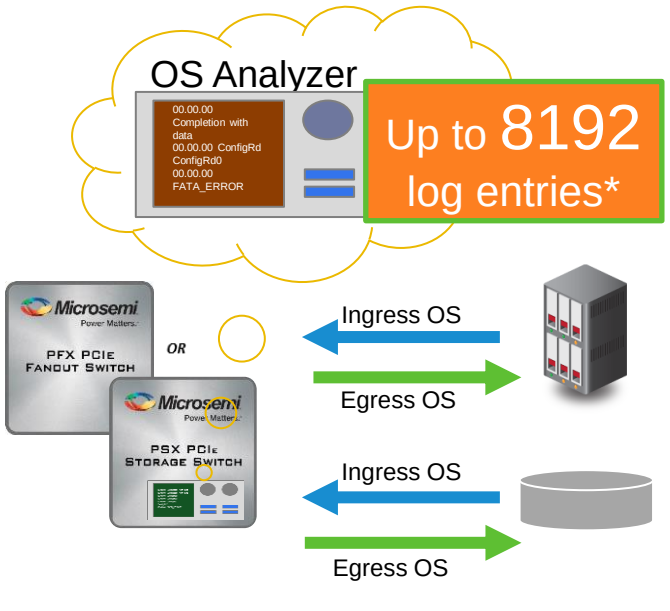
- Context-sensitive embedded documentation

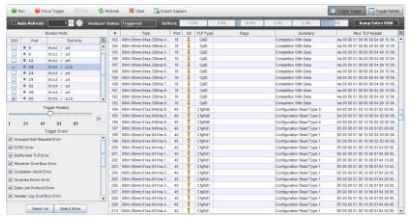


Dramatically reduce bring-up time, and improve development efficiency

OS Analyzer (NEW)

- **Ordered Set Analyzer**
  - Helps debug *link training* issues PER LANE where inserting a PCIe analyzer changes the channel and ultimately may mask the issue
  - Flexible filtering eliminates “analyzer garbage” and isolates transactions of interest
  - Flexible cross triggering enables *next level* debug capability





Types:
TS1, TS2, FTS, CTRL, SKP

Patterns:
Any 128b Value or Mask

Filters:
TS1, TS2, FTS, CTRL, SKP, EIEOS, EIOS, Error OS

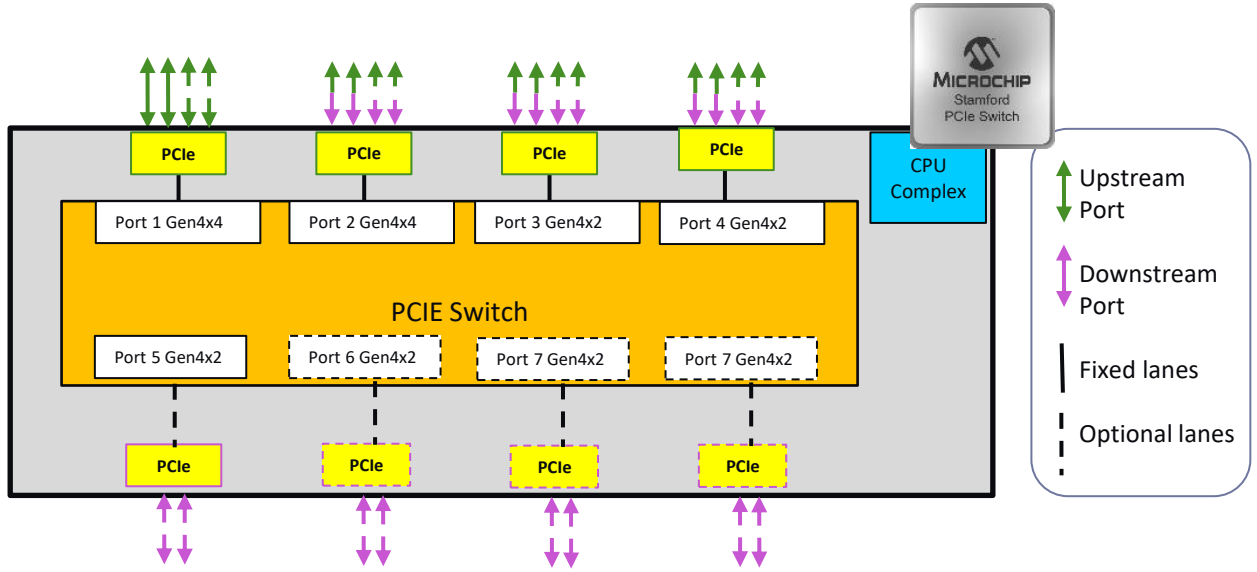
Non-Repeating Pattern Filter:
TS1, TS2, FTS

Triggers:
Tx can trigger Rx, Rx can trigger Tx, from same lane, from different lane, from another block (TLP Analyzer, LTMON, ARAM, GPIO)

* One lane in a stack, single direction (256 entries for 16 lanes in both directions)

Stamford PCIE Gen4 Switch
with Non-Transparent Bridging

- **16-Lane PCIE Gen4 Switch**
  - Bifurcation x2, x4
  - Up to 8 ports, pre-configured per table
- NTB Functionality on all ports
- Cross-link capability for 2x switches
- Fast data transfers: Peer-Peer / DMA
- Secure Boot & Secure Firmware Update
- ChipLink diagnostic and debug tool suite
- Commercial and Industrial temp
- Automotive Grade 2 (-40C to +105C)
- Functional Safety, ASIL-B Compliant
- Package 16mm x 16mm 353-FCBGA
- Pre-silicon emulation using Trident Evaluation Kit
- Samples September 2024



Stamford configuration options

Part number	UFP	DFP	NTBs	Lanes	Ports
PCI1003 8-port PCIe Gen4x16 Switch	2x4 + 2x2	2x2	4	16	6
PCI1004 4-port PCIe Gen4x16 Switch	4x4	0	4	16	4
PCI1001 4-port PCIe Gen4x16 Fanout Switch	1x4	3x4	0	16	4
PCI1005 7-port PCIe Gen4x16 Fanout Switch	1x4	6x2	0	16	7

Proven IP, low risk, faster time-to-market

Stamford and Trident Feature Comparison

	Stamford Automotive	Trident Automotive
PCIe Generation	Gen4	Gen4
# of Lane	16	28/36/52
# of Port	Up to 8	Up to 28
Multi-Host Support	up to 4 NTBs	up to 28 NTBs
Virtual Switch Partition	Up to 4	Up to 14
Dynamic Partitioning	No	Yes
SR-IOV	NVMe Supported	Supported with PAX
DMA Engine	Yes	Yes
Package	353-FCBGA 16x16mm	753-FCBGA 29x29mm
BGA ball pitch	0.8mm	1.0mm
Power Consumption	9W (typ) 16-lane	17W (typ) 28-lane
Temperature	Ta = -40 to 105degC	Tj = -40 to 105degC
Functional Safety	Compliant	No
Tool for Configuration	ChipLink	ChipLink
Schedule	Sample in September 2024	Production now

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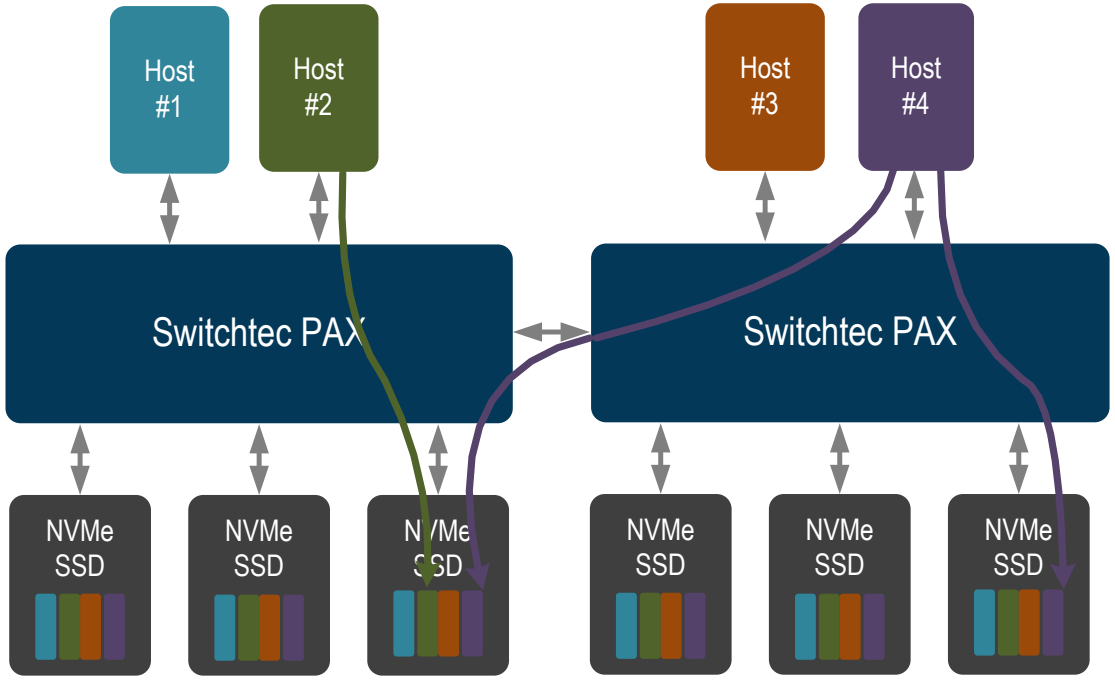
PAX for Multi-host IO Sharing

- **Key Features**
  - Multi-host sharing of SR-IOV and multifunction Endpoints (EPs)
  - Virtualize SR-IOV NVMe SSDs to appear to each host as dedicated NVMe Controllers with a single function
  - Allows host to run off-the-shelf NVMe drivers
  - Combined with Fabric to provide larger systems



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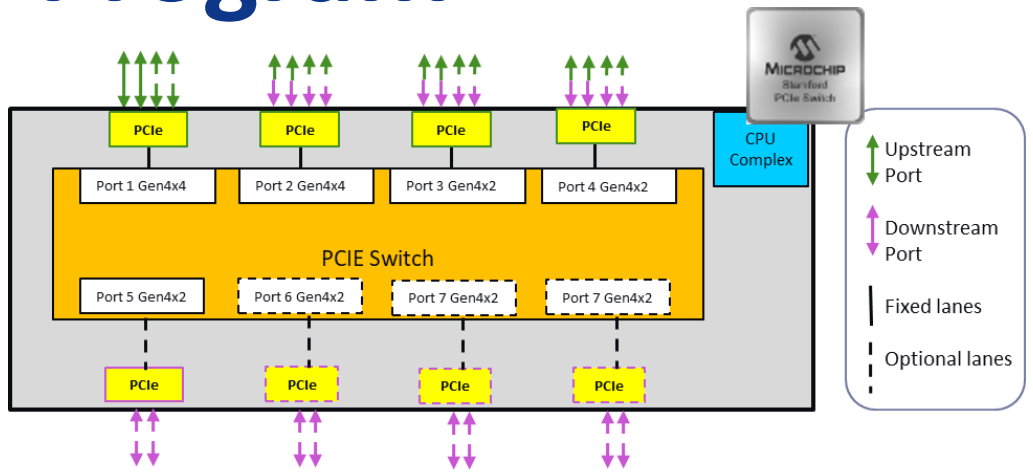
Stamford Enhanced Software Program

Datacenter Product Software
- **Firmware**
- **Host Applications & tools**
- **Secure boot**



Automotive Software Additions
- **Host Drivers & OS Support**
  - NTB Driver (2-NTB, 3-NTB and 4-NTB)
  - Management Endpoint Driver
  - DMA Endpoint Driver
  - Linux & **QNX** support
- **NVMe sharing software**
  - Virtual Root Complex
  - NVMe Virtualization Manager and EP Sharing
  - NVMe Inbox Driver
- **Enhanced security (ACS, CMA)**
  - Secure boot
  - Secure JTAG
  - Access Control Services
  - Component Measurement Authentication
- **SoC interop testing (Nvidia, Qualcomm, Renesas)**

ISO 26262

AUTOMOTIVE SPICE®

FUNCTIONAL SAFETY ASIL IEC61508-ISO26262

Expanded software support reduces development time

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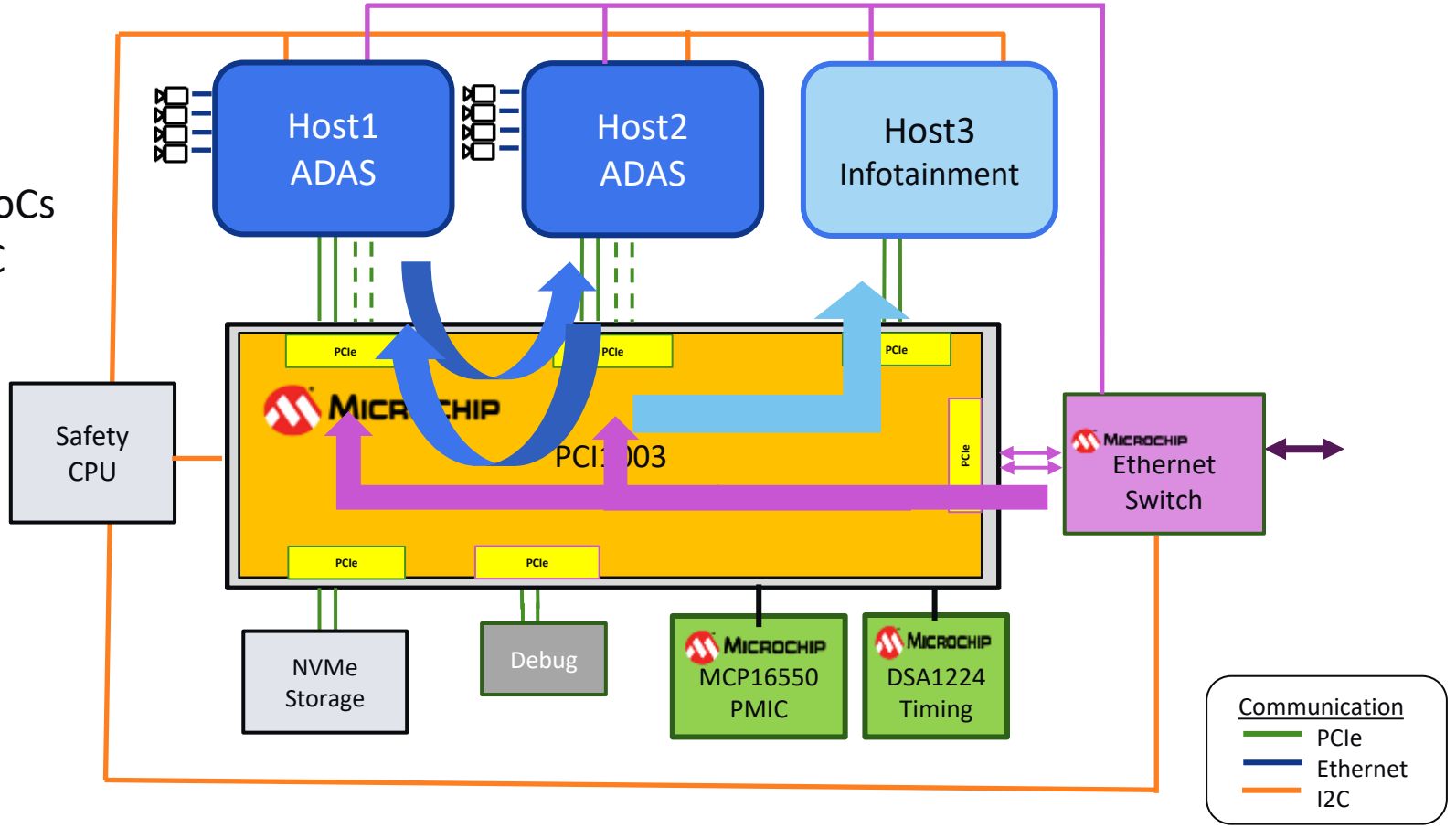
Embedded Use Case
Automotive L2+ thru L4 Driver Assist Platform

- **Data Processing**
  - Image recognition / Heuristics
  - Localization / perception
  - Workload sharing between ADAS SoCs
  - Data sharing with Infotainment SoC
  - Sensor Fusion
  - Driver Assist Policy

- **Safety**
  - Component health interrogation
  - System health policy
  - Redundant ADAS SoC



Microchip PCIe Switches

Hardware

- Built on 3rd Generation HW; deep expertise in signal integrity.
- Hardened IP, 8 yrs volume production at all top Cloud Datacenter, Server, and Storage providers.
- Worlds first auto grade PCIe switch announced March, 2022
- Latest generation optimized for Automotive
  - Enhanced test coverage
  - Flexible I/O blocks.
- Roadmap covering widest range of requirements

Software

- Industry leading feature set & flexibility
- Eight post-production FW releases: New features, bug fixes, maintenance
- Supported by Linux community, major OS and SoC vendors
- Six-year partnership with Dolphin Gen3-Gen4-Gen5 families

Support

- Dedicated local technical support
- Systems and device expertise
- SoC vendor reference designs. Proven interoperability with Qualcomm, Nvidia
- Ecosystem incl SoC, Storage, SW, & connector vendors
- Comprehensive ChipLink tool suite

Reliable Supplier

- Expanding investment in PCIe products for Automotive.
- Commitment to ISO26262
- Microchip NO EOL Policy for Long Term Automotive Support
- Top 10 WW Automotive Semiconductor Supplier

Microchip removes risks of first-generation products for safety critical applications

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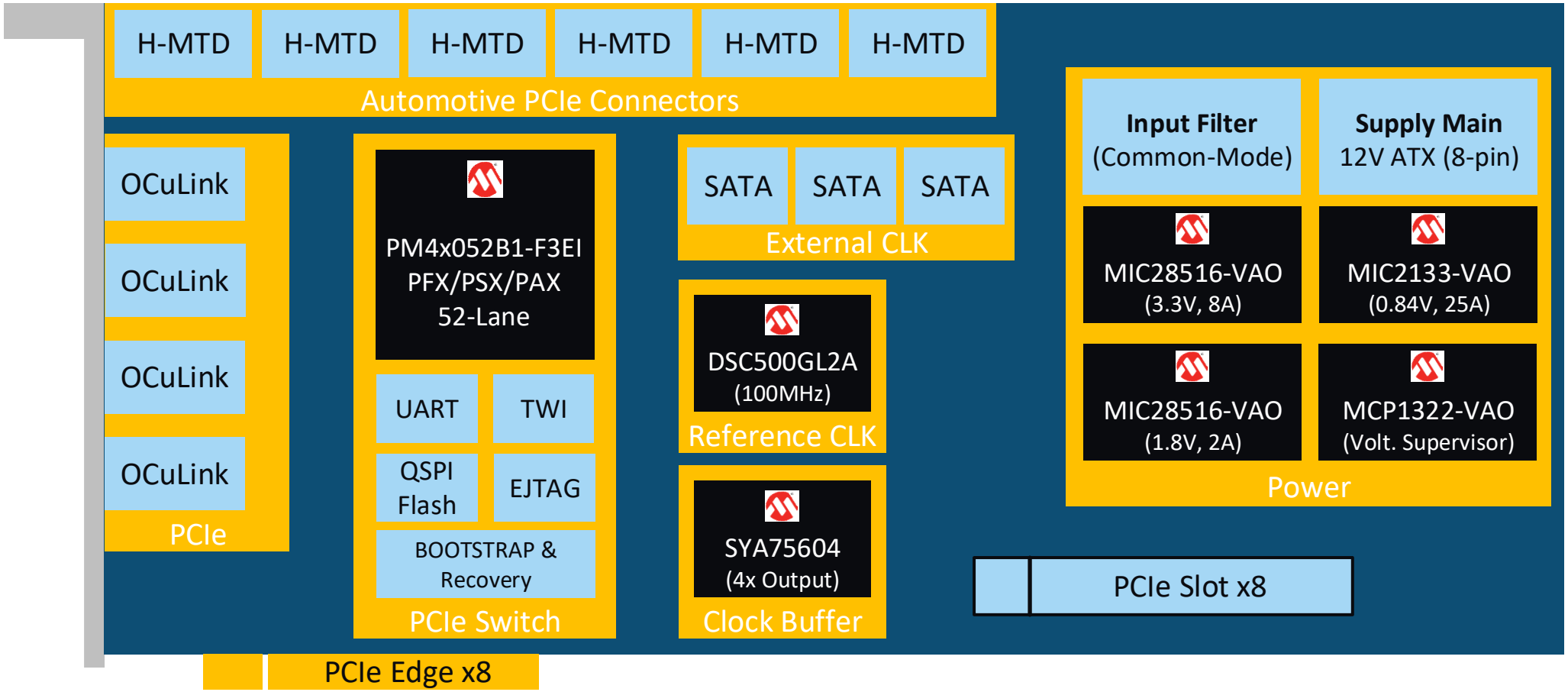
PCIe over Cable Demo

Agenda

- PCIe Applications
- What is PCIe?
- Microchip PCIe Solutions
- **PCIe over Cable Demo**

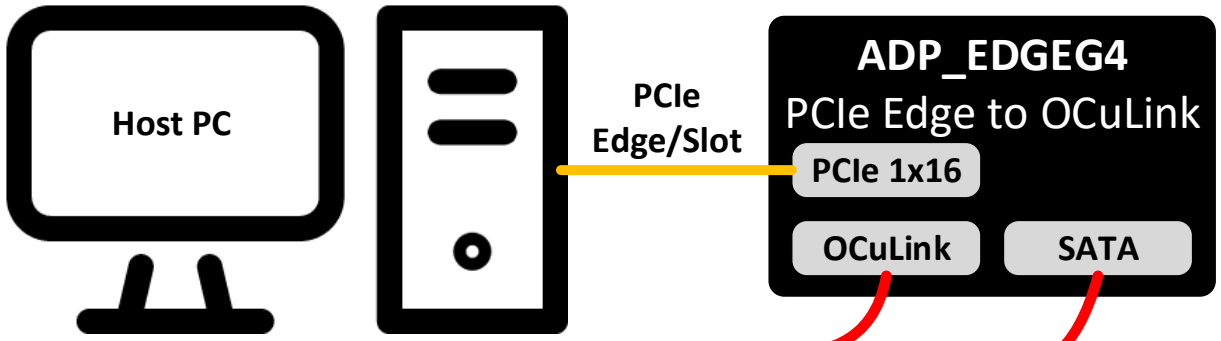
Automotive PCIe Reference Validation Board

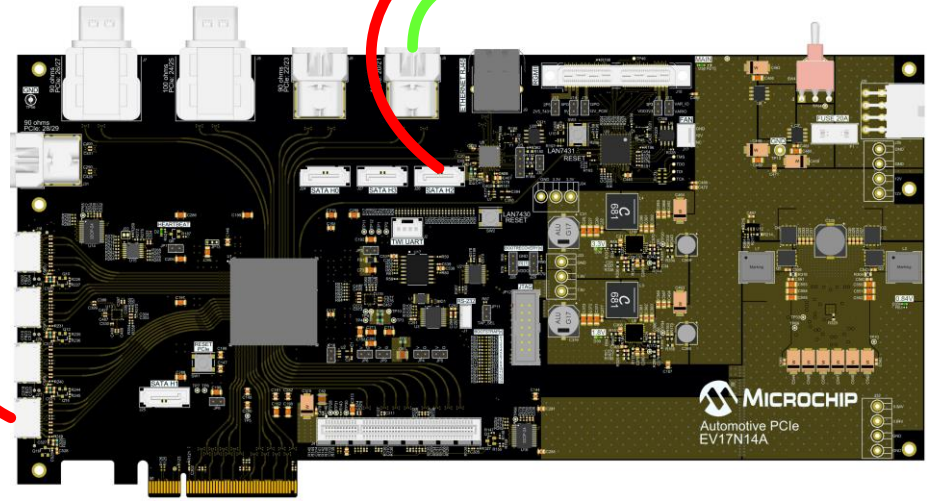
Microchip Total System Solution



Automotive PCIe Reference Validation Board

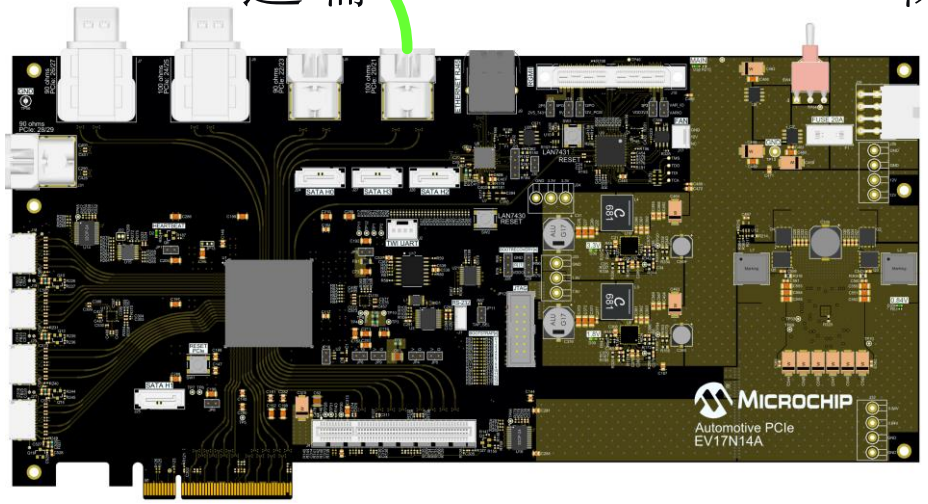
H-MTD PCIe Interface Functional Check





主機端 Trident Automotive 開發板

遠端 Trident Automotive 開發板



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PCIe Over Cable Demo

Remote Wedge Pelican Case Contents

Remote Wedge

GEMnet Cable (7m)

Webcam

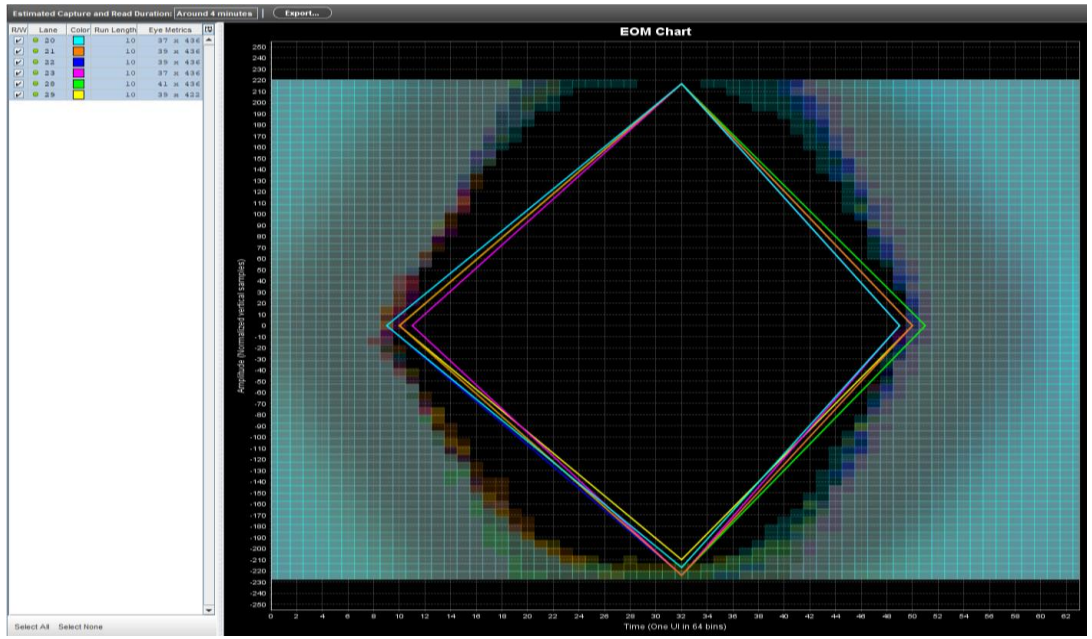
Toolkit

Eye Capture Results for Different Cable Length

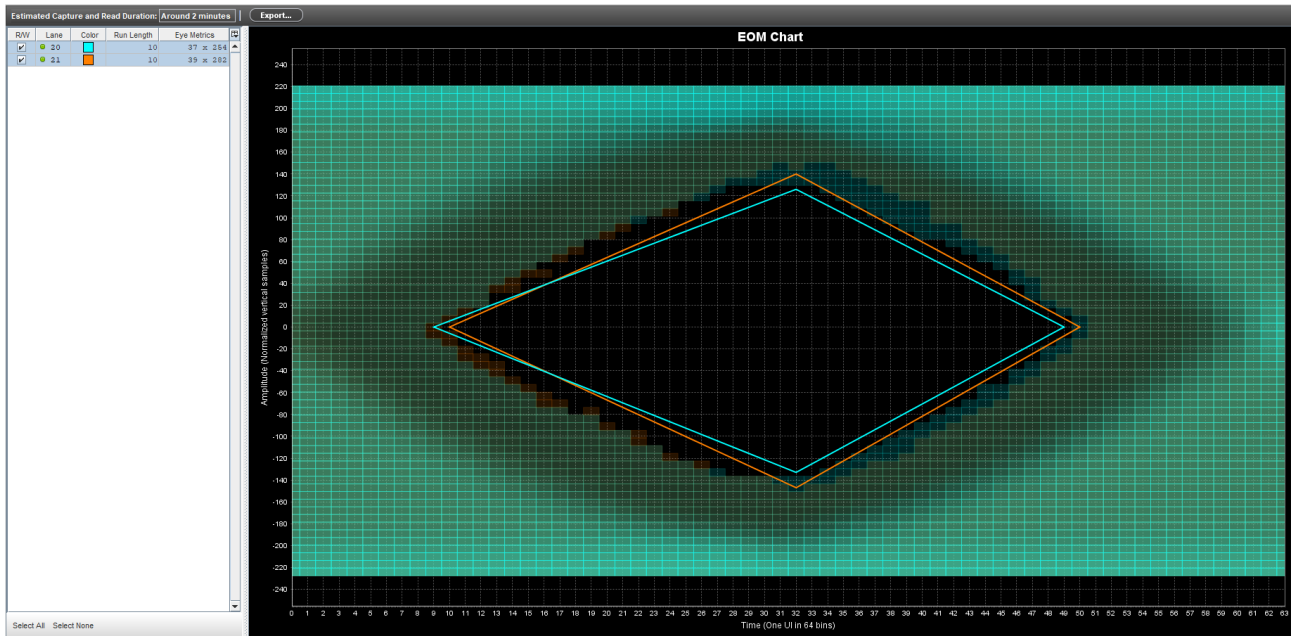
H-MTD PCIe Interface Functional Check

- **Test Objective**
  - Verify PCIe Performance over H-MTD

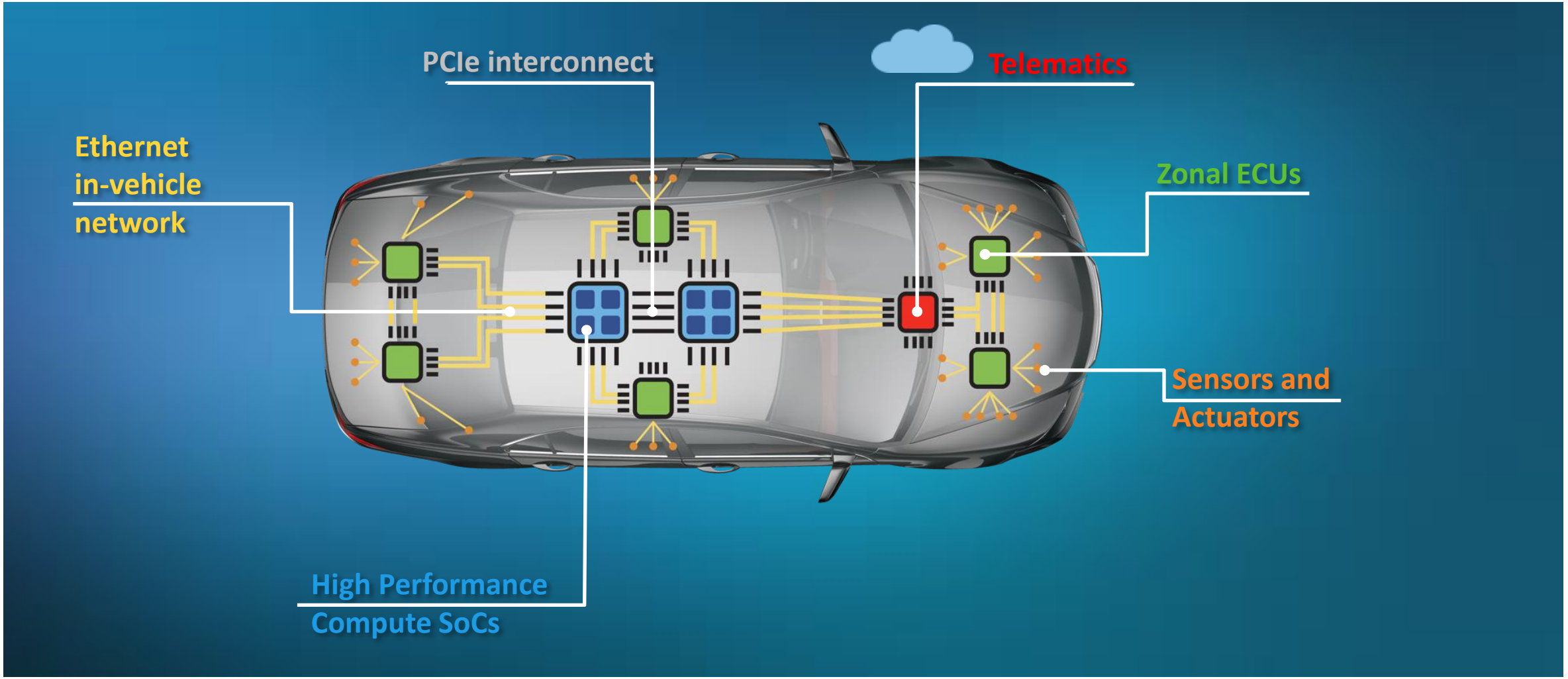
Eye Plot (Gen3 1m Cable)



Eye Plot (Gen3, 5m Cable)



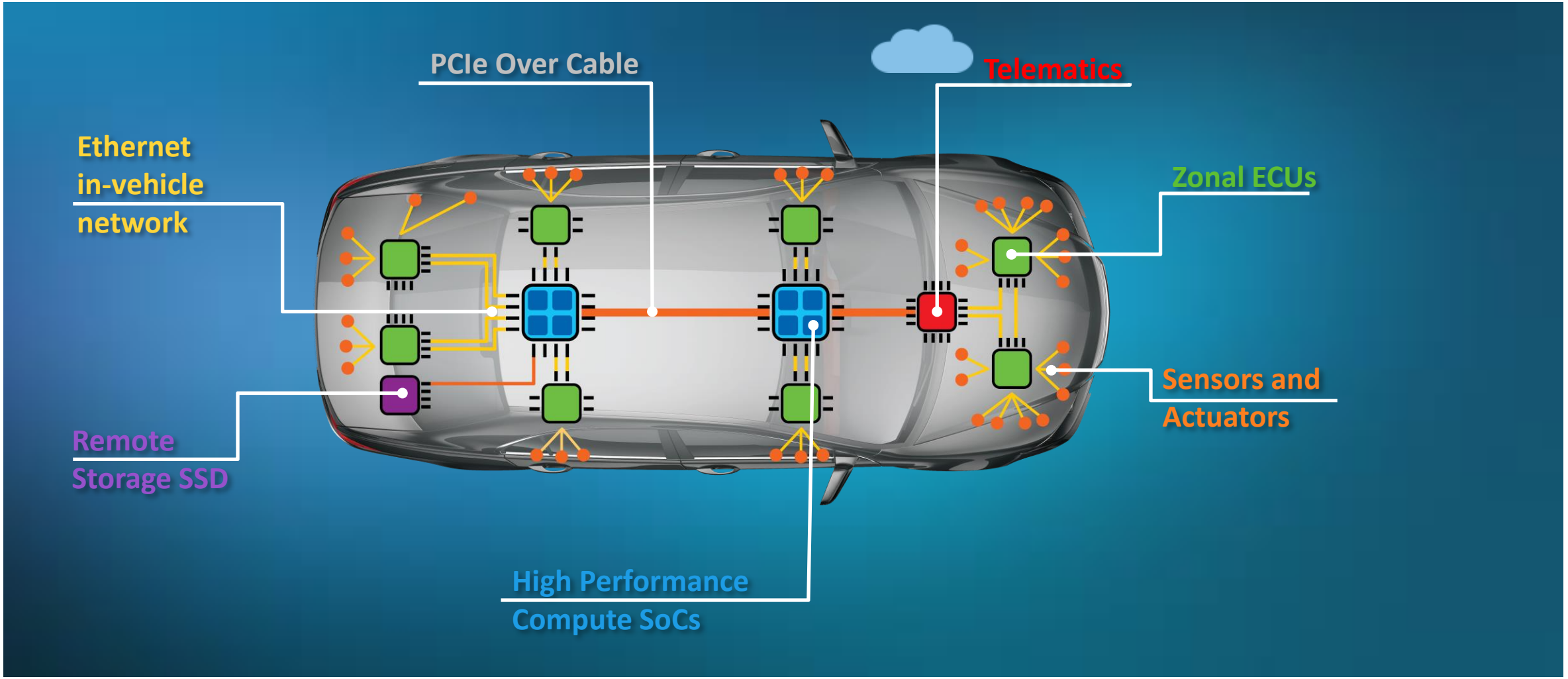
Zonal ECU with Centralized Compute Platform for ADAS Applications



PCIe Over Cable - End-Use Applications

- **Remote Storage Over Cable**
  - PCIe over cable connection to central compute SOC(s).
  - SSD storage located in accessible location (trunk, interior cabin, etc.).
- **Zonal Central Compute**
  - Distribute central compute SoCs to zonal locations.
    - Adds physical location redundancy.
    - Provides ECU scalability across multiple vehicle platforms.
    - Reduces overall thermal load of co-locating SoCs within single module/location.

Zonal SoCs (PCIe Over Cable) with Remote Storage for ADAS Applications



THANK YOU!