# Tech Forum 2024
# MCU8 - Configurable Logic Block


A Leading Provider of Smart, Connected and Secure Embedded Control Solutions


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# Agenda

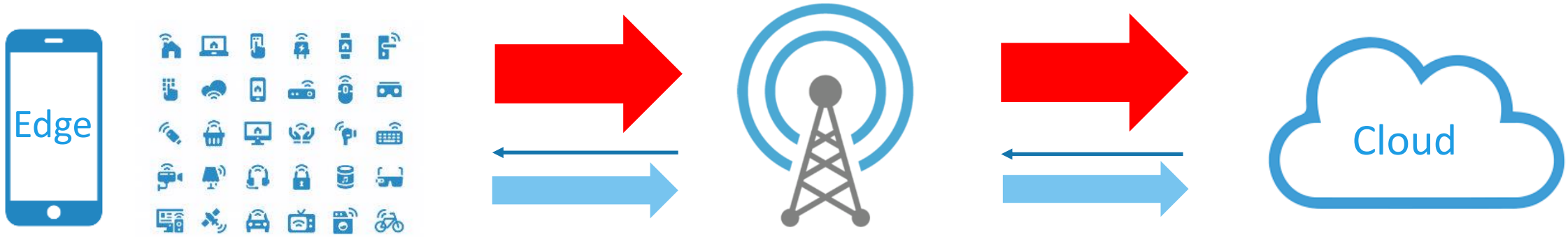
- Why
- PIC16F131 Family Overview and Peripherals
- Configurable Logic Block (CLB) Overview
- CLB Synthesizer Overview. MCC/Melody Integration

# Why

## Overview

# IoT Endpoints Have Sensors, Tons of Sensors

## Recent Trend: Push the data processing to the "Edge"




**Motion Sensors**
Gyroscope, radar, magnetometer, accelerator

**Acoustic Sensors**
Ultrasonic, Microphones, Geophones, Vibrometers

**Environmental Sensors**
Temperature, Humidity, Pressure, IR, etc.

**Touchscreen Sensors**
Capacitive, IR

**Image Sensors**
Thermal, Image

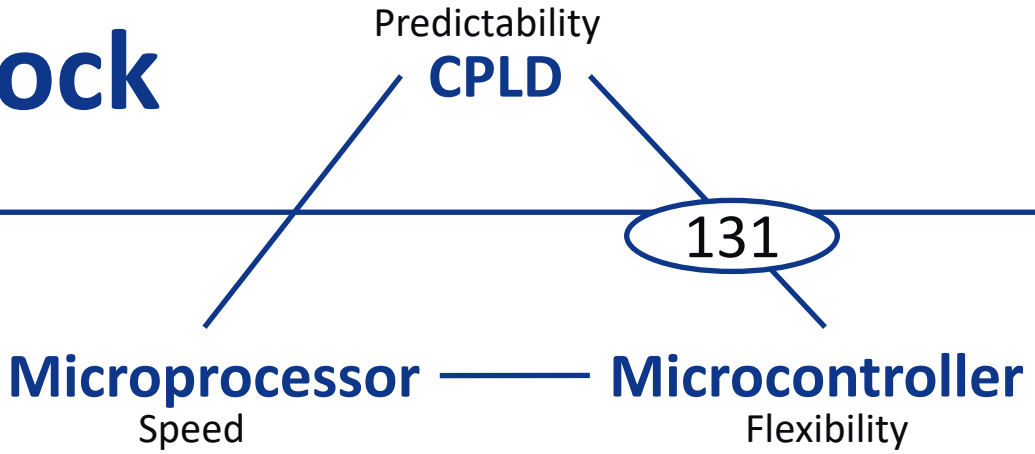
**Biometric Sensors**
Fingerprint, Heart rate, etc.

**Force Sensors**
Pressure, Strain

**Rotation Sensors**
Encoders

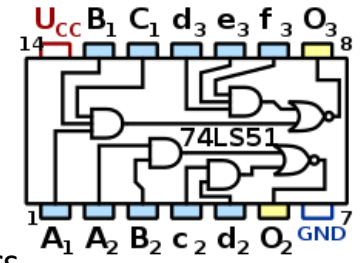
# 131's Configurable Logic Block

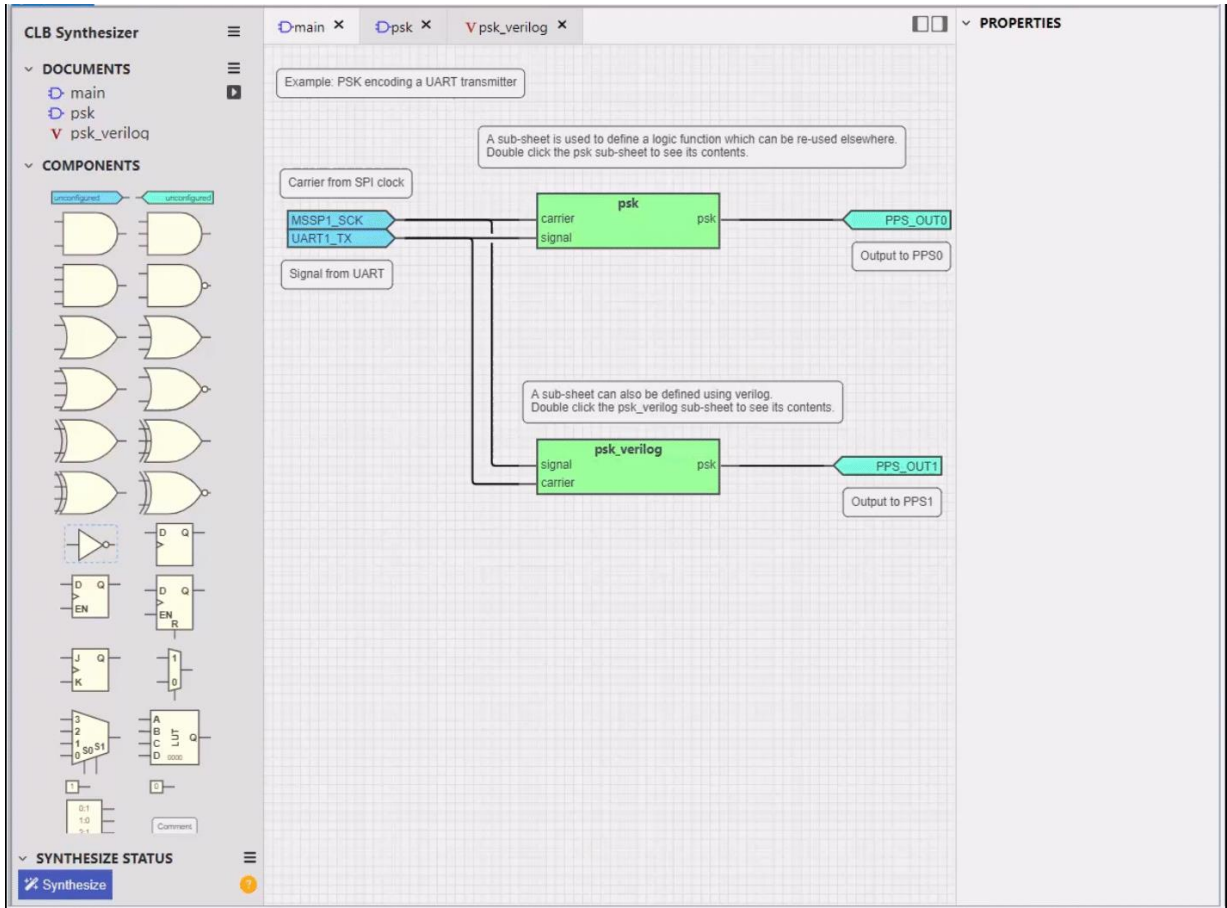
## Fast, Predictable, Low-Power




- **Key messages:**
  - Low Power Instruction-Less Task Execution
  - Predictable Low-Latency Operation
  - BOM Reduction (MCU + Logic Elements)
  - Graphical Configuration Tool

- **Where to use:**
  - Extremely timing-critical applications
    - Ex. Power up sequencing, input state monitoring
  - Repetitive signals needing similarly filtered
    - Ex. Multi-purpose buttons
  - Direct Logic Chip Replacement
    - Ex. 7400 Series chip ($0.84)
  - Custom peripherals
    - Ex. 10-bit SPI, serial encoders/decoders



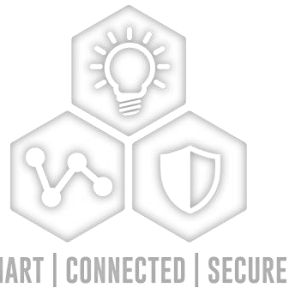



# Why ?

- **Low Latency**: The combination of CLB with the MCU enables real-time processing of input signals and data, which is highly beneficial for AI applications requiring quick responses.
- **Fast Logic Control**: CLB can achieve rapid logic control functions such as signal routing, state machine control, and peripheral coordination, thus improving the overall system response speed.
- **Low Power Design**: integrating their functions can reduce the overall power usage of the system, making it suitable for battery-powered devices.
- **Reduced Hardware Cost / PCB Space**: decrease the number of components and the complexity of the layout on the PCB, further reducing manufacturing costs and device size.
- **Reconfigurable Functionality**: offers programmable logic capabilities, allowing quick reconfiguration to adapt to changing application requirements, thus increasing system flexibility.
- **Reduced MCU Load**: By hardware-accelerating specific tasks, the MCU's computational burden is lessened, allowing it to focus on higher-level control and decision-making.
- **Copy, not easy!**

# Family Overview and Peripherals

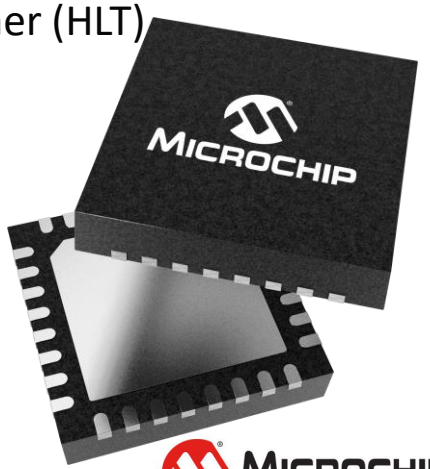

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



# PIC16F131 Family Introduction

- **PIC16 CPU**
  - Operating Speed:
    - DC-32 MHz clock input
    - 125 ns minimum instruction time
  - 16-Level Deep Hardware Stack
  - Low-Current Power-on Reset (POR)
  - Configurable Power-up Timer (PWRT)
  - Brown-out Reset (BOR)
  - Low-Power Brown-out Reset (LPBOR)
- **Memory**
  - 2 KW – 8 KW Flash
  - 256 – 1024 Bytes SRAM
- **Pins and Packages**
  - 8, 14 and 20 pins
  - DIP, SSOP, TSSOP, SOIC, VQFN
- **Temperature grades**
  - Standard: -40°C to 85°C
  - Extended: -40°C to 125°C

- **Key Features**
  - One Configurable Logic Block (CLB)
  - 10-bit Analog-to-Digital Converter with Computation (ADCC)
  - One 8-Bit Digital-to-Analog Converter (DAC)
  - Two Comparators (CMP) with configurable power modes for faster response time (50 ns) or lower power operation
  - One Host Synchronous Serial Port (MSSP)
  - One Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)
  - Four Configurable Logic Cells (CLC)
  - One Configurable 8/16-Bit Timer (TMR0)
  - One 16-Bit Timer (TMR1) with Gate Control
  - One 8-Bit Timer (TMR2) with Hardware Limit Timer (HLT)
  - Two Capture/Compare/PWM (CCP) Modules
  - Two Pulse-Width Modulators (PWM)



# PIC16F131 Family Introduction

| Device | Program Flash Memory (bytes) | Data SRAM (bytes) | Memory Access Partition/ Device Information Area | 32-Bit CRC with NVM Scanner | I/O Pins[1]/ Peripheral Pin Select | 8-Bit Timers with HLT/ 16-Bit Timers[2] | 10-Bit PWM/ CCP | 10-Bit ADC Channels (External/Internal) | I2C/SPI | EUSART | CLB | CLC | FVR | CMP | 8-bit DAC | SMBus Compatible I/O Pads | External Interrupt Pins | Interrupt-on-Change Pins | Windowed Watchdog Timer |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC16F13113 | 3.5k | 256 | Y/Y | Y | 6/Y | 1/1 | 2/2 | 5/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 6 | Y |
| PIC16F13114 | 7k | 512 | Y/Y | Y | 12/Y | 1/1 | 2/2 | 11/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 12 | Y |
| PIC16F13115 | 14k | 1024 | Y/Y | Y | 18/Y | 1/1 | 2/2 | 17/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 18 | Y |
| PIC16F13123 | 3.5k | 256 | Y/Y | Y | 6/Y | 1/1 | 2/2 | 5/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 6 | Y |
| PIC16F13124 | 7k | 512 | Y/Y | Y | 12/Y | 1/1 | 2/2 | 11/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 12 | Y |
| PIC16F13125 | 14k | 1024 | Y/Y | Y | 18/Y | 1/1 | 2/2 | 17/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 18 | Y |
| PIC16F13143 | 3.5k | 256 | Y/Y | Y | 6/Y | 1/1 | 2/2 | 5/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 6 | Y |
| PIC16F13144 | 7k | 512 | Y/Y | Y | 12/Y | 1/1 | 2/2 | 11/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 12 | Y |
| PIC16F13145 | 14k | 1024 | Y/Y | Y | 18/Y | 1/1 | 2/2 | 17/5 | 1/1 | 1 | 1 | 4 | 2 | 2 | 1 | Y | 1 | 18 | Y |

# PIC16F131xx – Introducing the CLB

- The PIC16F13145 product family adds to the cost-effective general-purpose PIC16 the Configurable Logic Block (CLB) peripheral for additional digital logic flexibility and faster response time
- The CLB extends the reach and build on our previous glue-logic type options, such as the Configurable Logic Cell (CLC) and Custom Configurable Logic (CCL)
- The CLB offers greater customization and allows more complex logic designs to be incorporated into the MCU. This module will help absorb discrete logic components into the microcontroller and reduce BOM and board space.
- This module will also provide flexibility to the user to create custom peripherals and protocols to interface with unique sensors and other components
- MCC integrated graphical tool for easy configuration of the CLB

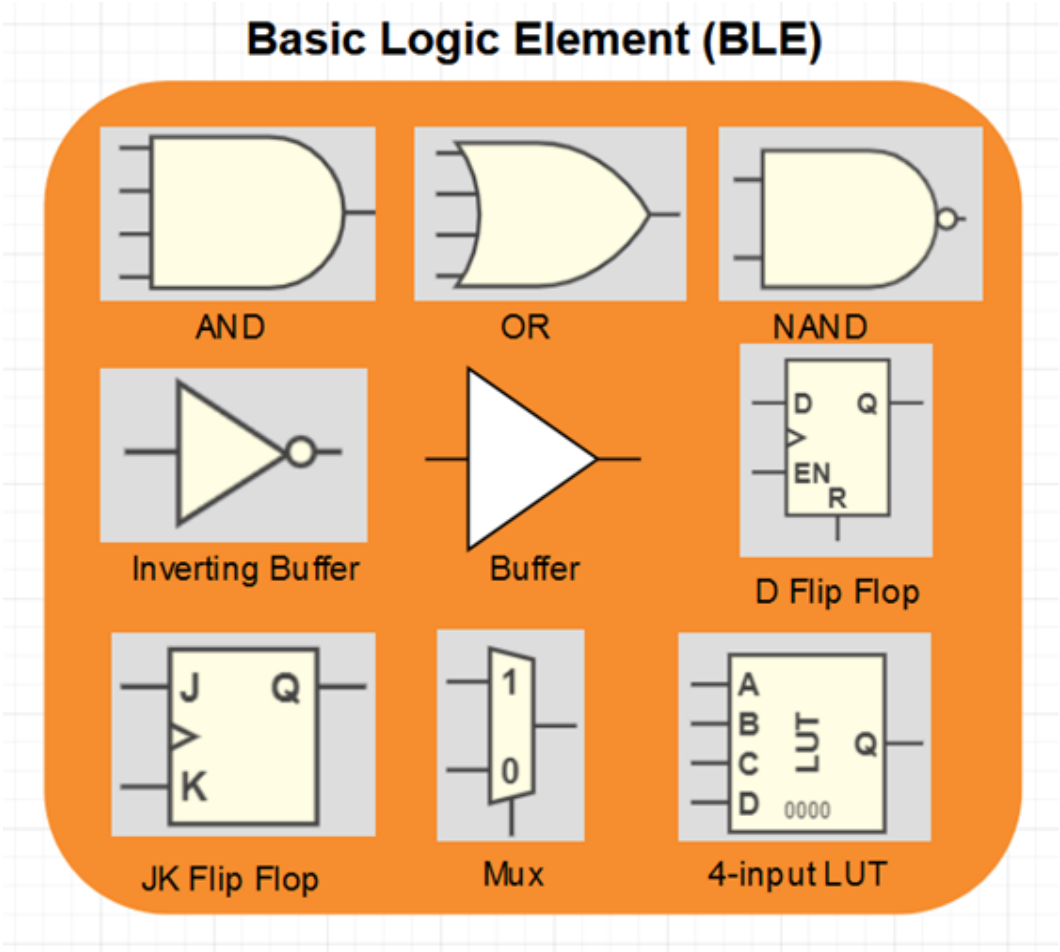
# Configurable Logic Block

Overview

# What Is CLB?

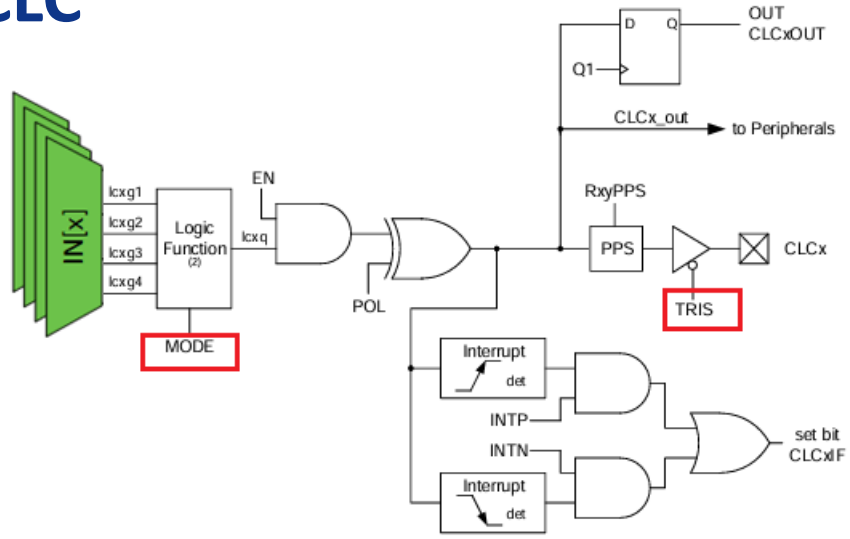
- **The Configurable Logic Block (CLB) module provides multiple Basic Logic Elements (BLEs) of user-programmed digital logic that operate without CPU intervention**
  - Support user-programmable asynchronous and synchronous binary logic operations (combinational, sequential or combination)
  - Internal and/or external signals may be used as input to each BLE
  - CLB outputs may be routed out to the port I/O pins, interrupts or directly to peripherals inputs

- **Two sets of register interfaces:**
  - Special Function Register (SFR) interface
  - Configuration interface



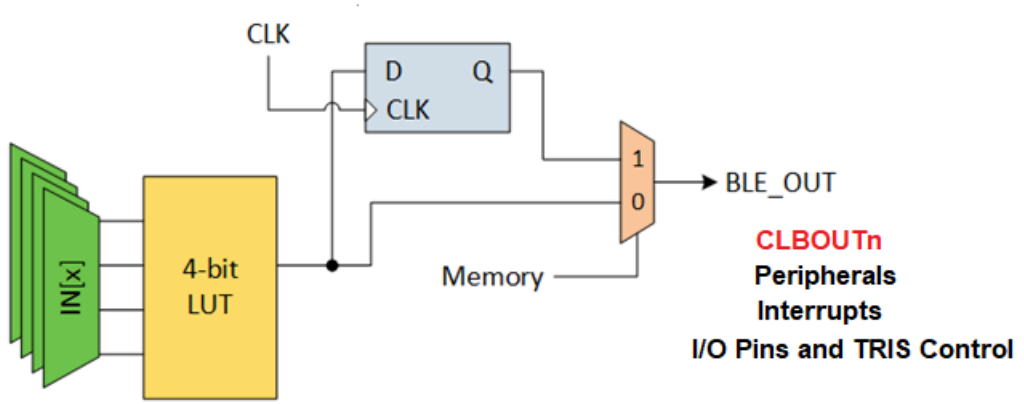
# CLC vs. CLB

## CLC




- 4/8 CLCs
- Predefined components (MODE)
- Configurable using MCC interface

## CLB

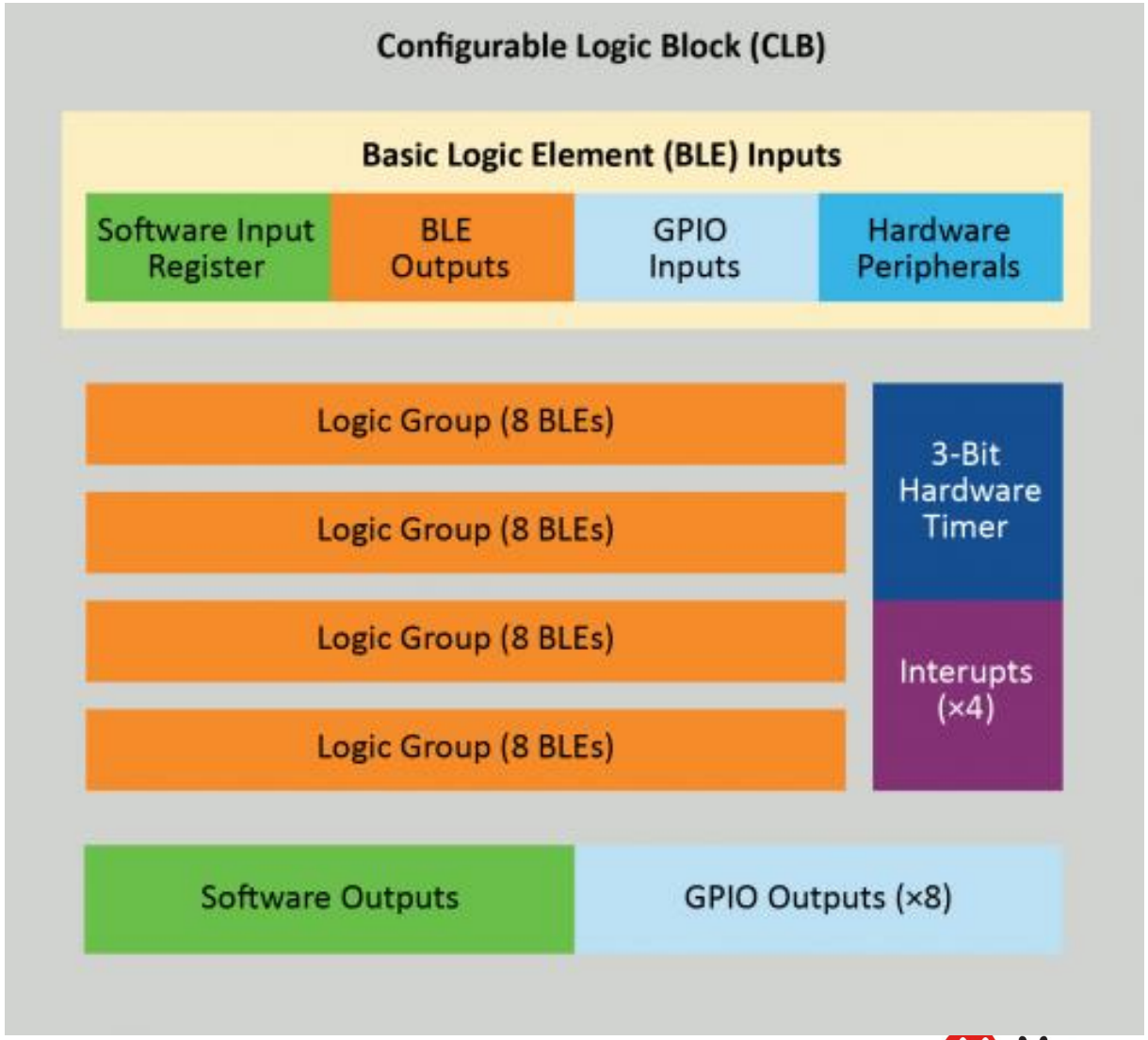



- 32+ BLEs
- Fully configurable using a graphic tool
  - Components included in the graphic tool
- Libraries/custom modules support
- I/O Tristate control
- Smaller Si area for one basic logic element
- Scalability

# Configurable Logic Block (CLB)

## What's Inside

- **32 interconnected Basic Logic Elements (BLEs)**
  - 4 input LUT + flip-flop
  - Limited interconnects
- **Inputs/outputs**
- **3-bit HW counter**
- **Common clock**
  - Selectable on device
  - Programmable divider
  - Shared by *everything*



# Configurable Logic Block (CLB)

## How It Is Connected

**External Inputs (on-chip connections):**

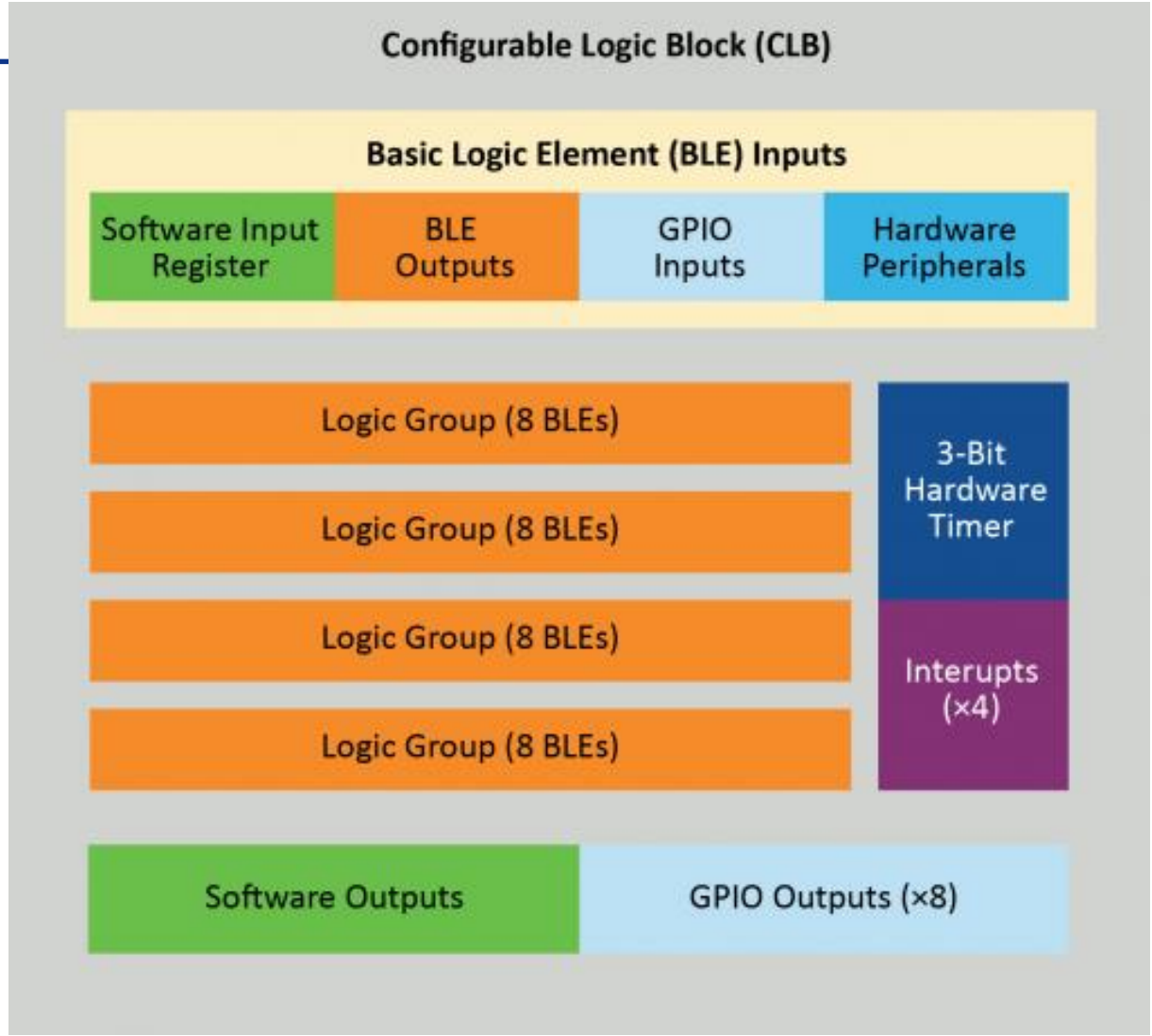
- **16 channels selectable from 29 sources**
  - Comparators, SPI, UART, CLCs, IOCIF, PWMs, CCPs, Timers, Clocks, PPS
  - Input options
  - Synchronous, direct, rising/falling edge detectors

**Internal Inputs**

- **Software Inputs**
  - 32 input bits (CLBSWINL/H/M/U SFR registers)
  - CLBSWIN_SFR_WR_HOLD strobe can be used as an input source
- **3-bit (8-state) Hardware Counter**
- **BLE outputs**

**Outputs:**

- **8 direct PPS outputs**
  - With optional PPSOE control
- **4 interrupt outputs**
- **5 outputs to other peripherals**
  - Timer clock, gate, reset source, CCP, ADC trigger
- **Software outputs***
  - One bit per BLE



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# Configurable Logic Block Synthesizer

Graphical Configuration Toolchain for CLB peripheral

# Configurable Logic Block Synthesizer

## Online version vs MCC version

| Feature | Online (bare-metal) | MCC |
|---|---|---|
| Accessibility | Visit logic.microchip.com | Install MPLABX and MCC |
| Sketching and verilog | ✓ | ✓ |
| Access all CLB features | ✓ | ✓ |
| Code generation | Simple ZIP file with .c, .h, .s | Embedded into your project |
| Code integration | ✗ | Fully integrated* ✓ |
| Output peripheral mappings | #defines in ZIP | Notifications in MCC* (integrated in future release*) |
| Works offline | ✗ | ✗ |
| Import/export/save/load | ✓ | ✓ |

# Configurable Logic Block Synthesizer

## A New Approach to Configuring the Peripheral

1. Sketch the logic you want on a canvas (or use Verilog)
2. Invoke an on-line backend server which synthesizes the design and returns a bitstream
3. Embed the bitstream as source into your project
   - The MCC/Melody version uses generated bitstream to create notifications/alerts with details about the required peripheral configuration
   - The MCC/Melody version includes all files into the project
4. Configure the CLB at start-up/run-time
   - The CLB configuration is loaded using CRC module

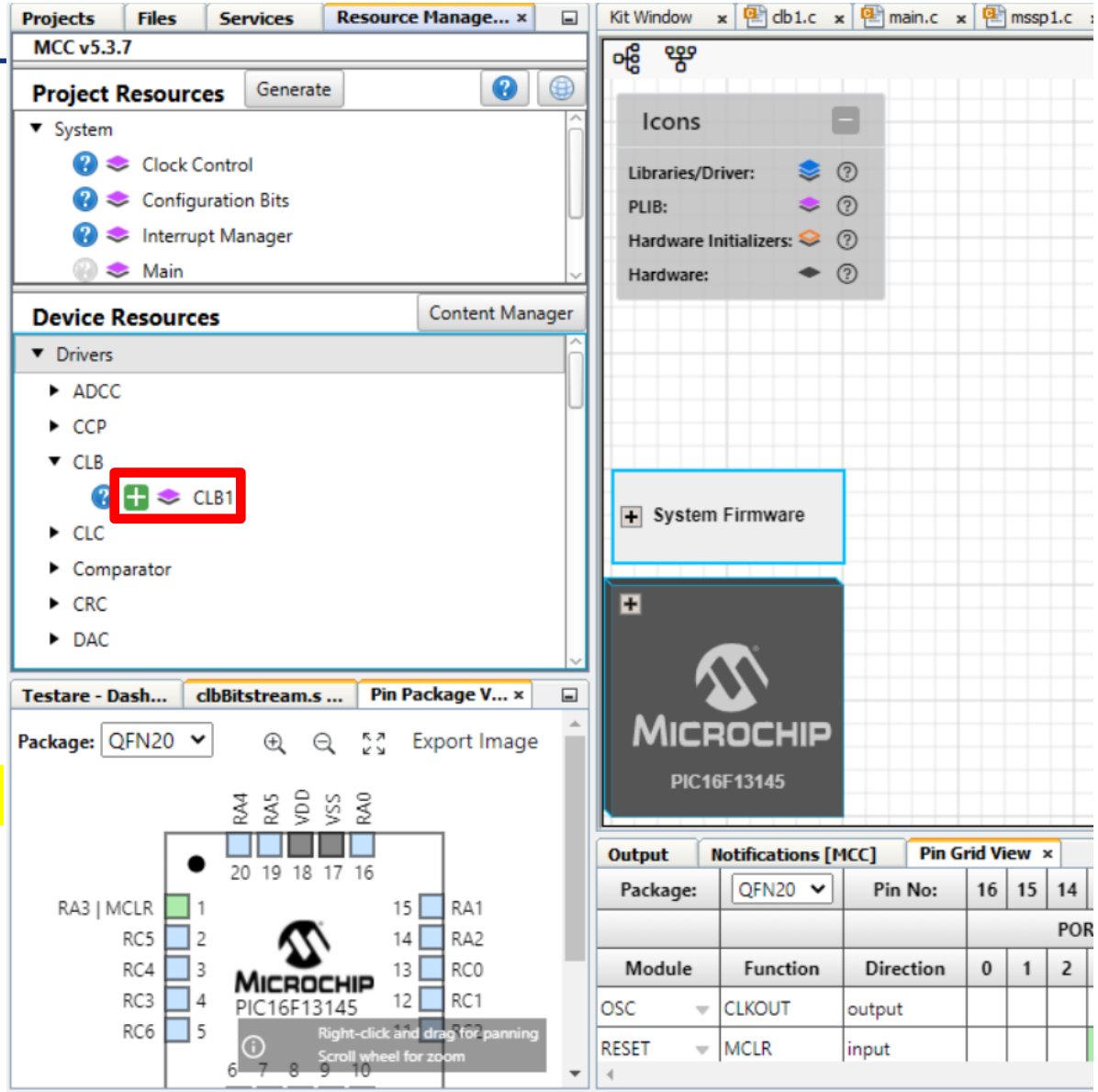
# Configurable Logic Block MCC Melody

CLB Synthesizer Melody Integration

# Configurable Logic Block

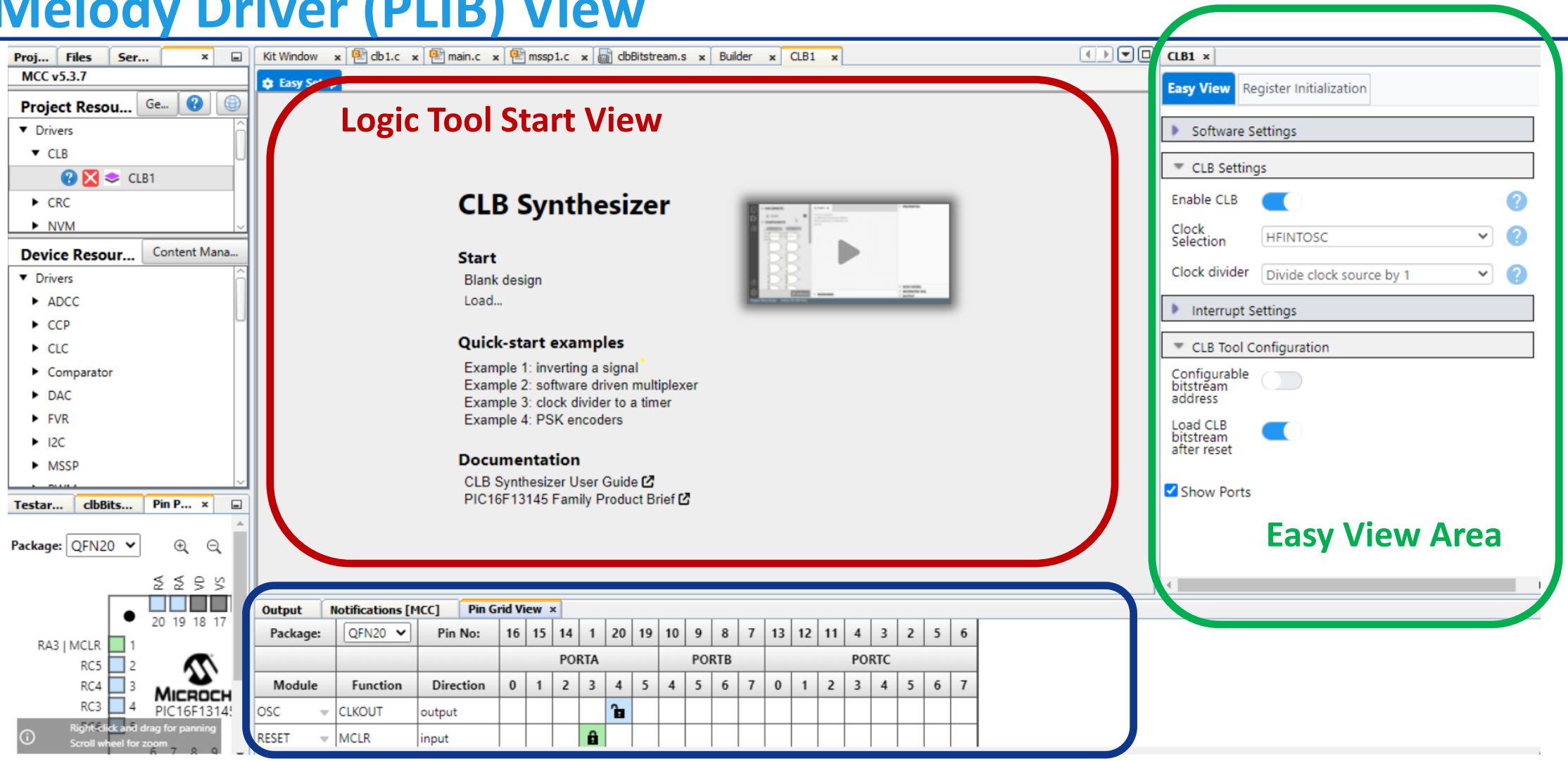
## Starting with MCC/Melody

1. New project for PIC16F13145
   - Prerequisites
   - PIC16F1xxxx_DFP.1.23.378
     - CLB PLIB V.1.0.0-dev.28
2. Add CLB to the project resources.
3. Use the graphic tool to create a logic design.
4. Synthesize
   - The inputs/outputs to/from peripherals should be configured by user after a successful synthesis (Notifications tab)
5. Generate code and build.



# Configurable Logic Block

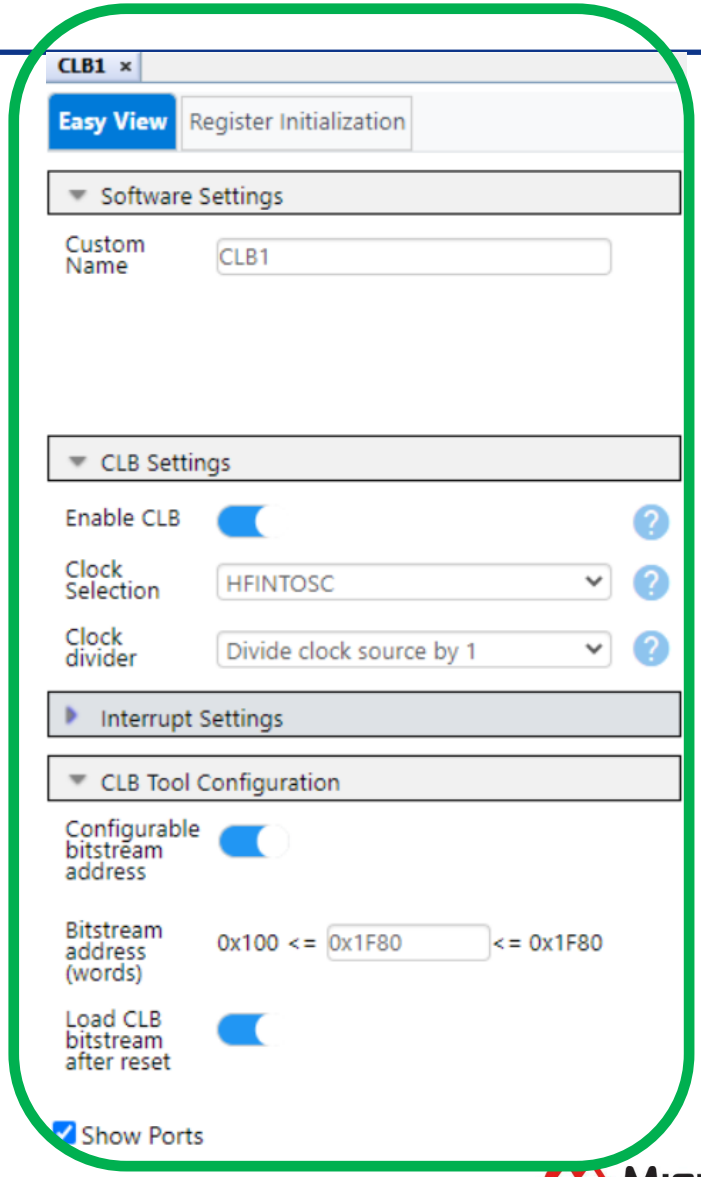
## Melody Driver (PLIB) View



# Configurable Logic Block in Melody

## Easy View

- Clock source and divider configuration
- Interrupt handlers
- Configurable bitstream address
- Options to enable and load configuration on reset
- Notifications for peripheral configuration
- Pin-grid view integration



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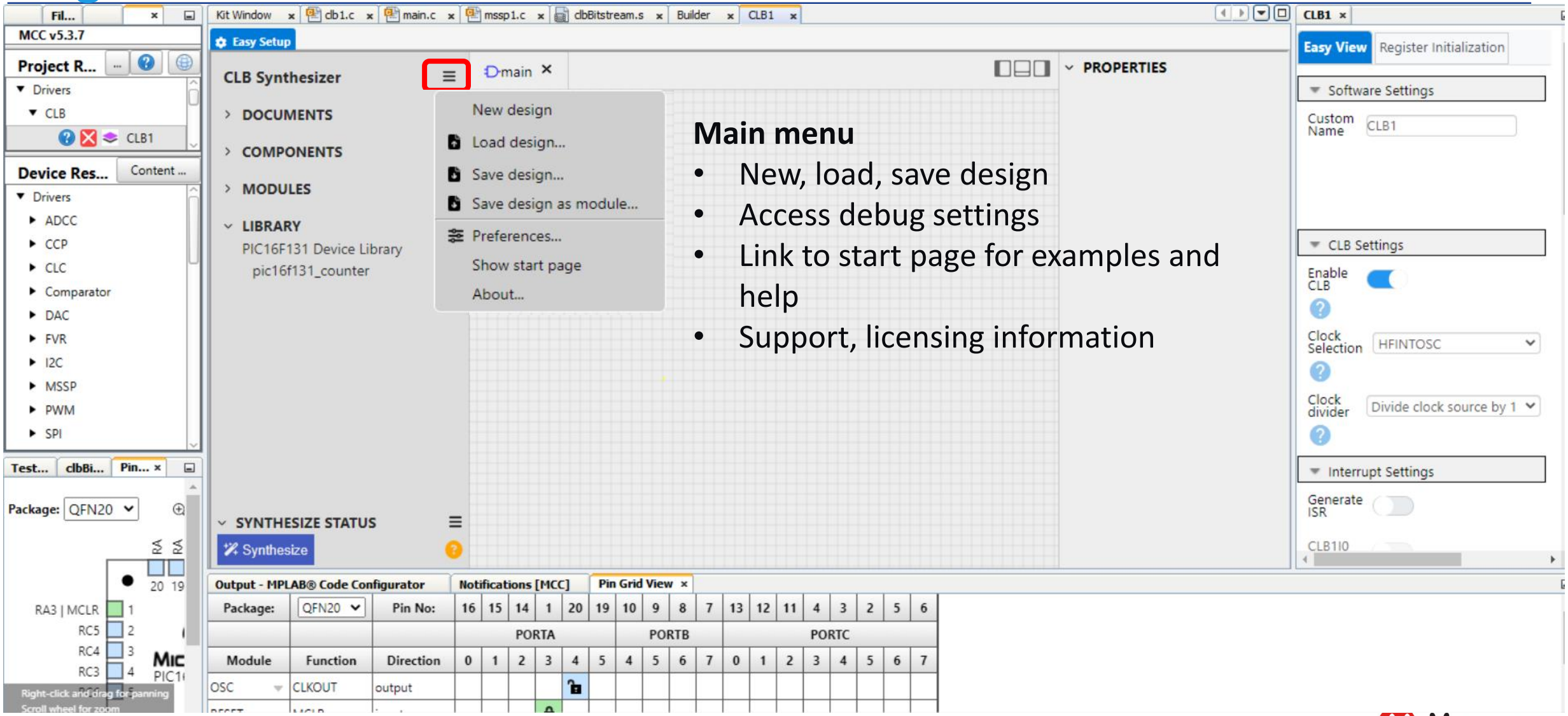
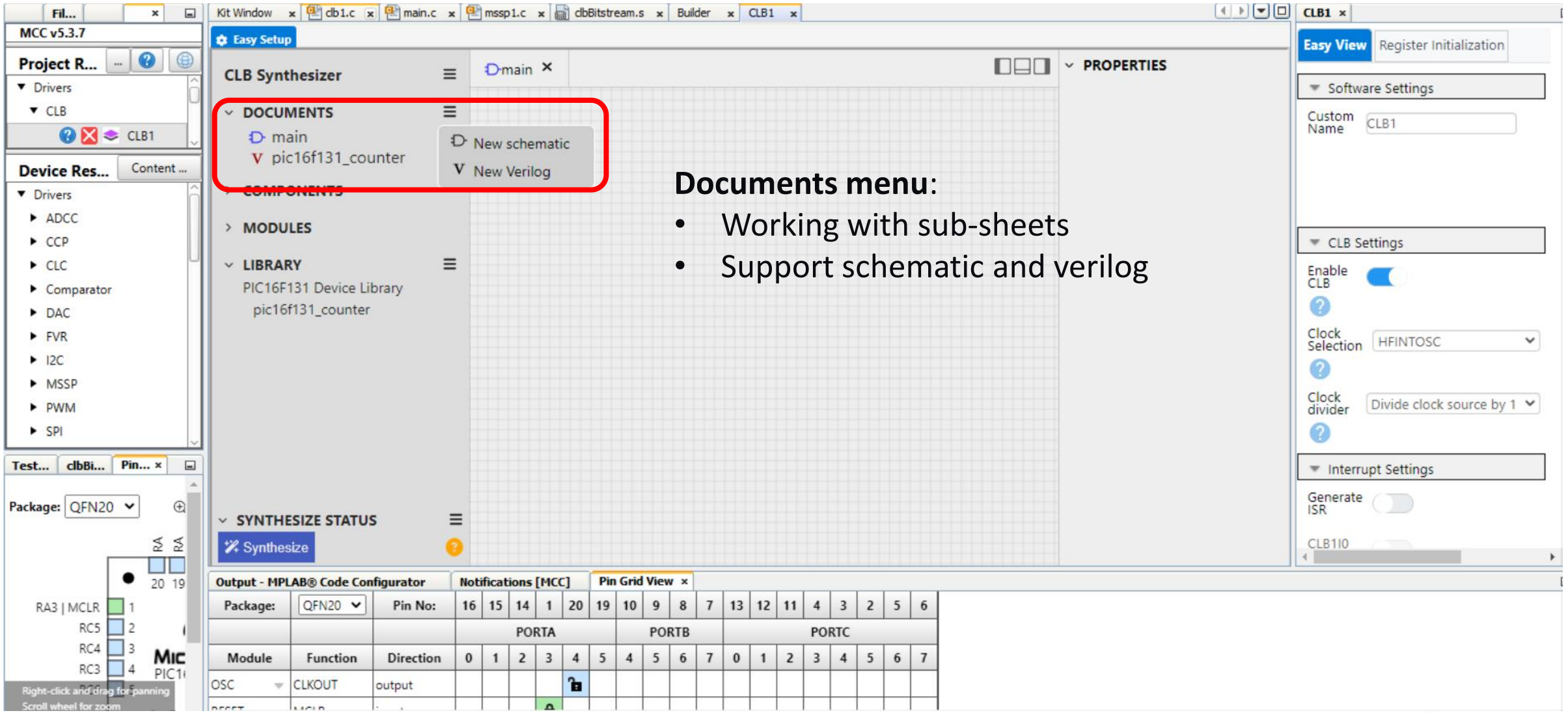
# Configurable Logic Block in Melody

## Logic Tool View



# Configurable Logic Block in Melody

## Logic Tool View

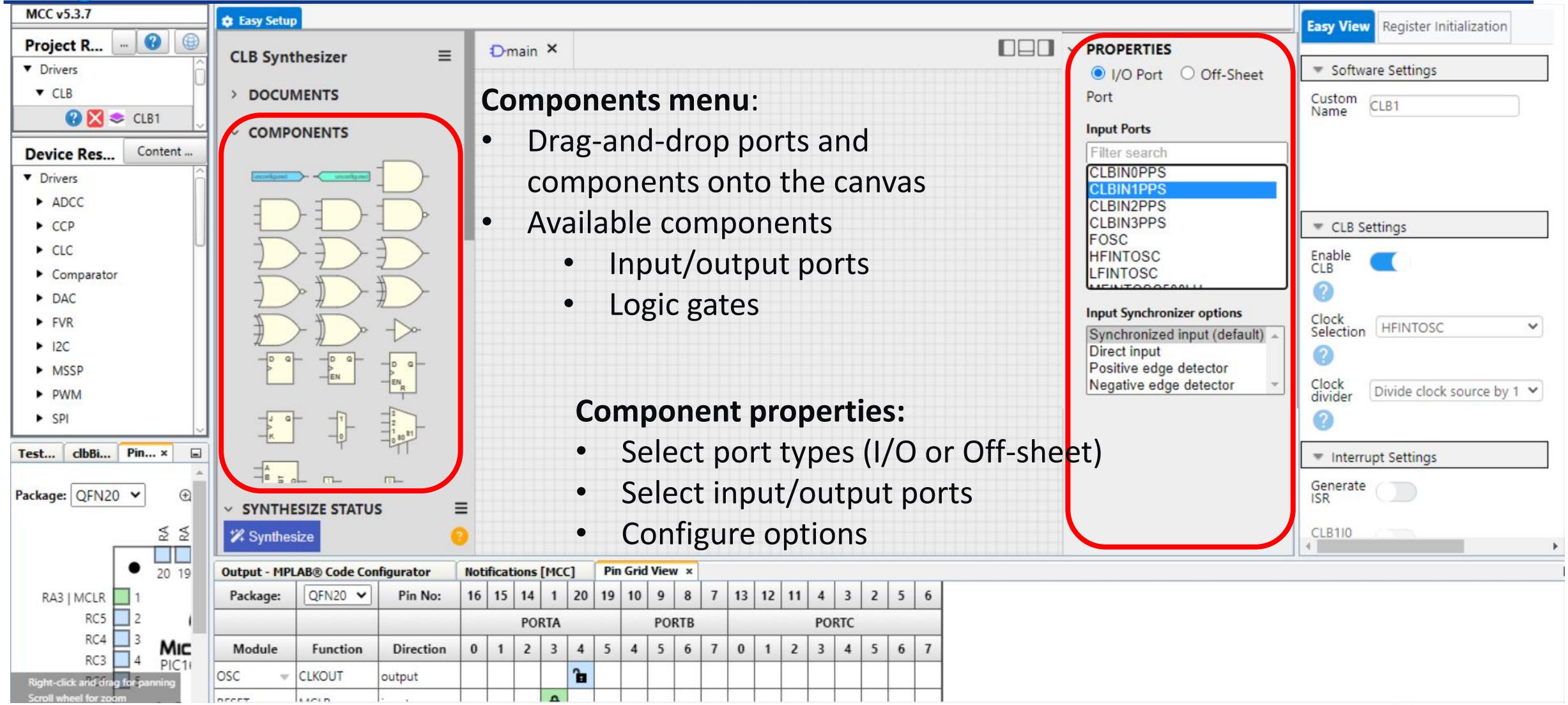



**Documents menu**:

- Working with sub-sheets
- Support schematic and verilog

# Configurable Logic Block in Melody

## Logic Tool View



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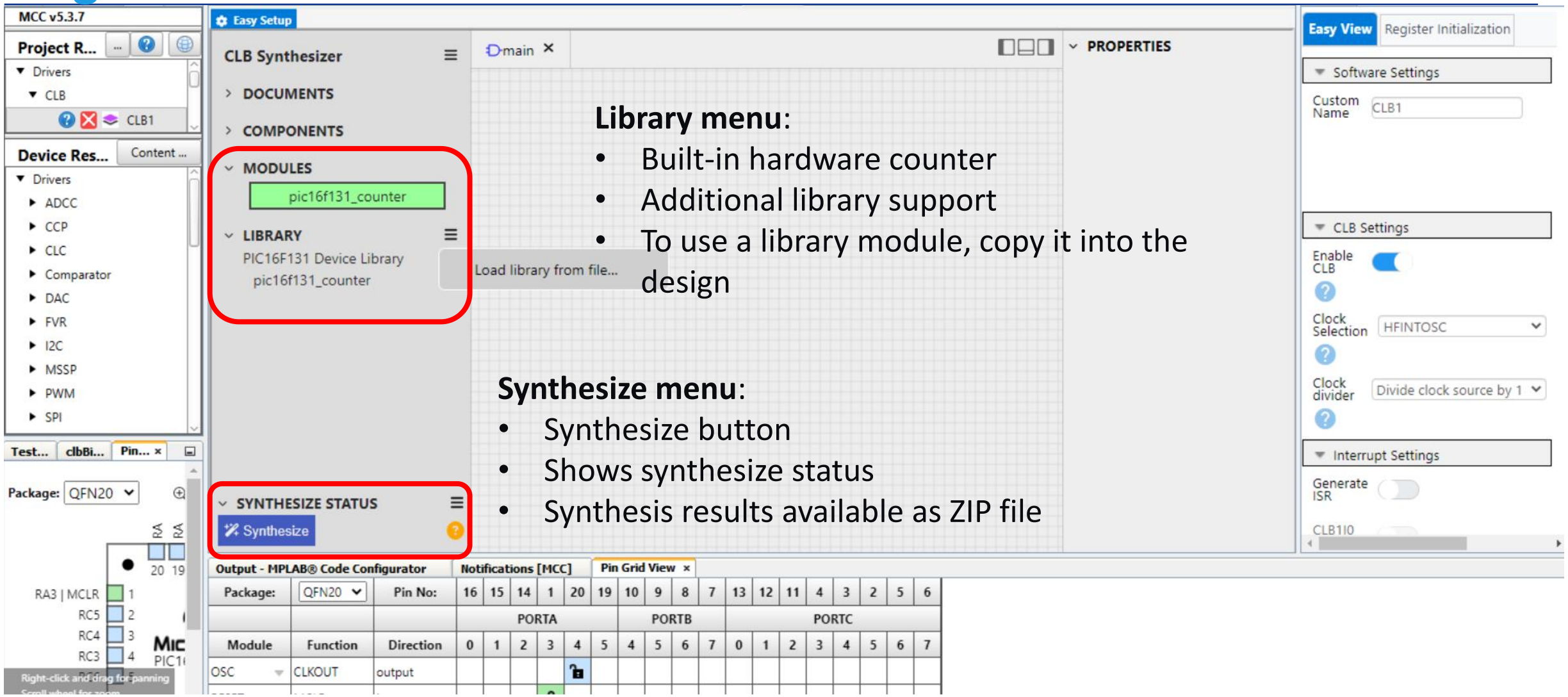
# Configurable Logic Block in Melody

## Logic Tool View




**Library menu**:

- Built-in hardware counter
- Additional library support
- To use a library module, copy it into the design

**Synthesize menu**:

- Synthesize button
- Shows synthesize status
- Synthesis results available as ZIP file

# Resources

- **MCC internal resources:**
  - Follow procedure: https://confluence.microchip.com/x/fdDgH
  - CLB PLIB used for code examples – scf-pic8-clb-v1 ***V.1.0.0-dev.28***
  - PIC16F131xx DFP: PIC16F1xxxx_DFP.1.23.378

- **CLB Synthesizer – web version**
  - https://logic.microchip.com/clbsynthesizer/

- **Need help?**
  - Press F1 (online docs content update in progress)
  - Send a mail to logic@microchip.com
  - Log a bug in Jira project: https://jira.microchip.com/projects/LOGIC/issues

# Resources

**Code examples**

7-segment decoder

- SPI to WS2812 peripheral
- Stepper motor control
  - Metronome
  - Tachometer
- Quadrature decoder
  - 2 x PIC timers
  - up/down CLB 4-bit timer
- Libraries
  - 4-bit counters
  - Shift registers
- WS2812 Matrix driver
  - Use external SPI EEPROM to store images
  - Support 1/2/4 digital streams up to 750 kbps (maximum 1/2/4 x 2048 LEDs @ 15 fps)

# Thank You