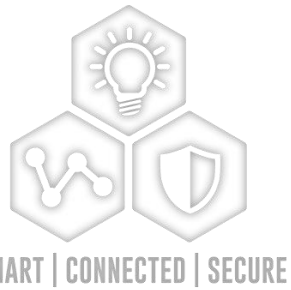
Microchip SPE Solutions



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



Darren Chen

November 12, 2026

Agenda

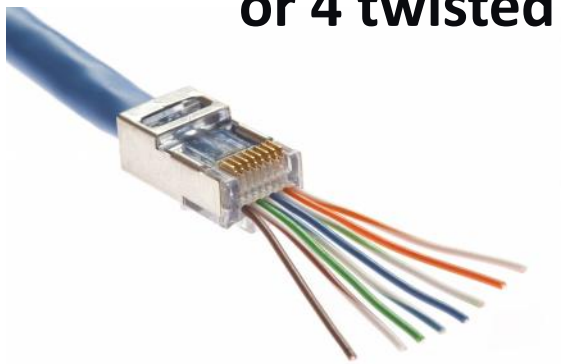
- Single Pair Technology
- 10Base-T1S Introduction
- OPEN Alliance Introduction
- 10Base-T1S Application
- Product Details

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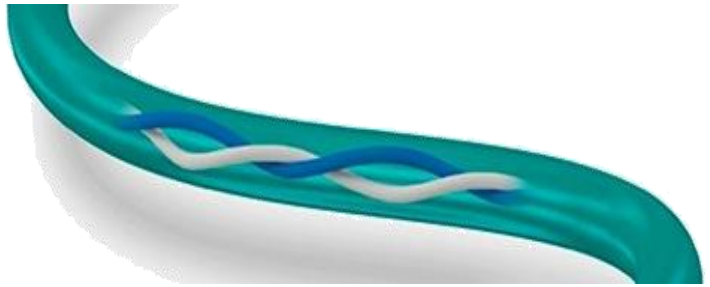
Single Pair Technology

What is Single Pair Ethernet (SPE)?

- Traditional ethernet uses 2 or 4 twisted pairs



- SPE = Single Pair Ethernet
- T1 = 1-Twisted Pair



- Just a new ethernet transceiver (PHY)
- Network layers 2-7 remain the same
- Independent of speed; 10BASE-T1, 100BASE-T1, NGBASE-T1…

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Why Single Pair Ethernet?

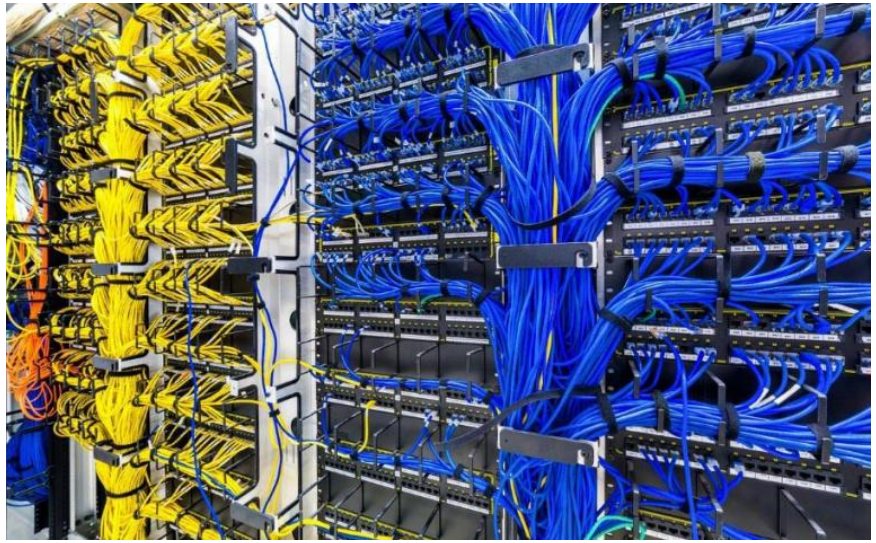
- Single Pair Ethernet reduces system cost, weight and wiring complexity

- **IEEE 802.3cg - 10BASE-T1S and 10BASE-T1L**
  - 10 Mbit/s connection over a single two-conductor cable
    - 10BASE-T1S: Short Reach (25m), multi-drop bus line or point-to-point connection
    - 10BASE-T1L: Long Reach (1 km), point-to-point connection

- **IEEE 802.3bw - 100BASE-T1**
  - 100 Mbit/s over single pair

- **IEEE 802.3bp - 1000BASE-T1**
  - 1000 Mbit/s over single pair cable

- **IEEE 802.3ch – NGBASE-T1**
  - 2.5Gbit/s, 5Gbit/s, 10Gbit/s over single pair cable

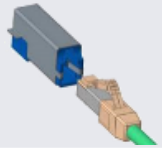
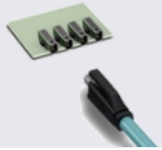


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SPE Connector Standard – Current Status

- **ISO/IEC 63171 CONNECTORS FOR ELECTRICAL AND ELECTRONIC EQUIPMENT**

	IEC 63171	IEC 63171-1	IEC 63171-2	IEC 63171-3	IEC 63171-4	IEC 63171-5	IEC 63171-6	IEC 63171-7
Initiator	N/A	Commscope	R&M	SIEMON	BKS	Phoenix Contact	Harting	TE
Picture								
Type		LC-Style	Rectangle	TERA 1P	Square-shaped	M8 / M12	Rectangle / M8 / M8 Hybrid/ M12	M12 Hybrid
Variants		1	1		1	2	4	7
IP-class		IP20	IP20	IP20	IP20	IP67	IP20 / IP67	IP67
Status Norm	**published**	ED1 published ED2 in progress	**published**	-	CDV	**2. CDV** publish in 2022	ED1 published ED2 in progress	CD
Target markets	N/A	Building	Building / Industry	-	Building / Data Center	Industry	Industry	Industry
Available products		-	**Sockets, Patchcables**	-	-	**M8 sockets, M8 Patchcable**	IP20 sockets, Patchcables	-

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Longer reach application

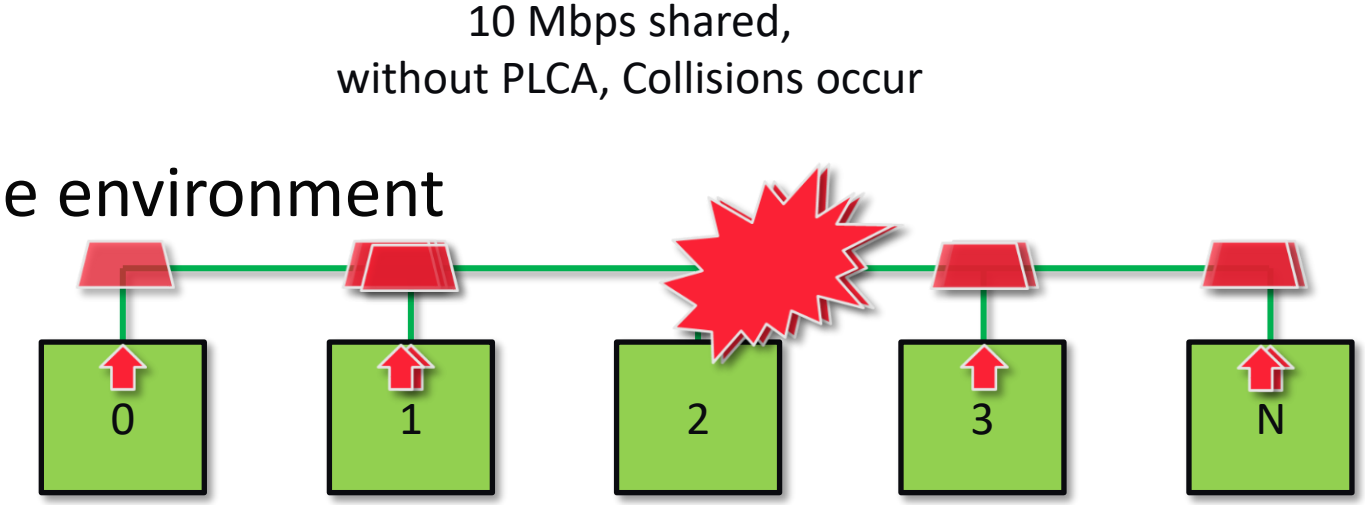
- AN1829 - Understanding System Intrinsic Noise: Enabling Longer Reach and More Nodes on 10BASE-T1S Systems
- Total 100M, 50 nodes , each node spacing for 2M



Introduction to T1S

What is 10BASE-T1S ?

- **Ethernet on a UTP bus line**
  - 10 Mbps shared
  - Half-duplex
  - 2-50 nodes, depending on the environment
  - Up to 25m bus length
  - IEEE 802.3cg standard
  - Low power
  - No collisions (PLCA)



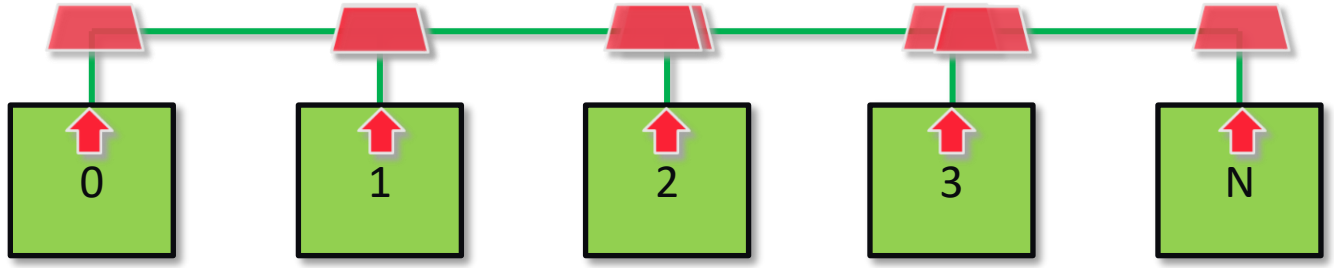
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What is 10BASE-T1S ?

- **Ethernet on a UTP bus line**
  - 10 Mbps shared
  - Half-duplex
  - 2-50 nodes, depending on the environment
  - Up to 25m bus length
  - IEEE 802.3cg standard
  - Low power
  - No collisions (PLCA)
- **Benefits**
  - No switch required
  - Inexpensive UTP cabling
  - Inexpensive analog front end
  - Less PHYs and cabling than with star topology
  - Supports Functional Safety

10 Mbps shared,
PLCA switched ON, avoids collisions



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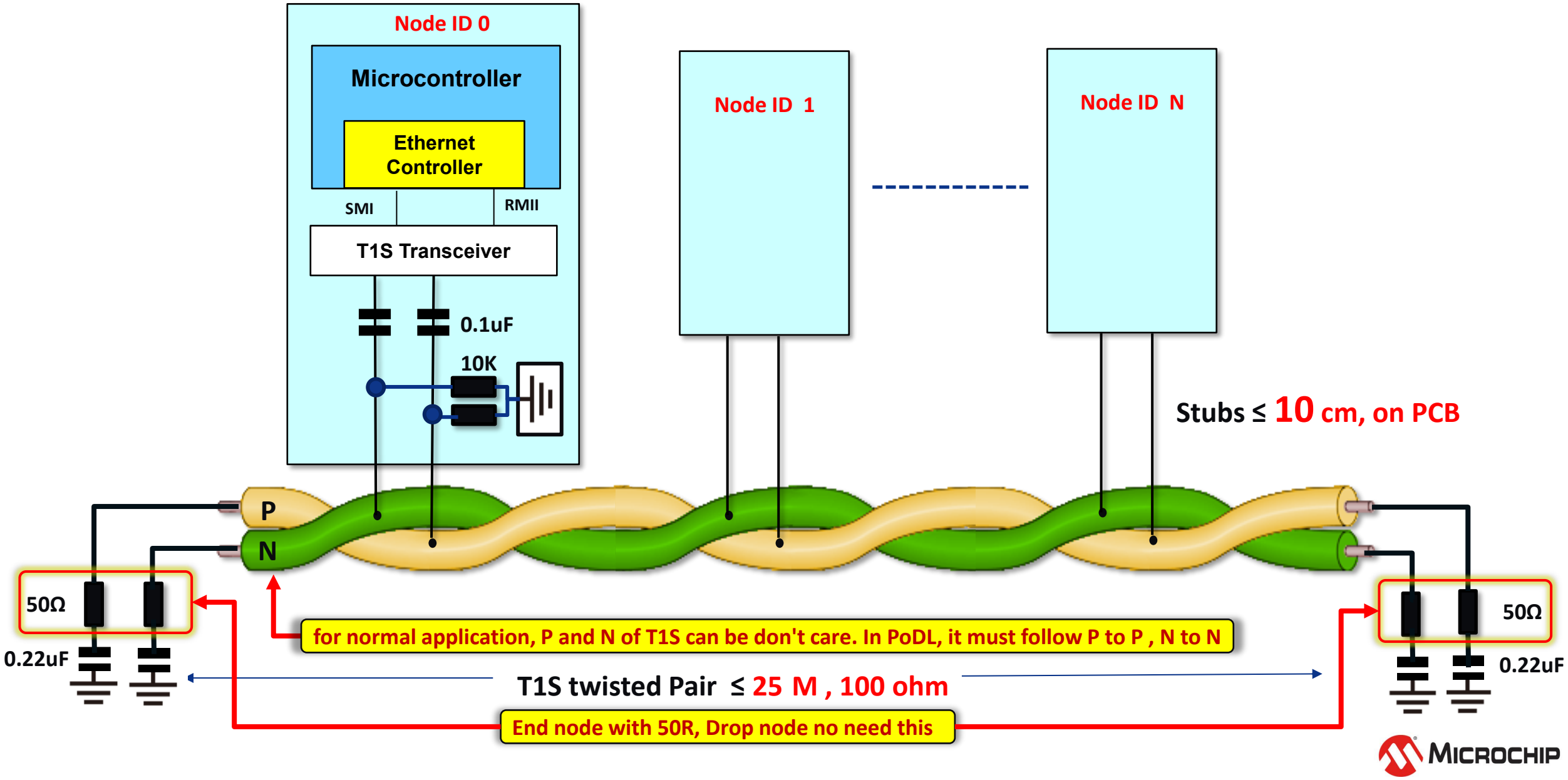
PLCA in IEEE 802.3 Ethernet Model

OSI Reference Model Layers	IEEE 802.3 Ethernet Model Layers	
Application	Higher Layers	
Presentation		
Session		
Transport		
Network		
Data Link	LLC = Logical Link Control (or other MAC client)	
	MAC Control	
	MAC = Media Access Control	
Physical	MII = Media Independent Interface	PHY
	PLCA Reconciliation	
	MII	
	PCS = Physical Coding Sublayer	
	PMA = Physical Medium Attachment	
	AN = Auto-Negotiation	
	MDI = Medium Dependent Interface	

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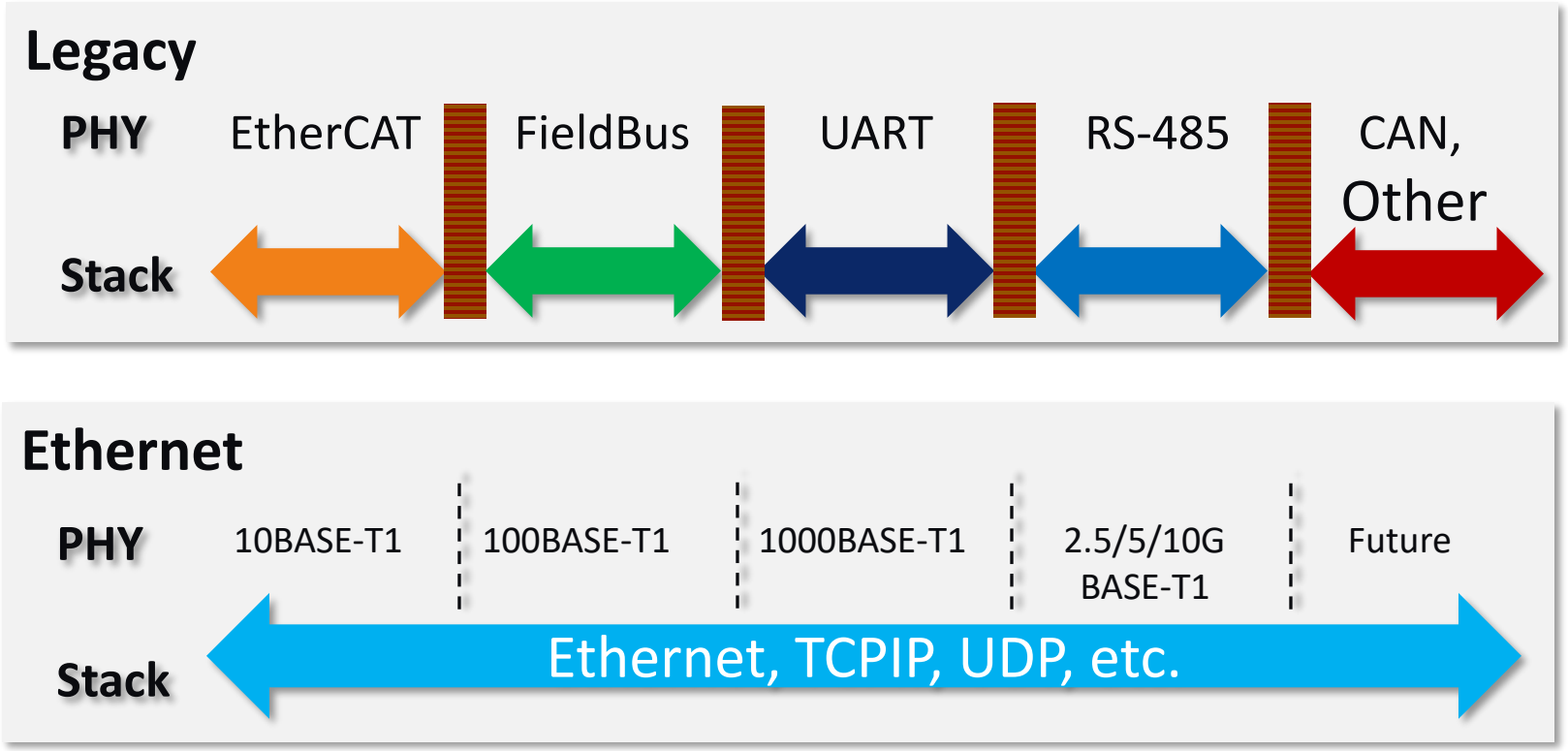
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T1S cabling example



Scalable from Low to High Bandwidths

- **Common network software stacks**
- **Physical layer independent**



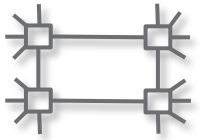
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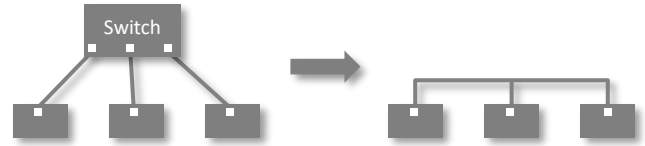
Motivation

Ethernet, a success story

- **Security**
  - Offering reliable standards (MACsec, IPsec)
- **Safety**
  - Preventing nodes from flooding network
  - Deterministic behavior
- **Synchronization**
  - Single time base for all nodes
- **Software defined system**
  - Sensors, actuators just offering a service
  - Independent applications operating on services
- **Wiring**
  - Shorter cables through zone architecture
  - Enabling machine-made wire-harness



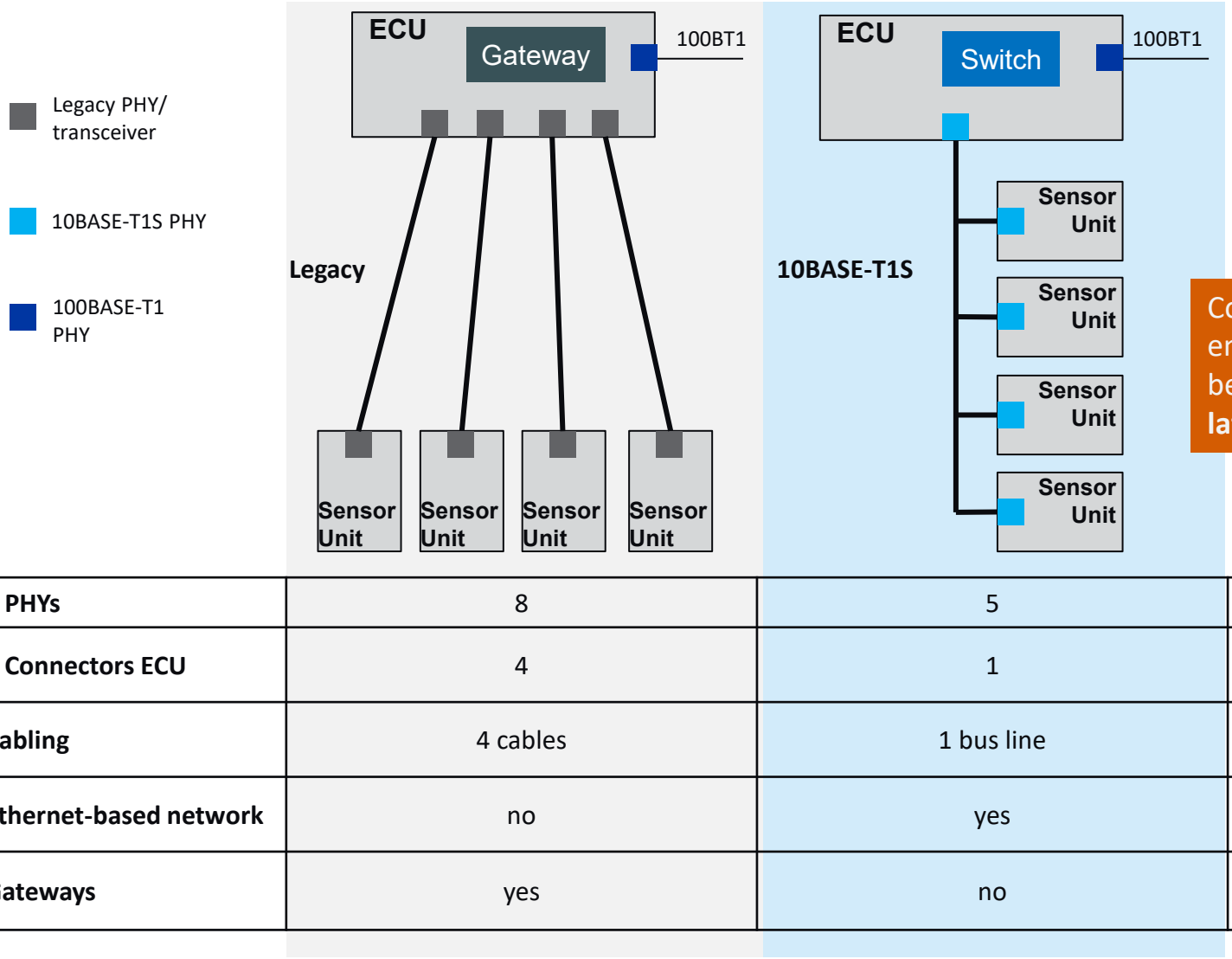
- **No Gateways**
  - Using switches instead of gateways
- **Multidrop**
  - Fewer PHYs
  - Less cables
  - Fewer switch ports
  - Simple UTP cabling



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No Gateway, Less Phys and Cables， Reduce Costs



Collision-free operation enables **deterministic** behavior with **low latency**

			Benefits of 10BASE-T1S
# PHYs	8	5	Fewer PHYs
# Connectors ECU	4	1	Fewer connectors and less connector space on ECU
Cabling	4 cables	1 bus line	Less cabling, extendibility, scalability
Ethernet-based network	no	yes	Seamless integration into overall Ethernet architecture
Gateways	yes	no	Eliminates need to translate messages

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Introduction to OPEN Alliance

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Standardization OPEN Alliance

- **TC6 (Technical Committee):**
  - SPI Protocol for MAC-PHY
  - Low pin count interface for Transceiver
- **TC10:**
  - Sleep/Wake-up
- **TC14:**
  - Compliance
  - Interoperability
  - EMC
  - Diagnosis
- **TC17:**
  - MACsec

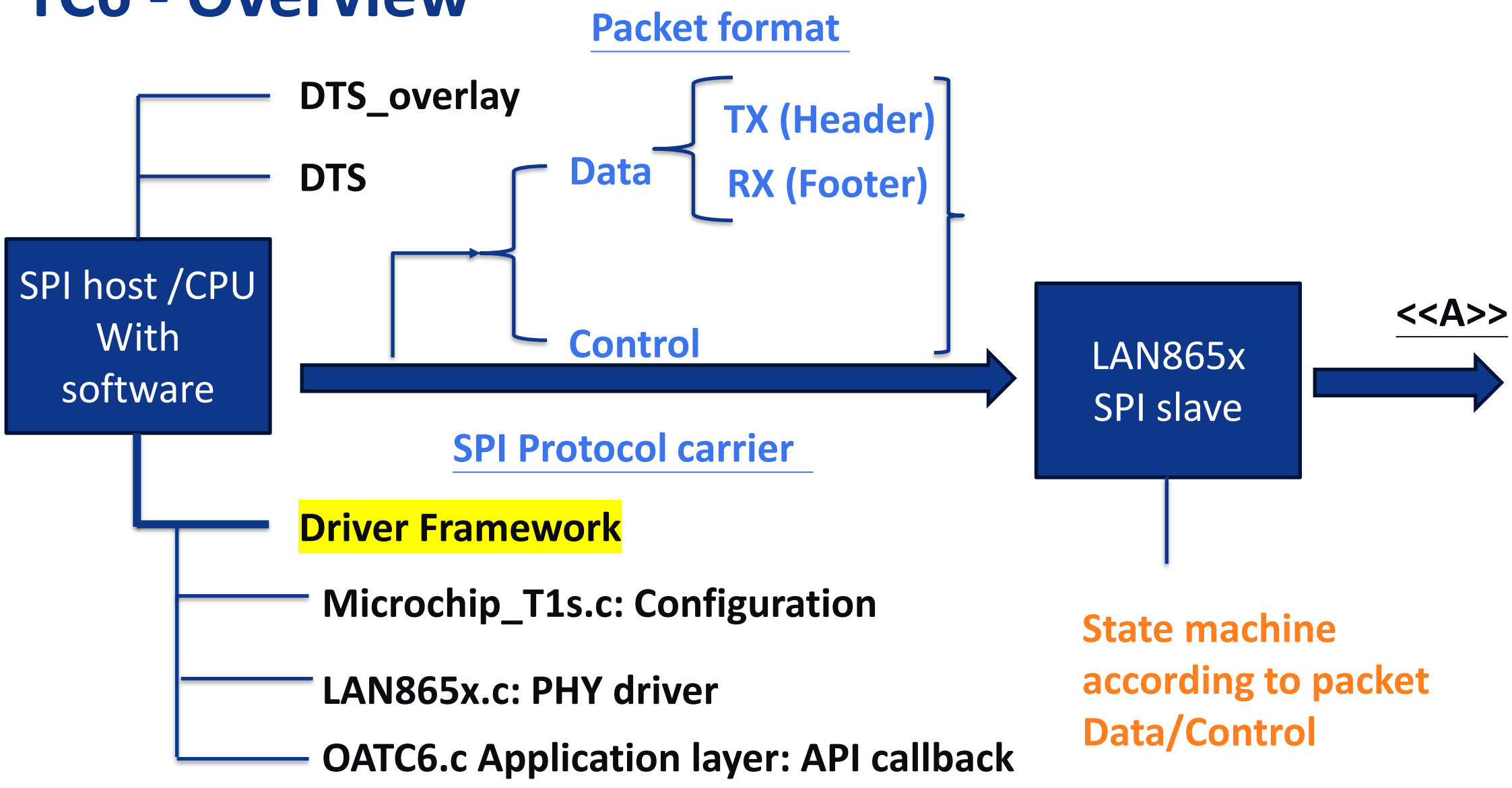
OPEN Alliance 成立於 2011 年，其理念是在蓬勃發展的汽車乙太網領域進行合作。該行業存在一個推動其形成的差距：一個透明的空間，由明確的規則管理，任何人都可以加入和參與。知識交流、市場開發和技術產業化是其支柱。但真正的基石是擺脫單一公司規範的願望。OPEN Alliance 設想了一個世界，在這個世界里，訪問這些關鍵規範將不依賴於偏袒或不透明的承諾，而是依賴於一個開放、公平和普遍可訪問的框架。通過促進透明的同行評審和非歧視性訪問，OPEN 聯盟旨在為乙太網創新真正蓬勃發展的協作未來鋪平道路

OPEN: One Pair Ethernet

小组	名称	Status
TC 1	Interoperability & Compliance Tests for 100BASE-T1 PHYs 100BASE-T1 PHY的物理层互操作性和一致性测试	on hold
TC 2	100BASE-T1 Ethernet Channel & Components 100BASE-T1 PHY的以太网通道和组件测试	on hold
TC 3	1000BASE-T1 CMC Requirements 1000BASE-T1 PHY CMC要求	rescoped
TC 4	Tools 工具	completed
TC 5	Gap Identification 差距识别	on hold
TC 6	Common Media Independent Interface Definitions for Automotive Purposes 车用通用媒体独立接口定义	in progress
TC 7	Gigabit Ethernet over Optical Fiber 千兆光纤以太网	in progress
TC 8	Automotive Ethernet ECU Test Specification 车载以太网ECU测试规范	on hold
TC 9	Automotive Ethernet Channel & Components 车载以太网通道和组件	in progress
TC 10	Automotive Ethernet Sleep/Wake-Up 车载以太网睡眠/唤醒	in progress
TC 11	Ethernet switch requirements and qualification 以太网交换机要求和资格	in progress
TC 12	Test specifications for the compliance testing of IEEE 1000BASE-T1(IEEE802.3bp, Cause 97) Physical Interface (PHY) devices 1000BASE-T1 PHY设备一致性测试规范	in progress
TC 13	New Test House Qualification Requirements 测试机构资格新要求	in progress
TC 14	Interoperability & Compliance Tests for 10BASE-T1S PHYs 10BASE-T1 PHY互操作性和一致性测试	in progress
TC 15	Multi Gig Interoperability and Compliance Tests 多千兆互操作性和一致性测试	in progress
TC 16	EEE Interoperability and Compliance EEE互操作性和一致性	in progress
TC 17	MACsec Automotive Profile MACsec汽车行业配置	in progress

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TC6 - Overview



TC10 - Key goal

- new service primitives provided by the ISO/OSI layer 1 (PHY) and supporting a controlled link shutdown and a fast global wake-up within an Ethernet network, The sleep and wake up process in a PHY shall fulfill SPEC'S timing requirement (next page
- Power consumption The following guidelines on the device power consumption in sleep mode target typical Ethernet products such as single and multiport PHYs and switches. A single-port PHY product should have a quiescence current of 35µA. A multi-port PHY or switch product should have a quiescence current of 25µA plus 10µA for each port4 .

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Pins and command about TC10

- **Pins**

Pin Name	Description
VBAT	This pin powers the sleep or wake management block.
INH	This is an open-drain output pin that goes low to disable power. During normal operation, an external resistor pulls it hight to enable power.
WAKE_IN	This is an input pin that can be used to wake up the PHY from Sleep state.
WAKE_OUT	This is an output pin that is asserted when the PHY receives a wake-up request.

- **Command**

Command Name	Description
Wake-Up Request (WUR)	This is the MDI wake-up request command sent on an active link.
Wake-Up Pulse (WUP)	This is the MDI wake-up request command sent on an inactive link.
Low-Power Sleep (LPS)	This is the MDI sleep request and acknowledge command.

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TC10 Specification / Terminology

- **Low Power Sleep (LPS)**
  - Command to indicate a sleep request to the link partner. Request transition to SLEEP state.
  - 100BASE-T1: Encoded in the IDLE scrambler stream. Sent for a minimum of 64 bits.
  - 1000BASE-T1: Sent in OAM (Operations, Administration, Maintenance) Frame.

- **Wake-Up Request (WUR), for PHY is link up case**
  - Command indicating a wake-up request to the link partner.
  - Can be sent by a node PHY or switch PHY to distribute the wake-up request over a link, which is already active.
  - 100BASE-T1: Encoded in the IDLE scrambler stream. Sent for a minimum of 64 bits.
  - 1000BASE-T1: Sent in OAM (Operations, Administration, Maintenance) Frame.

- **Wake-Up Pulse (WUP): for PHY is link down case**
  - Command indicating wake-up request to link partner. Sent when link is not active.
  - Transmitted using link training (idle) codes over the network, for a duration of 1 ms (+/- 0.3ms)

Result (both 100 and 1000 mode are PASS)

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C&S
OPEN ALLIANCE

Preliminary

P24_0286_LAN8870_1000B_TC10_Test_Report_00D_00

Date of Release: 2024-Nov-29

Test Report

Device Under Test		Customer	
Device Name	LAN8870	Order No.	P24_0286
Manufacturer	Microchip	Name	Microchip Technology Inc.
Type / Version	-	Address	80 Arkay Dr, Ste 100 11788 Hauppauge NY USA
Sample marking	LAN8870v VB000e3 241146Q		

Number of Pages	38
Test Period	from 2024-Nov-19 until 2024-Nov-28
Test Method / Test Requirement	1000BASE-T1 Interoperability Test Suite
Performed Tests and References	1000BASE-T1 Interoperability Test Suite v1.9.1 (2024-Feb-13) - TC10 Sleep/Wake-up functionality
Interoperability Test Results	The test results refer to the delivered device and the applicable test cases.
1 1000BASE-T1 Interoperability Test Suite[1]	**PHY Sleep/Wale-up Functionality: PASS**

	Link Partners		
Chapter	**RTK RTL9010AA**	**BCM 89884**	**MIC LAN8870[2]**
Group 5: Wake-up reception and signalizing	PASS	PASS	PASS
Group 6: Wake-up transmission	PASS	PASS	PASS
Group 7: Wake-up forwarding	NOT APPLICABLE[3]	NOT APPLICABLE[3]	NOT APPLICABLE[3]
Group 8: Sleep	PASS	PASS	PASS

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C&S group GmbH
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Preliminary

P24_0286_LAN8870_100B_TC10_Test_Report_00D_02

Date of Release: 2024-Nov-29

Test Report

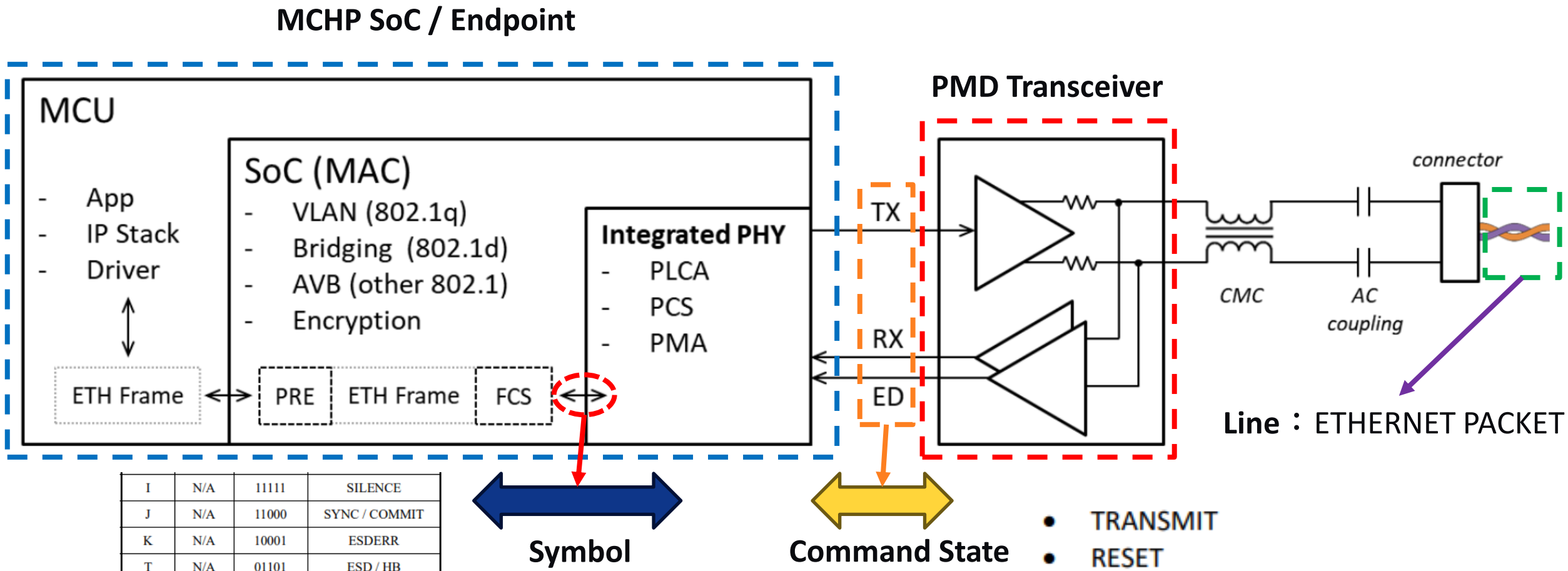
Device Under Test		Customer	
Device Name	LAN8870	Order No.	P24_0286
Manufacturer	Microchip	Name	Microchip Technology Inc.
Type / Version	-	Address	80 Arkay Dr, Ste 100 11788 Hauppauge NY USA
Sample marking	LAN8870v VB000e3 241146Q		

Number of Pages	40
Test Period	from 2024-Nov-6 until 2024-Nov-15
Test Method / Test Requirement	100BASE-T1 Interoperability Test Suite
Performed Tests and References	100BASE-T1 Interoperability Test Suite v1.2 (2024-Feb-13) - TC10 Sleep/Wake-up functionality
Interoperability Test Results	The test results refer to the delivered device and the applicable test cases.
1 100BASE-T1 Interoperability Test Suite[1]	**PHY Sleep/Wale-up Functionality: PASS**

	Link Partners			
Chapter	**RTK RTL9000AA**	**MVL 88Q1110**	**NXP TJA1101B**	**MIC LAN8870[2]**
Group 5: Wake-up reception and signalizing	PASS	PASS	PASS	PASS
Group 6: Wake-up transmission	PASS	PASS	PASS	PASS
Group 7: Wake-up forwarding	NOT APPLICABLE[3]	NOT APPLICABLE[3]	NOT APPLICABLE[3]	NOT APPLICABLE[3]
Group 8: Sleep	PASS	PASS	PASS	PASS

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TC14 - OA3P (open alliance 3 pins)



I	N/A	11111	SILENCE
J	N/A	11000	SYNC / COMMIT
K	N/A	10001	ESDERR
T	N/A	01101	ESD / HB
R	N/A	00111	ESDOK / ESDBRS
H	N/A	00100	SSD
N	N/A	01000	BEACON
S	N/A	11001	ESDJAB

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MCHP solution (SoC / Endpoint)

- **LAN8660 , LAN8661 : IO to OA3p**
  - **Control**
    - Sensors
    - Actuators
  - **Audio**
    - Microphones
    - Speakers
  - **Light**
    - Interior lights
    - Exterior lights
    - Small displays

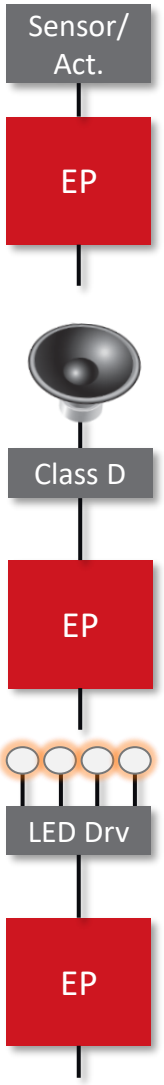
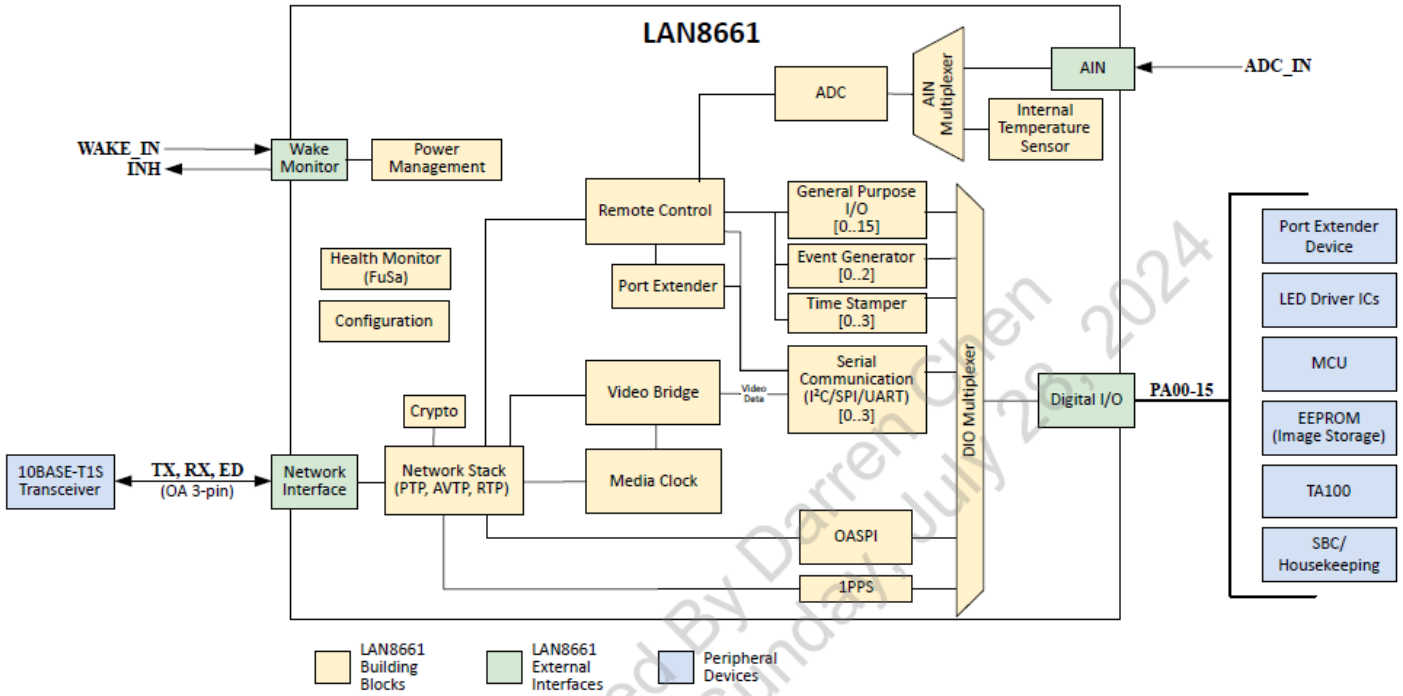


Figure 1-1. LAN8661 Block Diagram

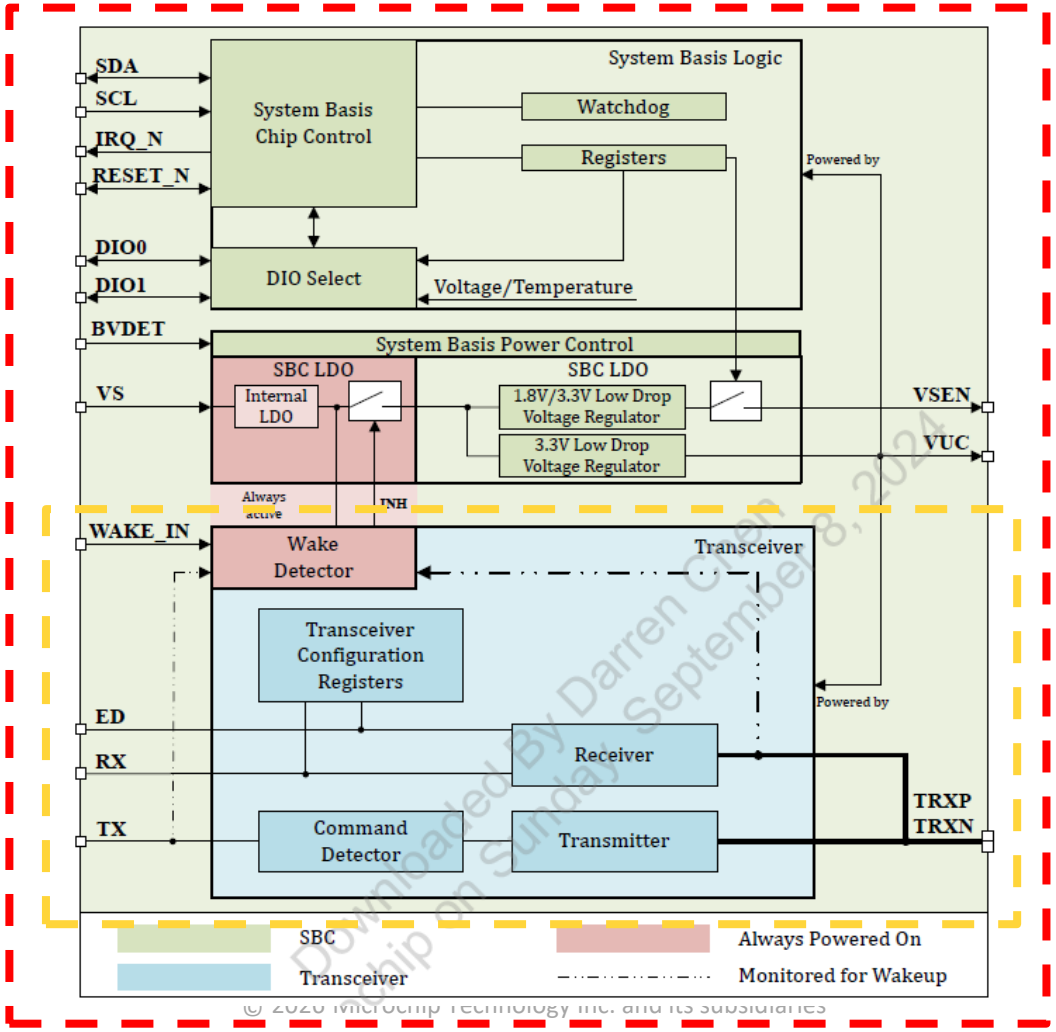


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MCHP solution (PMD Transceiver)

- **LAN8679**：**OA3p to T1S**
- **LAN8680**：**OA3p to T1S >> TC14 and I2C interface (SBC)**



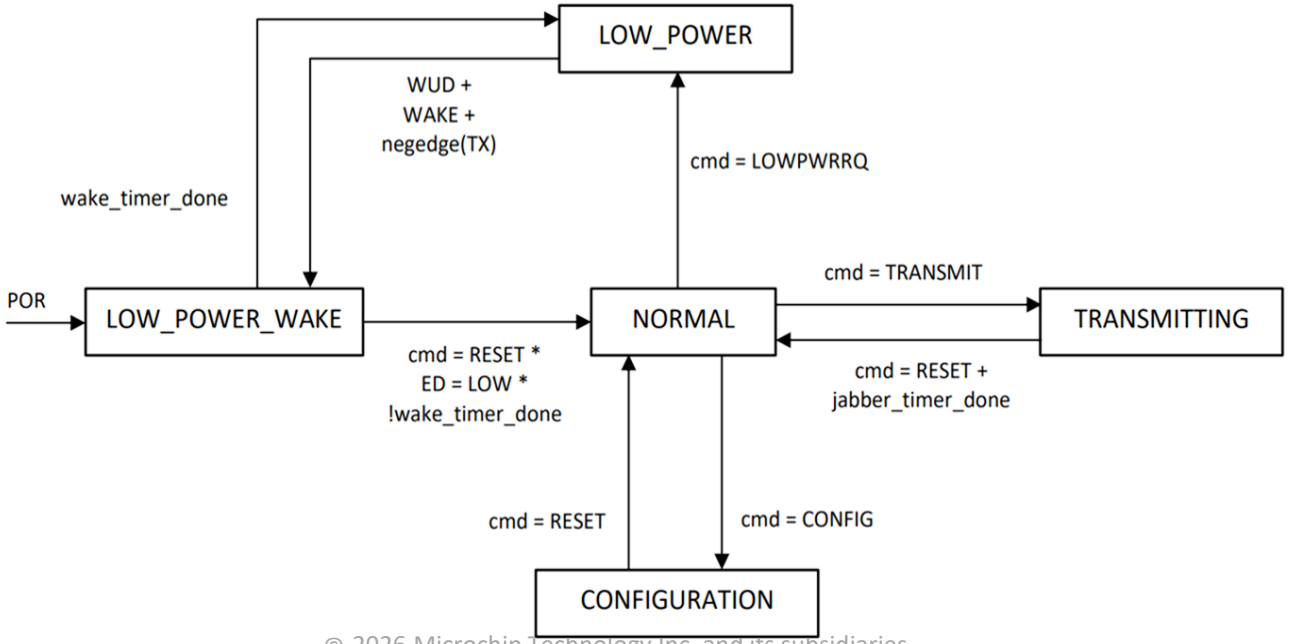
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Functional States available in Transceiver

- **The host controller uses the TX pin to send commands and activate the different function states of the transceiver. These states include the TRANSMITTING state, NORMAL state, LOW-POWER state, and CONFIGURATION state.**

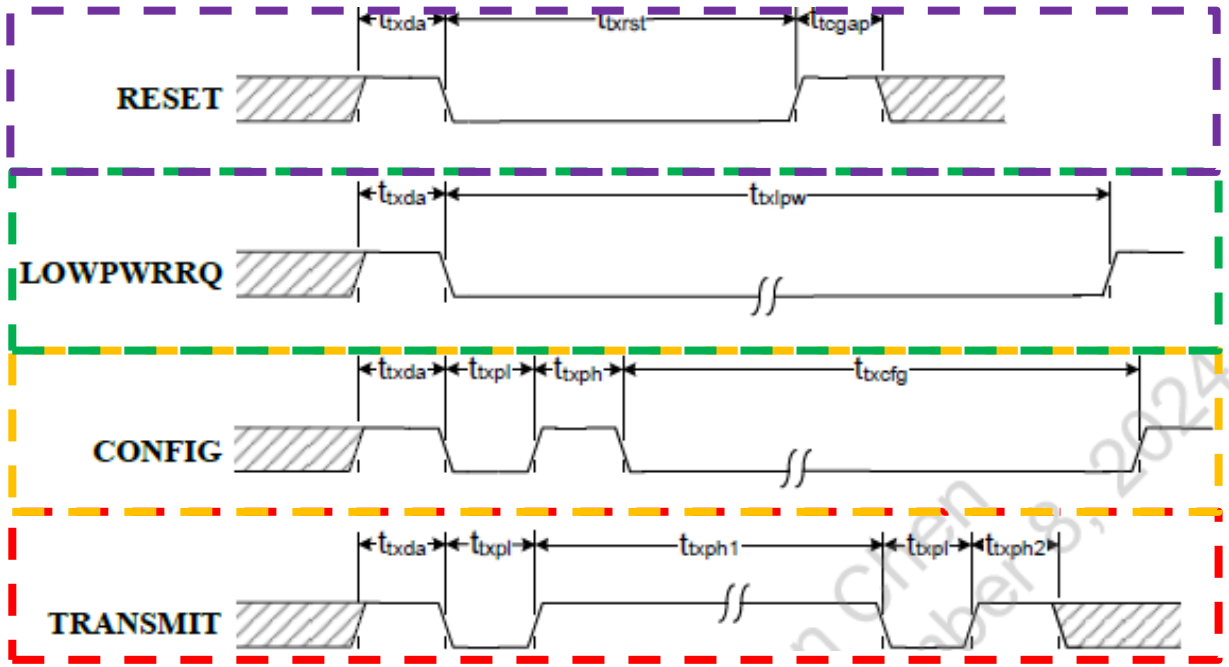
- **Instead of using a data line with a clock to transmit data and activate the functions in the transceiver, the TX pin instead sends pulses of defined length. This is done to reduce electromagnetic emissions.**



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Command timing on TX pin

- **The TX pin is a high-speed low-voltage 3.3V output to an external PMD transceiver. It encodes the transmit data and controls the PMD reset, configuration, and entering/exiting low-power states.**



Parameter	Symbol	Min	Typ	Max	Units
Multiple Commands					
Deassertion time before a command	t_{txda}	TBD	20	-	ns
Low pulse duration	t_{txpl}	TBD	20	TBD	ns
RESET Command					
RESET command assertion time	t_{txrst}	TBD	80	TBD	ns
Gap between commands	t_{tcgap}	TBD	20		ns
LOWPWRRQ Command					
LOWPWRRQ command assertion time	t_{txlpw}	TBD	16	-	µs
CONFIG Command					
High pulse duration	t_{txph}	TBD	20	TBD	ns
CONFIG command assertion time	t_{txcfg}	TBD	16	-	µs
TRANSMIT Command					
TRANSMIT command high pulse duration	t_{txph1}	TBD	180	TBD	ns
TRANSMIT end high pulse duration	t_{txph2}	TBD	20	TBD	ns

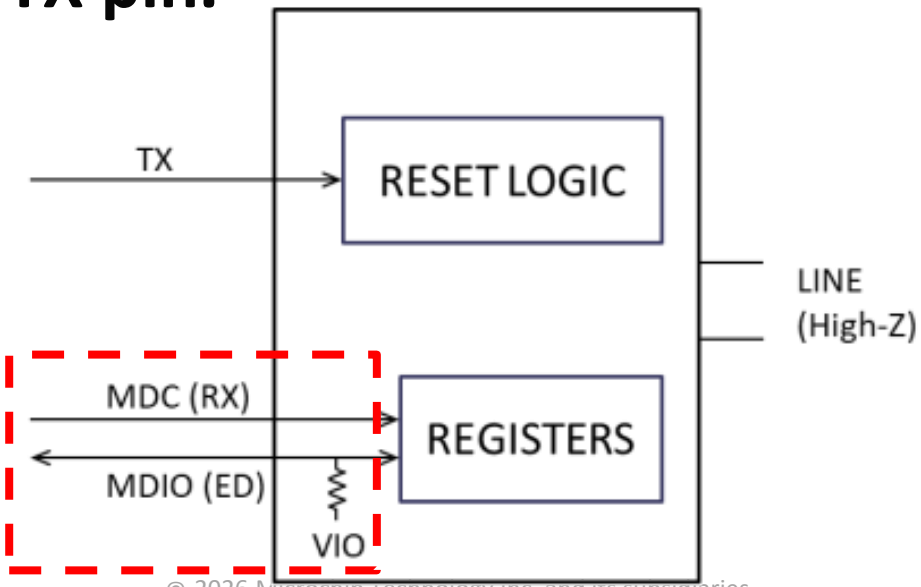
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Functional States available in Configuration

- When the PMD transceiver is set to configuration mode, the RX and ED pins are used as MII management interface (MIIM). pins are used as the MDC and MDIO pins to access configuration registers.

- During configuration mode, the transceiver does not drive any differential voltage at the line interface with low impedance, regardless of any activity on the TX pin.



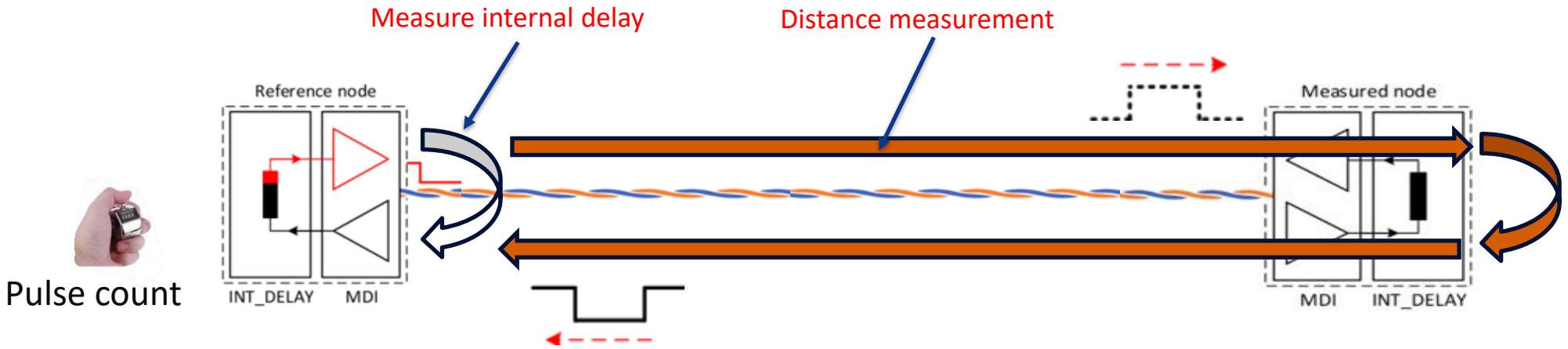
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Topology Discovery

- **TC14's topology discovery function :**
  - Automatically identify network topology:
    - In automotive Ethernet, 10BASE-T1S supports bus topology with multi-point connections. Topology discovery can help identify the physical connection relationship between nodes.
  - Diagnosis and troubleshooting:
    - Through topology discovery, the system can monitor the network structure in real time and detect and locate fault points early.
  - Improve system reliability:
    - Accurate topology information helps optimize data transmission paths, reduce latency and packet loss, and improve overall network performance.

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Topology Discovery



- **Procedure**
  - Only one Reference /Measure pair operating per time (topology configuration phase) , the rest nodes keep “listening/receive “ and PLCA suggestion to turn off during this phase
  - Enter CONFIGURATION mode by set the TPEN bit and configure the TPREFN bit in register CTRL0 and leave CONFIGURATION mode using a RESET command (for both reference (host) and measured node)
  - TX will keep generating Generate TP_pulse , this pulse will keep cycling within the loop. The refence node need keep counting how many pulse has been counted
  - “**unfiltered**” ED signal (Filtered signal will introduce delay) to calculate the pulse traveling time (Tp) between reference node and measure node at ED pin’s MEAS FSM period
  - Counting the # of “local count” as the reference (reference node loop back) :
  - Counting the # of “remote count” as the measured node : **Orange**
  - Longer distance will get more count
  - Program convert the counting # to distance
  - Normally , cable propagation delay about 5ns/m

Enabling TD in the LAN8680

Bit 1 – TPREFN Topology Discovery Reference Node select

When the PMD is configured for topology discovery operation, this bit will select which topology discovery mode the PMD operates in. When set, the PMD will function as a topology discovery measured node. When clear, the PMD will function as a topology discovery reference node. This configures the PMD topology discovery internal scrambler for the correct operation as a measured or reference topology discovery node.

Note: This bit has no effect when the Topology Discovery Enable (TPEN) bit is clear.

Value	Description
0	PMD operates as a topology discovery measured node
1	PMD operates as a topology discovery reference node

Bit 0 – TPEN Topology Discovery Enable

When set, the PMD operates in topology discovery mode.

Value	Description
0	Normal operation
1	Topology discovery mode

This does not include the setup and operation of the host.

Microchip

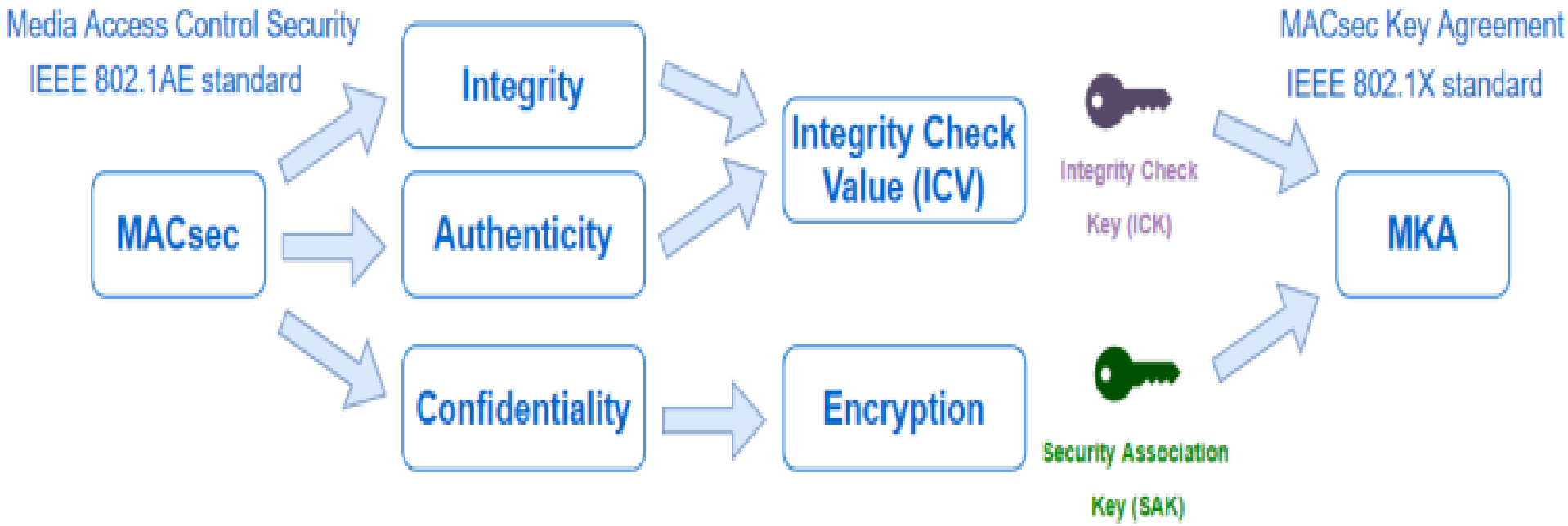
Open Alliance TC17 MACsec Auto Profile

- MACSec = Media Access Security IEEE 802.1AE
  - Point to point security protocol with Confidentiality, Integrity and Authentication
  - Transmit side Adds Security Tag (SecTag) and Integrity Check Value (ICV) while encrypting the payload
  - Receive side identifies and decrypts packets
    - Identifies packets
    - Decrypts
    - Prevents replay
    - Removes SecTag and ICV discarding invalid packets
    - All unencrypted frames dropped other than diagnostic and key agreement
- MKA can be cumbersome in automotive applications
- **Some OEM's mandating keys are stored in secure elements / HSM's with tamper protection**

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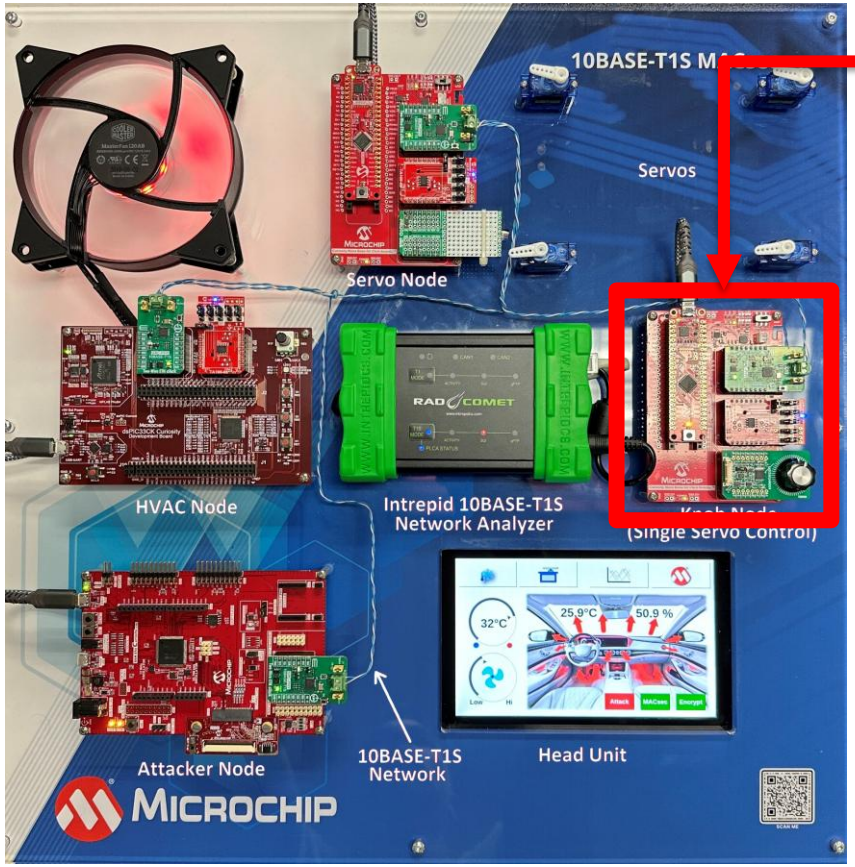
Goal

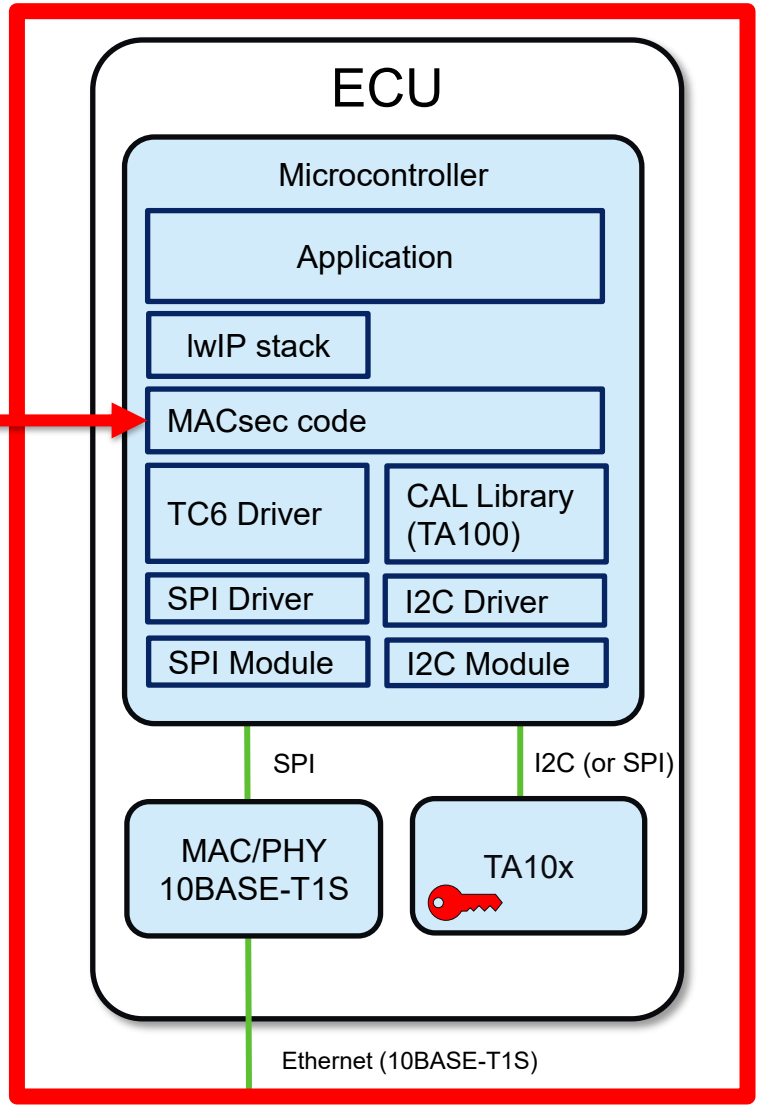
- 它通過身份認證、資料加密、完整性校驗、重播保護等功能保證乙太網數 據幀的安全性，防止設備處理有安全威脅的報文



TC17 MACSEC for automotive

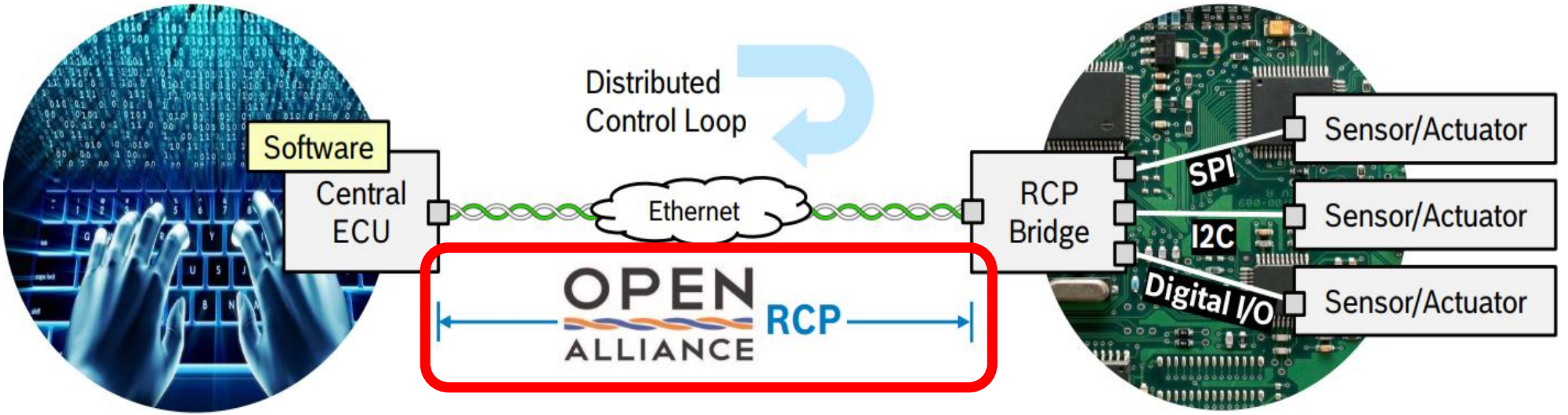
- **10M SPE :**
  - The MACSEC is implement by software suite
  - Key was loaded in the TA100
  - JIL FISP certificated

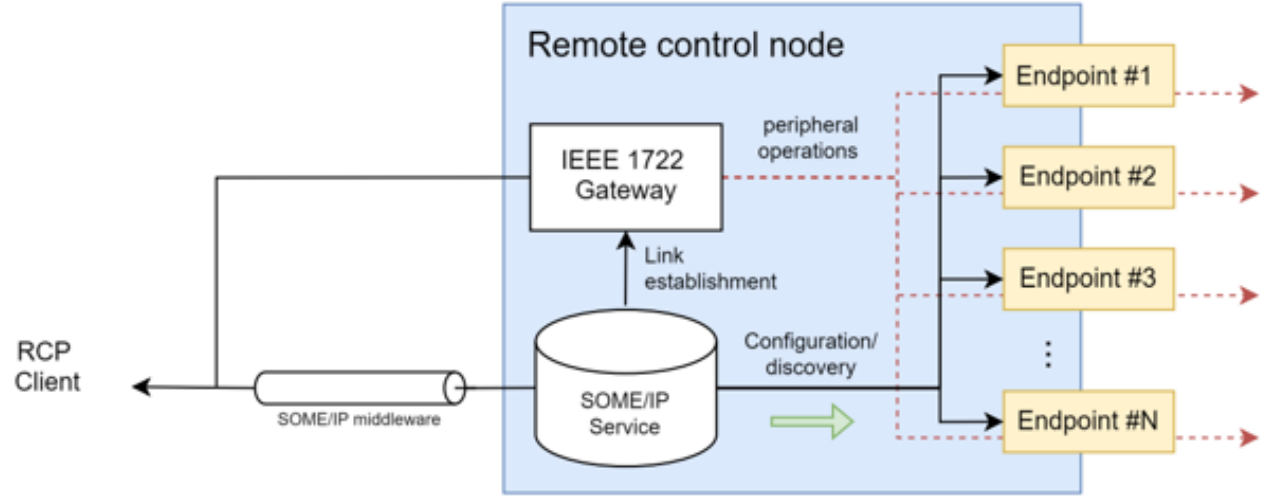




MICROCHIP

Remote Controlled Peripherals/Protocol





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MICROCHIP

10BASE-T1S Control/Lighting/Audio Endpoints

Optimized for MCU-less edge devices

- **Features**
  - Control protocol
    - SOME/IP
    - TC18 RCP
  - Streaming protocol
    - AVTP
    - UDP/RTP
  - Security / Safety
    - MACsec, E2E Profile 4, SecOC
    - External HSM TA100 (opt.)
    - Secure Configuration / Firmware Update
  - Content delivery modes(LAN8661X only)
    - Video streaming
    - Edge Node Rendering (graphic commands)
    - Play pre-stored graphics, videos
  - gPTP Slave
  - PDM to PCM conversion (LAN8662X only)
  - External MCU via I2C or SPI (optional)
  - ISO26262 (SEooC ASIL-B)
  - Temperature Grade 1

Control/Lighting/Audio

Available Features	LAN8660X	LAN8661X	LAN8662X
SOME/IP	✓	✓	✓
RCP	✓	✓	✓
OPEN Alliance TC10/14 Wake/Sleep	✓	✓	✓
gPTP	✓	✓	✓
PWM Interface	✓	✓	—
AVTP	—	✓	✓
RTP	—	✓	✓
Video Streaming and LED Driver IC Control	—	✓	—
Audio Interfaces	—	—	✓
CAN FD Controller	✓	✓	—
SERCOMs	Up to 4	Up to 4	Up to 3
GPIOs	Up to 16	Up to 16	Up to 12
ADC Channels	1	1	1

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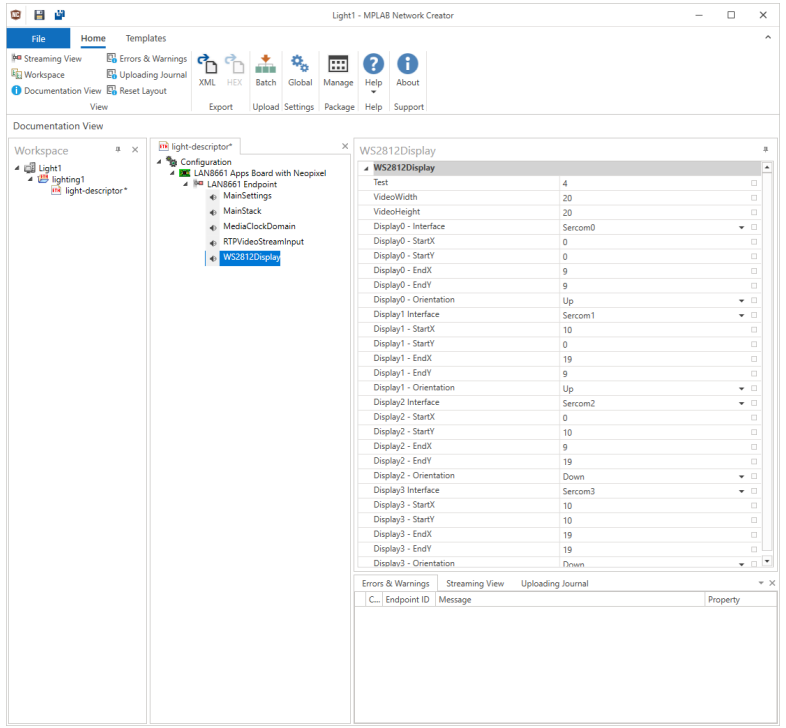
MICROCHIP

RCP

Remote-
Control-
Client

MCU less

End point configurator



RCP Client

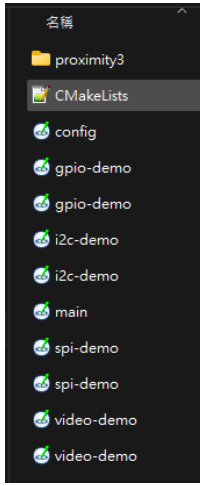
T1S

RCP Server 8680

866X

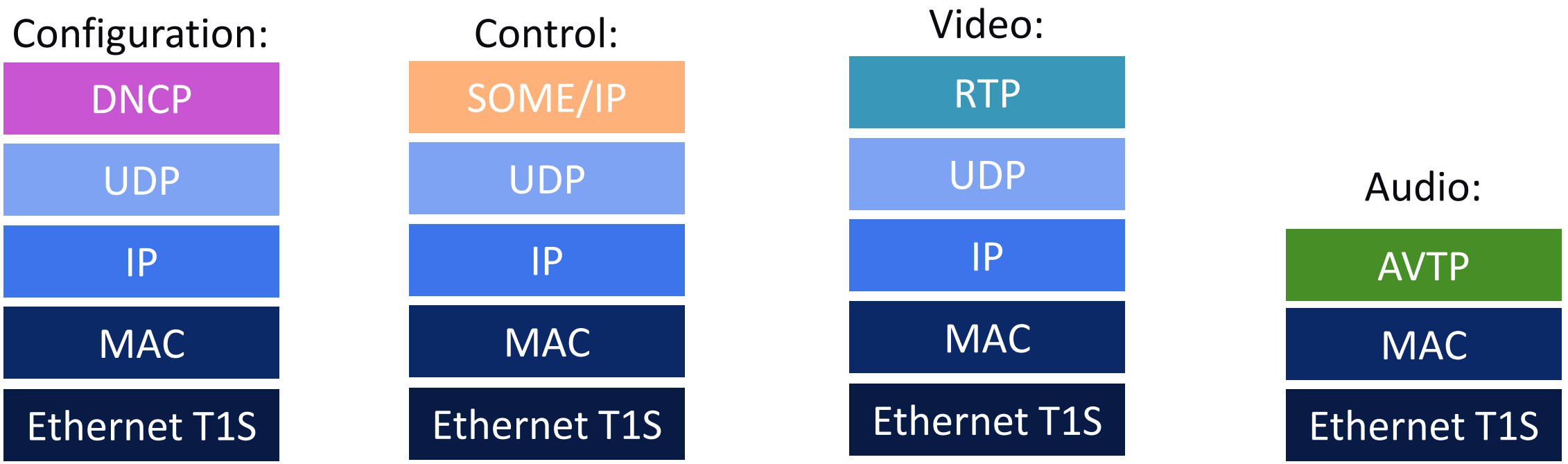
IO
Audio
LED
SPI

Software data flow



MICROCHIP

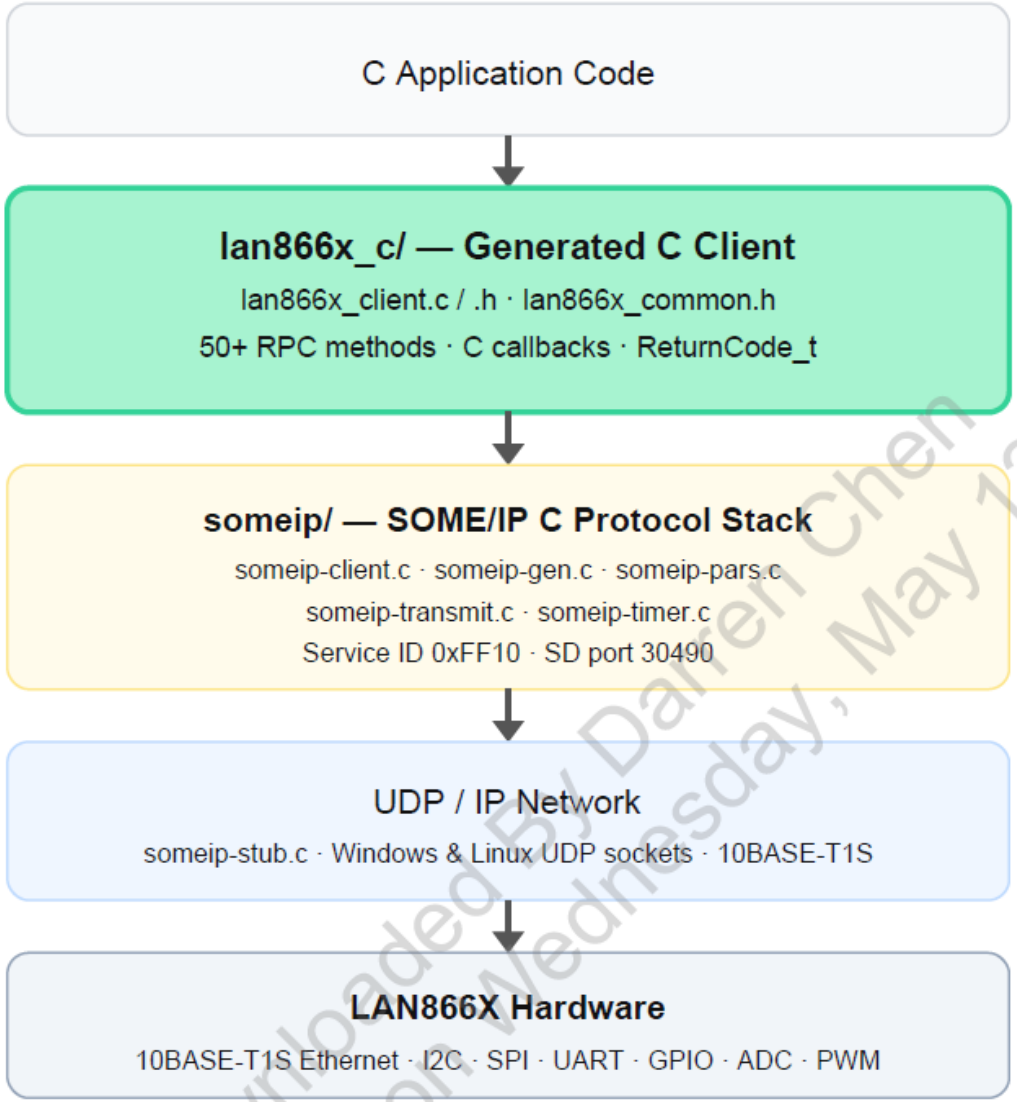
LAN866x Protocols



confidential

MICROCHIP

Client Tools



We support multiple tools

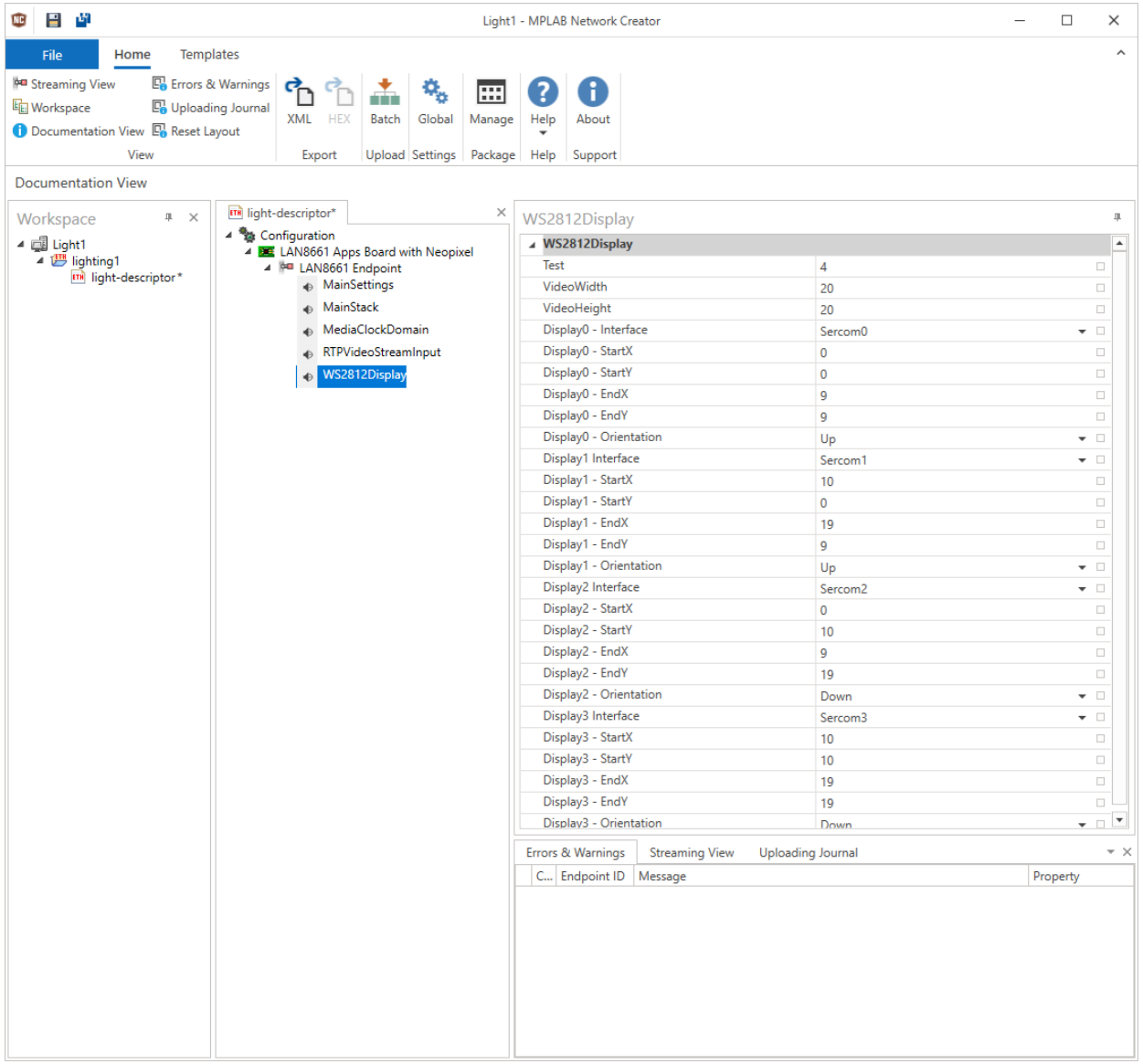
Folder	Content
generator/	Code generator: lan866x.proto, Jinja2 templates, generate-lan866x.{bat,sh}, Doxyfile, version-sync helper.
lan866x_c/	Generated C client (lan866x_client.c/.h + lan866x_common.h) with C examples.
lan866x_cpp/	Generated C++ client with C++20 examples.
lan866x_python/	Python client (pybind11 bindings + wrappers), prebuilt Windows wheels, examples.
lan866x_csharp/	.NET 8 C# client, NuGet package, examples.
lan866x_java/	Java 11 client, JNI shim, prebuilt Windows JAR, examples.
lan866x_rust/	Rust client, FFI bindings, prebuilt Windows DLL, examples.
lan866x_blockly/	Drag-and-drop Blockly frontend for the Python client.
lan866x_arxml/	Generated AUTOSAR XML (lan866x.arxml).
lan866x_wireshark/	Wireshark SOME/IP dissector config files.
lan866x_doxygen-cpp/	Generated Doxygen HTML for the C++ API.
someip/	Git submodule: the SOME/IP protocol stack.
tools/	Developer utilities (ARXML validator, CA bundle maker).
docs/	Architecture SVGs, design documents, specifications.

Uploaded By Darren Chen On Wednesday, May 13, 2026
Downloaded By Darren Chen @ Microchip On Wednesday, May 13, 2026

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Endpoint Configuration

- **MPLAB Network Creator**
  - SAME GUI for config PHYs, Switches, Endpoints
  - Access to all available parameters
  - Selection of Peripheral Modules
  - Output of configuration
    - Config file for End-Of-Line programming
    - MDI/network (e.g. during OTA or in repair shop)

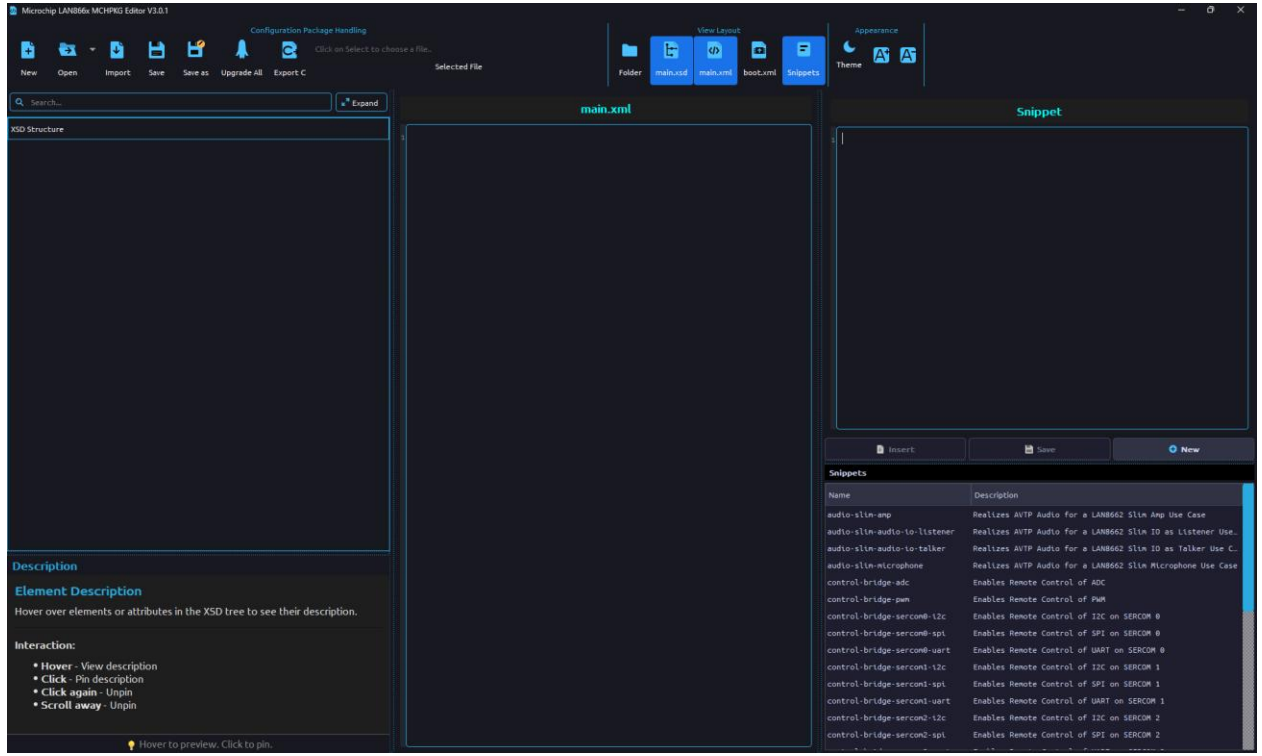


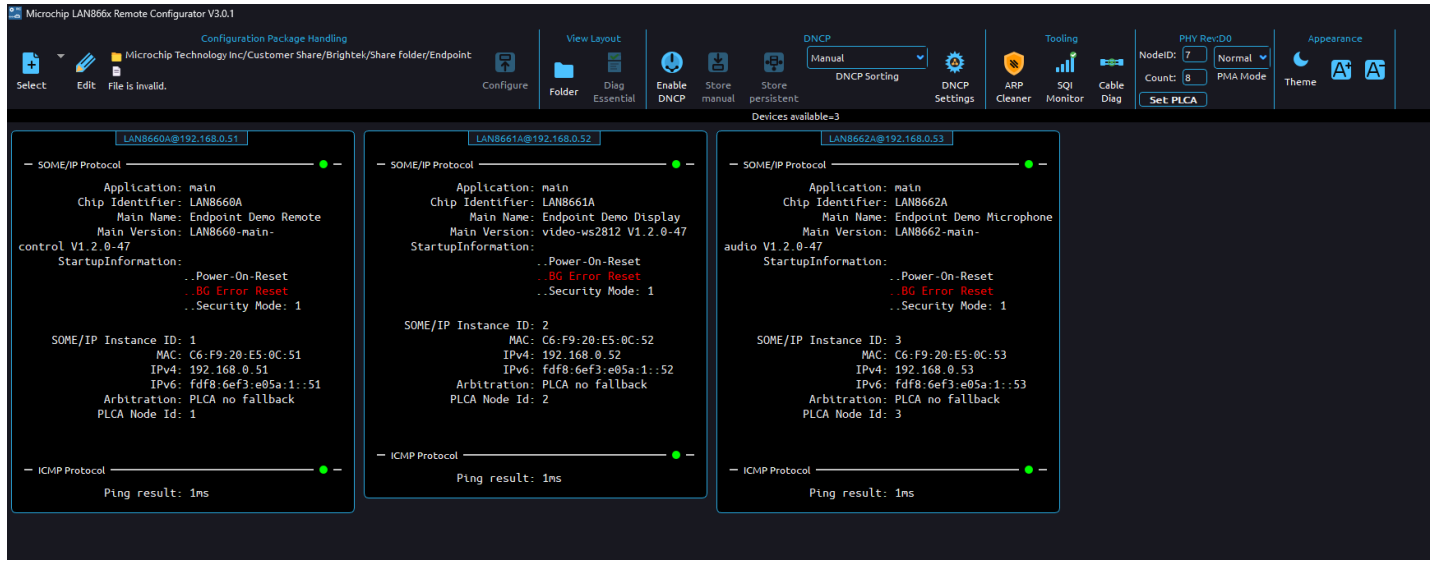
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Remote Configurator

GUI:

- Configure over Network
- Uses config file from
- MPLAB Network Creator
- Display found EPs at once
- List all parameters
- Send to sleep / wakeup
- Windows / Linux support

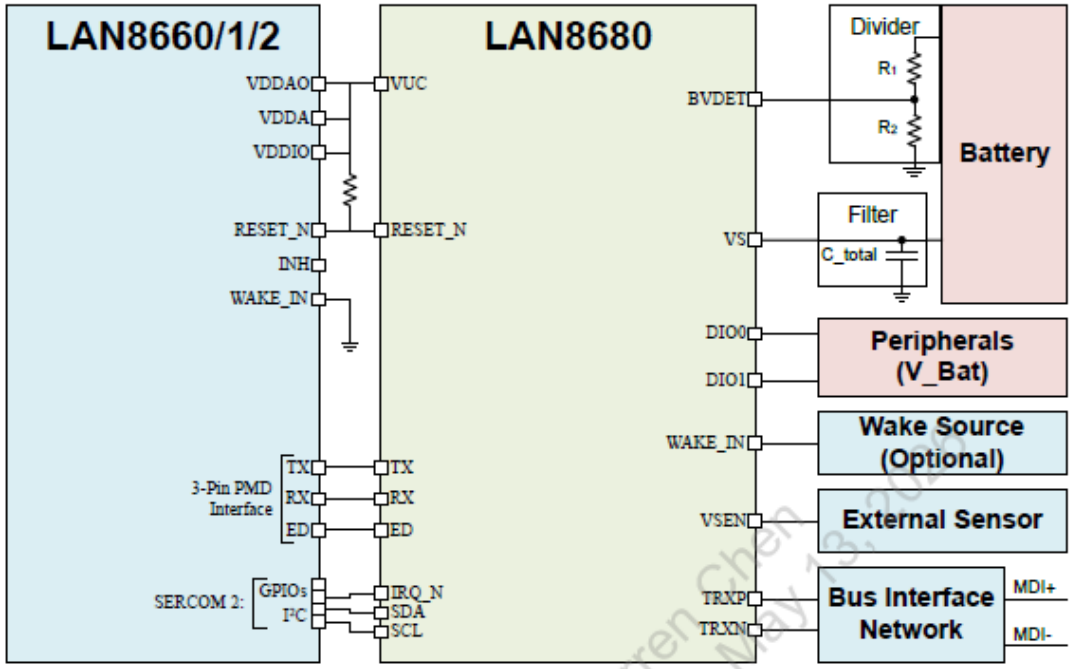


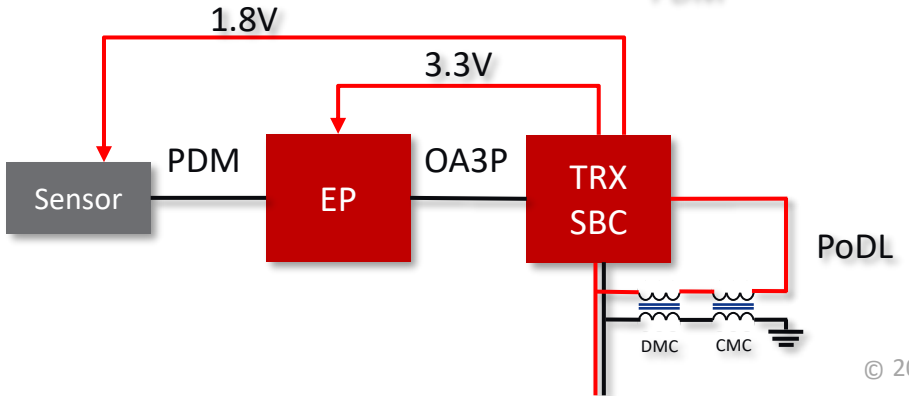


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Microchip solutions

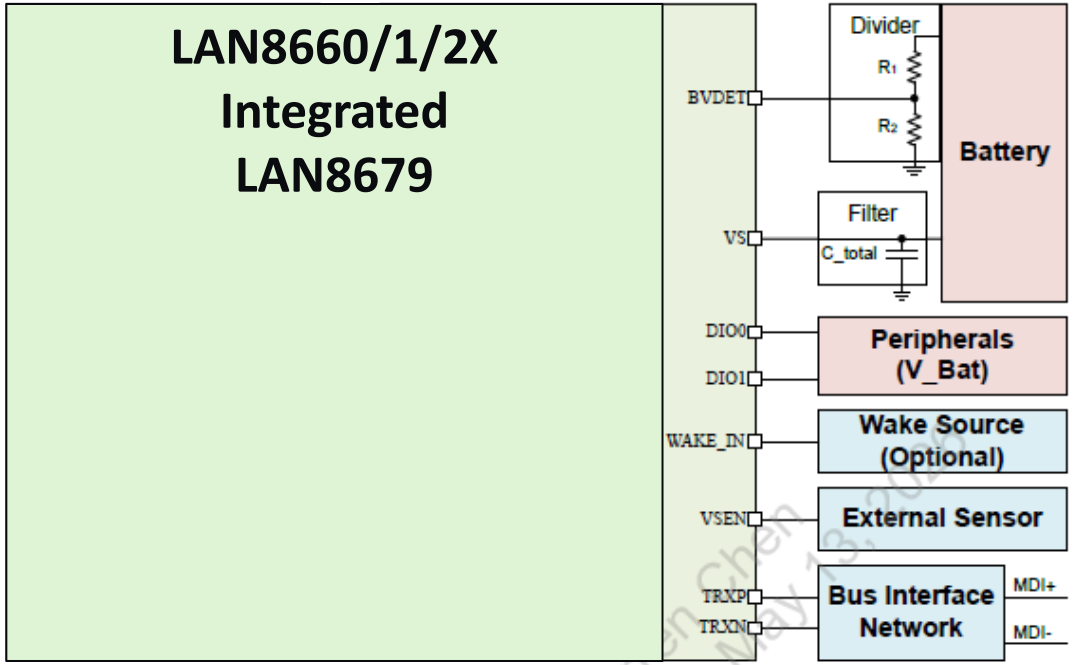
Endpoint + PMD Transceiver

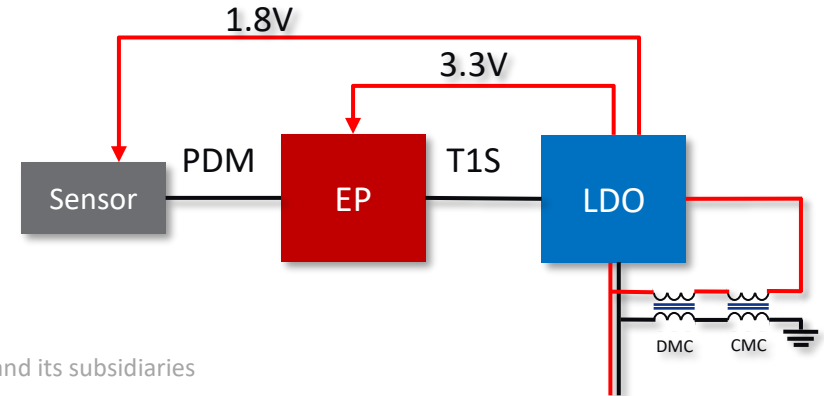




PDM

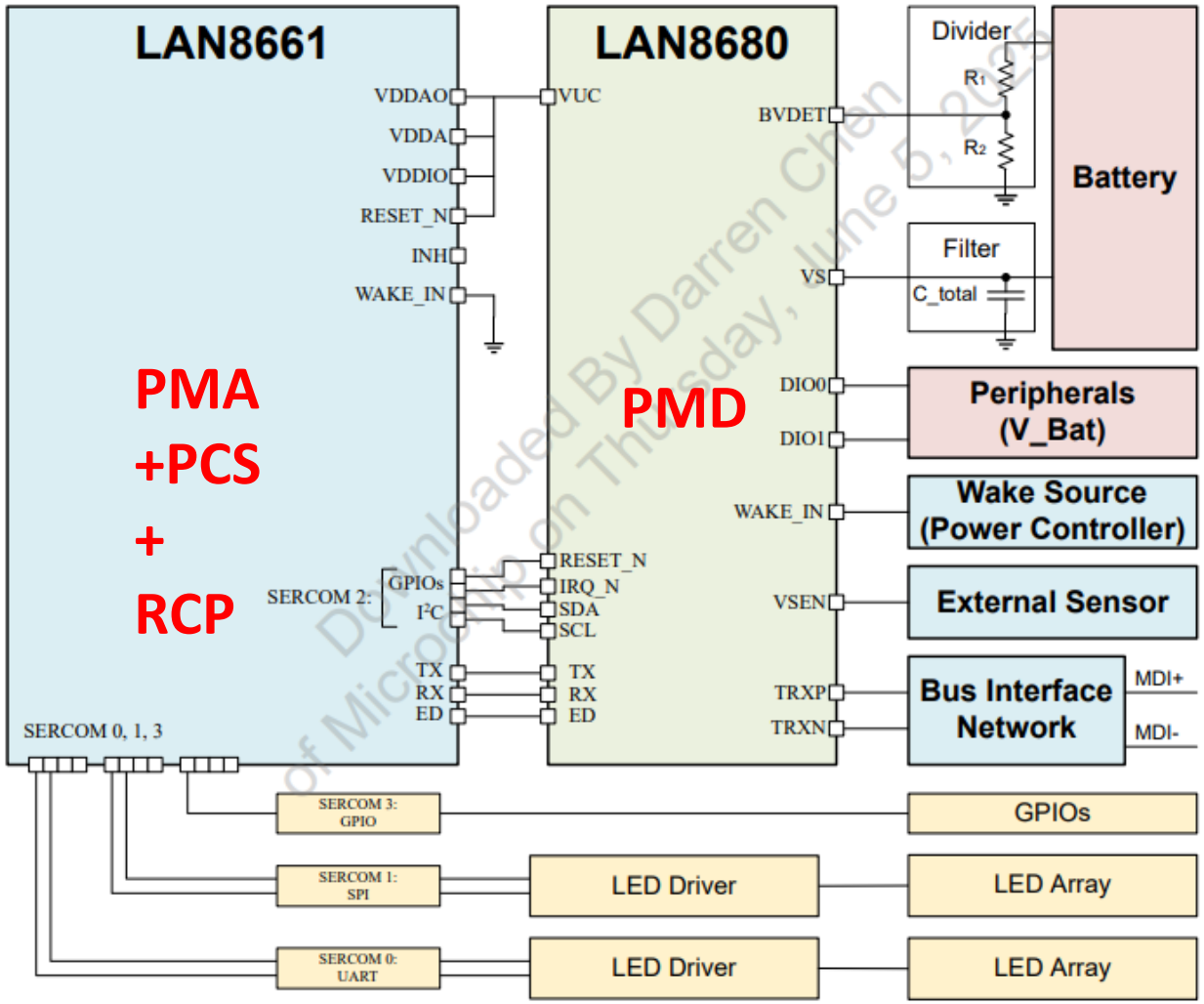
Endpoint Integrated PMD Transceiver



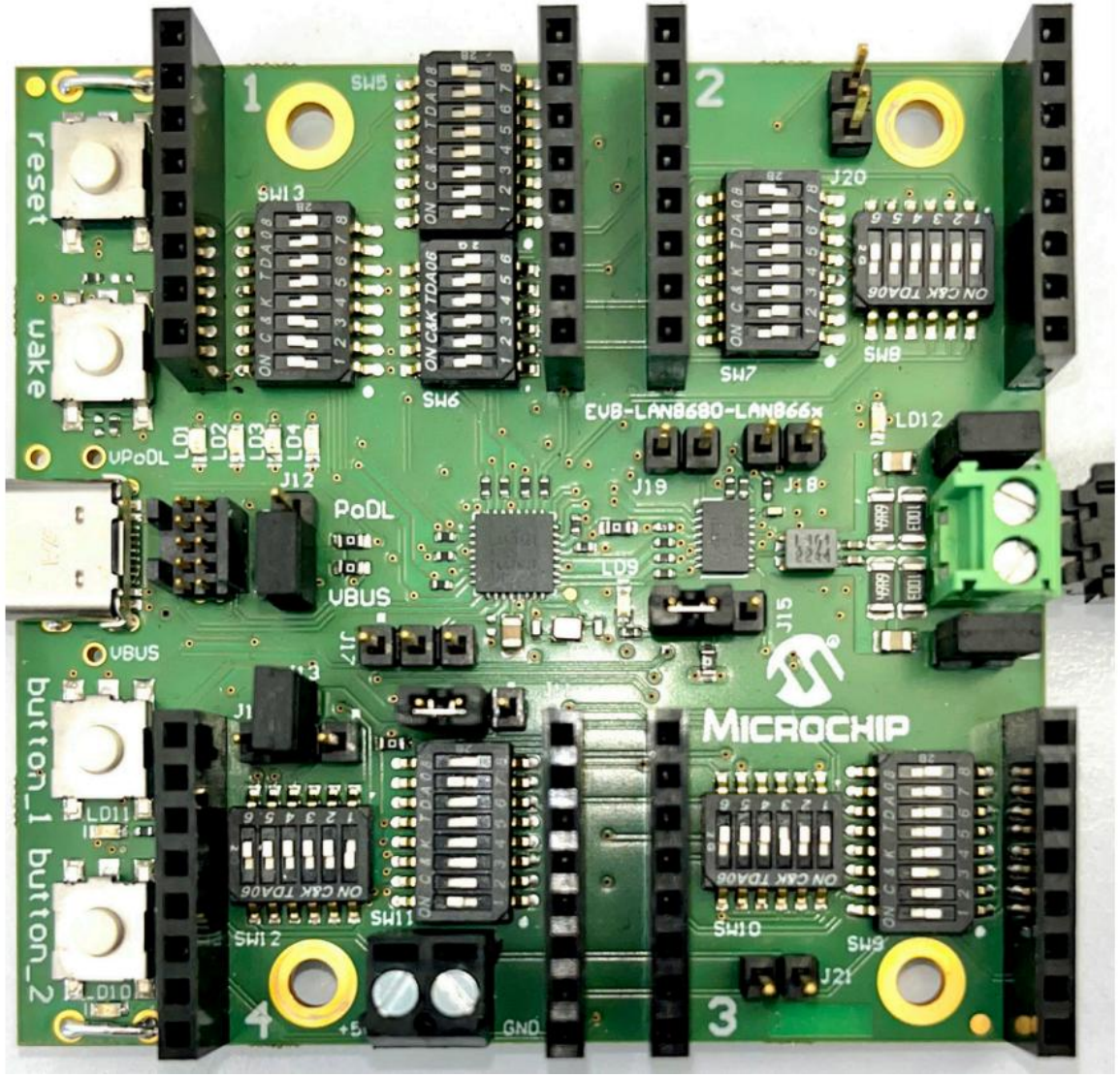


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MCHP RCP solution



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MICROCHIP

Introduction to T1S Application

Evolving In Vehicle networking

Microchip's Long-Term Vision for In-Vehicle Networking (IVN)

Today's Automotive Networking Landscape…

CAN

FPD LINK

APIX®

GMSL

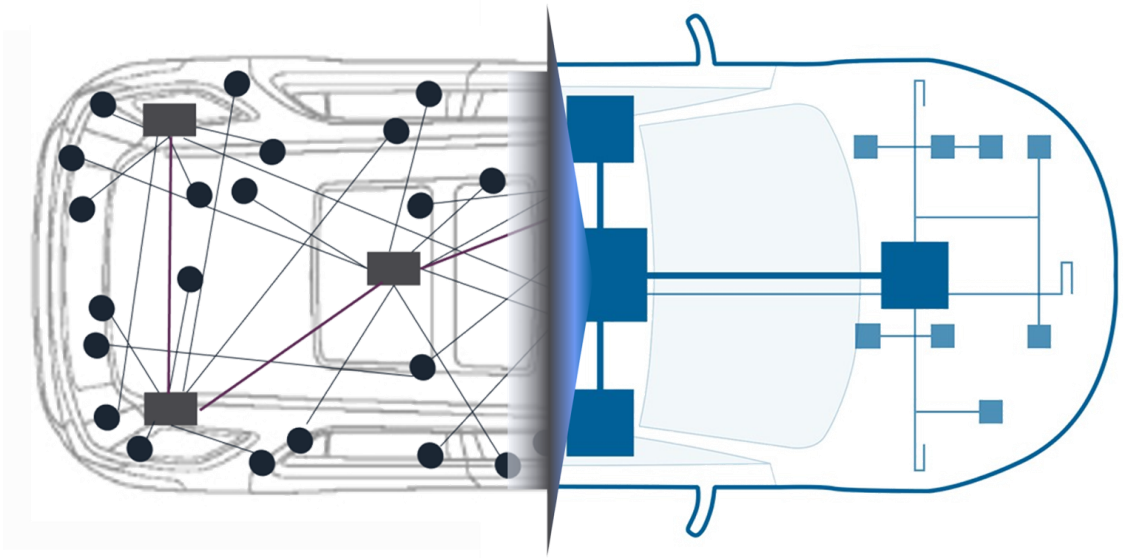
MOST®

CoaXPress®

A2B®

FlexRay™

lin LOCAL INTERCONNECT NETWORK



Future Automotive Networking Landscape…

Low Speed & Backbone

OPEN ALLIANCE *Ethernet*

HPC & Storage

PCI EXPRESS®

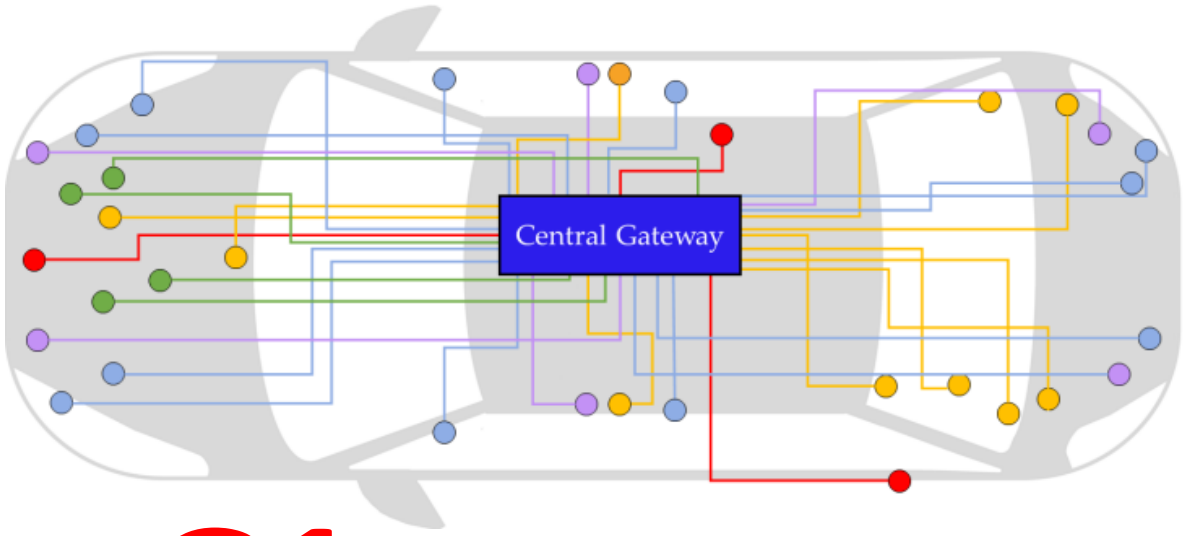
Camera & Display

ASA

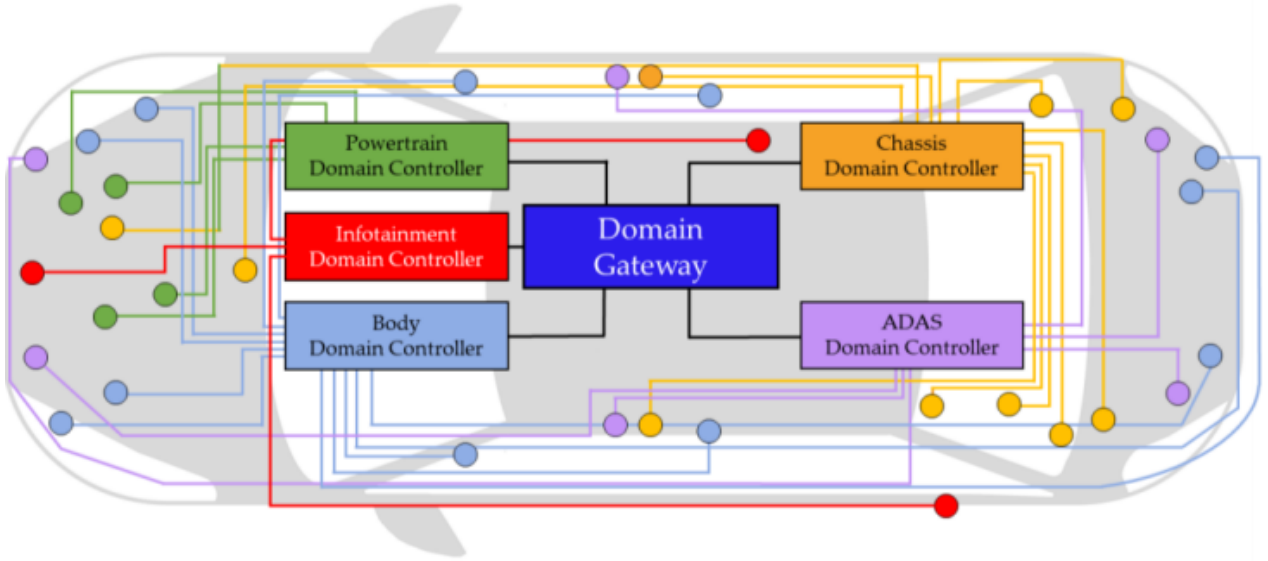
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Generations of ECU connections

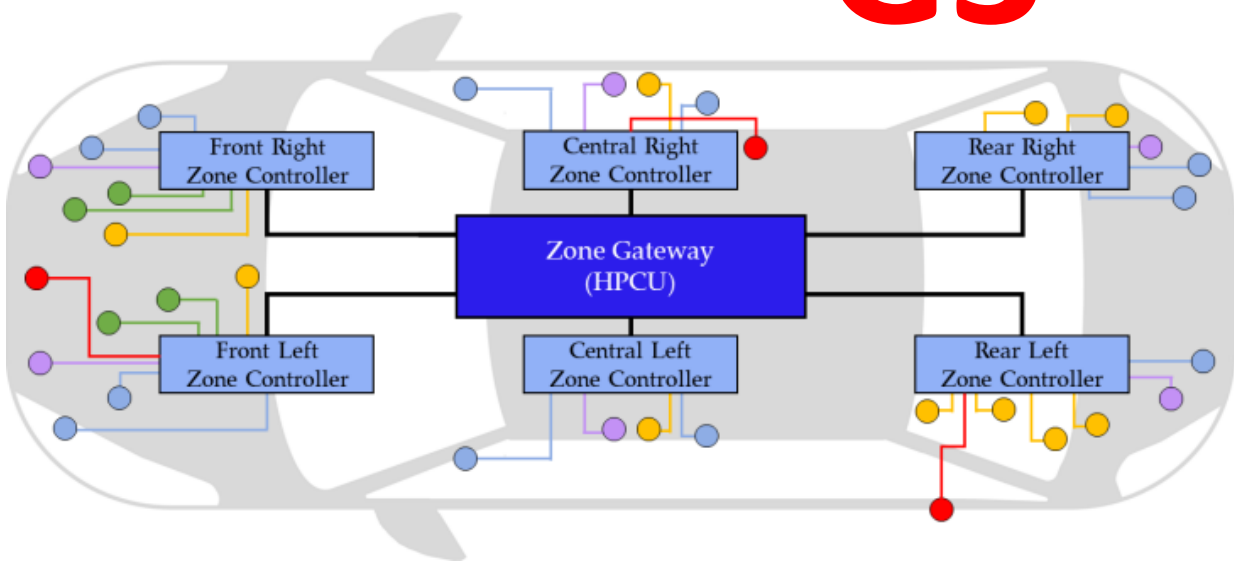


G1



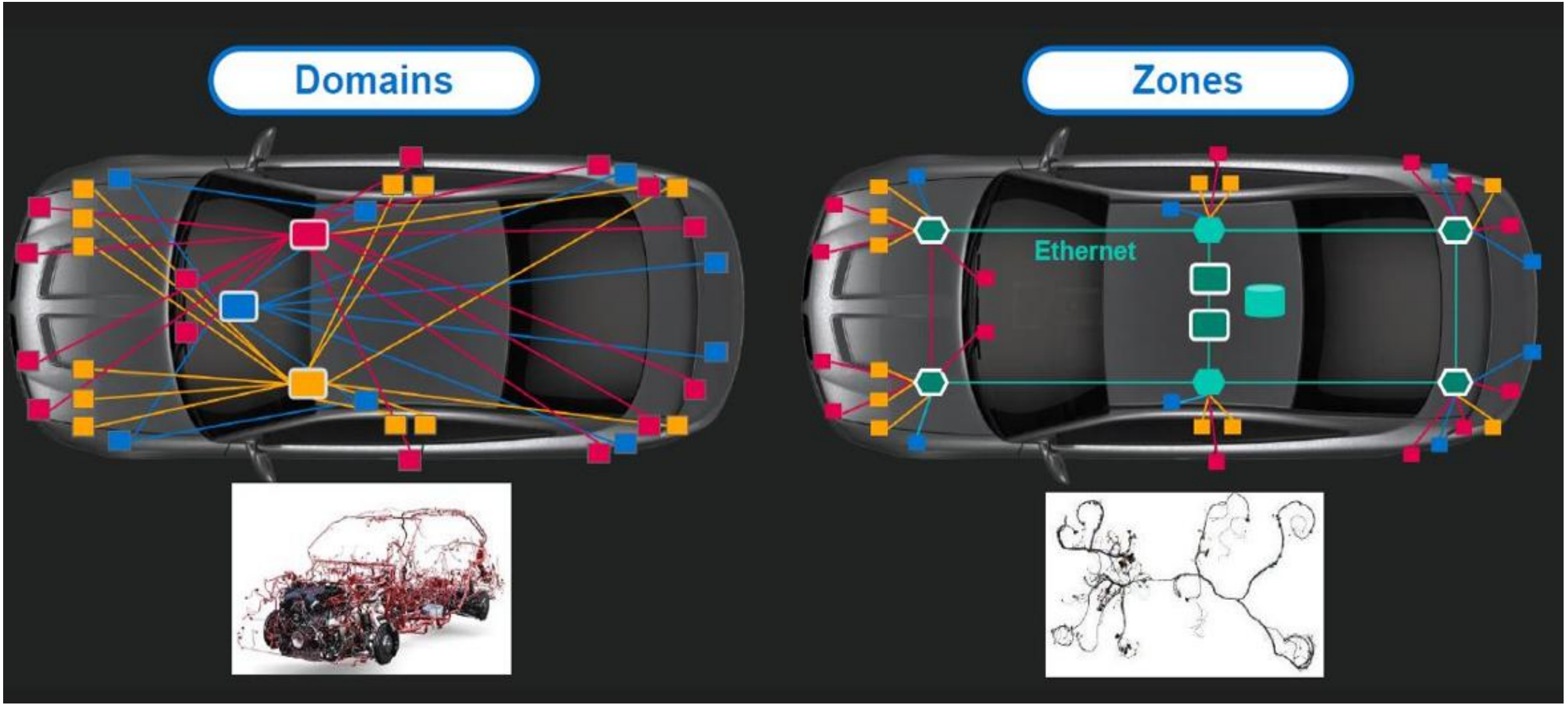
G2

G3

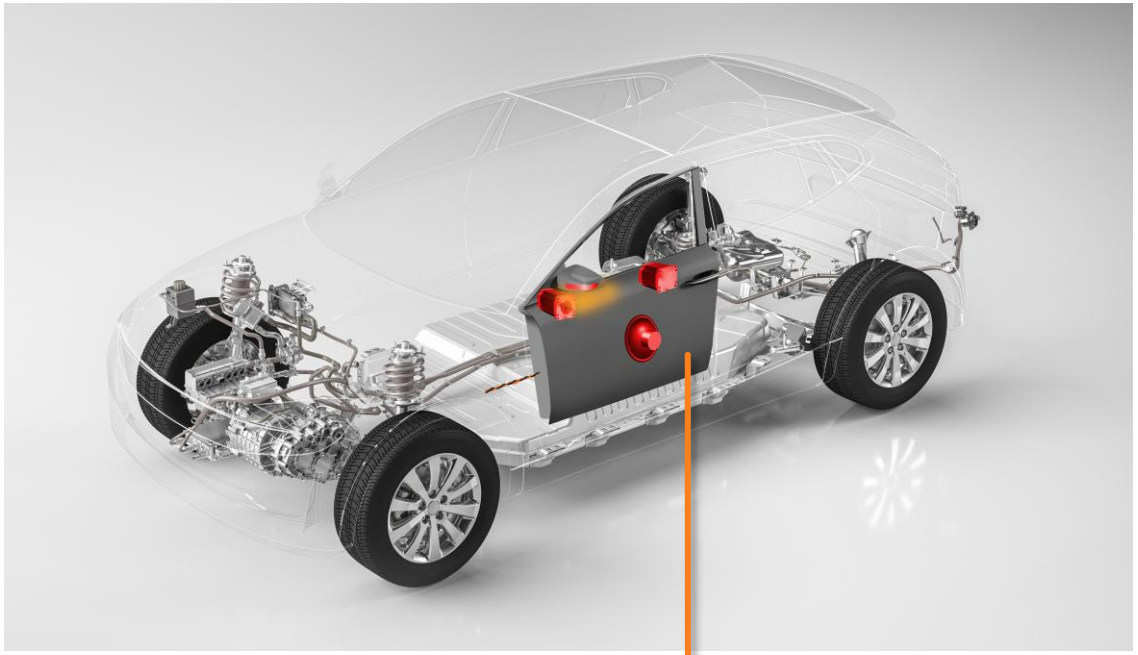


MICROCHIP

Saving in cable and harness



Automotive Zone Architecture



10BASE-T1S bus: Multiple applications on a single cable!

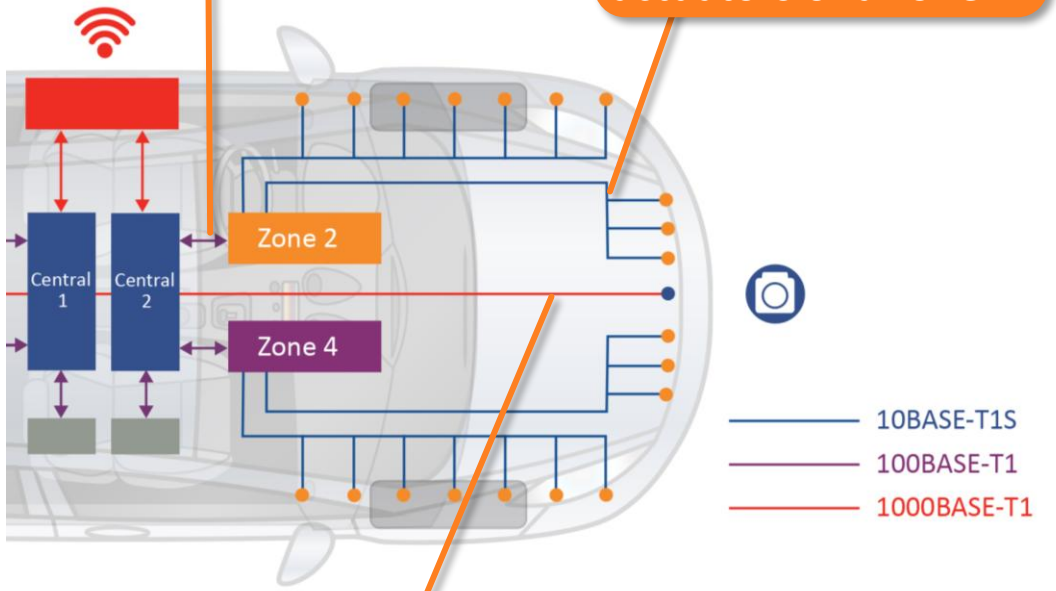
Example: Door Zone

- **Window lifter**
- **Mirror control**
- **Speakers**
- **Lock**
- **Ambient/interior light**

Typical Zone Architecture using All-Ethernet

100/1000BASE-T1 connects zone and central computer

10BASE-T1S connects sensors and actuators of a zone

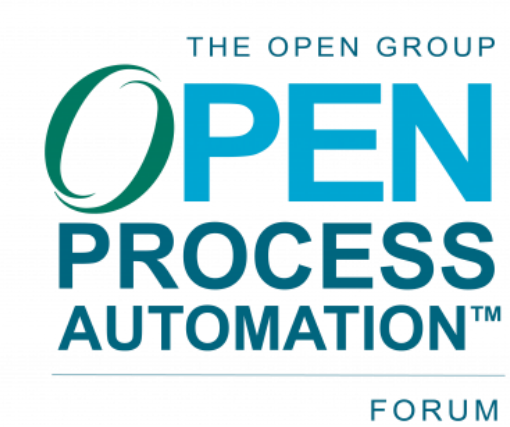


NGAUTO-T1 backbone connects several central computers and maybe cameras

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DCS (Distributed control system)

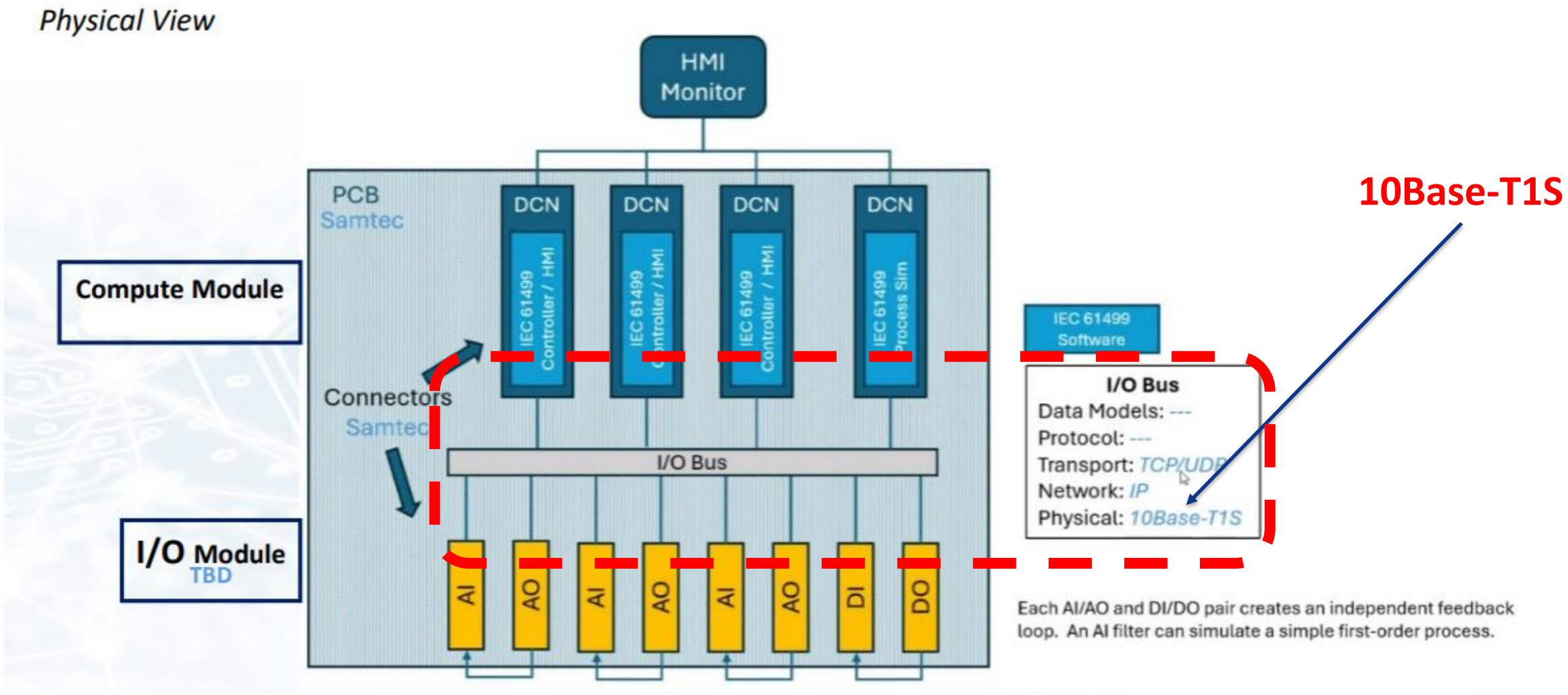




Schneider Electric, Intel, and Red Hat explore modern DCSs

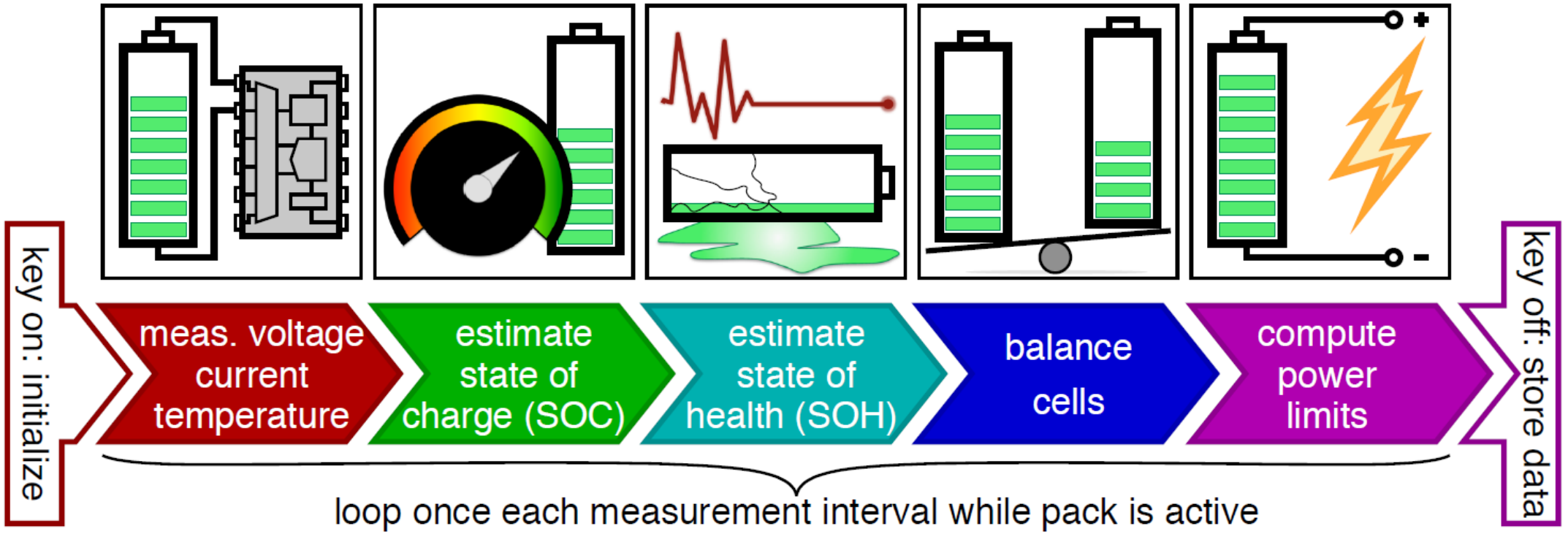
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DCN : field terminal & controller connection



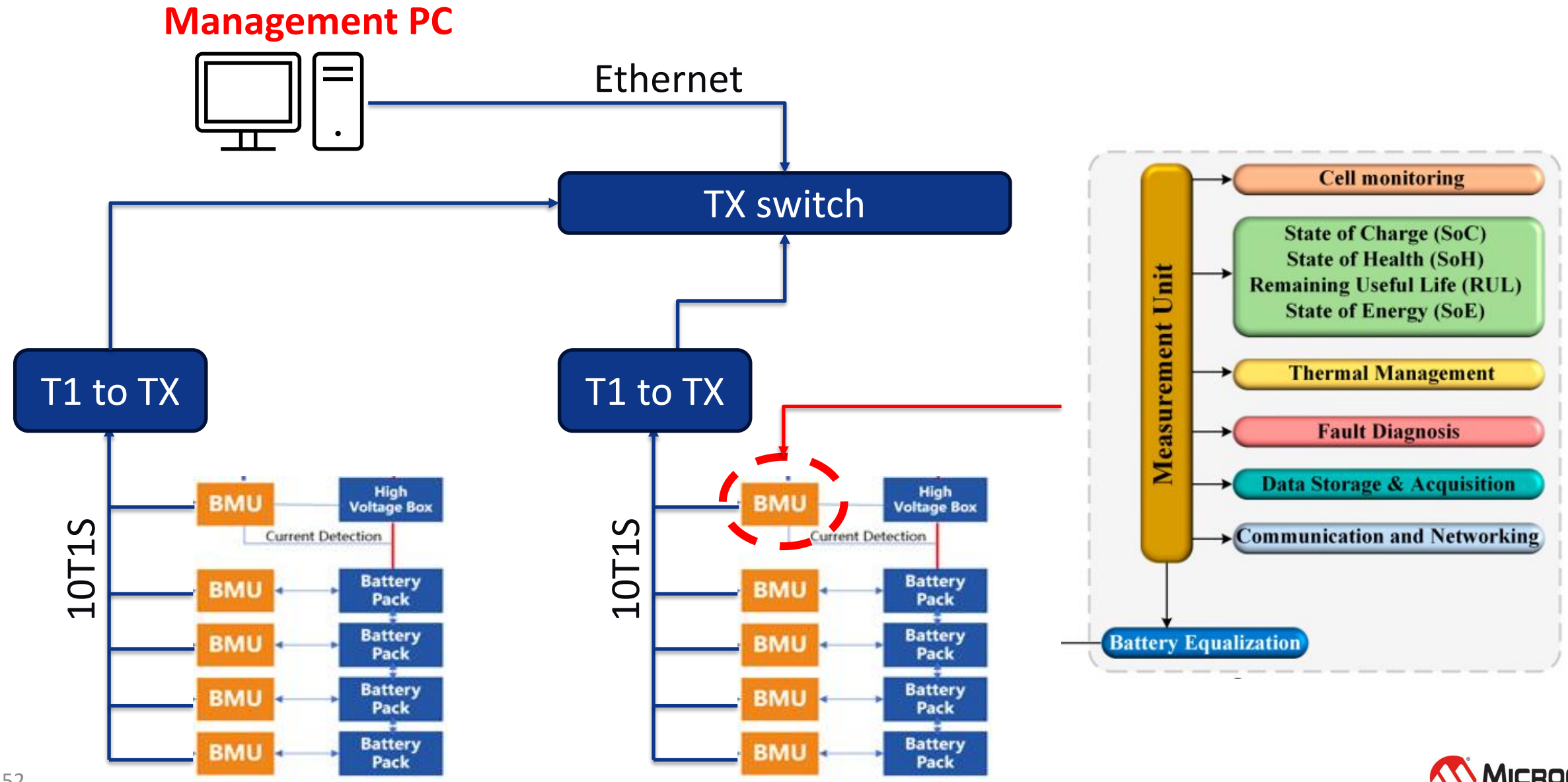
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Software flow of a BMS



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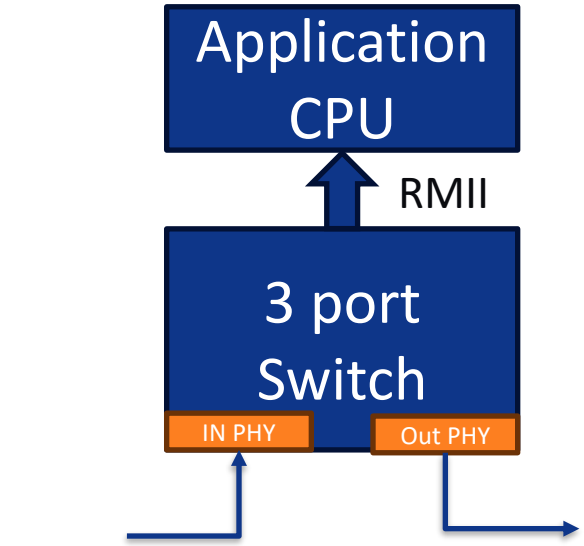
BMU based EMS (communication)



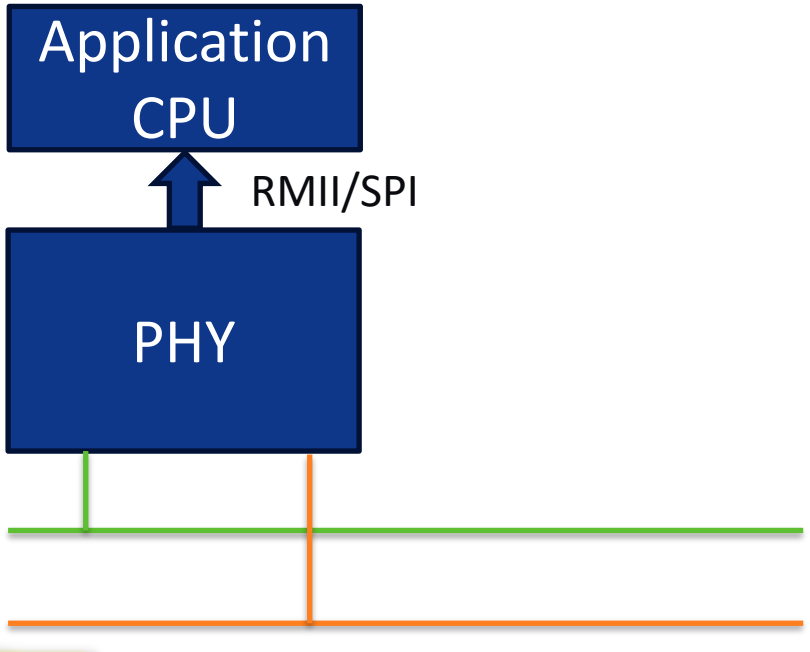
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Daisy chain replacement

3 port switch implement



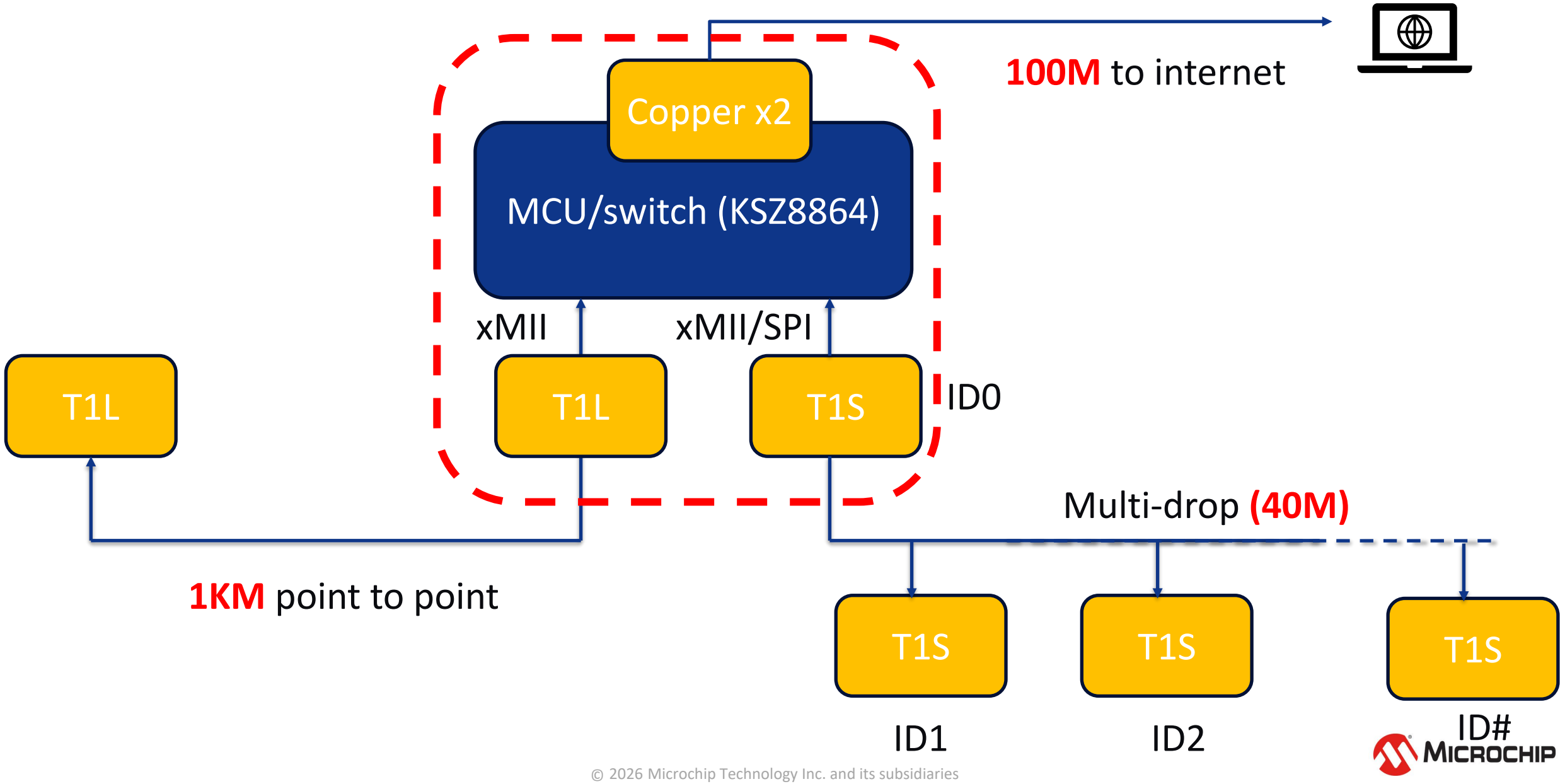
10Base-T1S PHY implement



Less cost

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Full range process automation

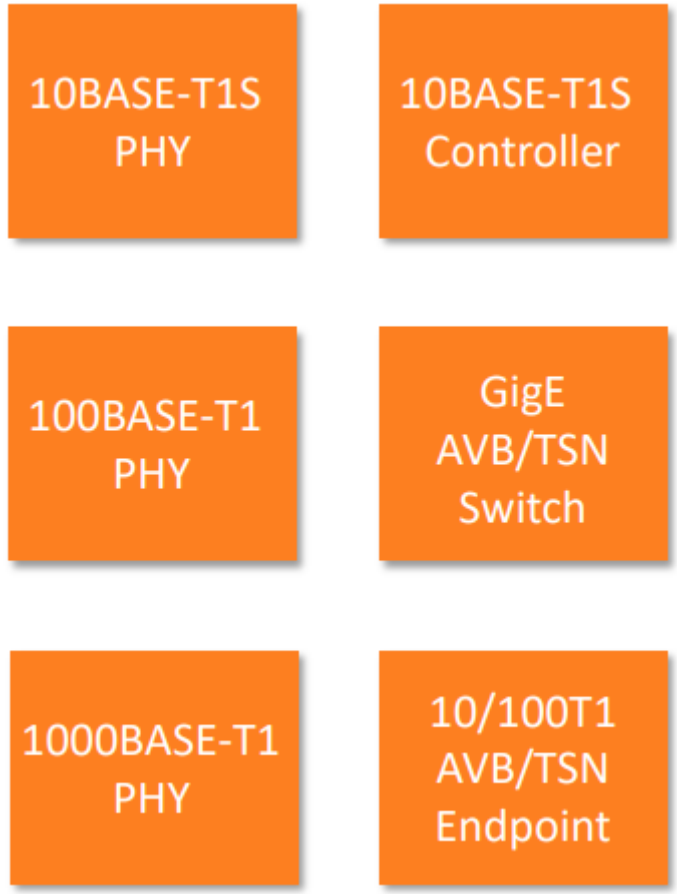


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SPE Product Details

Microchip SPE Solutions

- Flexible and scalable system solutions
- Extended cable reach
- Smallest packages
- Lowest power, wake/sleep
- Security support
- Functional safety ready
- Ambient temperatures up to 125 ◦C
- Comprehensive software & tool support



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MICROCHIP

10BASE-T1S Roadmap

Development | Sampling | Production

PHY (MII, RMII)

- LAN8670 — 32 QFN — MII/RMII
- LAN8671 — 24 QFN — RMII

Updated to latest OA Spec Q3 2025

MAC-PHY (SPI)

- LAN8650 — 32 QFN — Ext. LDO
- LAN8651 — 32 QFN — Int. LDO
- LAN865x — Latest OA Spec — 48V

Samples Q4 2026

Transceiver SBC (OA3p)

- LAN8680 — 16 DFN — 12V LDO

RTP Q3 2026

Transceiver (OA3p)

- LAN8679 — 8 DFN

RTP Q2 2026

- LAN8681 — 14 DFN — Wake/Sleep,48V

Samples Q4 2026

Endpoint (OA3p)

- LAN8660 — 32 QFN — Control EP, RCP
- LAN8661 — 32 QFN — Lighting EP, RCP
- LAN8662 — 32 QFN — Audio EP, RCP
- LAN8660X/1X/2X — 32 QFN — integrated TRX

RTP Q3 2026

MCU, Switch (OA3p)

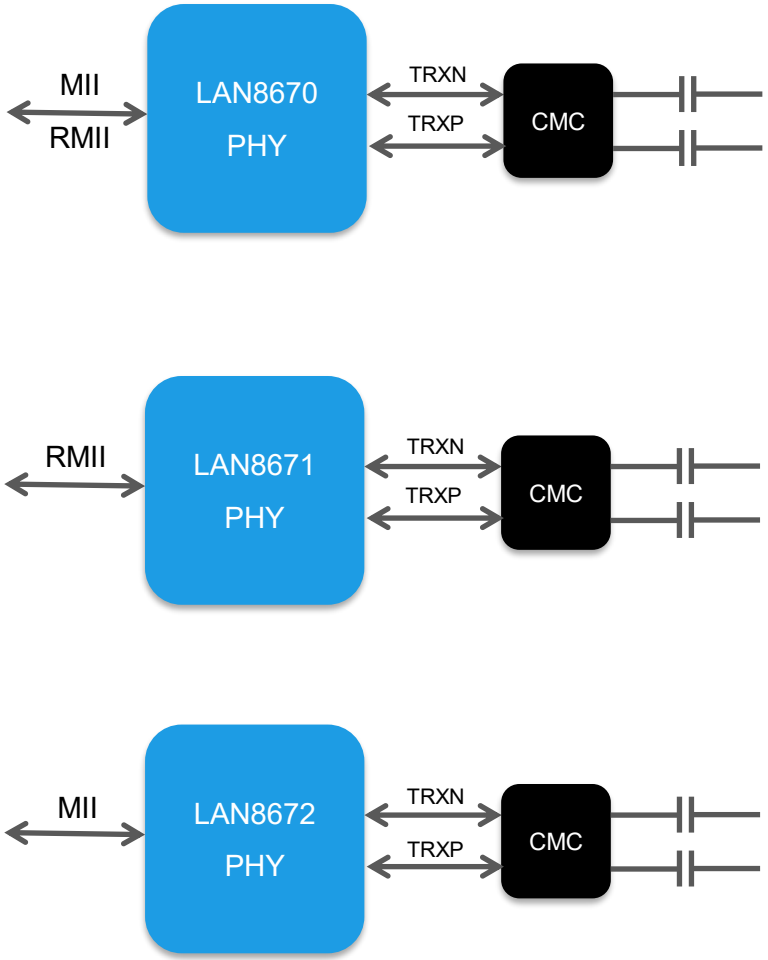
- PIC32CM — 32 QFN — MCU
- dsPIC33A — 48 QFN — MCU
- Hallberg — 30G, 100/1000T1 — Switch
- Buzz — 3G, 100T1/SGMII — Switch

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MICROCHIP

LAN867x 10BASE-T1S PHYs

10BASE-T1S Ethernet PHY



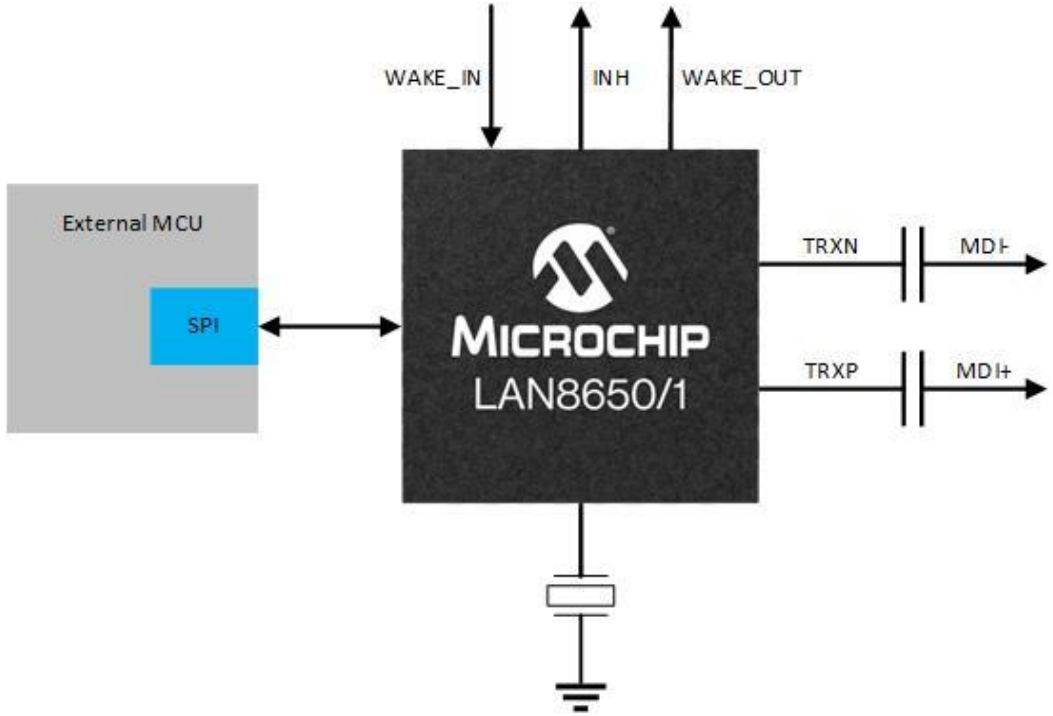
- **Designed according to IEEE Std 802.3cg-2019™**
  - 10 Mbps over single balanced pair of conductors
  - Half-duplex point-to-point segments up to at least 15 m
  - Half-duplex multidrop segments up to at least 25 m with up to at least 8 nodes
- **High bandwidth utilization and latency optimization**
  - Physical Layer Collision Avoidance (PLCA)
  - Multiple PCLA IDs per node
  - Burst mode
- **Time Sensitive Networking (TSN) support**
  - Enables high-precision clock recovery with ultra-low jitter (IEEE Std 802.1AS™ / IEEE 1588™)
- **Standard interface**
  - MII / RMII
  - SMI (MDIO, MDC) for rapid register access
- **Ultra-low power sleep mode**
  - Wake on network activity or input pin
- **Functional Safety Ready**
  - SGS TUV Certified ISO 26262 ASIL B ready
  - FMEDA, Safety Manual,
- **Small footprint**
  - 24 & 32 & 36-pin
  - VQFN package with wettable flanks
- **AEC-Q100 Grade 1 (-40 to +125C)**

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LAN865x 10BASE-T1S PHYs

10BASE-T1S MAC-PHY Ethernet Controller with SPI



- **Designed according to IEEE Std 802.3cg-2019™**
  - 10 Mbps over single balanced pair of conductors
  - Half-duplex point-to-point segments up to at least 15 m
  - Half-duplex multidrop segments up to at least 25 m with up to at least 8 nodes
- **High bandwidth utilization and latency optimization**
  - Physical Layer Collision Avoidance (PLCA)
  - Multiple PCLA IDs per node
  - Burst mode
- **Standard interface**
  - Serial Peripheral Interface (SPI)
  - Designed to the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification, V1.1
- **Ultra-low power sleep mode**
  - Wake on network activity or input pin
- **Functional Safety Ready**
  - SGS TUV Certified ISO 26262 ASIL B ready
  - FMEDA, Safety Manual
- **Small footprint**
  - 32-pin (5x5 mm)
  - VQFN package with wettable flanks
- **AEC-Q100 Grade 1 (-40 to +125C)**

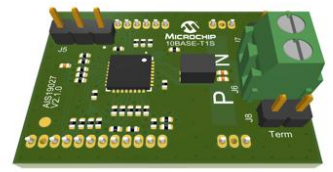
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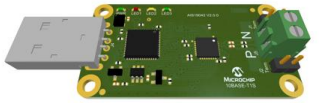
10BASE-T1S Evaluation Boards

Evaluation Boards and MPLAB® Harmony

- **10BASE-T1S PHY RMII Evaluation Board EVB-LAN8670-RMII**
  - Fits to many Microchip MCU boards
  - Small form factor
  - Available from MicrochipDirect (EV06P90A)



- **10BASE-T1S PHY USB Evaluation Board EVB-LAN8670-USB**
  - Makes every USB host a potential 10BASE-T1S node
  - Drivers for Linux and Windows
  - Available from MicrochipDirect (EV08L38A)



- **10BASE-T1S MAC-PHY SPI Evaluation Board**
  - Enables Ethernet communication for various Microchip evaluation kits that support click boards™ and the SPI interface
  - Available from MikroE (www.mikroe.com, Two-Wire Eth Click, MIKROE-5543)

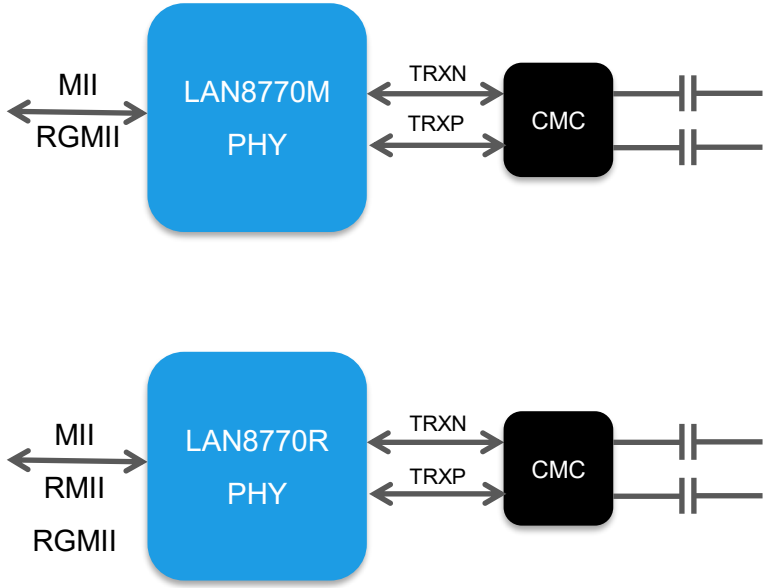


- **MPLAB® Code Configurator Development Framework**
  - Integration into development framework for Microchip microcontrollers and microprocessors

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LAN877x 100BASE-T1 PHY

100BASE-T1 Ethernet PHY



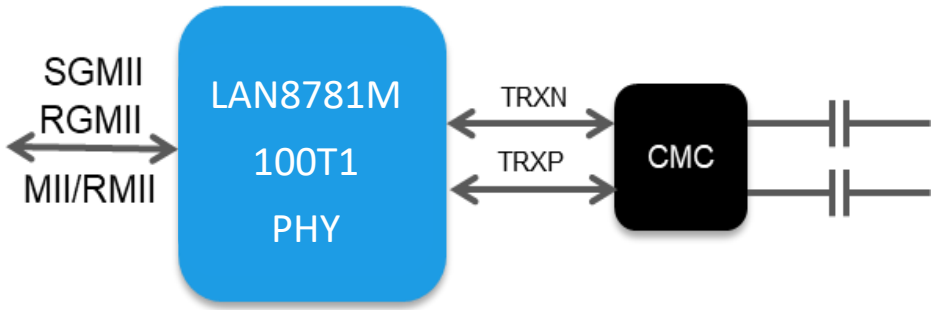
- **Fully compliant IEEE802.3bw Single-Port PHY**
- **Leading Energy Efficiency**
  - Low Power ~130mW operation
  - TC10 Wake up / Sleep (< 15uA)
- **Reduced BOM**
  - Fully integrated line termination and filtering
  - RGMII, RMII, MII w/ FlexPWR®
  - 125MHz RGMII output
- **Enhanced LinkMD™ diagnostics**
  - OPEN Alliance (TC1) Advanced diagnostics compliant
  - SQI counter w/ MSE, peak, threshold interrupt
- **Functional Safety Ready**
  - SGS TUV Certified ISO 26262 ASIL B ready
  - FMEDA, Safety Manual,
- **Smallest T1 PHY**
  - 32-Pin & 36-Pin Wettable QFN (5x5mm, 6x6mm)
- **AEC-Q100 Grade 1 (-40 to +125C)**

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LAN878x MACsec 100BASE-T1 PHYs

Facilitating System Level Safety and Security



40-Pin QFN (6 mm x 6 mm)

CPN	MAC sec	RGMII	SGMII	MII / RMII	100M bps	Auto-Neg
LAN8781M	X	X		X	X	X
LAN8781		X		X	X	X
LAN8782M	X		X		X	X
LAN8782			X		X	X

- **Fully compliant IEEE802.3bw PHY**
  - Force speed or auto-negotiation mode
- **IEEE 802.1AE/TC17 MACsec support**
  - With secure key load and storage
- **22nm FDX Global Foundries low power process**
  - Dual FAB locations
- **Reduced power consumption**
  - <100mW
  - TC10 sleep and wake support
- **ISO26262 functional safety compliant**
  - ASIL B rating
  - Enhanced safety diagnostics and notifications*
- **AEC-Q100 Grade 1 (-40°C to +125°C)**
- **Pin compatibility with LAN878x 100BASE-T1**

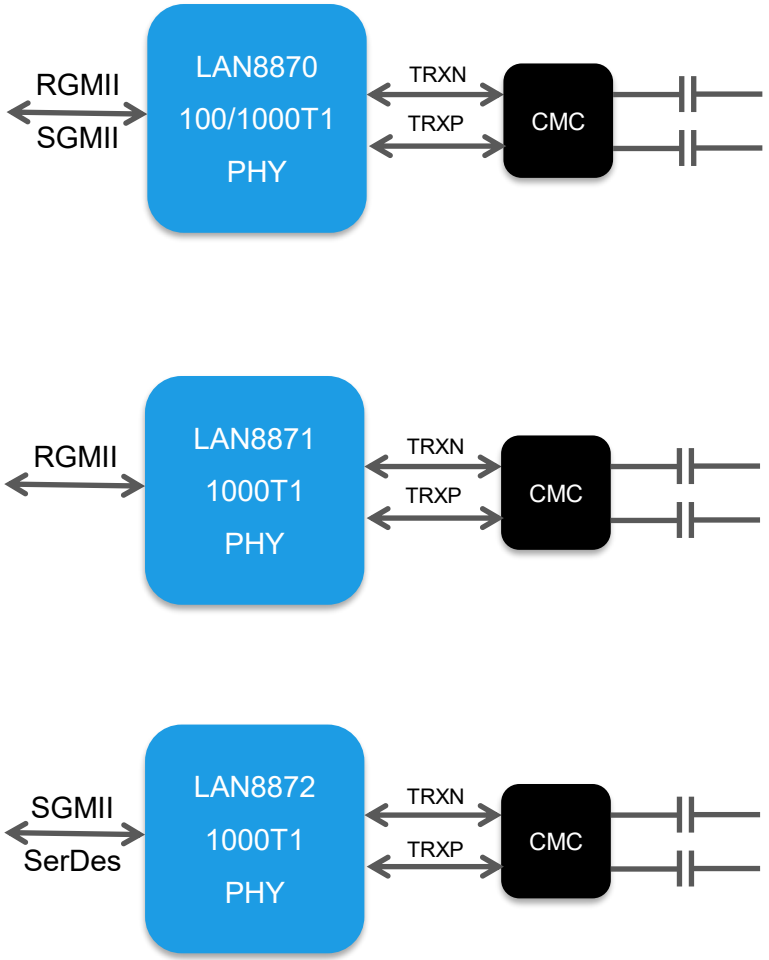
* Additional enhanced diagnostics and actions to improve system level Functional Safety. Delivered as continual PHY revision enhancements, while maintaining backward compatibility

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LAN887x 1000BASE-T1 PHY

1000BASE-T1 Ethernet PHY

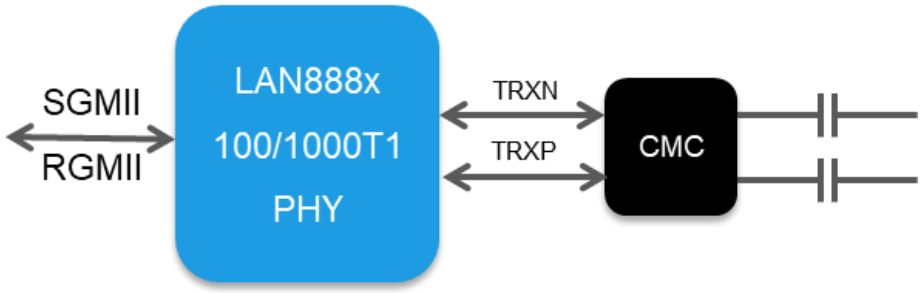


- **Fully compliant IEEE802.3bw/bp Single-Port PHY**
  - Force or auto-negotiation mode
- **IEEE 1588 / .1AS Time synchronization support**
  - 8ns jitter accuracy
- **Cable reach**
  - Type A (15m) and Type B (40m)
  - Extended reach (>40m*)
- **TC10 Sleep and Wakeup support**
  - <20uA standby power consumption
- **Enhanced Diagnostics**
  - Cable diagnostics, Signal Quality Indicator
  - BIST, link, error, temperature, voltage and clock monitoring
- **Functional Safety Ready**
- **48-Pin (7mm x 7mm) package**
- **AEC-Q100 Grade 2 (-40degC to +105degC)**

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LAN888x MACsec 100/1000BASE-T1 PHYs

Facilitating System Level Safety and Security



40-Pin QFN (6 mm x 6 mm)

CPN	MACsec	RGMII	SGMII	100M bps	1000M bps	Auto -Neg
LAN8881M	X	X	-	-	X	X
LAN8881	-	X	-	-	X	X
LAN8882M	X	-	X	-	X	X
LAN8882	-	-	X	-	X	X
LAN8883M	X	X		X	X	X
LAN8883	-	X		X	X	X
LAN8884M	X		X	X	X	X
LAN8884	-		X	X	X	X

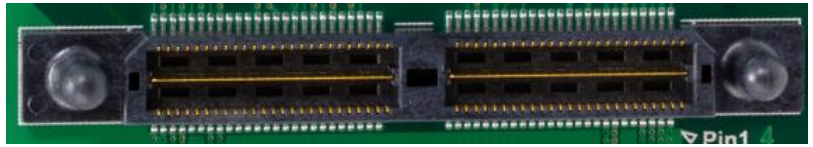
- **Fully compliant IEEE802.3bw/bp PHYs**
  - Force speed or auto-negotiation mode
- **IEEE 802.1AE/TC17 MACsec support**
  - With secure key load and storage
- **22nm FDX Global Foundries low power process**
- **Reduced power consumption**
  - 1000Mbps: <350mW
  - TC10 sleep and wake support
- **ISO26262 functional safety compliant**
  - ASIL B rating
  - Enhanced safety diagnostics and notifications*
- **AEC-Q100 Grade 1 (-40°C to +125°C)**
- **Pin compatibility with LAN888x 1000BASE-T1**

* Additional enhanced diagnostics and actions to improve system level Functional Safety. Delivered as continual PHY revision enhancements, while maintaining backward compatibility

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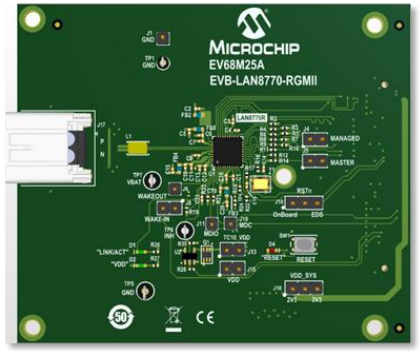
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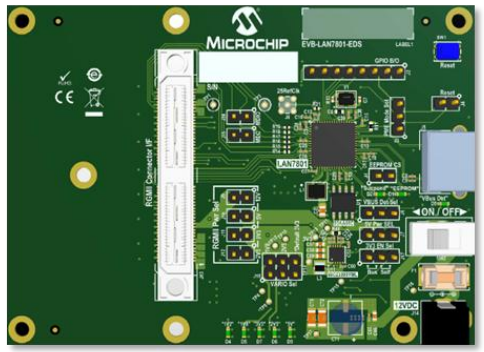
100/1000 BASE-T1 Plug-in Bridge Solutions





100BASE-T1
LAN8770

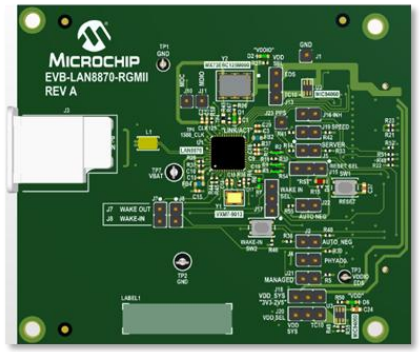


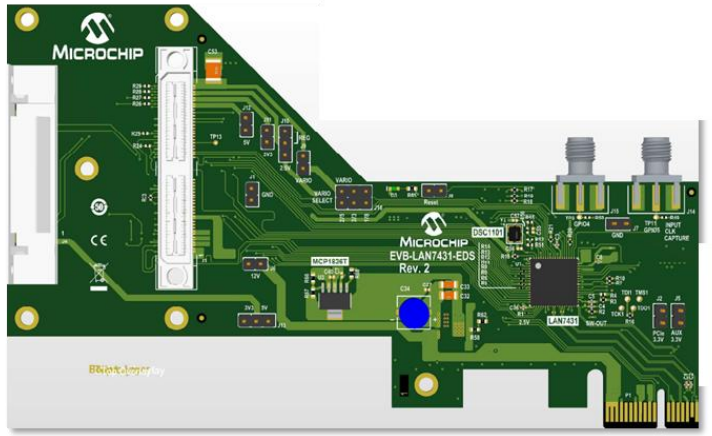


SUPERSPEED CERTIFIED USB

LAN7801 + Software

1000BASE-T1
LAN8870





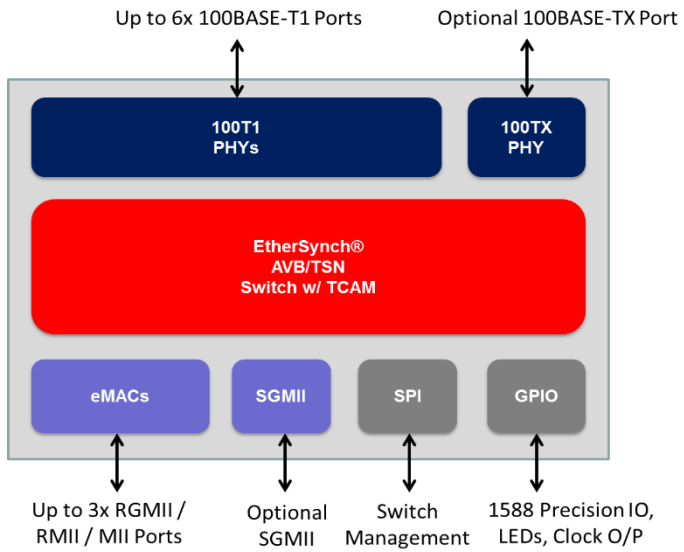
PCI EXPRESS

LAN7431 + Software

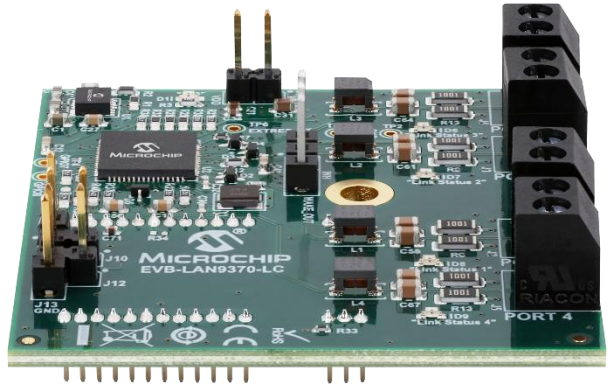
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LAN937x 100T1 GigE Switch



Part Number	T1 PHY Ports	TX PHY Ports	RGMII/ RMII/MII Ports	SGMII Ports	Temperature	Package
LAN9370	4	0	1	0	-40°C +105°C	64-QFN
LAN9371	3	1	2	0	-40°C +105°C	128-TQFP
LAN9372	5	1	2	0	-40°C +105°C	128-TQFP
LAN9373	5	0	2	1	-40°C +105°C	128-TQFP
LAN9374	6	0	2	0	-40°C +105°C	128-TQFP



- **5 to 8-Port AVB/TSN Switch**
- **Cascade for up to 14-Ports**
- **Software and pin compatible**
- **TC11 compliant**
- **TC10 wake up and sleep**
- **AEC-Q100 Grade 2**

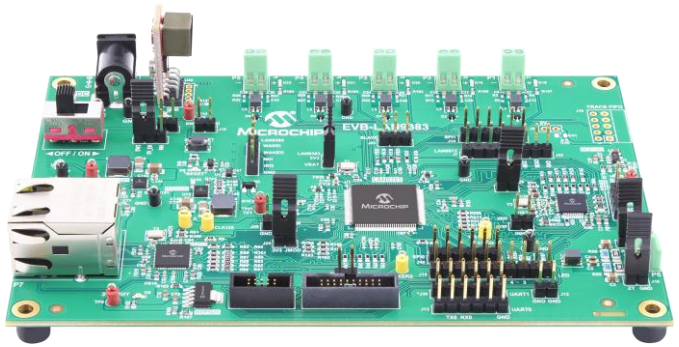
- **Advanced AVB/TSN support**
  - 802.1AS Time Sync
  - 802.1Qat Stream Reservation
  - 802.1Qav Shaper
  - 802.1Qbv Scheduler
  - 802.1Qci Ingress Policing

EVB-LAN9370

- Partner: SAME70 XULT, SAMA5D3-EDS, Audio End Point
- Software: Autosar, FreeRTOS, Linux

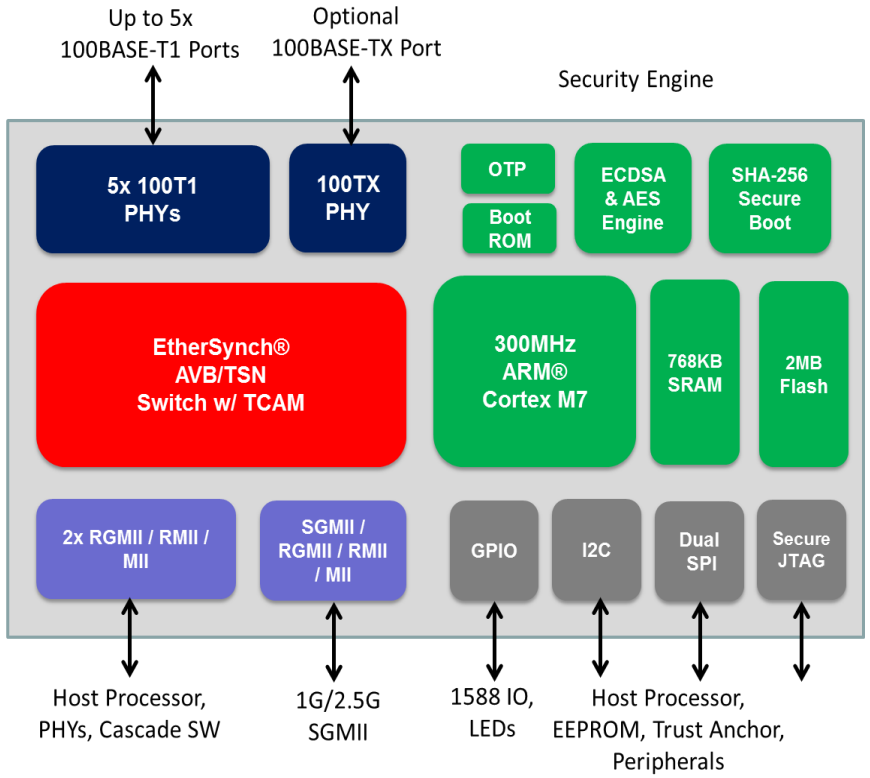
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LAN938x 100T1 GigE Switch w/ CPU



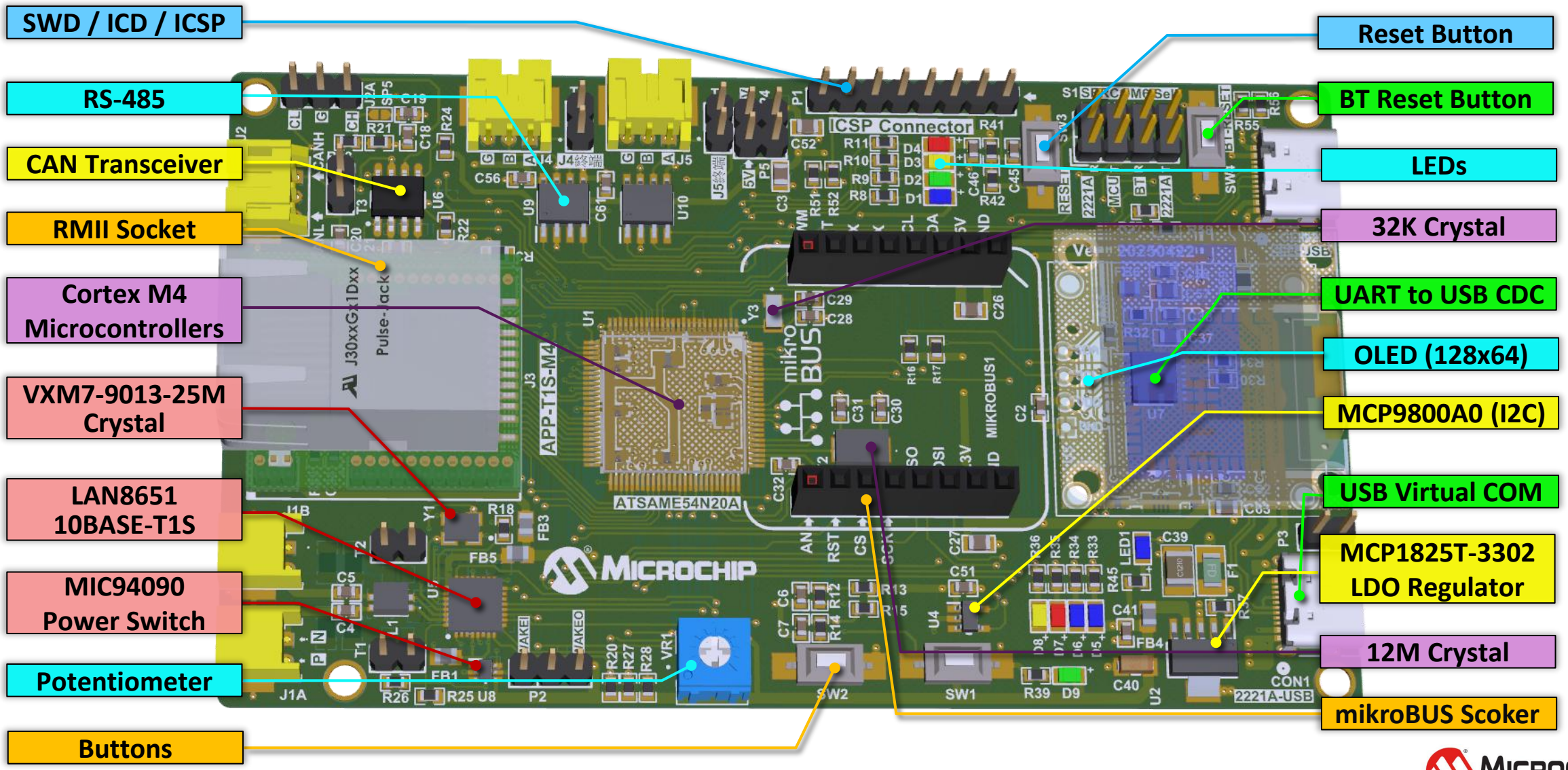
Part Number	T1 PHY Ports	TX PHY Ports	RGMII / RMII / MII Ports	SGMII OR RGMII MUX Port	Temperature	Package
LAN9384	5	1	0	1	-40 +105	128-TQFP
LAN9383	5	0	1	1	-40 +105	128-TQFP
LAN9382	4	1	1	1	-40 +105	128-TQFP
LAN9381	4	0	2	1	-40 +105	128-TQFP

- **7-Port AVB/TSN Switch**
- **300MHz Cortex M7**
- **Integrated Flash & ECC RAM**
- **1G/2.5G SGMII Uplink**
- **Advanced TSN support**
  - 802.1AS-2020 Time Sync
  - 802.1Qbv Scheduler
  - 802.1Qci Ingress Policing
  - 802.1CB Redundancy
- **Advanced Security Engine**
- **TC10 wake up and sleep**
- **Functional Safety ready**
- **AEC-Q100 Grade 2**



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APP-ATSAM-M4-Ethernet Overview



Thank you!