MICROCHIP

Regional Training Centers

Microchip Ethercat

LAN9252

基礎設計流程

參考資料

- LAN9252 網頁
- SSC Help link
  - Application Note ET9300 (EtherCAT Slave Stack Code)
  - EtherCAT Slave Design Quick Guide
- EtherCAT Communication
- TWINCAT user manual
- MPLABX and PIC kit 3 user manual
- LAN9252 SDK application note
- Microchip 《LAN9252 数据手册》
- Microchip 《EVB-LAN9252-HBI 评估板用户指南》
- Microchip 《PIC32MX 数据手册》
- Microchip 《LAN9252 EEPROM 配置和编程》

Regional Training Centers

課程內容 (Agenda)

- **LAN9252介紹**
- **TWINCAT 端的設定/MASTER端網卡尋找**
- **PDO mapping excel and SSC flow**
- **EEPROM programming**
- **MPLABX 流程**
- **PLC Structure text code basic**
- **UART/MIO/ADC application**
- **APPL_ application code briefing**
- **Hand on**
- **Q&A , dismiss**

不包含以下項目 (T.B.D)

- **Mail box /SDO application (XOE)**
  - EOE, SOE,FOE,VOE application
- **Hardware FX application**
- **Deep HBI mode operation (porting to other SOC)**
- **Advance application**
  - FSOE
  - MCM
  - Power quality distribution
  - Motion control
- 如果課堂上**LAB**沒做完**/**沒時間做 請連繫代理商**FAE**

MICROCHIP

Regional Training Centers

LAN9252介紹

TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

Before we start

- 你是否有 (ETG) 帳號 你必須有這個帳號去獲得設計工具 **Check if u have ETG account to access ETG database to get all tool set and document**
- **Application contact →** **https://www.ethercat.org/en/membership_application.html**
- 準備好 **SSC tool and TWINCAT in this course**
- 準備好 **MPLAB X tooling set**
- **An HBI-EVB is encourage to have via M-direct**

Regional Training Centers

About LAN9252

Target Applications

- Motor Motion Control
- Process / Factory Automation
- Sensors
- Robotics

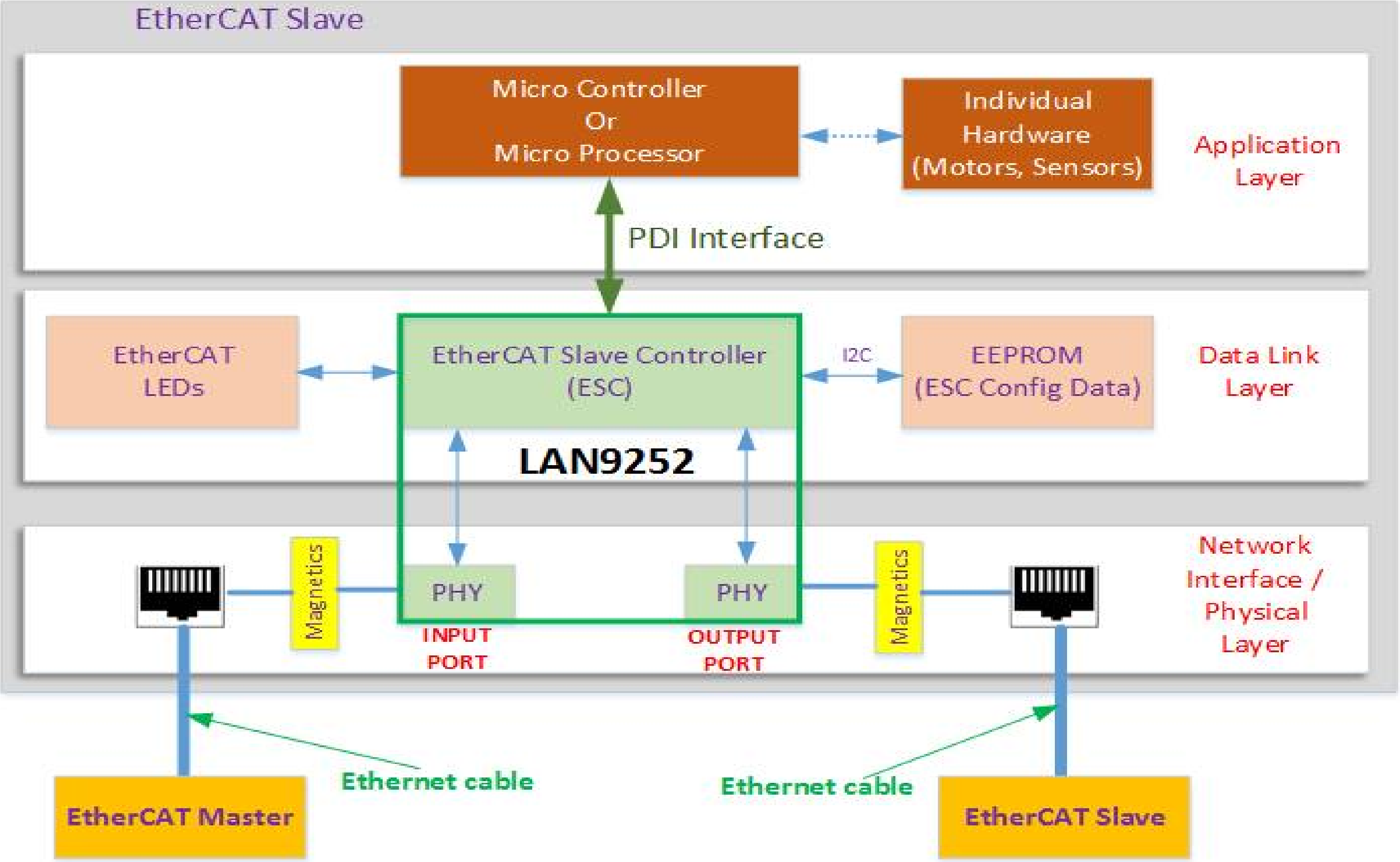
Commercial (0 to +85C) Industrial (-40 to +85C) and Extended temp. (-40 to +105C) supported

Features

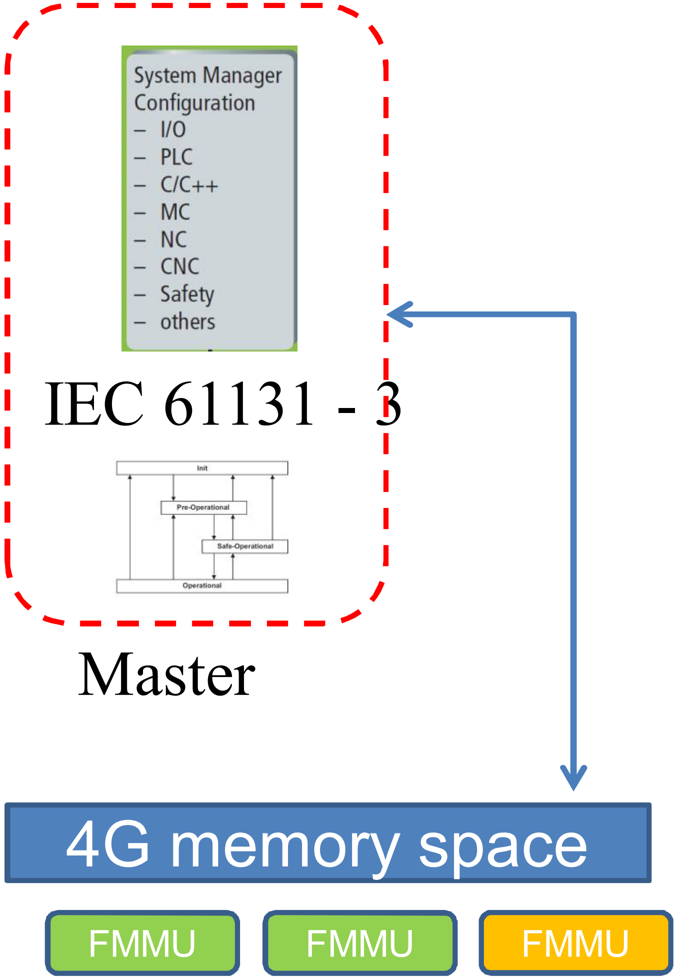
- ***2/3-port EtherCAT® slave controller***
  - *3 Field Bus Memory management Units*
  - *4 Sync managers*
- ***Interfaces to most 8/16/32-bit embedded controllers***
  - *8/16 bit Asynchronous interface*
  - *SPI/SQI up to 80 MHz (PIC32MZ)*
- ***Dual integrated 10/100 PHY's***
  - *Auto-MDIX*
- ***Cable Diagnostics Open, Short, Cable length detection***
- ***Low power mode***
- ***1.6V to 3.6V variable I/O voltage***
- **IEEE 802.3u 100Base-FX Fiber Interface**
- **Integrated 1.2V regulator enables single 3.3V supply**
- ***LAN9252: 64-pin QFN / TQFP-EP***

LAN9252 ESC Architecture

- **LAN9252 is the ESC with 2 internal PHYs**



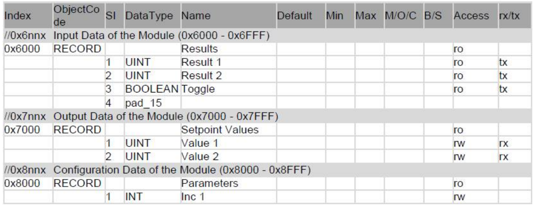
Simple design flow


System Manager Configuration
- I/O
- PLC
- C/C++
- MC
- NC
- CNC
- Safety
- others

IEC 61131 - 3

Master

4G memory space



Index	ObjectCode	SI	DataType	Name	Default	Min	Max	M/O/C	B/S	Access	rx/tx
//0x6nnx	Input Data of the Module (0x6000 - 0x6FFF)										
0x6000	RECORD			Results						ro	
		1	UINT	Result 1						ro	tx
		2	UINT	Result 2						ro	tx
		3	BOOLEAN	Toggle						ro	tx
		4	pad_15								
//0x7nnx	Output Data of the Module (0x7000 - 0x7FFF)										
0x7000	RECORD			Setpoint Values						ro	
		1	UINT	Value 1						rw	rx
		2	UINT	Value 2						rw	rx
//0x8nnx	Configuration Data of the Module (0x8000 - 0x8FFF)										
0x8000	RECORD			Parameters						ro	
		1	INT	Inc 1						rw	

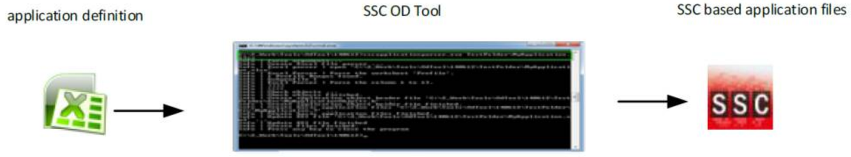
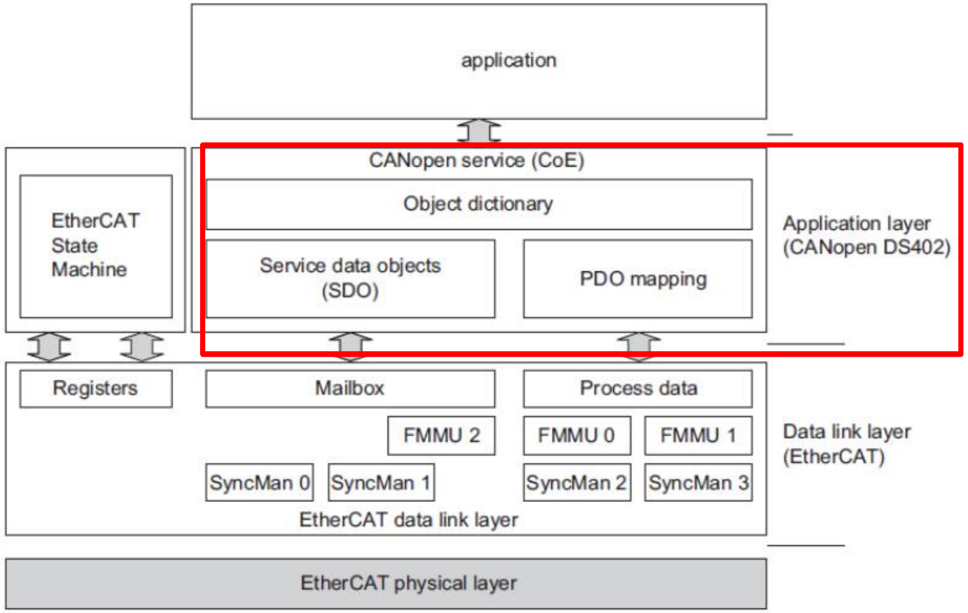
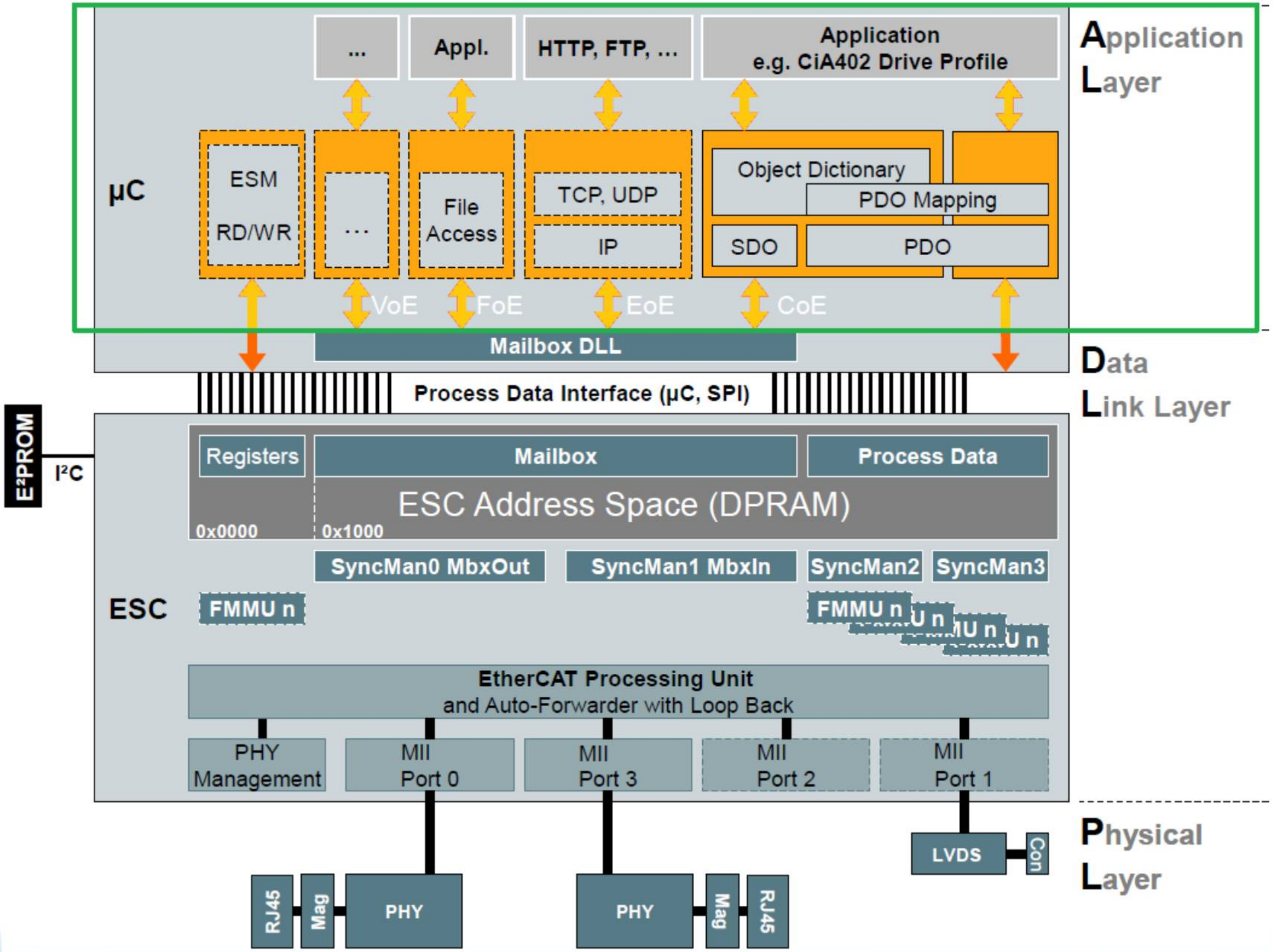


Figure 52: SSC OD Tool workflow



Regional Training Centers

EtherCAT – Application Layer



ESC Components

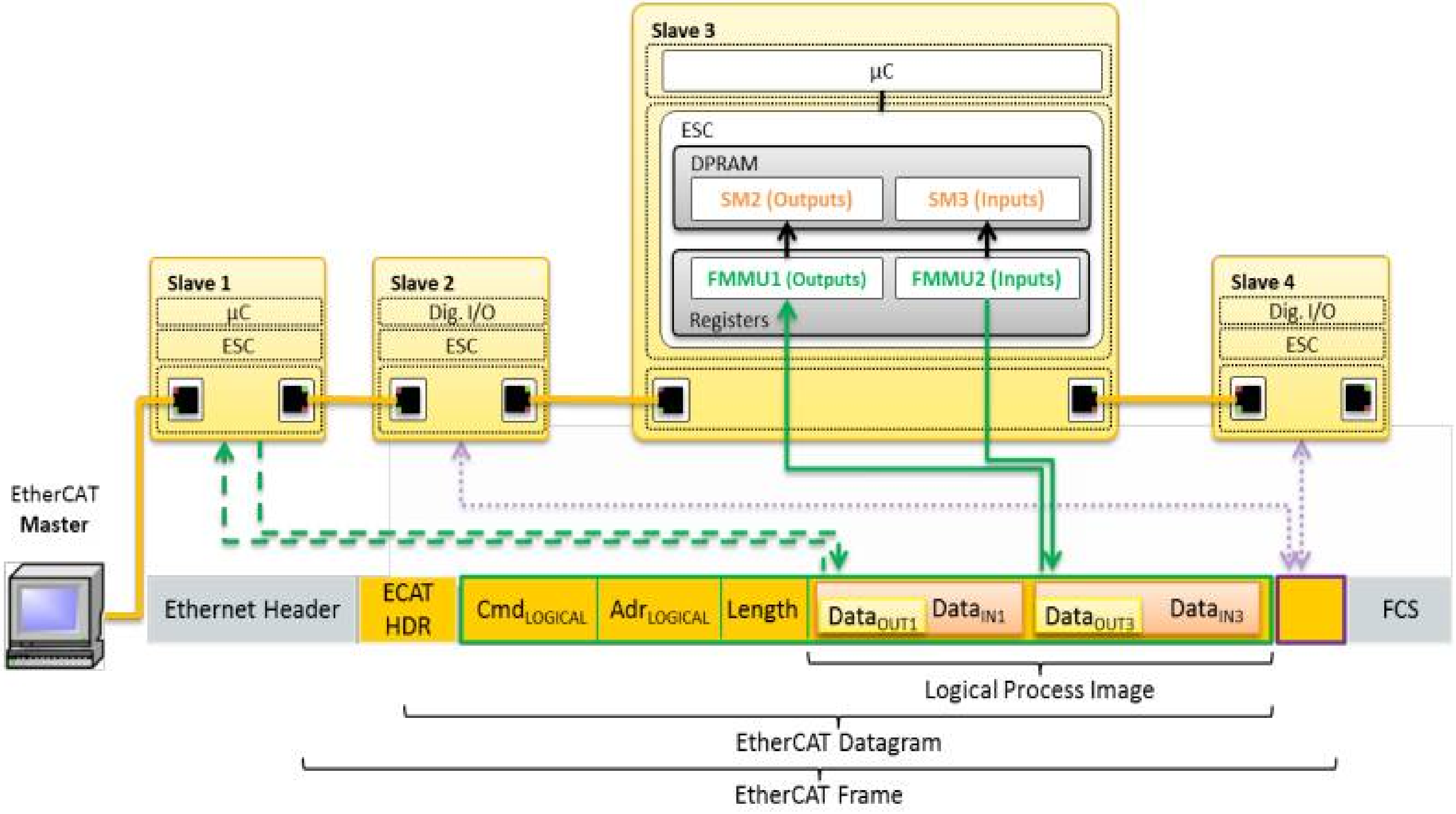
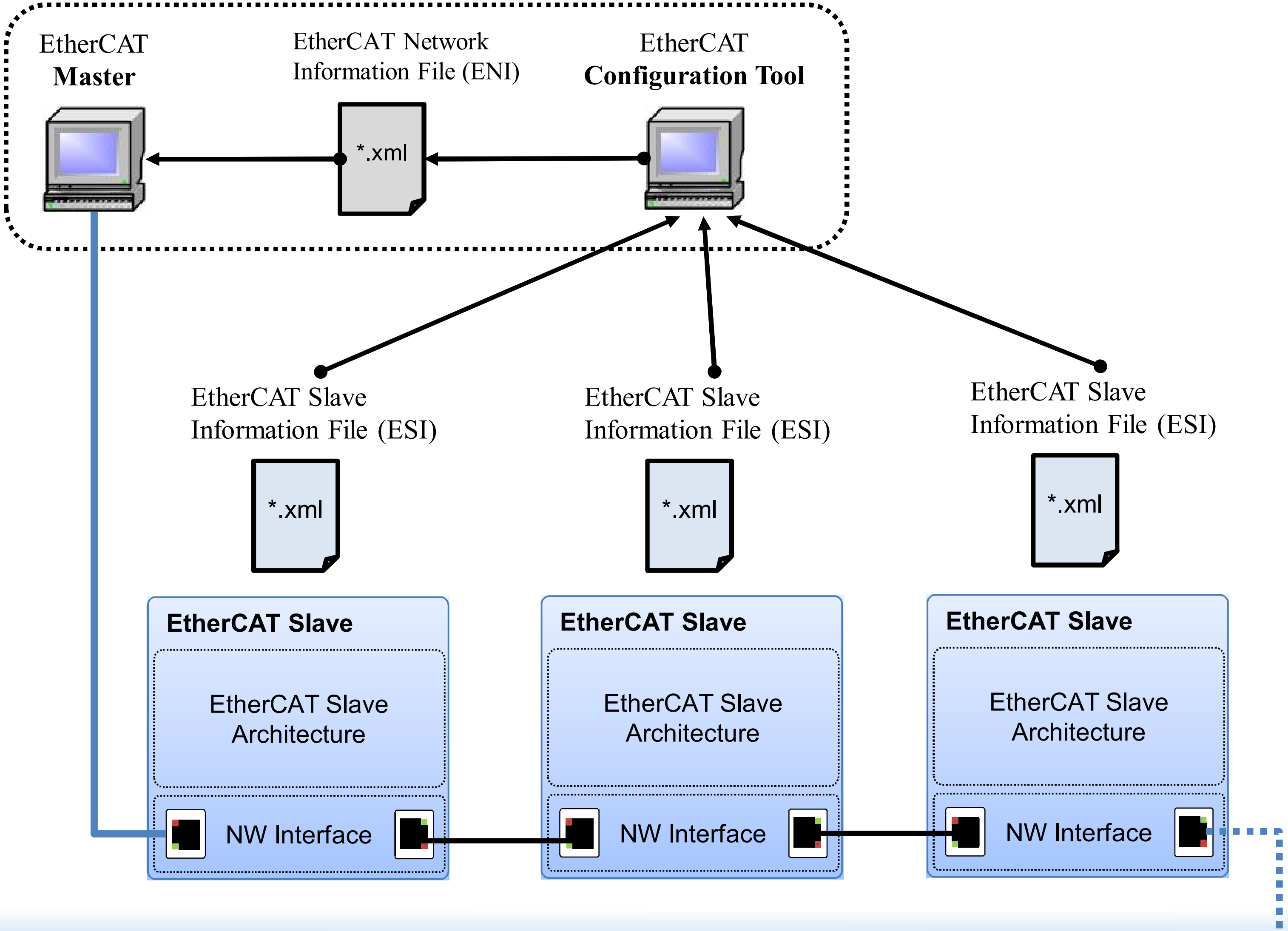


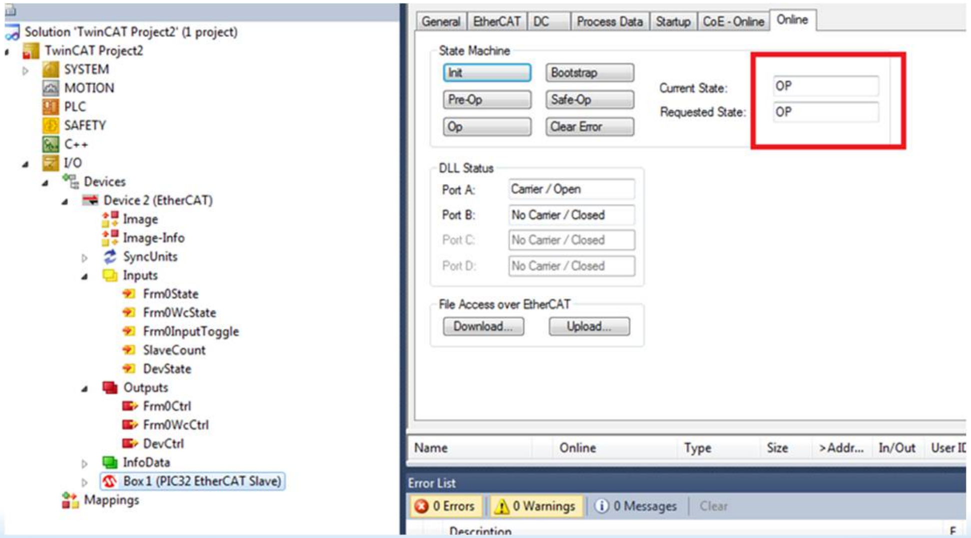
Figure 7: Mapping Example of Process Data with FMMU

EtherCAT®:Network Architecture



Ethercat 的狀態機

- **ETHERCAT**有下列幾種狀態
    - INIT, PRE-OP, OP, Safe-OP
    - PDO的模式　只有OP mode 才是正常的
    - SDO可在PRE-OP and Safe OP 運作
- 在**TWINCAT**中,常利用狀態機來判斷從站是否正常工作



Current State: OP
Requested State: OP

Port A: Carrier / Open
Port B: No Carrier / Closed
Port C: No Carrier / Closed
Port D: No Carrier / Closed

0 Errors | 0 Warnings | 0 Messages

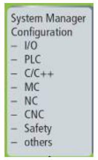
MICROCHIP

Regional Training Centers

LAN9252介紹

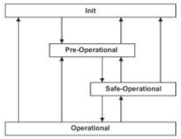
Application (other than robot)

System view



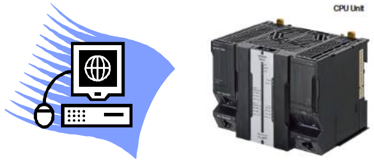
System Manager
Configuration
- I/O
- PLC
- C/C++
- MC
- NC
- CNC
- Safety
- others

IEC 61131 - 3

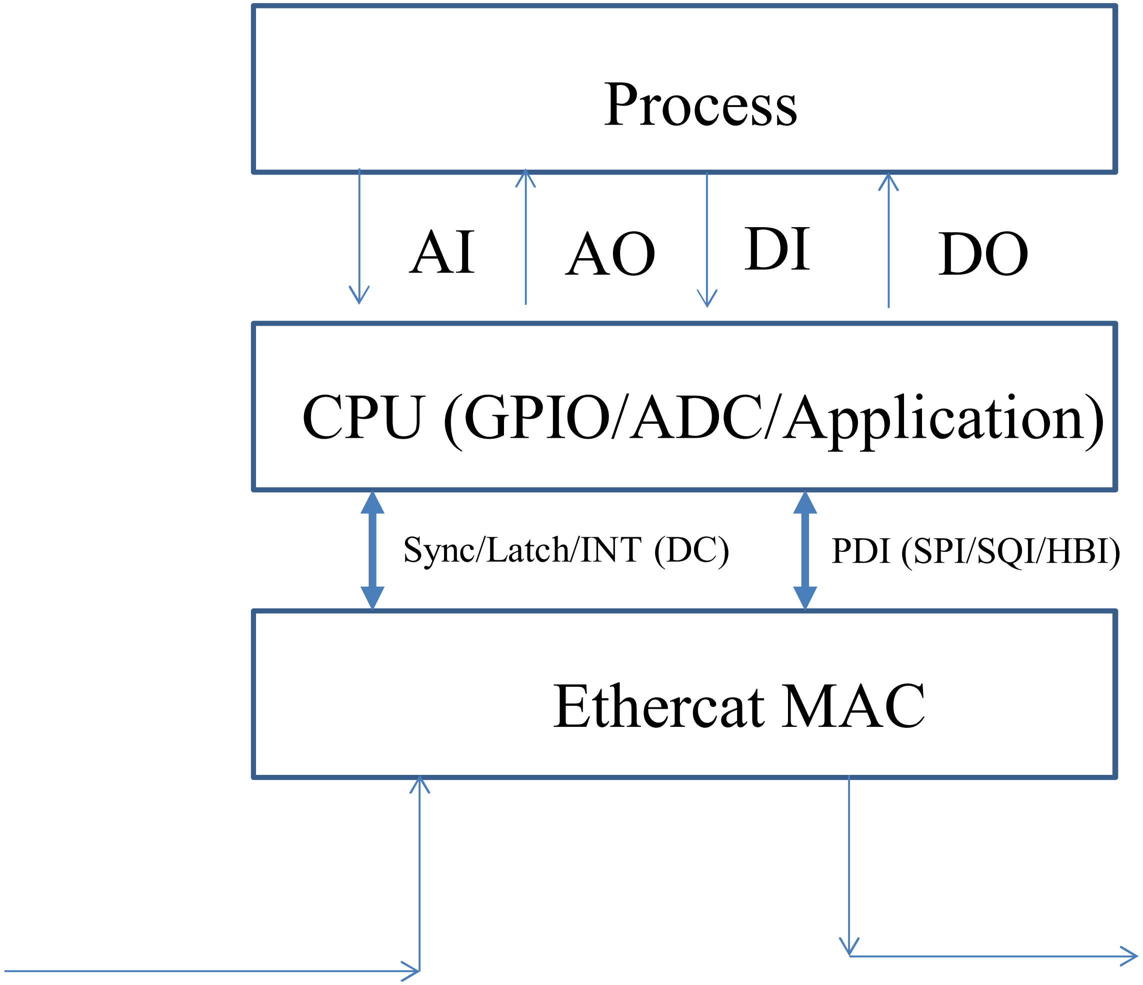


Master node

PC base



Stand alone CPU
With configurator



Process

AI AO DI DO

CPU (GPIO/ADC/Application)

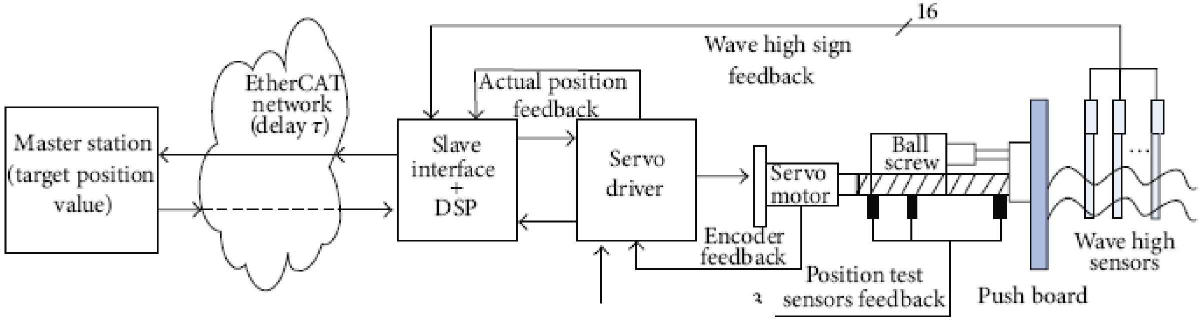
Sync/Latch/INT (DC)

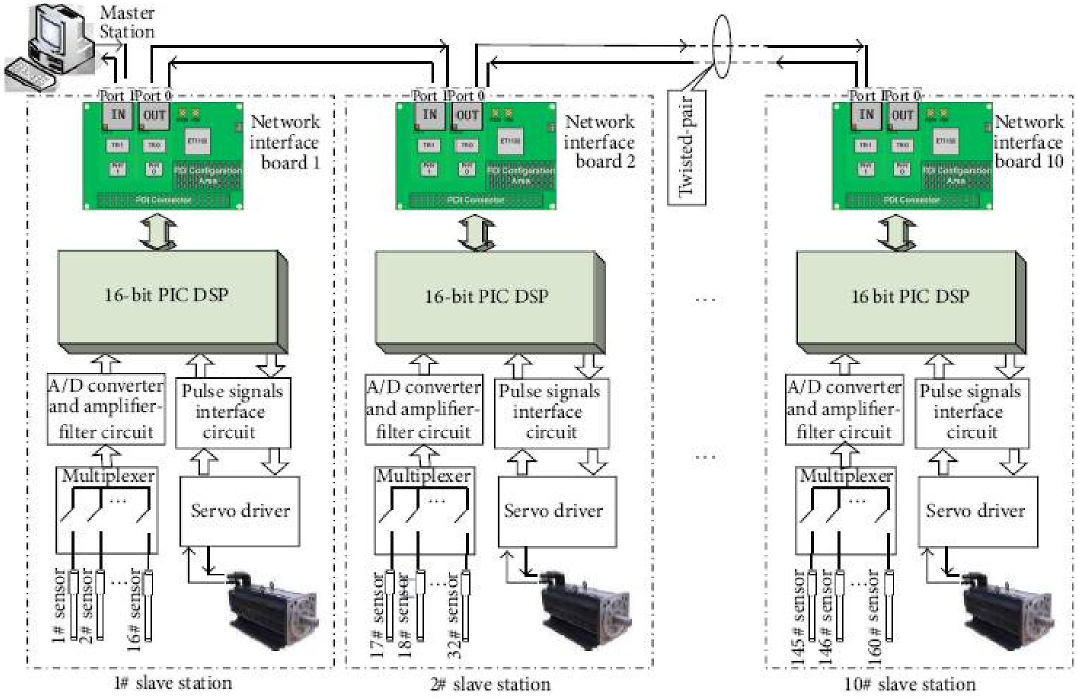
PDI (SPI/SQI/HBI)

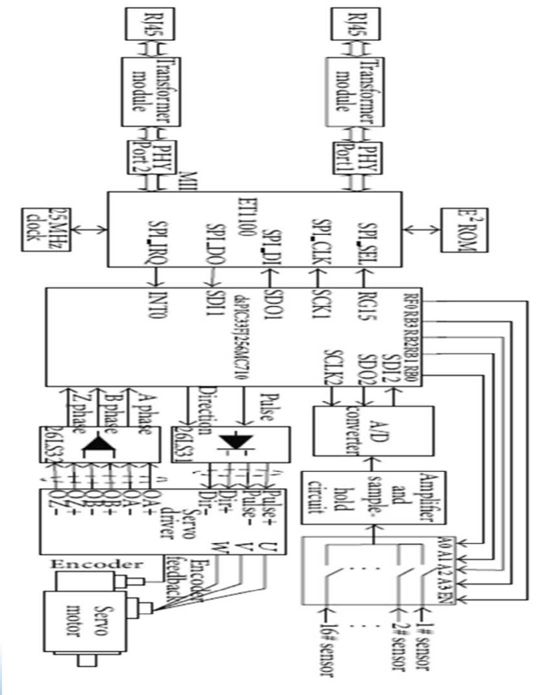
Ethercat MAC

Next slave node

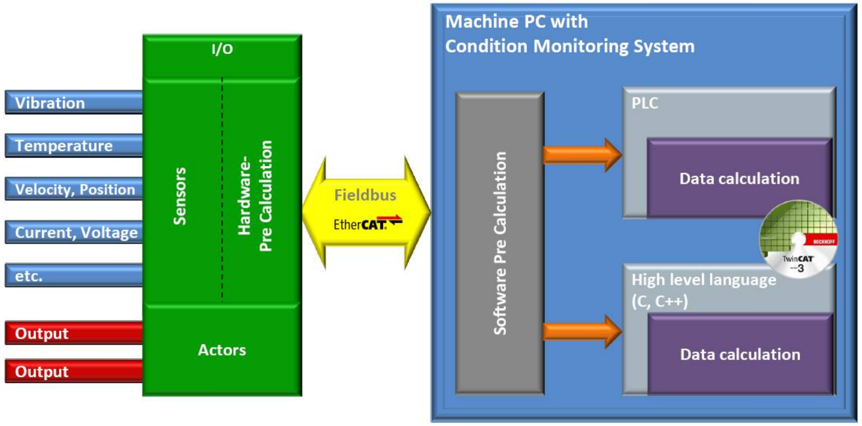
Wave maker machine



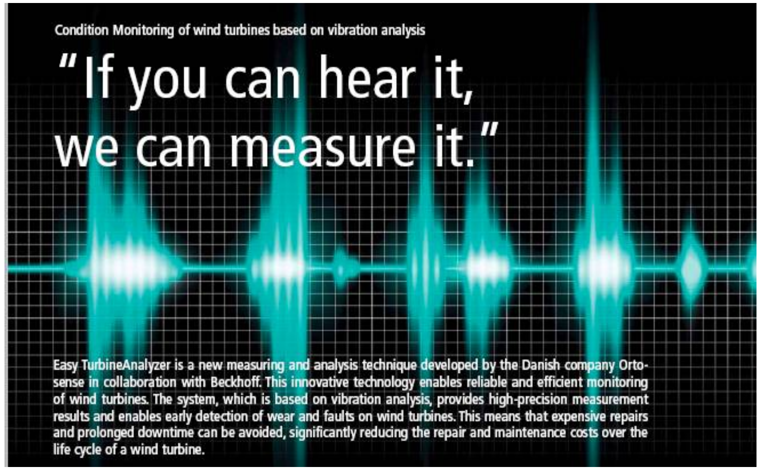




MCM



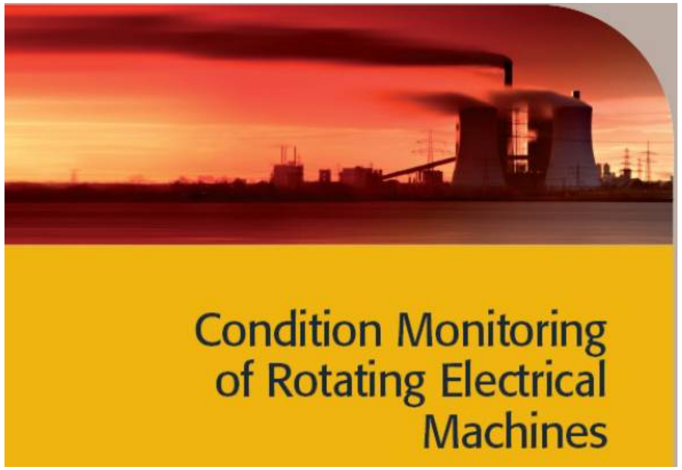
I/O
Vibration
Temperature
Velocity, Position
Current, Voltage
etc.
Output
Output
Sensors
Hardware-Pre Calculation
Actors
Fieldbus
EtherCAT
Machine PC with Condition Monitoring System
Software Pre Calculation
PLC
Data calculation
High level language (C, C++)
Data calculation



Condition Monitoring of wind turbines based on vibration analysis

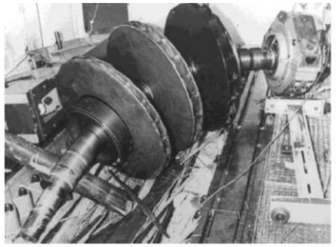
"If you can hear it, we can measure it."

Easy TurbineAnalyzer is a new measuring and analysis technique developed by the Danish company Ortosense in collaboration with Beckhoff. This innovative technology enables reliable and efficient monitoring of wind turbines. The system, which is based on vibration analysis, provides high-precision measurement results and enables early detection of wear and faults on wind turbines. This means that expensive repairs and prolonged downtime can be avoided, significantly reducing the repair and maintenance costs over the life cycle of a wind turbine.



Condition Monitoring of Rotating Electrical Machines

http://timestranscript.canadaeast.com/gallery



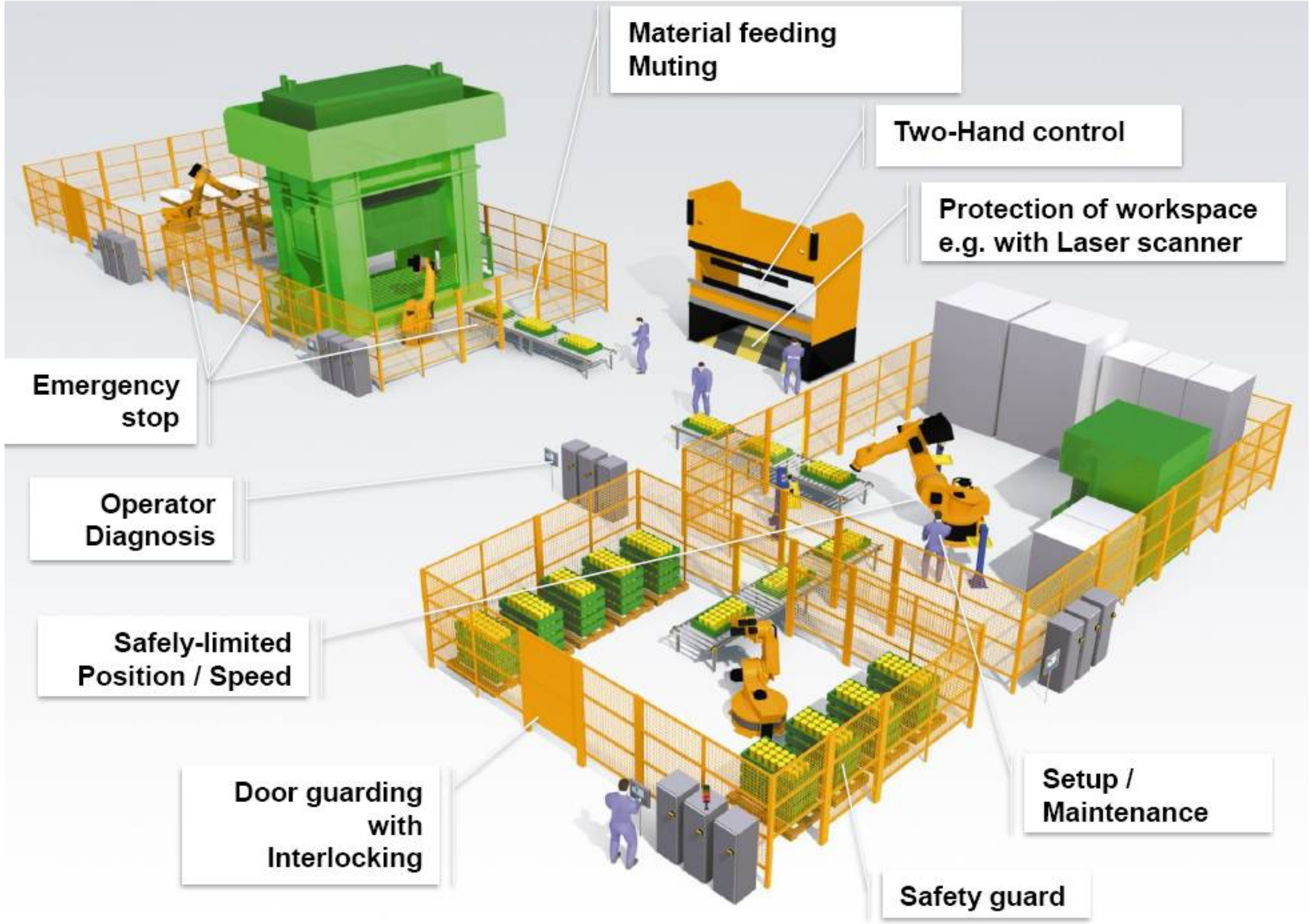
http://www.virginia.edu/romac/

kes.bham.sch.uk

allworldcars.com

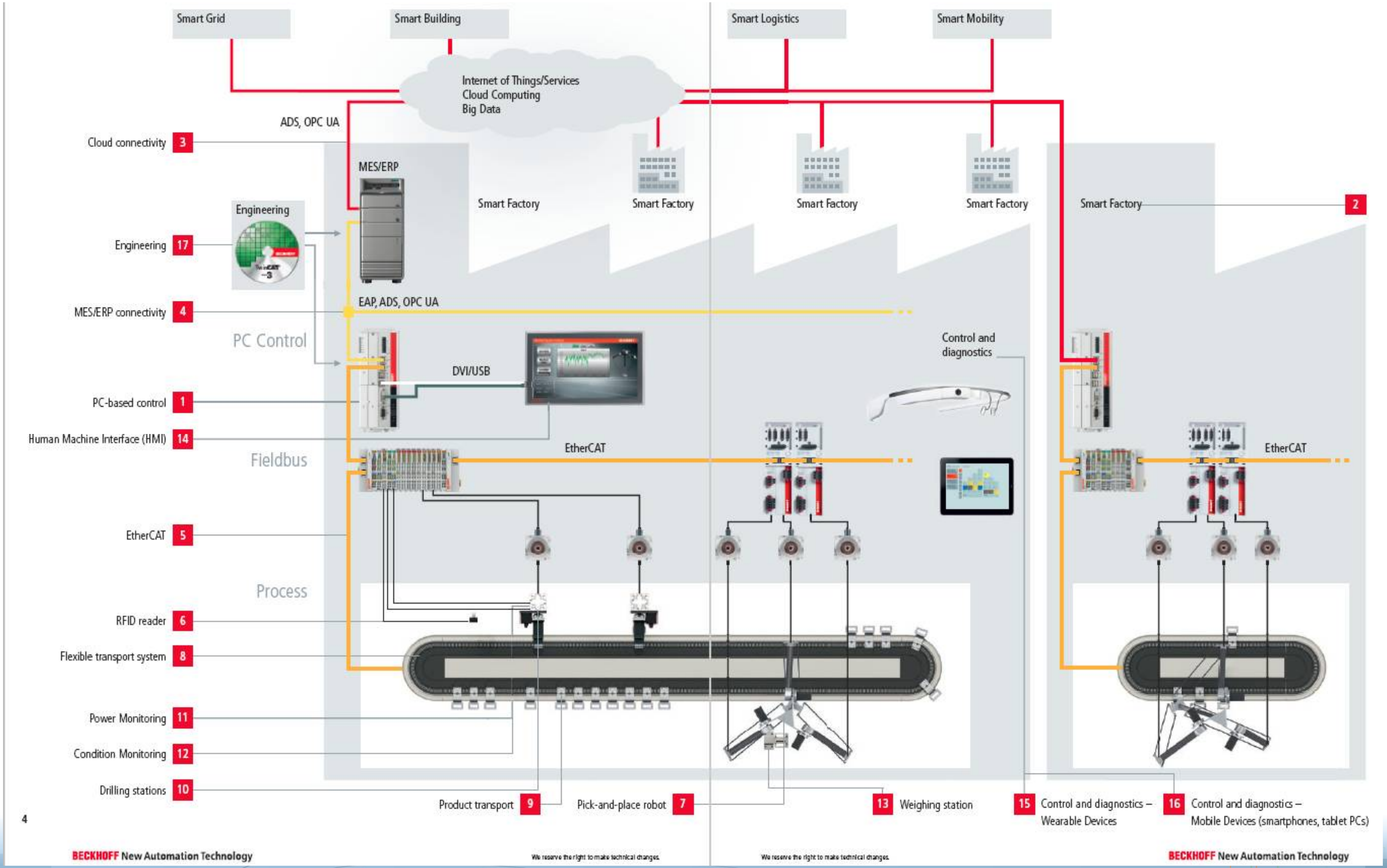
© SmartSignal Corporation 2009

Fail safe over Ethercat

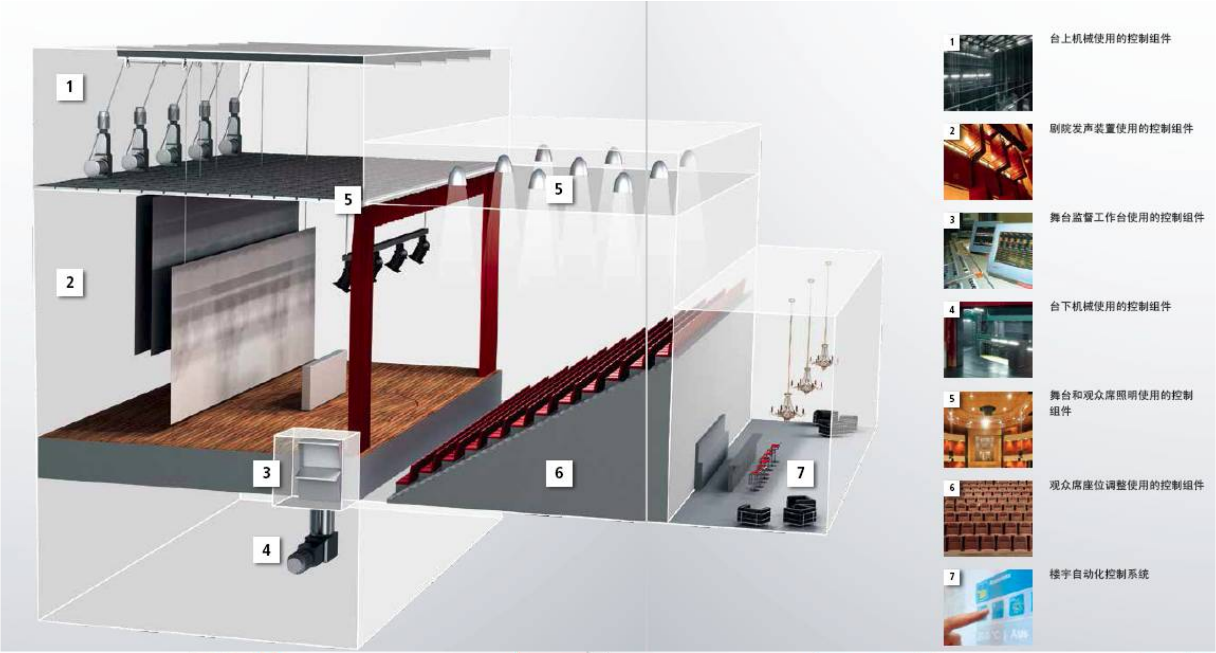


Regional Training Centers

Technology demonstration for a Smart Factory **ID4.0**



Performing art/ Theater



1 台上机械使用的控制组件

2 剧院发声装置使用的控制组件

3 舞台监督工作台使用的控制组件

4 台下机械使用的控制组件

5 舞台和观众席照明使用的控制组件

6 观众席座位调整使用的控制组件

7 楼宇自动化控制系统

Allianz Arena
Changi Airport Group © by Changi Airport

特殊应用

动力学雨，新加坡， **MKT AG and ART+COM AG**， 德国

提供的控制组件：

工业 PC
- 7 台 C6525 工业 PC

I/O
- EtherCAT 耦合器 EK1100 和
- EtherCAT 端子模块

运动控制
- 1216 个伺服端子模块 EL7201
- 1216 个带制动闸的伺服电机 AM3121

自动化软件
- TwinCAT NC PTP
- TwinCAT NC 凸轮控制

主题公园 / 4D 电影院

4D/5D 特效， **Alterface S.A.**， 比利时

提供的控制组件：

I/O
- EtherCAT 耦合器 EK1100 和
- EtherCAT 扩展耦合器 EK1110 和
- EtherCAT I/O 端子模块（数字量和模拟量）
- EtherCAT 安全端子模块

自动化软件
- TwinCAT PLC
- TwinCAT I/O

体育场

- 安联足球场外里面幕墙照明控制和楼宇自动化，慕尼黑，德国，VA Tech Elin EBG，奥地利

楼宇自动化

德国博物馆，德国

提供的控制组件：

工业 PC
- 控制柜式工业 PC C5102
- CX1000 嵌入式控制器

I/O
- 以太网总线耦合器 BC9000 和总线端子模块

自动化软件
- TwinCAT PLC

MICROCHIP

Regional Training Centers

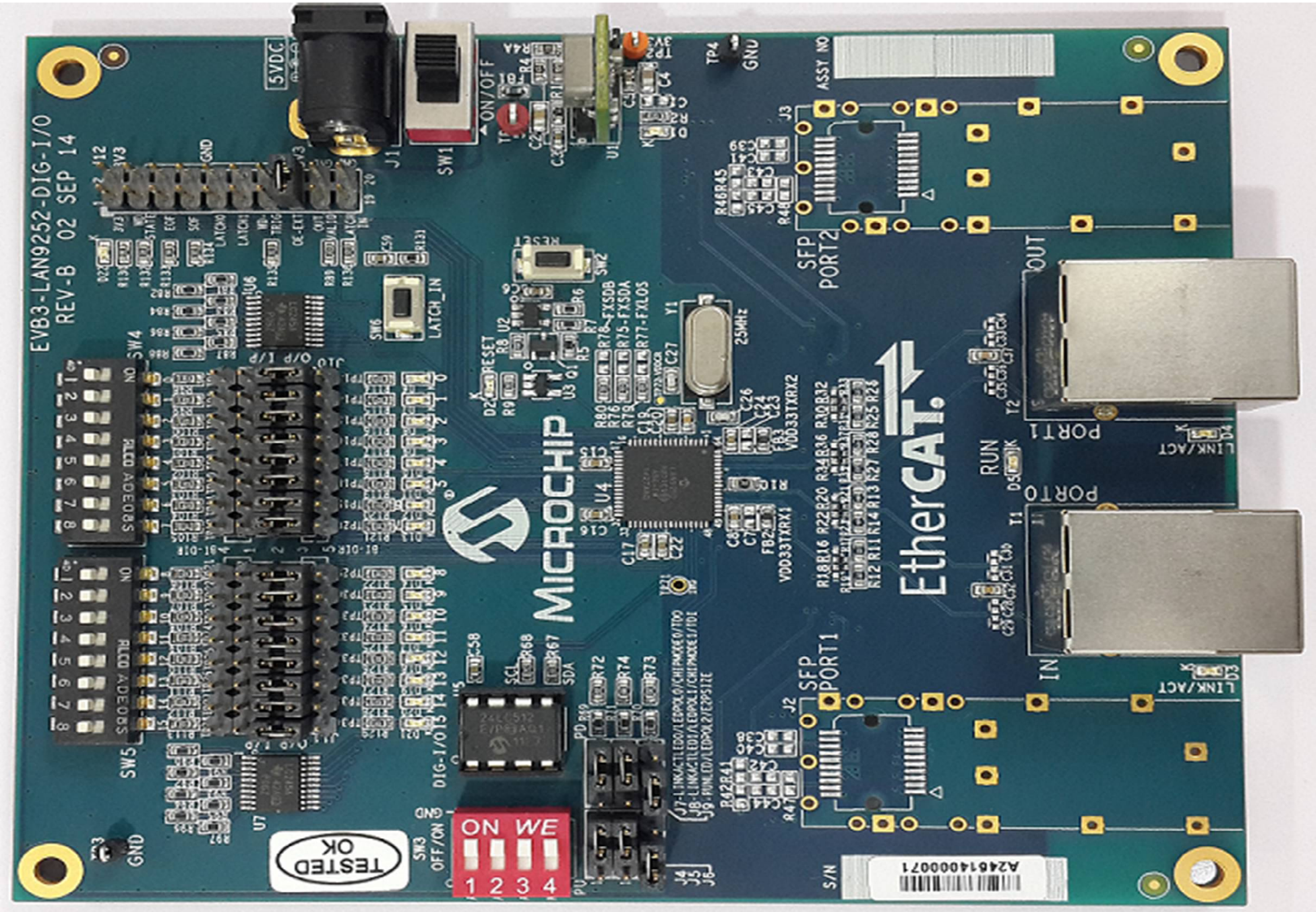
LAN9252介紹

EVB

Microchip
Regional Training Centers

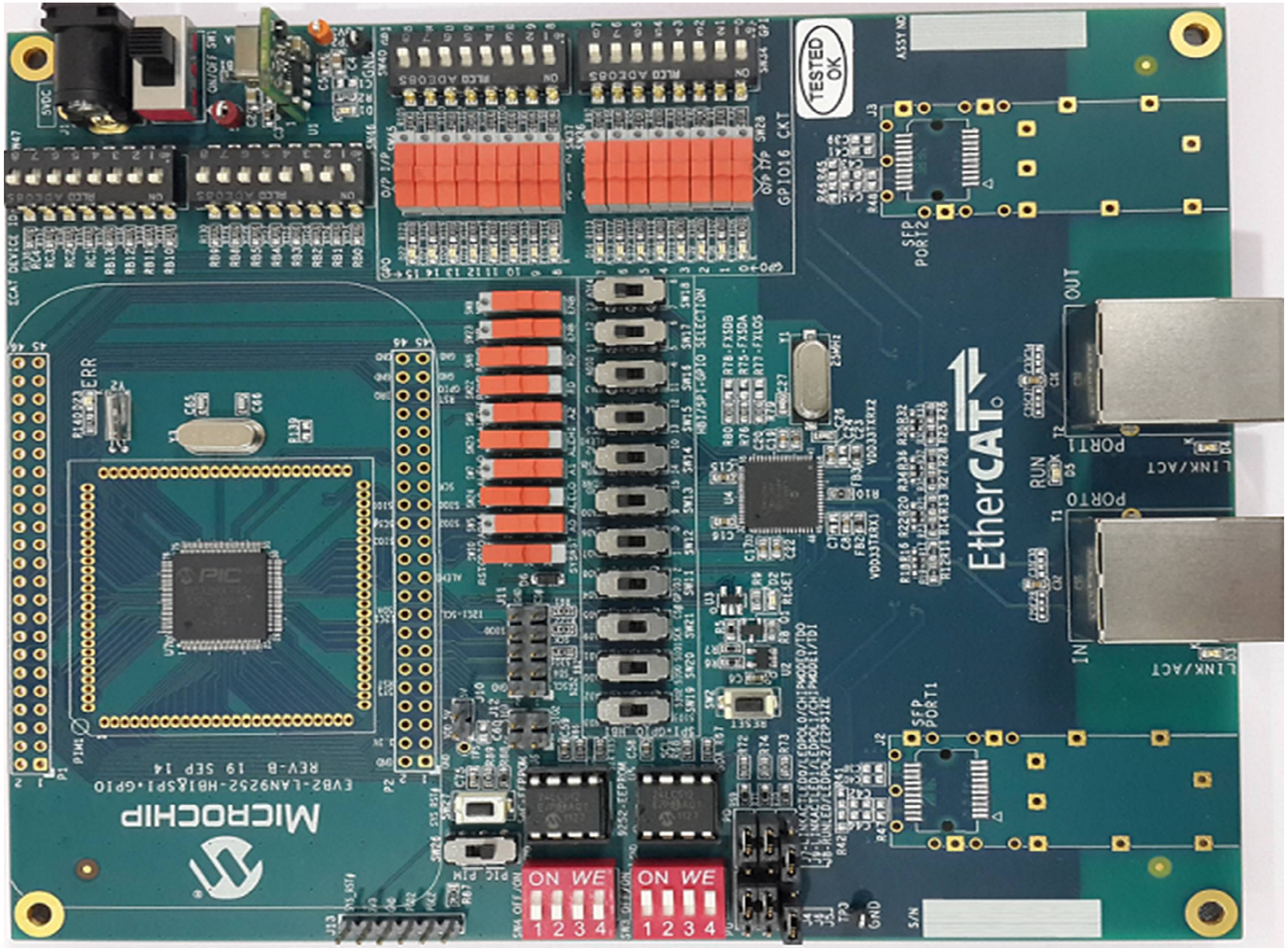
LAN9252- DIG-IO Interface

2-Port EtherCAT Slave Controller with DIGIO Interface

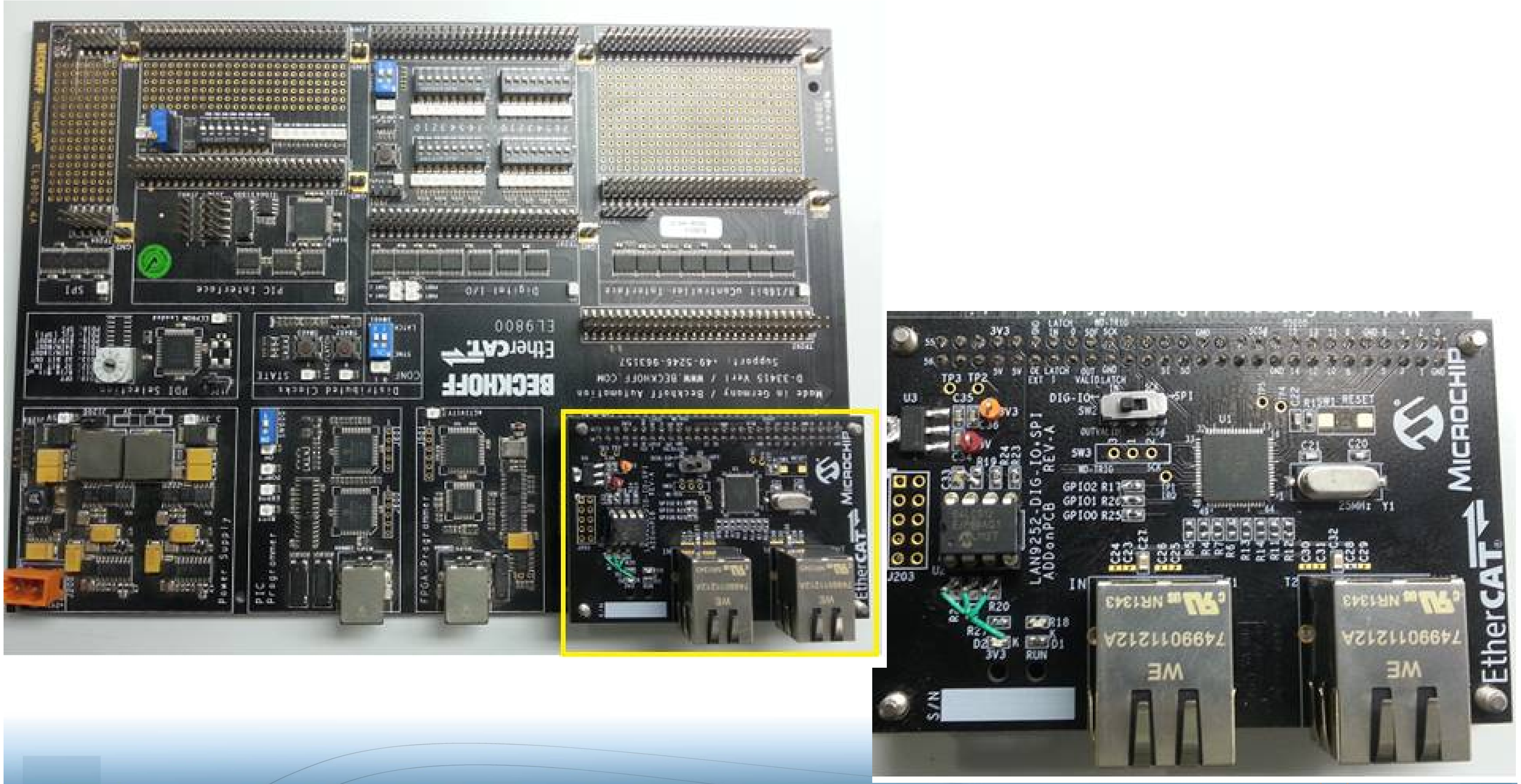


Starter Kit PIC32 + LAN9252

2-Port ESC with Integrated EtherCAT PHY's & PIC32MX uC I/F



Beckhoff's EL9800 EVB

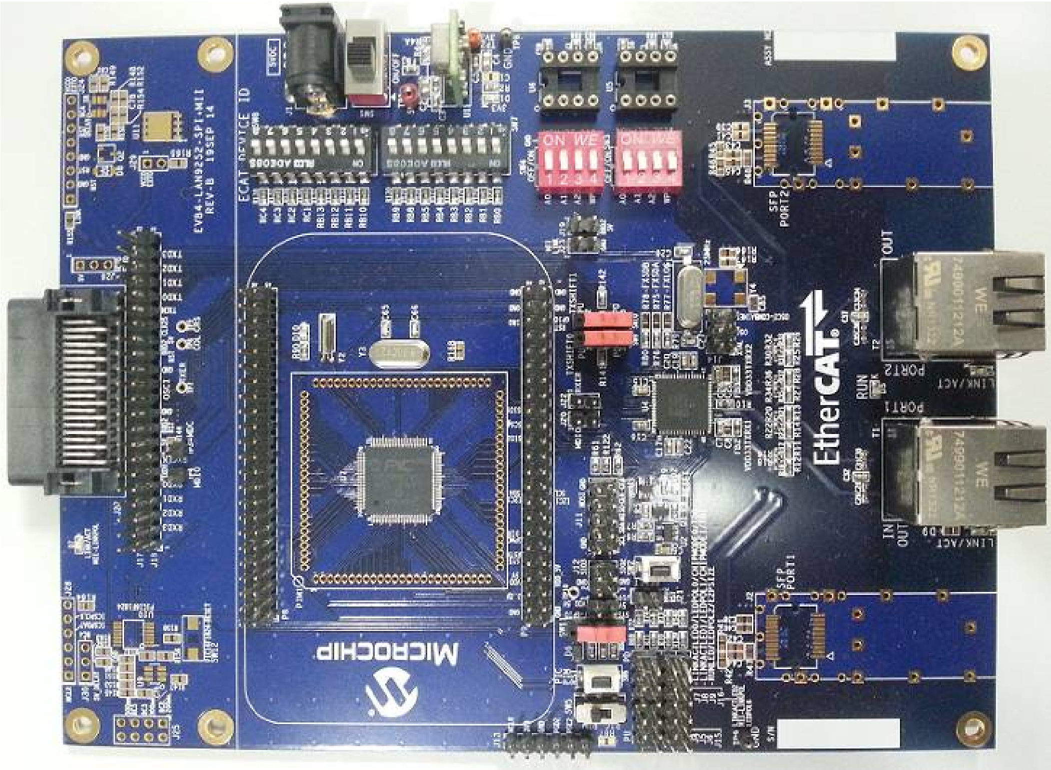


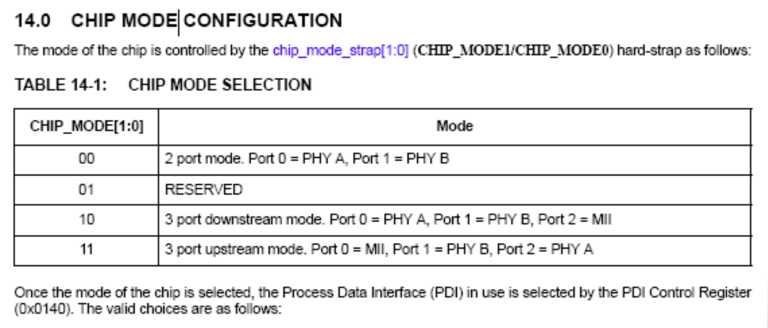
Starter Kit LAN9252 for Explorer 16

- Evaluate with PIC24 and dsPIC33F platform

LAN9252 EVB

3-Port ESC with Integrated Ethernet PHYs -w\ SPI/SQI uC Interface





14.0 CHIP MODE CONFIGURATION

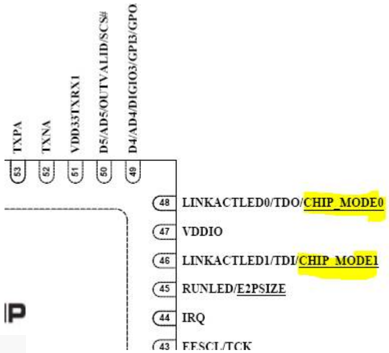
The mode of the chip is controlled by the chip_mode_strap[1:0] (**CHIP_MODE1/CHIP_MODE0**) hard-strap as follows:

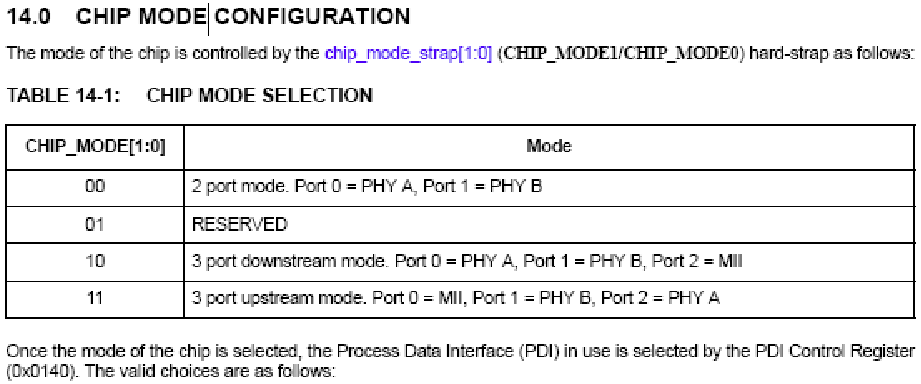
TABLE 14-1: CHIP MODE SELECTION

CHIP_MODE[1:0]	Mode
00	2 port mode. Port 0 = PHY A, Port 1 = PHY B
01	RESERVED
10	3 port downstream mode. Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII
11	3 port upstream mode. Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A

Once the mode of the chip is selected, the Process Data Interface (PDI) in use is selected by the PDI Control Register (0x0140). The valid choices are as follows:

3 port Connection





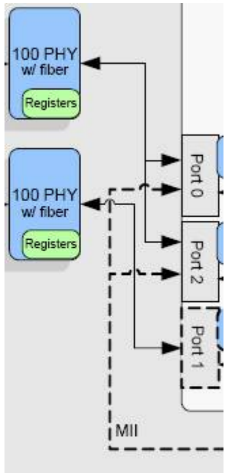
14.0 CHIP MODE CONFIGURATION

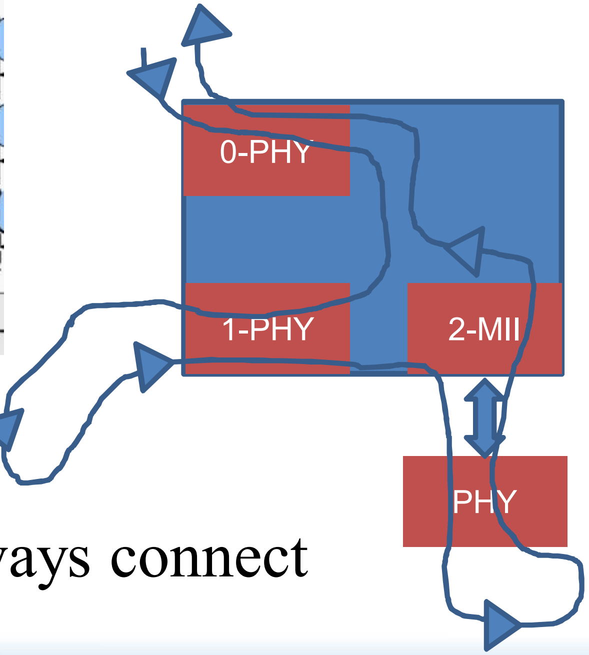
The mode of the chip is controlled by the chip_mode_strap[1:0] (CHIP_MODE1/CHIP_MODE0) hard-strap as follows:

TABLE 14-1: CHIP MODE SELECTION

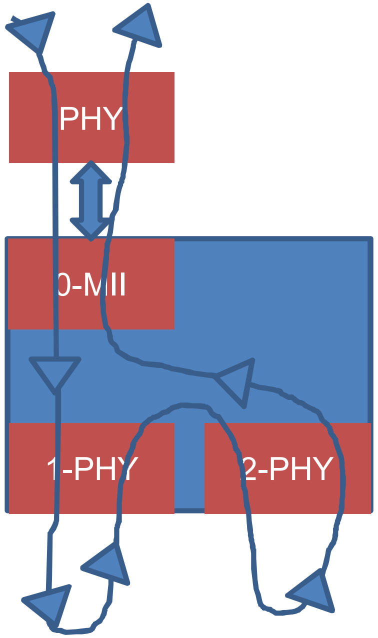
CHIP_MODE[1:0]	Mode
00	2 port mode. Port 0 = PHY A, Port 1 = PHY B
01	RESERVED
10	3 port downstream mode. Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII
11	3 port upstream mode. Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A

Once the mode of the chip is selected, the Process Data Interface (PDI) in use is selected by the PDI Control Register (0x0140). The valid choices are as follows:





Mode =10

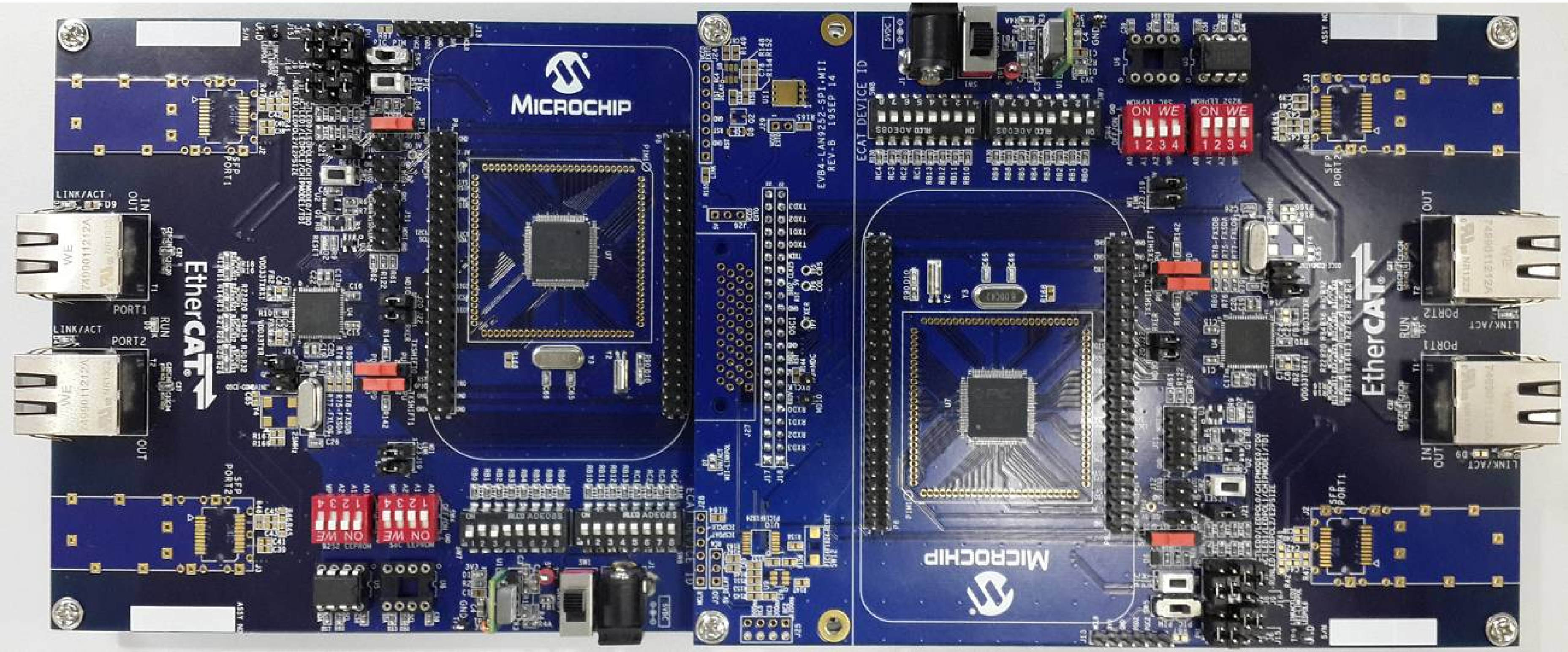


Mode =11

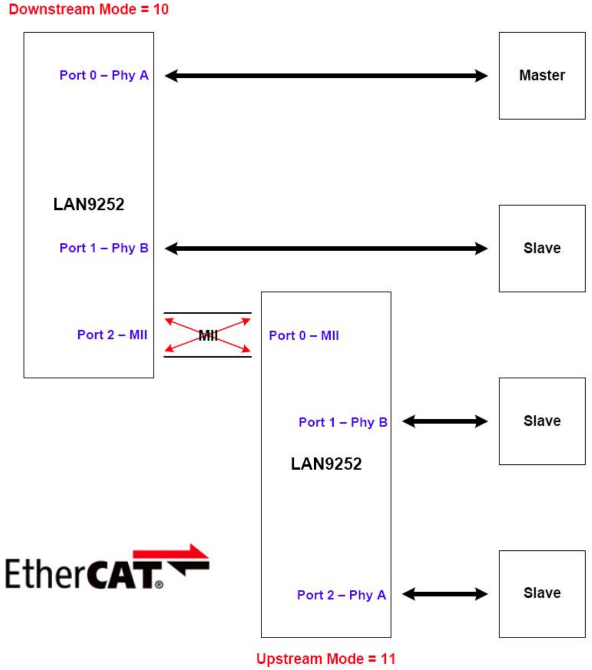
Port 0 always connect to master

LAN9252 EVB

4-Port ESC with Integrated Ethernet PHYs -w\ SPI/SQI uC Interface

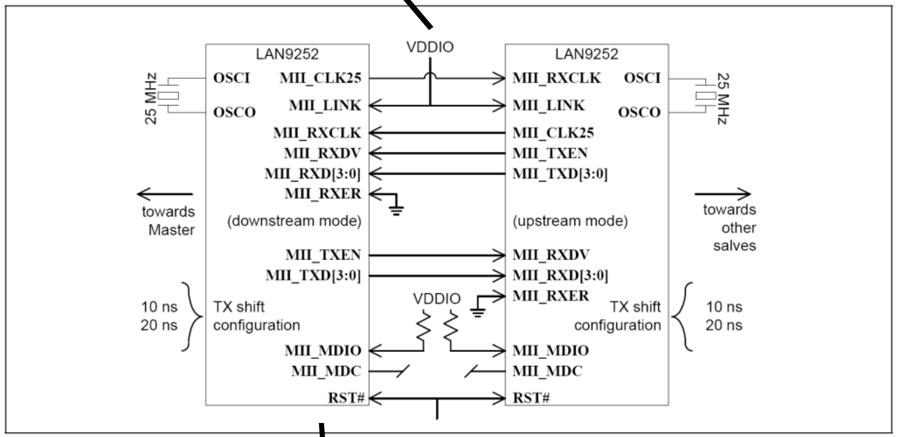


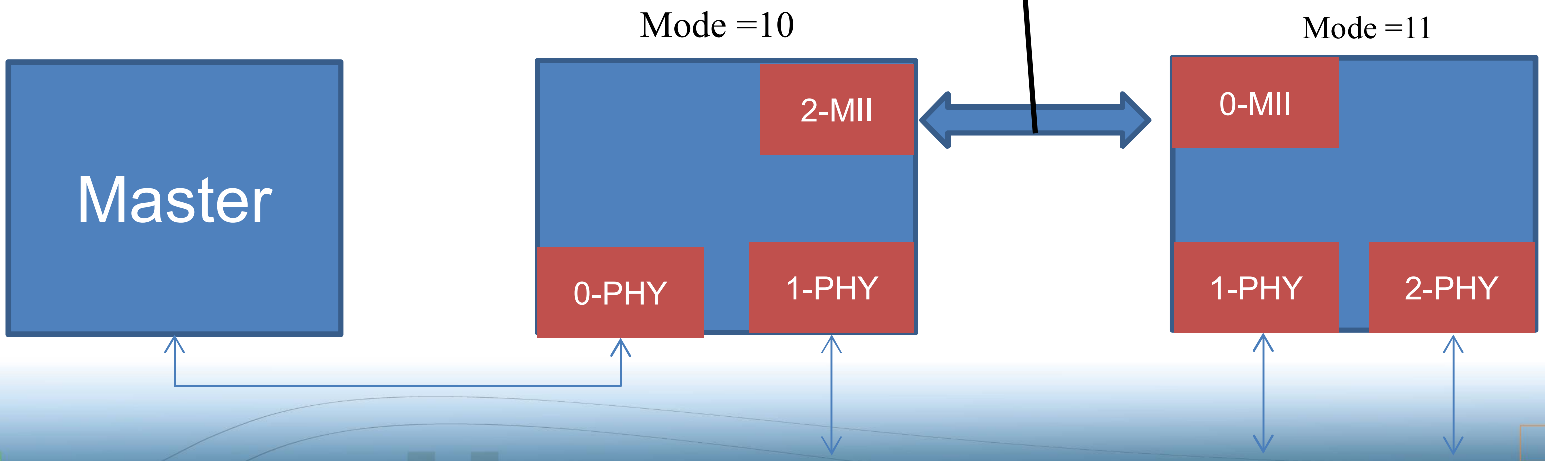
4 port Connection



MII_LINK = 0 when MII_LINKPOL = 0
MII_LINK = 1 when MII_LINKPOL = 1

FIGURE 12-6: ETHERCAT BACK-TO-BACK MII CONNECTION





MICROCHIP

Regional Training Centers

LAN9252介紹

DC 與同步

DC 與同步

- 分散時鐘 (DC) 主要是將每一個從站的系統時鐘調整一致, 通常第一個從站當作是**Reference clock**
- **DC**提供以下功能
  - 系統時間：從2000.1.1+500年(64 bit @ “ns”) Or 4.2S (32bit @ “ns”)
  - 參考時鐘
  - 本地時鐘drift, compensation, wire delay offset ..
- 同步是將每一個從站彼此間的**OUTPUT/ INPUT**進行
  - 沒有同步→Free Run
  - 有 Jitter 的同步→Sync to Sync manager
  - 精密的同步→ Sync to DC

LATCH/SYNC Signal Definition

SYNC/LATCH are multiplexed on the same pin .

LATCH

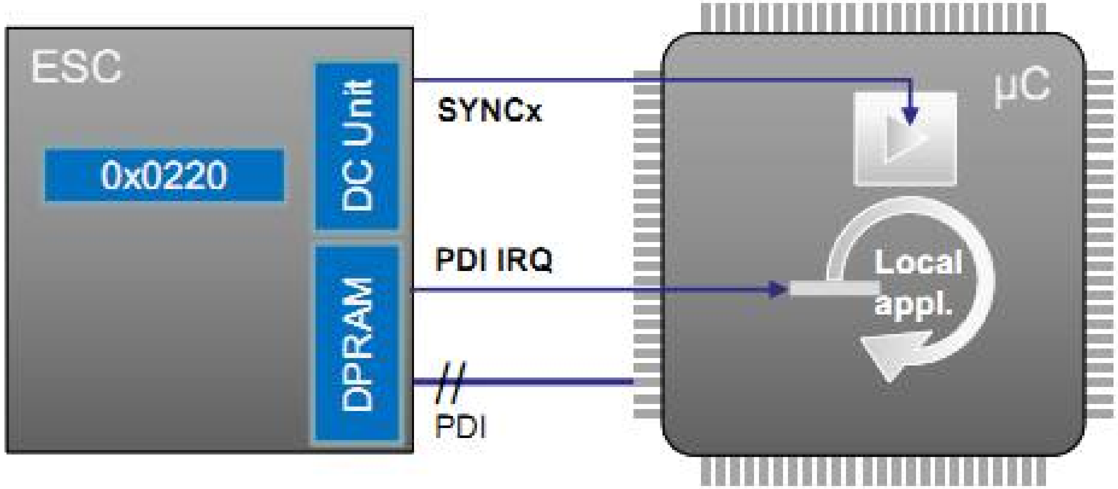
- **The EtherCAT Core provides two input pins (LATCH0 and LATCH1) which are used for time stamping of external events.**
- **Both rising edge and falling edge time stamps are recorded.**
- **These pins are shared with the SYNC0 and SYNC1 output pins, which are used to indicate the occurrence of time events**

SYNC

- **The SYNC0 and SYNC1 states can be mapped into the State of DC SYNC0 and State of DC SYNC1 bits of the AL Event Request Register.**
- **The SYNC0 and SYNC1 pulse length is controlled via the Pulse Length of SyncSignals Register.**

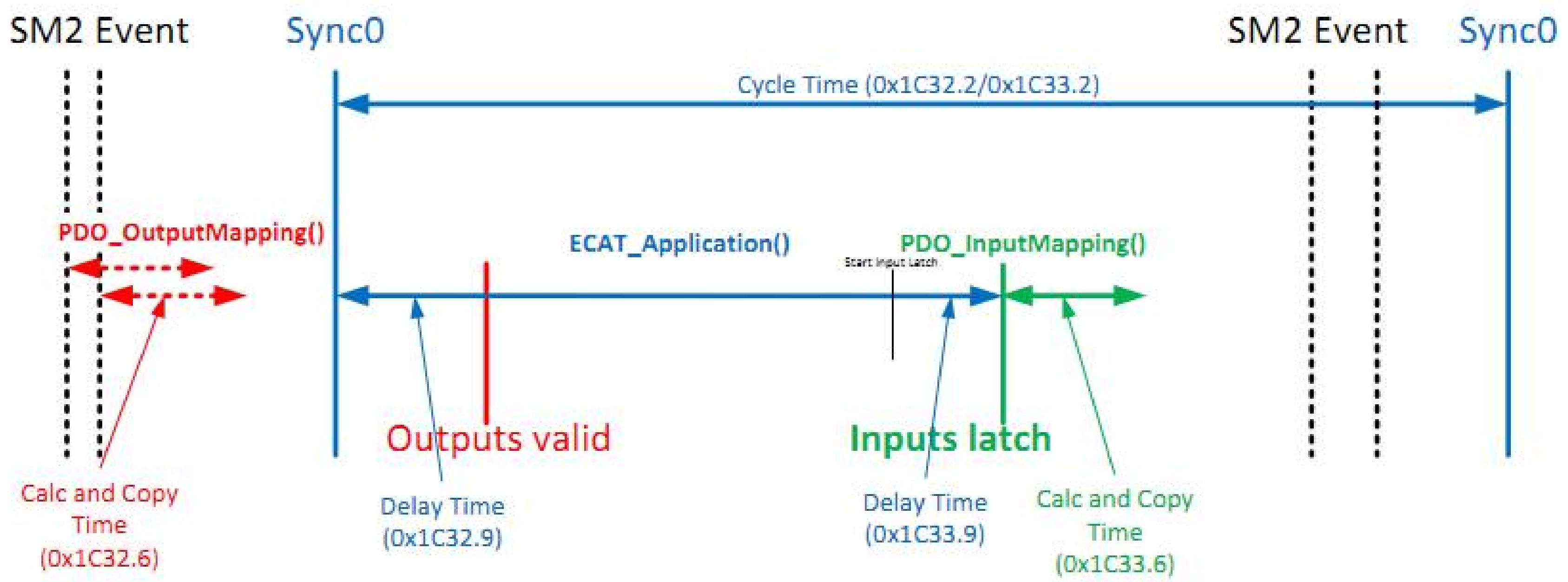
Synchronization with SOC

- Synchronization with Distributed Clock
  - Local application in µC can be triggered by PDI IRQ or polling the SM-Event Register
  - Setting of Outputs or latching of inputs shall be triggered by Sync0-Signal from ESC



Synchronization with SOC

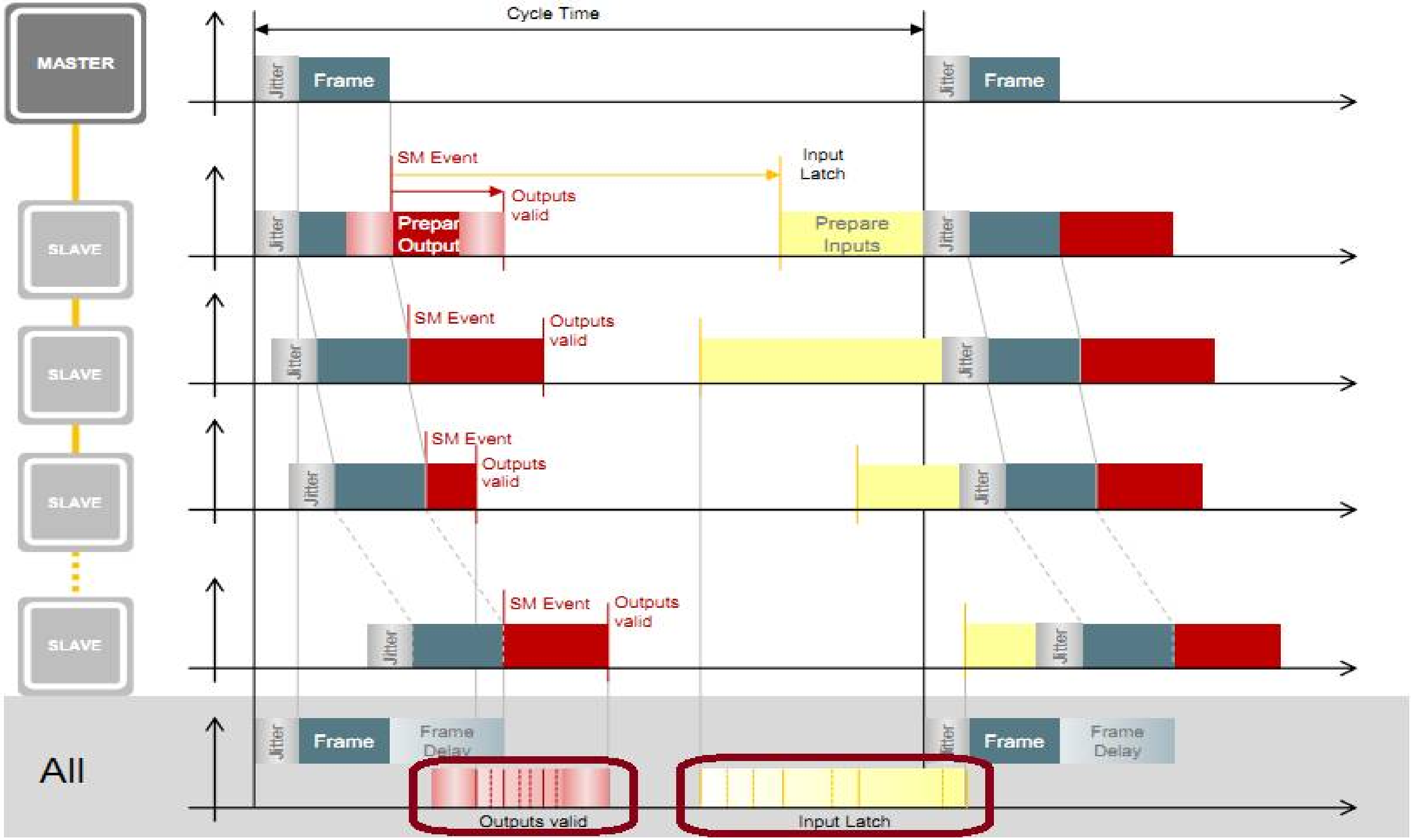
1. Sync 0 Event is used for Synchronization
2. output process data mapping is triggered by the SM2 event
3. ECAT_Application to set the output values



Regional Training Centers

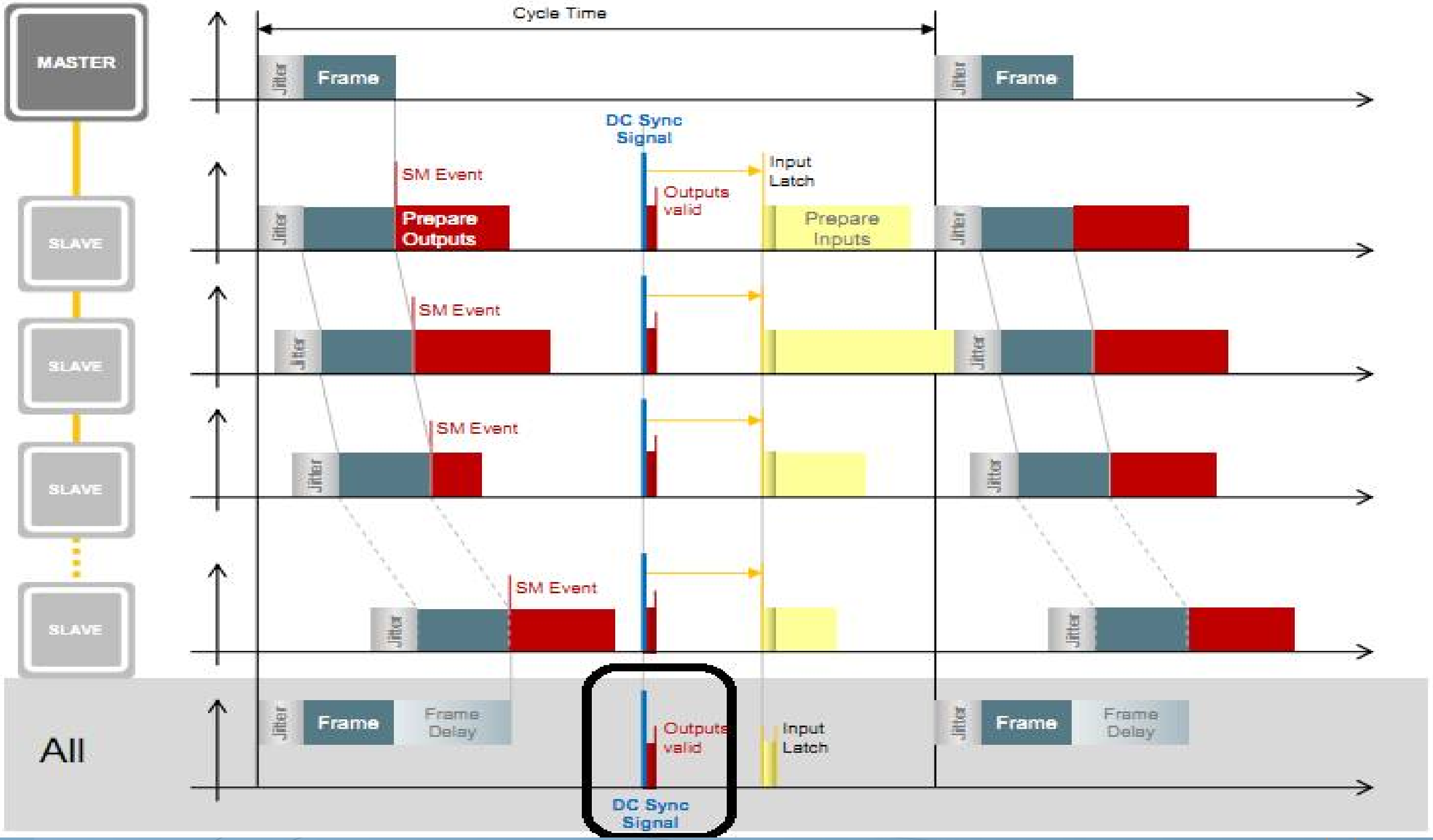
Synchronization- Disabled

- With Sync disabled, outputs valid from each slave at different time.



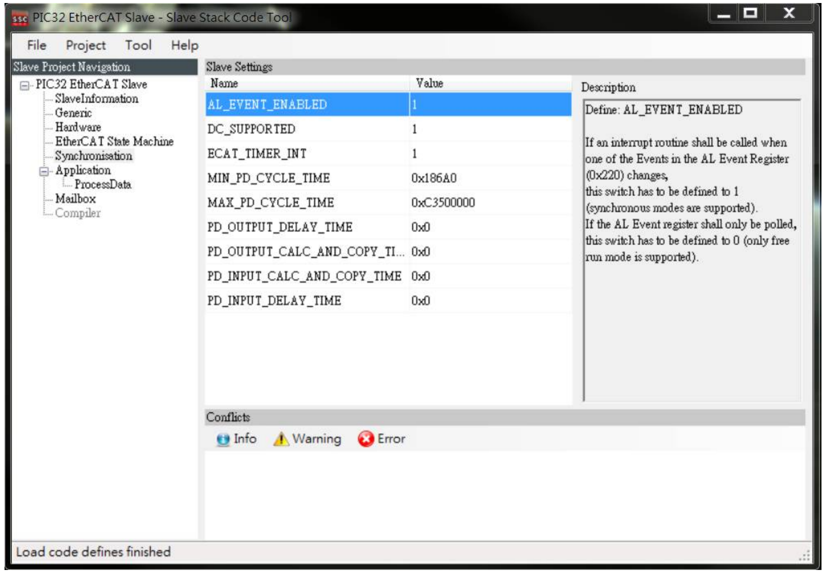
Synchronization- Enabled

- With Sync enabled, outputs valid from each slave at same time.
- Precise synchronization achieved between all slaves (<<1us)



Enable DC

- 在SSC內設定
- 在TWINCAT內也必須設定



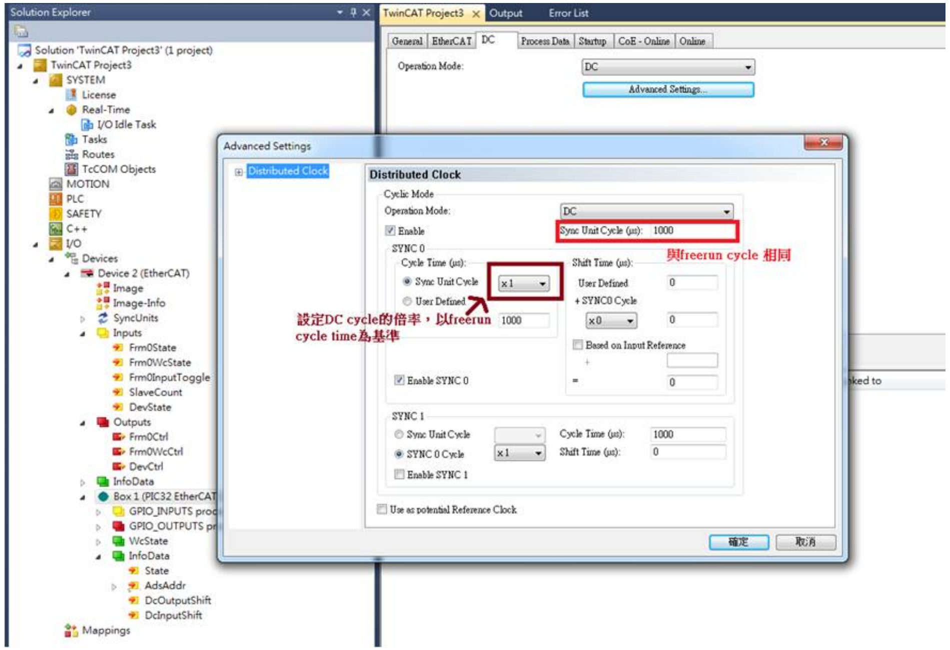
Name	Value
AL_EVENT_ENABLED	1
DC_SUPPORTED	1
ECAT_TIMER_INT	1
MIN_PD_CYCLE_TIME	0x186A0
MAX_PD_CYCLE_TIME	0xC3500000
PD_OUTPUT_DELAY_TIME	0x0
PD_OUTPUT_CALC_AND_COPY_TI...	0x0
PD_INPUT_CALC_AND_COPY_TIME	0x0
PD_INPUT_DELAY_TIME	0x0

Description

Define: AL_EVENT_ENABLED

If an interrupt routine shall be called when one of the Events in the AL Event Register (0x220) changes, this switch has to be defined to 1 (synchronous modes are supported). If the AL Event register shall only be polled, this switch has to be defined to 0 (only free run mode is supported).

Load code defines finished



Operation Mode: DC

Distributed Clock

Cyclic Mode
Operation Mode: DC
☑ Enable
Sync Unit Cycle (µs): 1000

與freerun cycle 相同

SYNC 0
Cycle Time (µs):
● Sync Unit Cycle x 1
○ User Defined 1000

設定DC cycle的倍率，以freerun cycle time為基準

Shift Time (µs):
User Defined 0
+ SYNC0 Cycle x 0 0
☐ Based on Input Reference
= 0
☑ Enable SYNC 0

SYNC 1
○ Sync Unit Cycle
● SYNC 0 Cycle x 1
Cycle Time (µs): 1000
Shift Time (µs): 0
☐ Enable SYNC 1

☐ Use as potential Reference Clock

MICROCHIP

Regional Training Centers

LAN9252介紹

Hardware注意事項

Regional Training Centers

LAN9252 : PDI Interfaces

- **Digital I/O Mode (DIGIO)**
  - Supports 16 digital I/O’s
    - 16 Inputs
    - 16 Outputs
    - Mixed Inputs/Outputs
    - 16 Bi-directional
  - Provides six control signals for Handshake

- **Microcontroller Mode**
  - Supports HBI 8/16 bit parallel bus interface
  - Supports SPI/SQI modes.

不同PDI的選定

- 透過EEPROM或暫存器設定

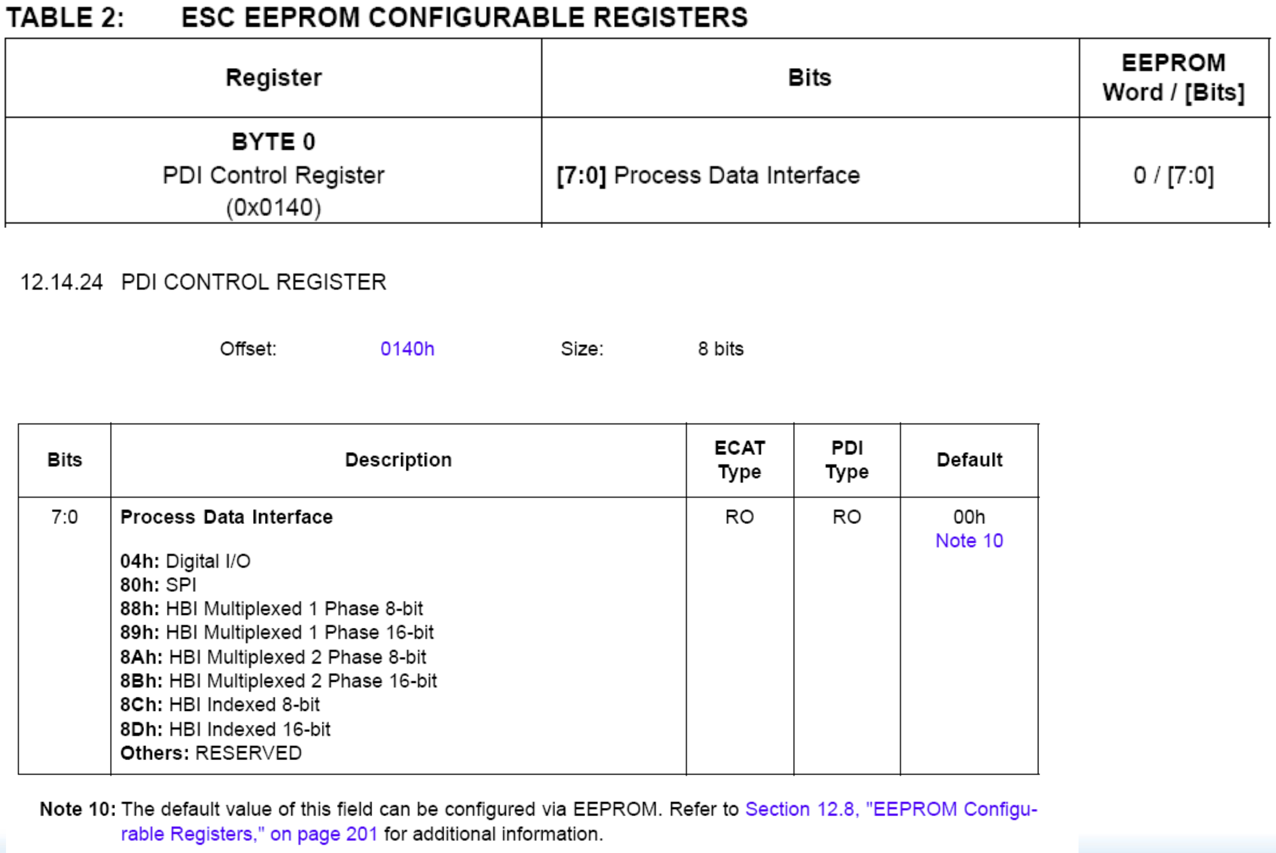


TABLE 2: ESC EEPROM CONFIGURABLE REGISTERS

Register	Bits	EEPROM Word / [Bits]
BYTE 0 PDI Control Register (0x0140)	**[7:0]** Process Data Interface	0 / [7:0]

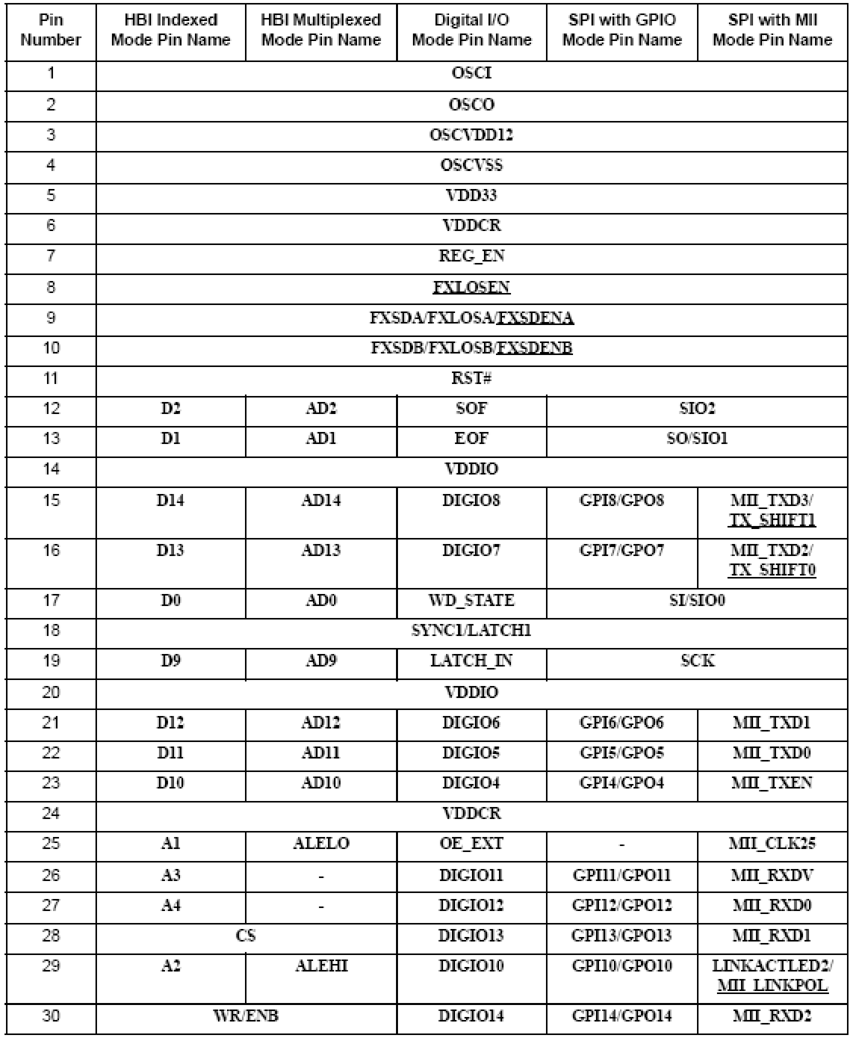
12.14.24 PDI CONTROL REGISTER

Offset: 0140h Size: 8 bits

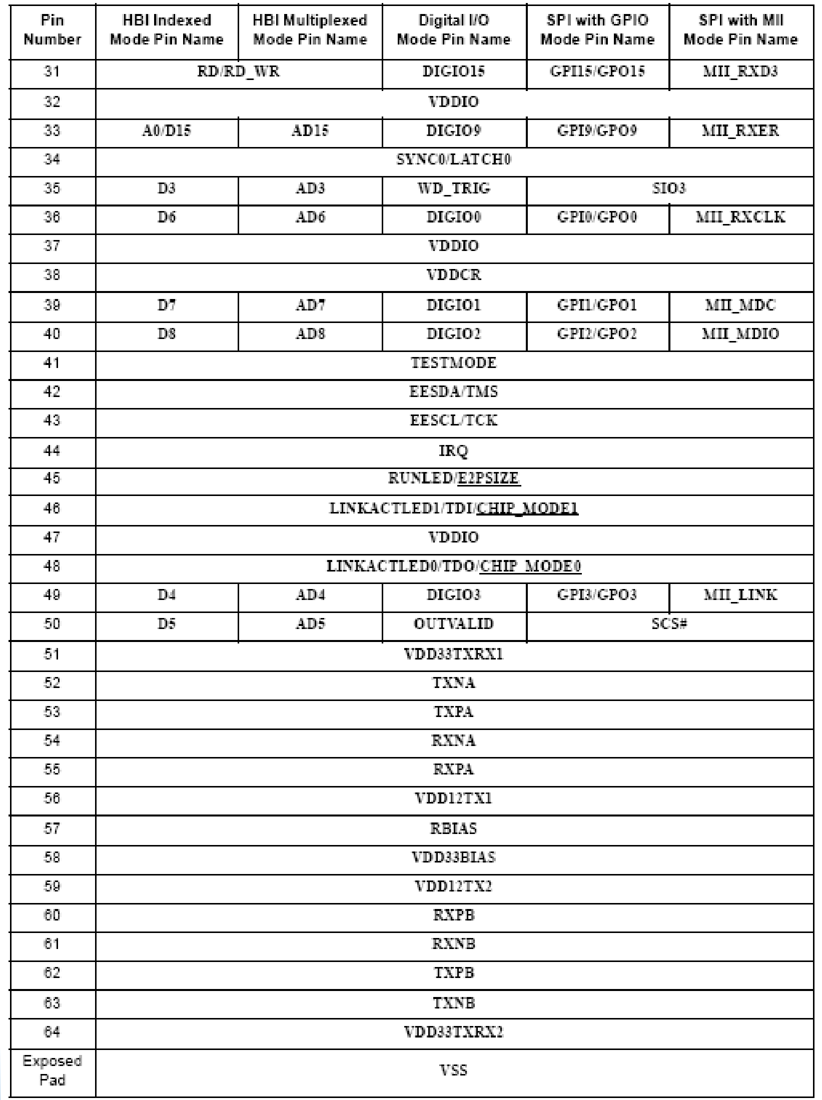
Bits	Description	ECAT Type	PDI Type	Default
7:0	**Process Data Interface** **04h:** Digital I/O **80h:** SPI **88h:** HBI Multiplexed 1 Phase 8-bit **89h:** HBI Multiplexed 1 Phase 16-bit **8Ah:** HBI Multiplexed 2 Phase 8-bit **8Bh:** HBI Multiplexed 2 Phase 16-bit **8Ch:** HBI Indexed 8-bit **8Dh:** HBI Indexed 16-bit **Others:** RESERVED	RO	RO	00h Note 10

Note 10: The default value of this field can be configured via EEPROM. Refer to Section 12.8, "EEPROM Configurable Registers," on page 201 for additional information.

不同PDI間的 pin assignment



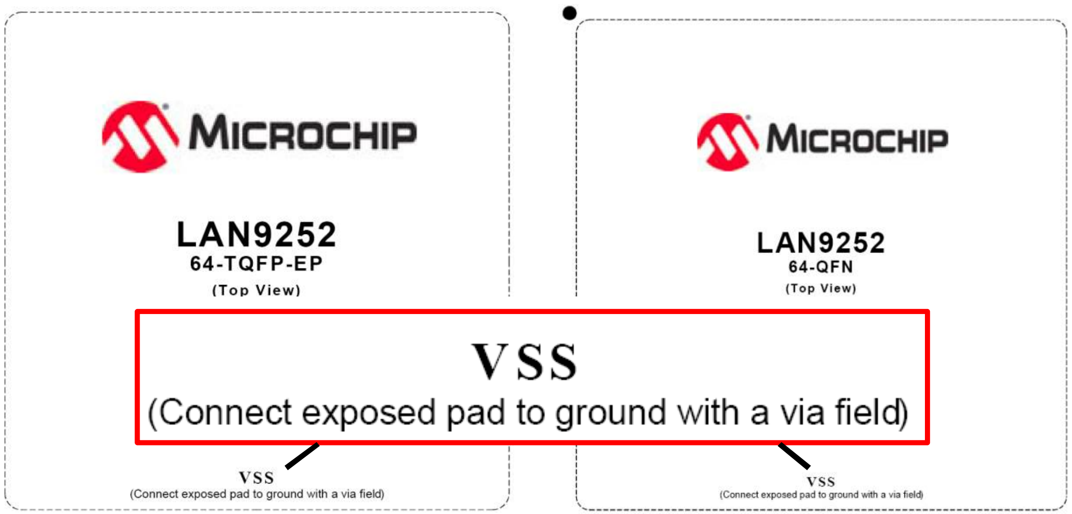
Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
1	OSCI				
2	OSCO				
3	OSCVDD12				
4	OSCVSS				
5	VDD33				
6	VDDCR				
7	REG_EN				
8	FXLOSEN				
9	FXSDA/FXLOSA/FXSDENA				
10	FXSDB/FXLOSB/FXSDENB				
11	RST#				
12	D2	AD2	SOF	SIO2	
13	D1	AD1	EOF	SO/SIO1	
14	VDDIO				
15	D14	AD14	DIGIO8	GPI8/GPO8	MII_TXD3/ TX_SHIFT1
16	D13	AD13	DIGIO7	GPI7/GPO7	MII_TXD2/ TX_SHIFT0
17	D0	AD0	WD_STATE	SI/SIO0	
18	SYNC1/LATCH1				
19	D9	AD9	LATCH_IN	SCK	
20	VDDIO				
21	D12	AD12	DIGIO6	GPI6/GPO6	MII_TXD1
22	D11	AD11	DIGIO5	GPI5/GPO5	MII_TXD0
23	D10	AD10	DIGIO4	GPI4/GPO4	MII_TXEN
24	VDDCR				
25	A1	ALELO	OE_EXT	-	MII_CLK25
26	A3	-	DIGIO11	GPI11/GPO11	MII_RXDV
27	A4	-	DIGIO12	GPI12/GPO12	MII_RXD0
28	CS		DIGIO13	GPI13/GPO13	MII_RXD1
29	A2	ALEHI	DIGIO10	GPI10/GPO10	LINKACTLED2/ MII_LINKPOL
30	WR/ENB		DIGIO14	GPI14/GPO14	MII_RXD2



Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	Digital I/O Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name
31	RD/RD_WR		DIGIO15	GPI15/GPO15	MII_RXD3
32	VDDIO				
33	A0/D15	AD15	DIGIO9	GPI9/GPO9	MII_RXER
34	SYNC0/LATCH0				
35	D3	AD3	WD_TRIG	SIO3	
36	D6	AD6	DIGIO0	GPI0/GPO0	MII_RXCLK
37	VDDIO				
38	VDDCR				
39	D7	AD7	DIGIO1	GPI1/GPO1	MII_MDC
40	D8	AD8	DIGIO2	GPI2/GPO2	MII_MDIO
41	TESTMODE				
42	EESDA/TMS				
43	EESCL/TCK				
44	IRQ				
45	RUNLED/E2PSIZE				
46	LINKACTLED1/TDI/CHIP_MODE1				
47	VDDIO				
48	LINKACTLED0/TDO/CHIP_MODE0				
49	D4	AD4	DIGIO3	GPI3/GPO3	MII_LINK
50	D5	AD5	OUTVALID	SCS#	
51	VDD33TXRX1				
52	TXNA				
53	TXPA				
54	RXNA				
55	RXPA				
56	VDD12TX1				
57	RBIAS				
58	VDD33BIAS				
59	VDD12TX2				
60	RXPB				
61	RXNB				
62	TXPB				
63	TXNB				
64	VDD33TXRX2				
Exposed Pad	VSS				

Hardware 注意事項

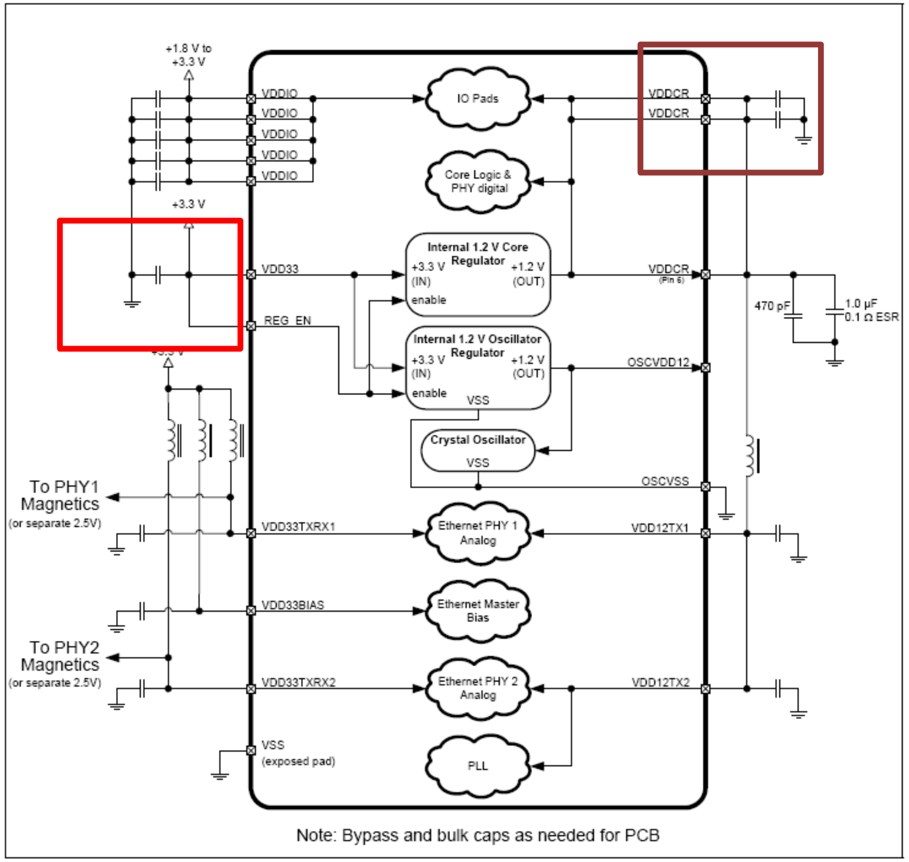
- 最近**debug** 板子 有兩個注意事項
  - ◆ **Thermal pad** 忘記接地**, if not →** VDDCR = 1.6V and RST keep cycling.
  - ◆ EEPROM應該選512 byte, E2PSiZE → Hi


MICROCHIP
LAN9252
64-TQFP-EP
(Top View)
VSS
(Connect exposed pad to ground with a via field)
MICROCHIP
LAN9252
64-QFN
(Top View)
VSS
(Connect exposed pad to ground with a via field)

VSS
(Connect exposed pad to ground with a via field)

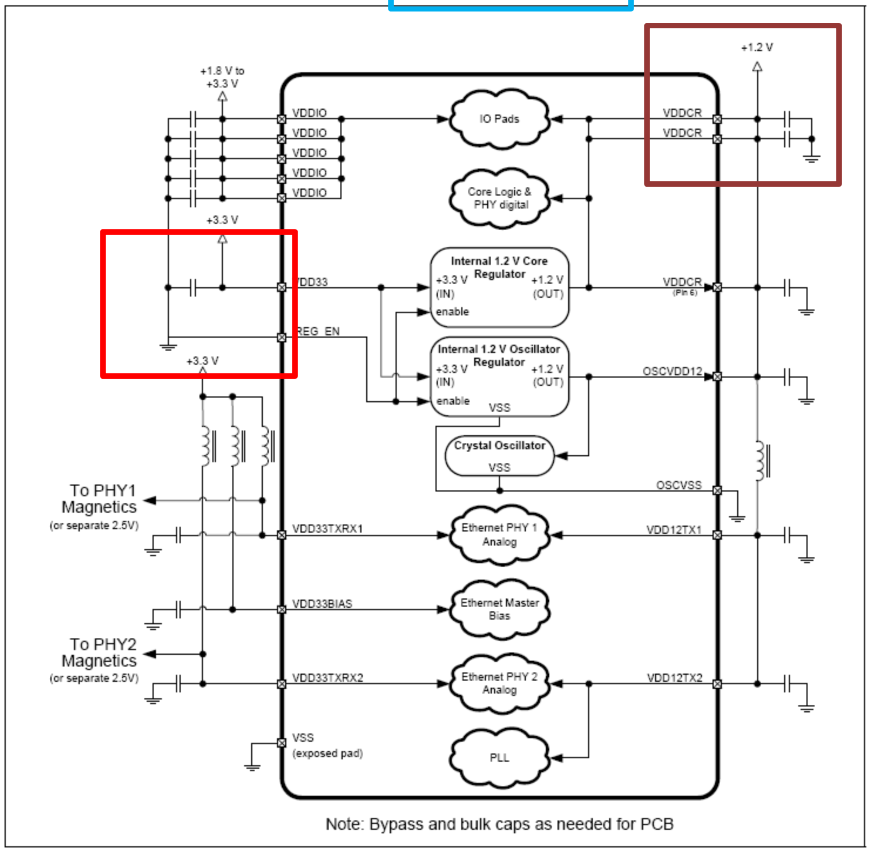
Power connection

FIGURE 4-1: POWER CONNECTIONS - REGULATORS ENABLED



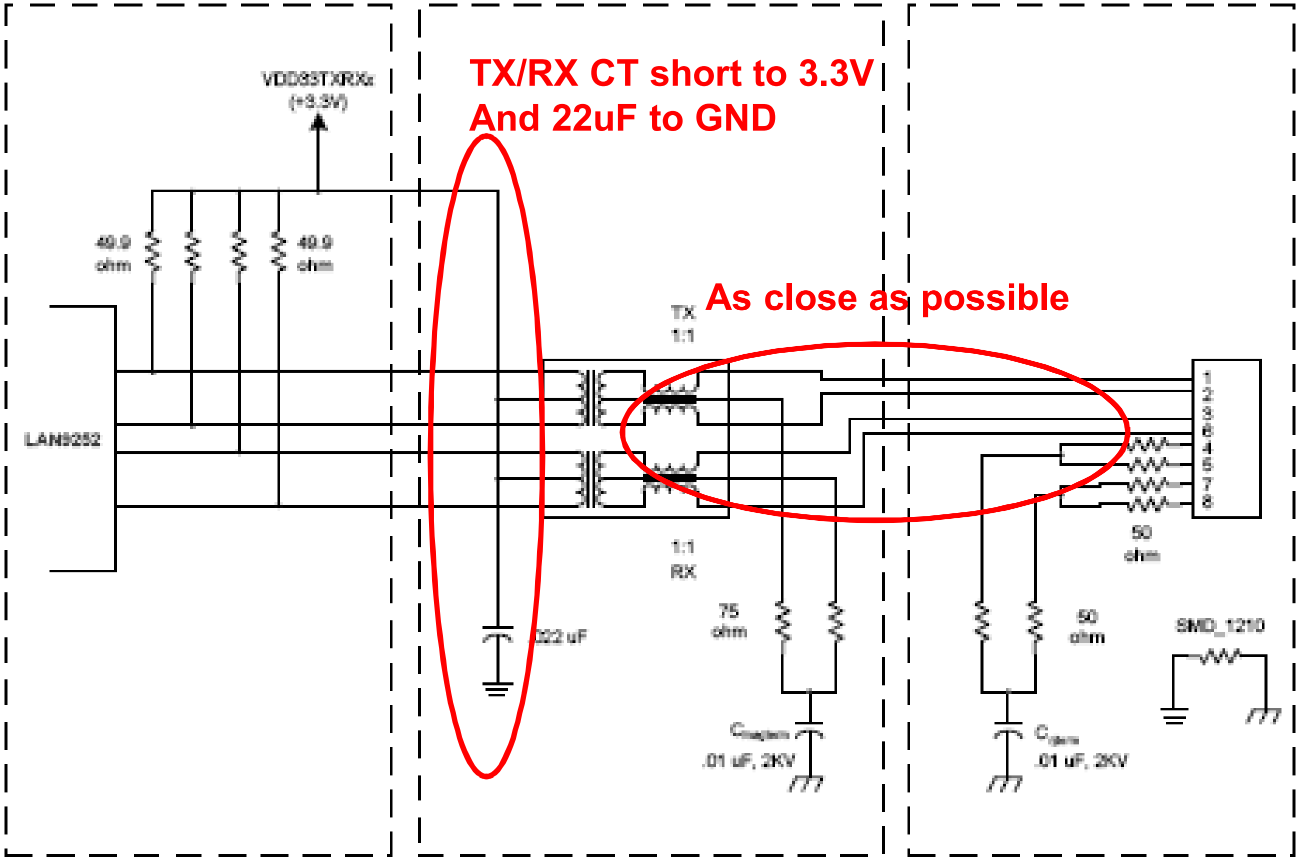
Note: Bypass and bulk caps as needed for PCB

FIGURE 4-2: POWER CONNECTIONS - REGULATORS DISABLED



Note: Bypass and bulk caps as needed for PCB

PHY/Magnetic/RJ45



TX/RX CT short to 3.3V
And 22uF to GND

As close as possible

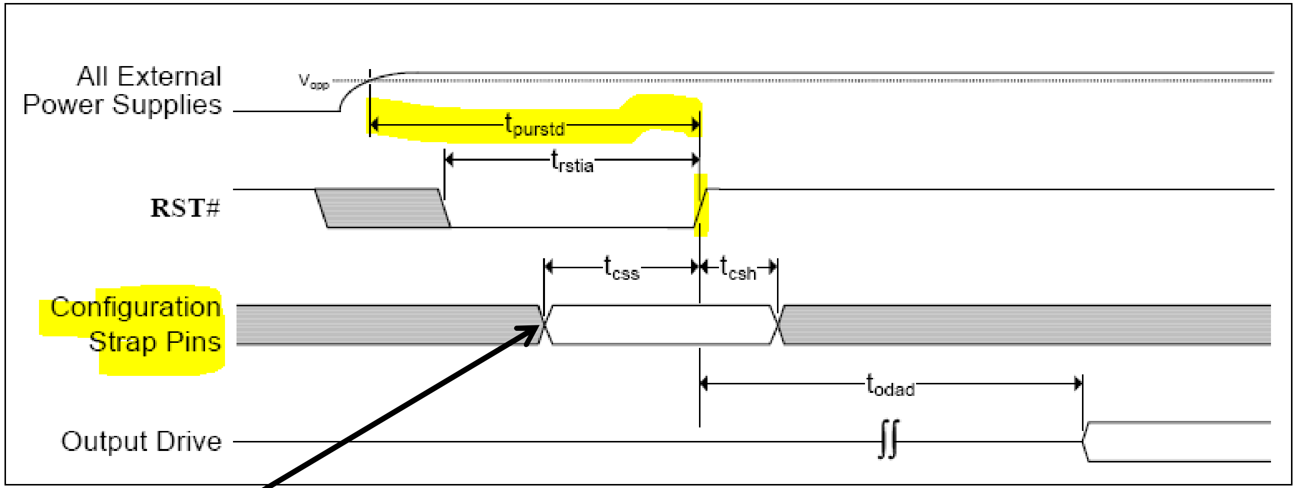
Locate the four 49.9 ohm differential terminations close to the LAN9252

Locate these three resistors and two caps close to the magnetics

Locate all these components close to the RJ45 connector

RST circuit

FIGURE 18-4: RST# PIN CONFIGURATION STRAP LATCHING TIMING



Configuration data should be ready after Power into Vopp + 15ms (max)

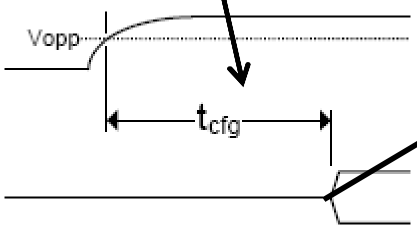


TABLE 18-10: RST# PIN CONFIGURATION STRAP LATCHING TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{purstd}	External power supplies at operational level to RST# deassertion	25			ms
t_{rstia}	RST# input assertion time	200	-	-	µs
t_{css}	Configuration strap pins setup to RST# deassertion	200	-	-	ns
t_{csh}	Configuration strap pins hold after RST# deassertion	10	-	-	ns
t_{odad}	Output drive after deassertion	3	-	-	us

Note: The clock input must be stable prior to RST# deassertion.

Note: Device configuration straps are latched as a result of RST# assertion. Refer to Section 6.2.1, "Chip-Level Resets," on page 39 for details.

Note: Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 18.6.4, "Power-On and Configuration Strap Timing" apply.

Crystal spec

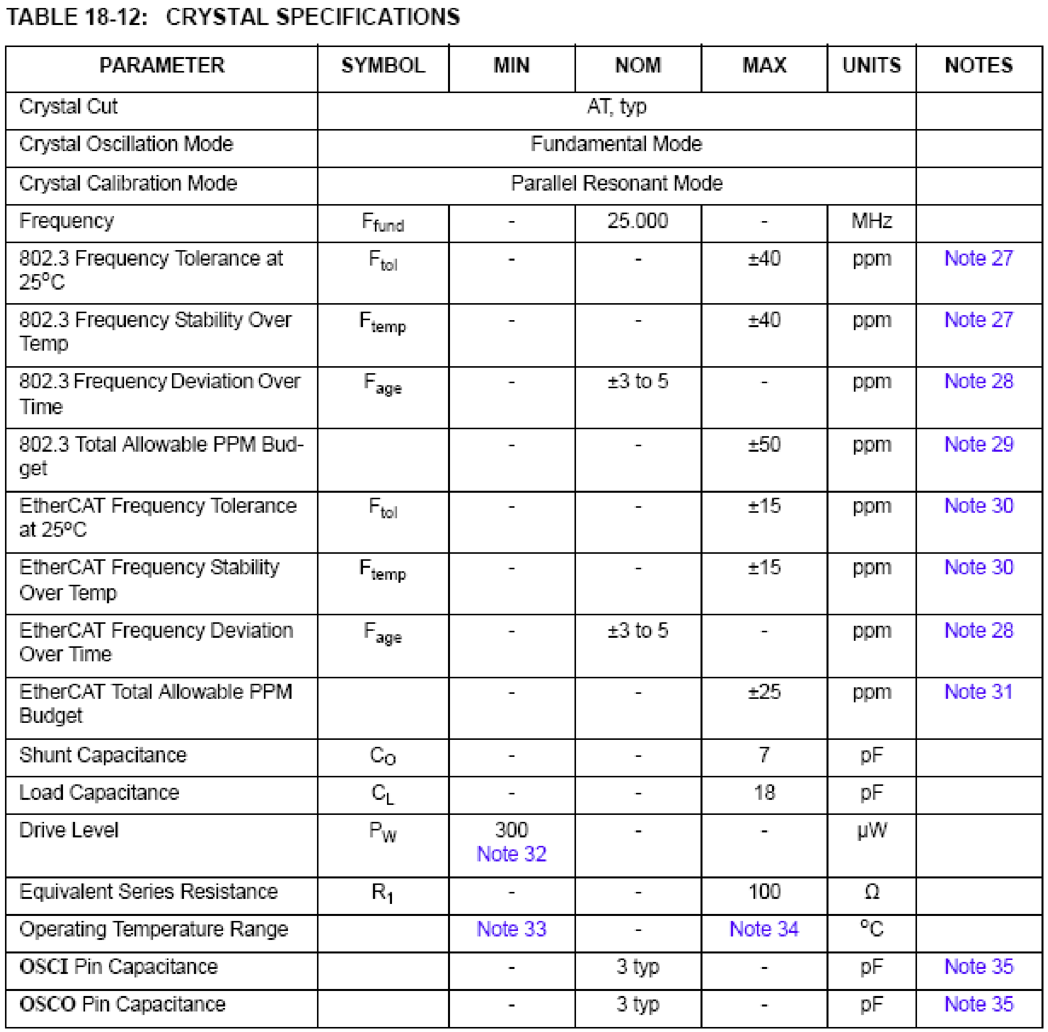


TABLE 18-12: CRYSTAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
802.3 Frequency Tolerance at 25°C	F_{tol}	-	-	±40	ppm	Note 27
802.3 Frequency Stability Over Temp	F_{temp}	-	-	±40	ppm	Note 27
802.3 Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	ppm	Note 28
802.3 Total Allowable PPM Budget		-	-	±50	ppm	Note 29
EtherCAT Frequency Tolerance at 25°C	F_{tol}	-	-	±15	ppm	Note 30
EtherCAT Frequency Stability Over Temp	F_{temp}	-	-	±15	ppm	Note 30
EtherCAT Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	ppm	Note 28
EtherCAT Total Allowable PPM Budget		-	-	±25	ppm	Note 31
Shunt Capacitance	C_O	-	-	7	pF	
Load Capacitance	C_L	-	-	18	pF	
Drive Level	P_W	300 Note 32	-	-	µW	
Equivalent Series Resistance	R_1	-	-	100	Ω	
Operating Temperature Range		Note 33	-	Note 34	°C	
OSCI Pin Capacitance		-	3 typ	-	pF	Note 35
OSCO Pin Capacitance		-	3 typ	-	pF	Note 35

The minimum drive level requirement PW is reduced to 100 uW with the addition of a 500 Ω series resistor,
if CO < 5 pF, CL <12 pF and R1<80 Ω
Else, it should follow 300uW

maximum allowable values for frequency tolerance and frequency stability are application dependent. Since any particular application must meet the EtherCAT ±25 ppm Total PPM Budget, the combination of these two values must be approximately ±15 ppm (allowing for aging).

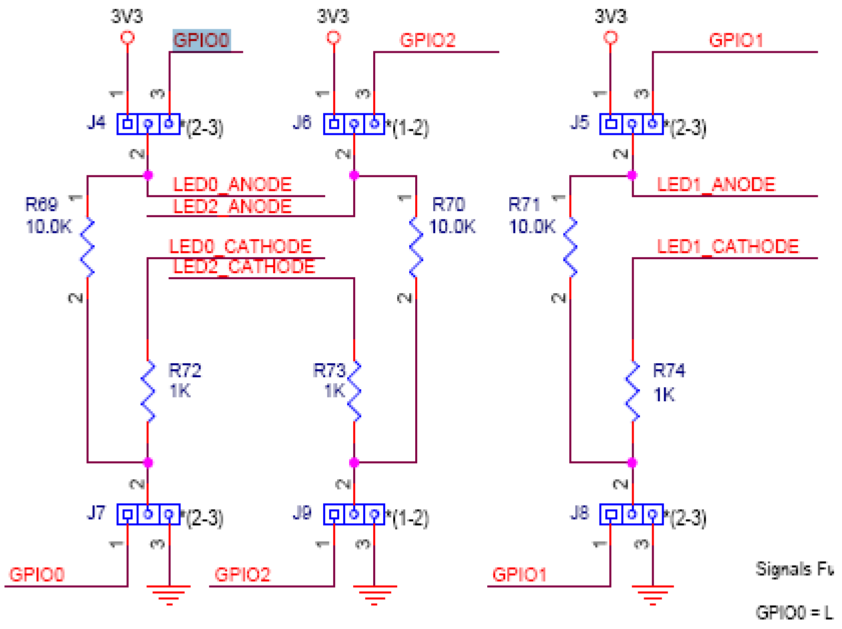
Regional Training Centers

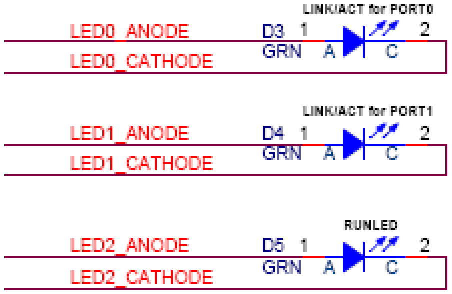
Hardware note

- Crystal :25ppm
- Suggest to put “RUN” LED on PCB
- port 0 (pin 48) never be an unused port
- Slaves communicate without SII EEPROM / invalid SII EEPROM content is possible but need specify PDI configuration (EEPROM offset 0) for correct PDI W/R

困擾的LED問題

- 很多客戶詢問EVB LED問題



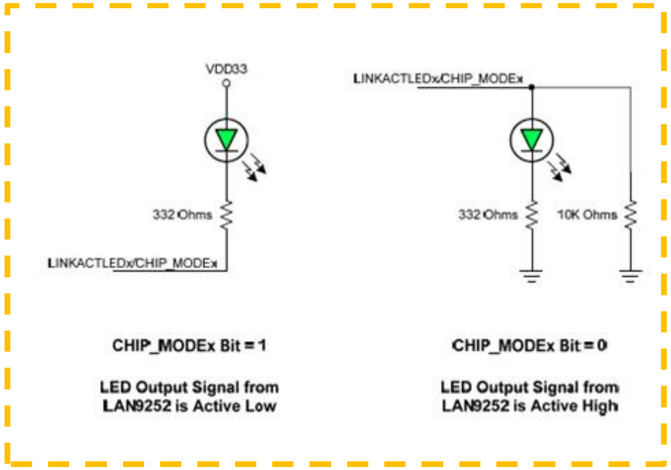


LED application note

- All LED are share pin with another strap function. This strapping function works only when chip change from Rest→ Normal
- 9252, 2 PHY(PHY A,B) and 3 logic port (Port 0,1,2)
- 4 LED pins in LAN9252
    - **Pin 29:LINKACTLED2/MII_LINKPOL→ Port 2 status**
    - **Pin 45:RUNLED/E2PSIZE**
    - **Pin 46:LINKACTLED1/Chip_Mode1→ Port 1 status**
    - **Pin 48:LINKACTLED0/Chip_Mode0 → Port 0 status**
- External PHY LED can be controlled either LAN9252 or PHY it's self

LED application note

- 先決定 strapping function
- 由strapping function 決定LED 是active hi or low
- Active hi , low circuit as following

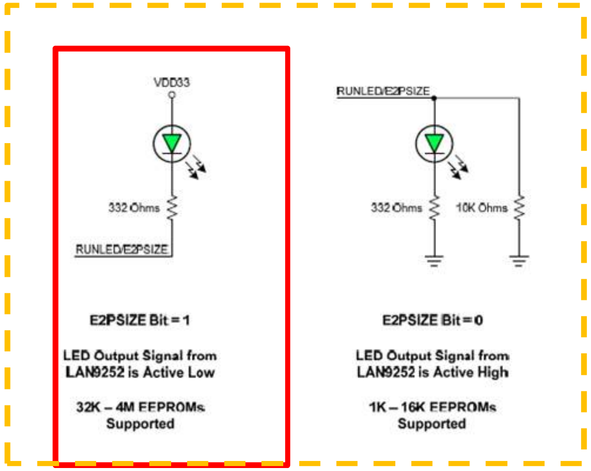


CHIP_MODEx Bit = 1

LED Output Signal from LAN9252 is Active Low

CHIP_MODEx Bit = 0

LED Output Signal from LAN9252 is Active High



E2PSIZE Bit = 1

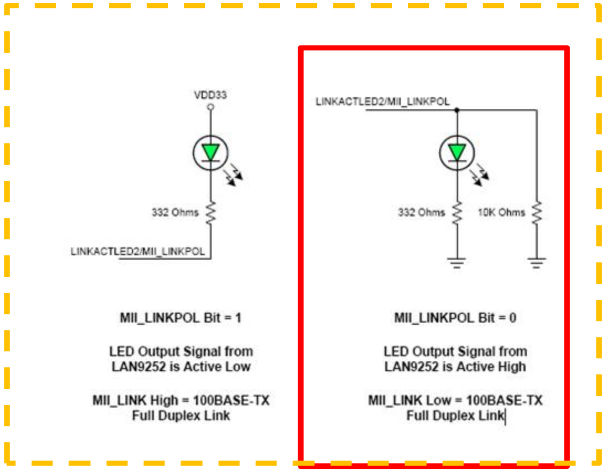
LED Output Signal from LAN9252 is Active Low

32K – 4M EEPROMs Supported

E2PSIZE Bit = 0

LED Output Signal from LAN9252 is Active High

1K – 16K EEPROMs Supported



MII_LINKPOL Bit = 1

LED Output Signal from LAN9252 is Active Low

MII_LINK High = 100BASE-TX Full Duplex Link

MII_LINKPOL Bit = 0

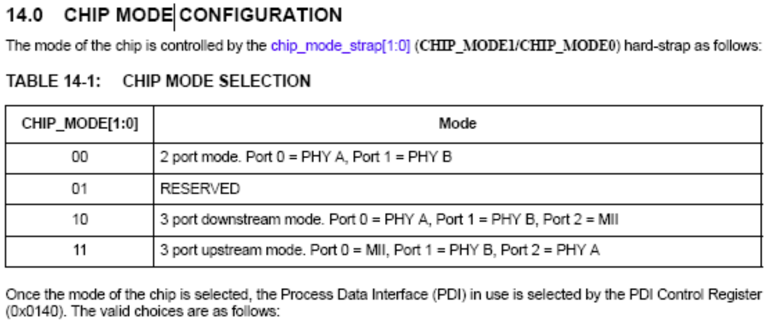
LED Output Signal from LAN9252 is Active High

MII_LINK Low = 100BASE-TX Full Duplex Link

Regional Training Centers

LED application note for 3 port

- **Chip_mode 在不同設定下的意義**
- **Modes**
  - ***For Modes [00] & [10] :***
    Port 0 is connected to Phy A
    Port 1 is connected to Phy B
    Port 2 is connected to the MII channel
  - ***For Mode [11]:***
    Port 0 is connected to the MII channel
    Port 1 is connected to Phy B
    Port 2 is connected to Phy A



14.0 CHIP MODE CONFIGURATION

The mode of the chip is controlled by the chip_mode_strap[1:0] (CHIP_MODE1/CHIP_MODE0) hard-strap as follows:

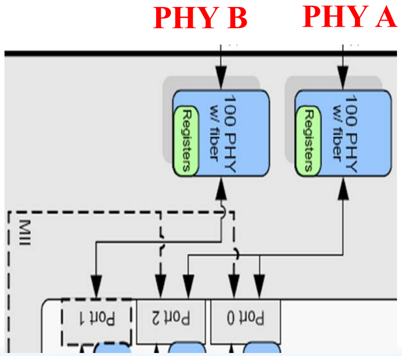
TABLE 14-1: CHIP MODE SELECTION

CHIP_MODE[1:0]	Mode
00	2 port mode. Port 0 = PHY A, Port 1 = PHY B
01	RESERVED
10	3 port downstream mode. Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII
11	3 port upstream mode. Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A

Once the mode of the chip is selected, the Process Data Interface (PDI) in use is selected by the PDI Control Register (0x0140). The valid choices are as follows:

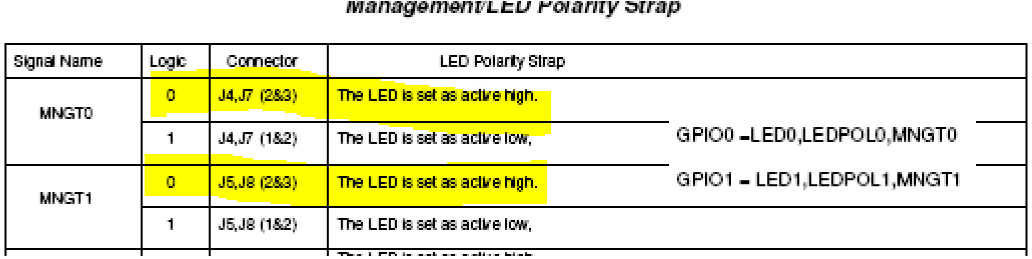
- **Pins**
  - **Pin 29:LINKACTLED2/MII_LINKPOL→ Port 2 status**
  - **Pin 45:RUNLED/E2PSIZE**
  - **Pin 46:LINKACTLED1/Chip_Mode1→ Port 1 status**
  - **Pin 48:LINKACTLED0/Chip_Mode0 → Port 0 status**

接LED active/h/l circuit



Example

- Normal two port, chip_mode:00

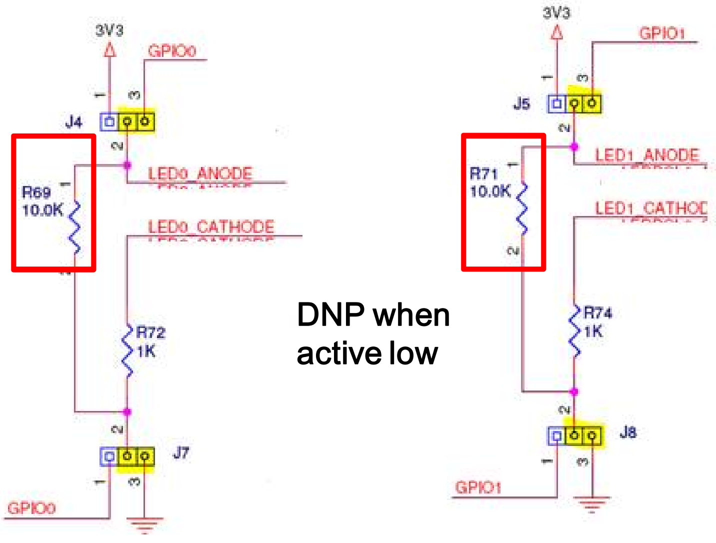


Management/LED Polarity Strap

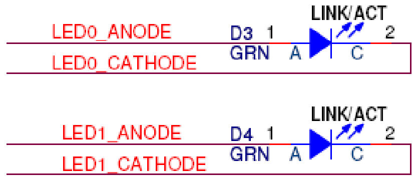
Signal Name	Logic	Connector	LED Polarity Strap
MNGT0	0	J4,J7 (2&3)	The LED is set as active high.
	1	J4,J7 (1&2)	The LED is set as active low,
MNGT1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,

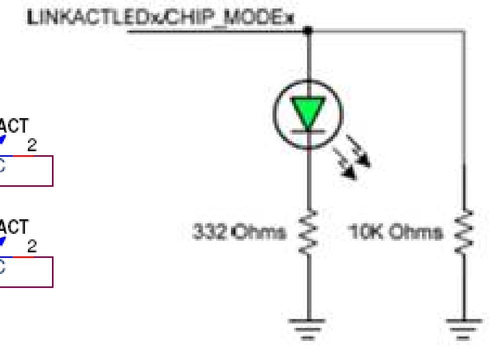
GPIO0 -LED0,LEDPOL0,MNGT0

GPIO1 - LED1,LEDPOL1,MNGT1



DNP when active low





CHIP_MODEx Bit = 0

LED Output Signal from LAN9252 is Active High

MICROCHIP

Regional Training Centers

LAN9252介紹

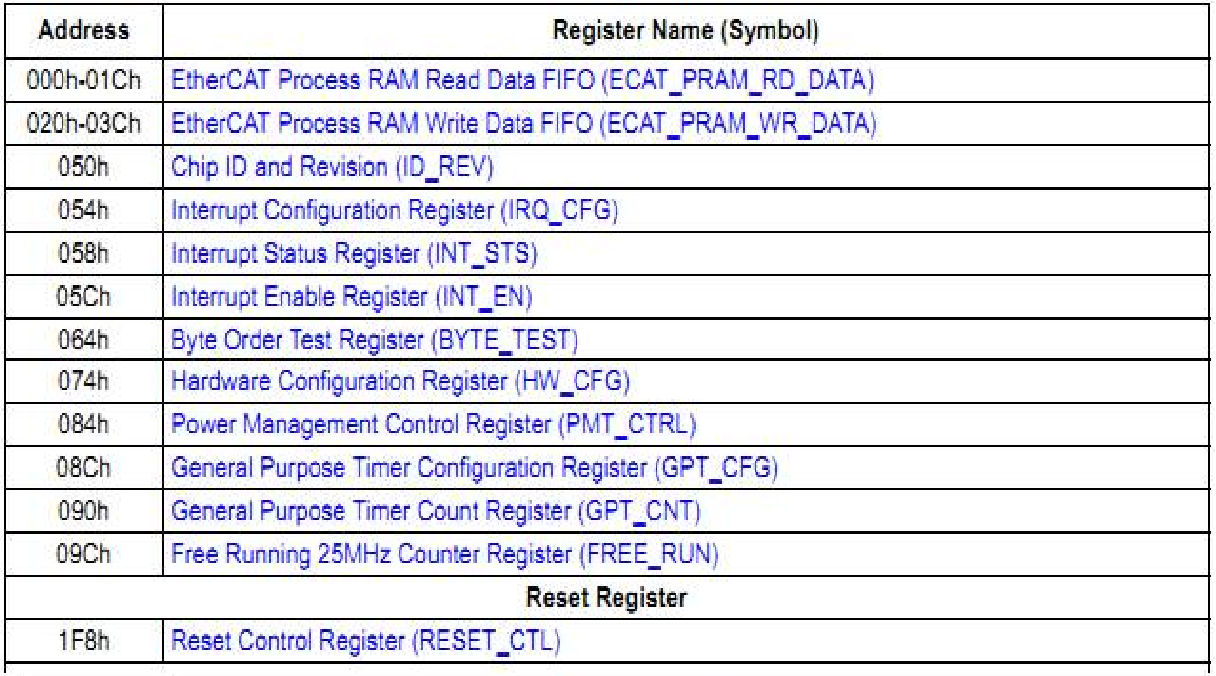
SPI porting notice
(from ET1100 to LAN9252)

LAN9252 Register Access from PDI

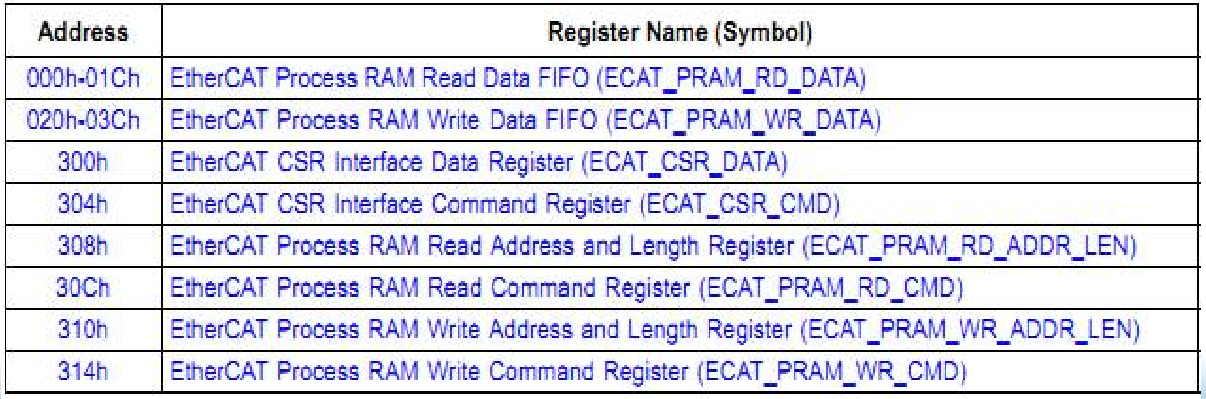
EtherCAT CSR and Process Data RAM Access:

- The EtherCAT CSRs provide register level access to the various parameters of the EtherCAT Core.
- EtherCAT related registers can be classified into two main categories based upon their method of access:
  - ☐ Directly Accessible
  - ☐ indirectly accessible
- These registers provide data/command registers (for access to the indirect EtherCAT Core registers).
- All EtherCAT core registers are indirectly accessible registers.

Directly Accessible Registers



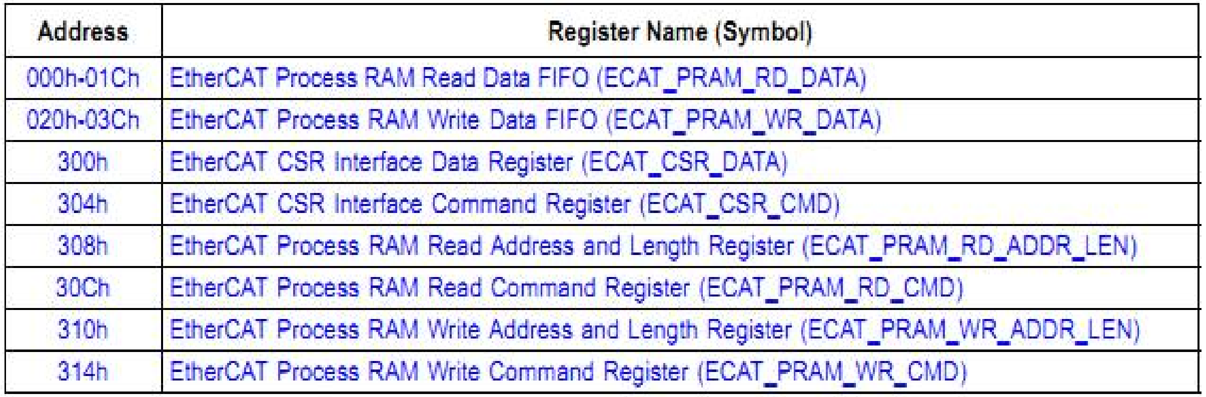
Address	Register Name (Symbol)
000h-01Ch	EtherCAT Process RAM Read Data FIFO (ECAT_PRAM_RD_DATA)
020h-03Ch	EtherCAT Process RAM Write Data FIFO (ECAT_PRAM_WR_DATA)
050h	Chip ID and Revision (ID_REV)
054h	Interrupt Configuration Register (IRQ_CFG)
058h	Interrupt Status Register (INT_STS)
05Ch	Interrupt Enable Register (INT_EN)
064h	Byte Order Test Register (BYTE_TEST)
074h	Hardware Configuration Register (HW_CFG)
084h	Power Management Control Register (PMT_CTRL)
08Ch	General Purpose Timer Configuration Register (GPT_CFG)
090h	General Purpose Timer Count Register (GPT_CNT)
09Ch	Free Running 25MHz Counter Register (FREE_RUN)
Reset Register	
1F8h	Reset Control Register (RESET_CTL)



Address	Register Name (Symbol)
000h-01Ch	EtherCAT Process RAM Read Data FIFO (ECAT_PRAM_RD_DATA)
020h-03Ch	EtherCAT Process RAM Write Data FIFO (ECAT_PRAM_WR_DATA)
300h	EtherCAT CSR Interface Data Register (ECAT_CSR_DATA)
304h	EtherCAT CSR Interface Command Register (ECAT_CSR_CMD)
308h	EtherCAT Process RAM Read Address and Length Register (ECAT_PRAM_RD_ADDR_LEN)
30Ch	EtherCAT Process RAM Read Command Register (ECAT_PRAM_RD_CMD)
310h	EtherCAT Process RAM Write Address and Length Register (ECAT_PRAM_WR_ADDR_LEN)
314h	EtherCAT Process RAM Write Command Register (ECAT_PRAM_WR_CMD)

CSR access

- To perform a read/write of an individual EtherCAT Core register, the read cycle must be initiated by performing a single write to the EtherCAT CSR Interface Command Register (ECAT_CSR_CMD) with the CSR Busy (CSR_BUSY) bit set, the CSR Address (CSR_ADDR) field set to the desired register address, the Read/Write (R_nW) bit set and the CSR Size (CSR_SIZE) field set to the desired size.
- Valid data is available for reading when the CSR Busy (CSR_BUSY) bit is cleared, indicating that the data can be read from the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA).
- Valid data is always aligned into the lowest bits of the EtherCAT CSR Interface Data Register (ECAT_CSR_DATA).



Address	Register Name (Symbol)
000h-01Ch	EtherCAT Process RAM Read Data FIFO (ECAT_PRAM_RD_DATA)
020h-03Ch	EtherCAT Process RAM Write Data FIFO (ECAT_PRAM_WR_DATA)
300h	EtherCAT CSR Interface Data Register (ECAT_CSR_DATA)
304h	EtherCAT CSR Interface Command Register (ECAT_CSR_CMD)
308h	EtherCAT Process RAM Read Address and Length Register (ECAT_PRAM_RD_ADDR_LEN)
30Ch	EtherCAT Process RAM Read Command Register (ECAT_PRAM_RD_CMD)
310h	EtherCAT Process RAM Write Address and Length Register (ECAT_PRAM_WR_ADDR_LEN)
314h	EtherCAT Process RAM Write Command Register (ECAT_PRAM_WR_CMD)

Porting from ET1100 to AN9252

- Refer to AN1907
- Two type of connection is possible
  - HBI
    - Synchronous mode is not supported in LAN9252, only async mode support
    - LAN9252 can be configured as 8-bit indexed mode
    - LAN9252 can be configured as 16-bit indexed mode (A0 pin is not used)
  - SPI (Dual, Quad SPI not support), always as slave

Regional Trainin
Centers

SPI command format in LAN9252

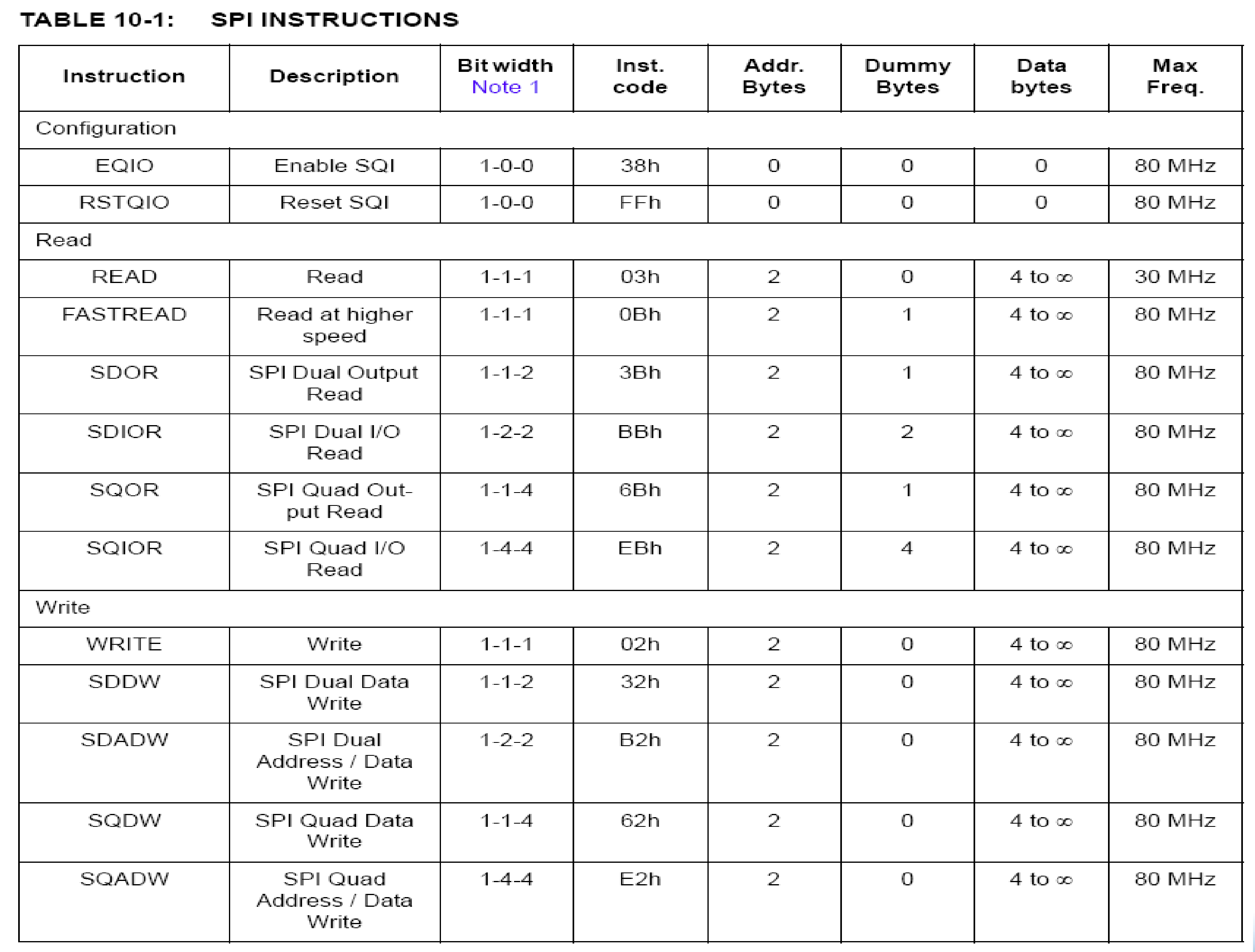
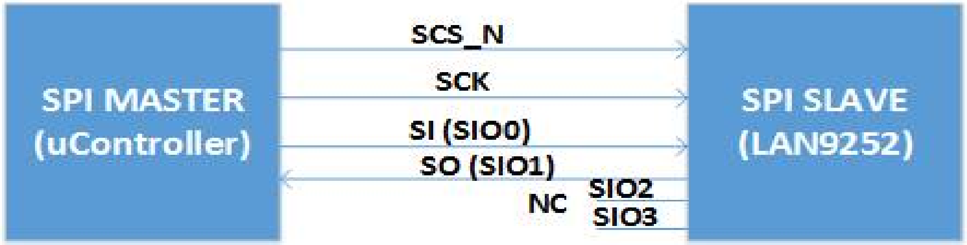


TABLE 10-1: SPI INSTRUCTIONS

Instruction	Description	Bit width Note 1	Inst. code	Addr. Bytes	Dummy Bytes	Data bytes	Max Freq.
Configuration							
EQIO	Enable SQI	1-0-0	38h	0	0	0	80 MHz
RSTQIO	Reset SQI	1-0-0	FFh	0	0	0	80 MHz
Read							
READ	Read	1-1-1	03h	2	0	4 to ∞	30 MHz
FASTREAD	Read at higher speed	1-1-1	0Bh	2	1	4 to ∞	80 MHz
SDOR	SPI Dual Output Read	1-1-2	3Bh	2	1	4 to ∞	80 MHz
SDIOR	SPI Dual I/O Read	1-2-2	BBh	2	2	4 to ∞	80 MHz
SQOR	SPI Quad Output Read	1-1-4	6Bh	2	1	4 to ∞	80 MHz
SQIOR	SPI Quad I/O Read	1-4-4	EBh	2	4	4 to ∞	80 MHz
Write							
WRITE	Write	1-1-1	02h	2	0	4 to ∞	80 MHz
SDDW	SPI Dual Data Write	1-1-2	32h	2	0	4 to ∞	80 MHz
SDADW	SPI Dual Address / Data Write	1-2-2	B2h	2	0	4 to ∞	80 MHz
SQDW	SPI Quad Data Write	1-1-4	62h	2	0	4 to ∞	80 MHz
SQADW	SPI Quad Address / Data Write	1-4-4	E2h	2	0	4 to ∞	80 MHz

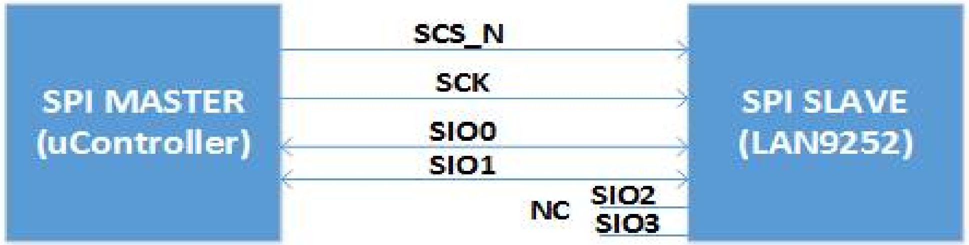
Connection

Serial and FAST READ/WRITE



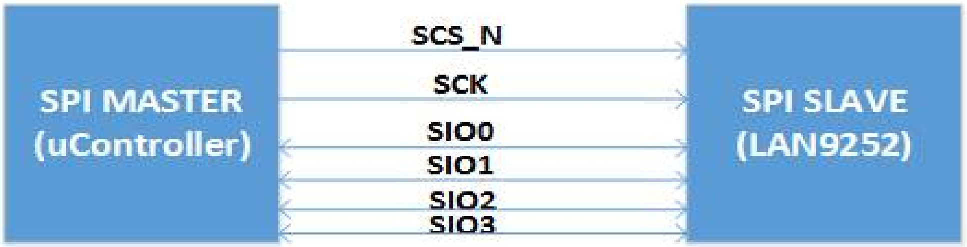
SPI MASTER (uController)
SCS_N
SCK
SI (SIO0)
SO (SIO1)
NC
SIO2
SIO3
SPI SLAVE (LAN9252)

DUAL O/P and DUAL I/O READ/WRITE



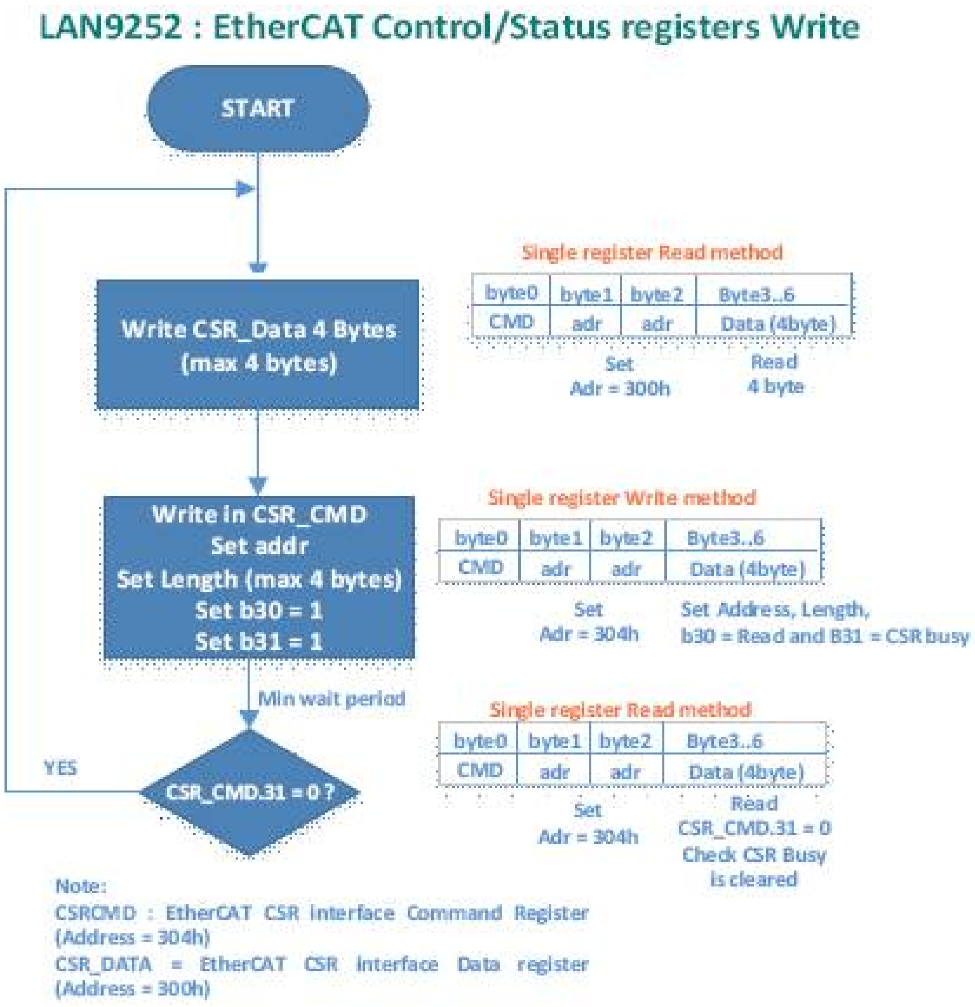
SPI MASTER (uController)
SCS_N
SCK
SIO0
SIO1
NC
SIO2
SIO3
SPI SLAVE (LAN9252)

SQI,QUAD O/p and QUAD I/O READ/WRITE



SPI MASTER (uController)
SCS_N
SCK
SIO0
SIO1
SIO2
SIO3
SPI SLAVE (LAN9252)

An example : single Write



LAN9252 : EtherCAT Control/Status registers Write

START

Write CSR_Data 4 Bytes (max 4 bytes)

Write in CSR_CMD
Set addr
Set Length (max 4 bytes)
Set b30 = 1
Set b31 = 1

Min wait period

CSR_CMD.31 = 0 ?

YES

Single register Read method

byte0	byte1	byte2	Byte3..6
CMD	adr	adr	Data (4byte)

Set
Adr = 300h

Read
4 byte

Single register Write method

byte0	byte1	byte2	Byte3..6
CMD	adr	adr	Data (4byte)

Set
Adr = 304h

Set Address, Length,
b30 = Read and B31 = CSR busy

Single register Read method

byte0	byte1	byte2	Byte3..6
CMD	adr	adr	Data (4byte)

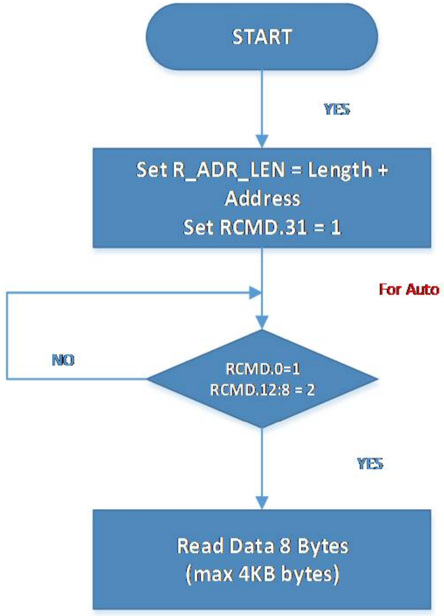
Set
Adr = 304h

Read
CSR_CMD.31 = 0
Check CSR Busy
is cleared

Note:
CSRCMD : EtherCAT CSR Interface Command Register (Address = 304h)
CSR_DATA = EtherCAT CSR Interface Data register (Address = 300h)

SPI M-write

Process RAM READ



START

YES

Set R_ADR_LEN = Length + Address
Set RCMD.31 = 1

NO

RCMD.0=1
RCMD.12:8 = 2

YES

Read Data 8 Bytes
(max 4KB bytes)

Multiple register (increment address) write method

byte0	byte1	byte2	Byte3..6	Byte7..10
CMD	adr	adr	Data (4byte)	Data (4byte)

Set
Adr = 4308h

For Auto increment address

Set Length + Start
Address (in 308h)

Set
RCMD.31 = 1
(in 30Ch)

Single register Read method

byte0	byte1	byte2	Byte3..6
CMD	adr	adr	Data (4byte)

Set
Adr = 30Ch

Read
RCMD.0=1
RCMD.12:8 = 2 (for 8 bytes) (from 30Ch)

Multiple register Read method

byte0	byte1	byte2	Byte3..6	Byte7..10
CMD	adr	adr	Data (4byte)	Data (4byte)

Set
Adr = 0h

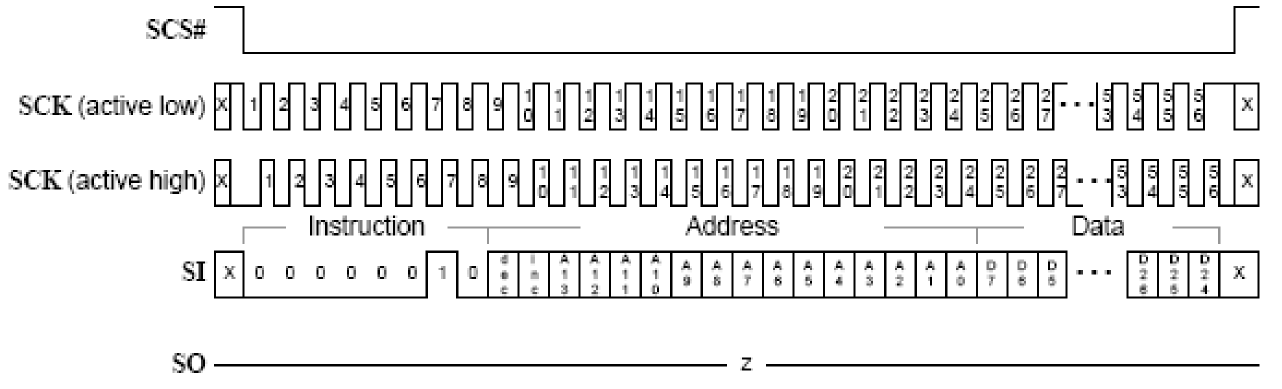
Read
First 4 byte

Read
Second 4 byte

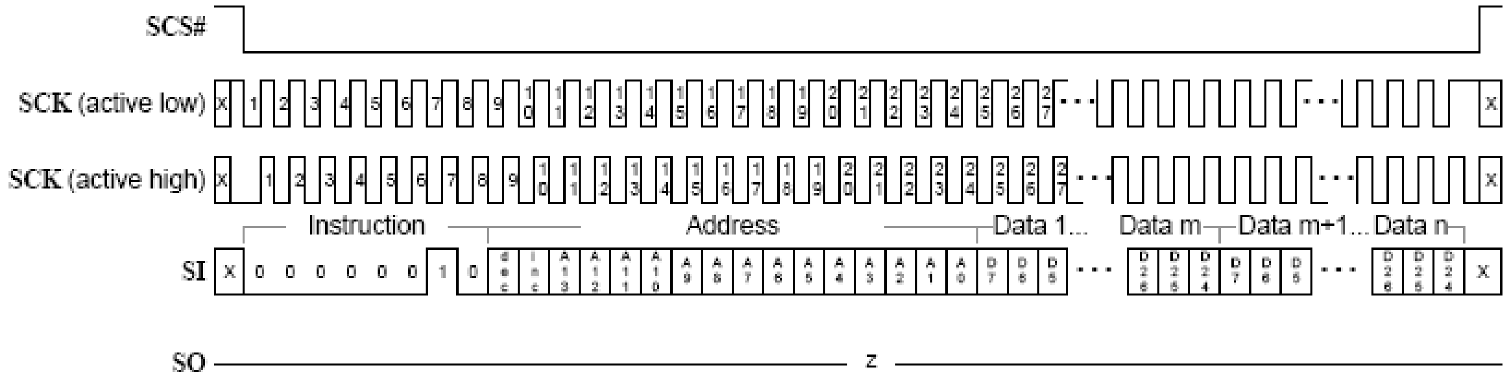
Note1:

R_ADR_LEN	= EtherCAT Process RAM Read Address and Length Register (Address = 308h)
RCMD	= EtherCAT Process RAM Read Command Register (Address = 30Ch)

Waveform



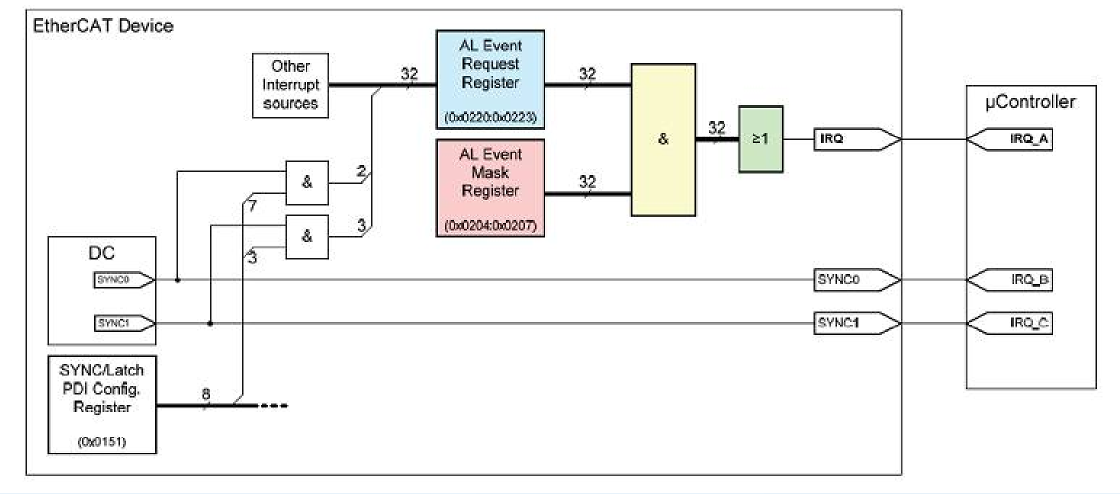
SPI Write Single Register



SPI Write Multiple Registers

Interrupt configuration

- @ 9252_HW.C
- {
- //IRQ enable,IRQ polarity, IRQ buffer type in Interrupt Configuration register.
- //Wrte 0x54 - 0x00000101
- //Write in Interrupt Enable register
- //Write 0x5c - 0x0000000
- //Read Interrupt Status register (register are read and clear)
- //Read 0x58.
- }



MICROCHIP

Regional Training Centers

LAN9252介紹

HBI porting notice (connect to other MCU like TI_DSP in motion control)

Available HBI Modes

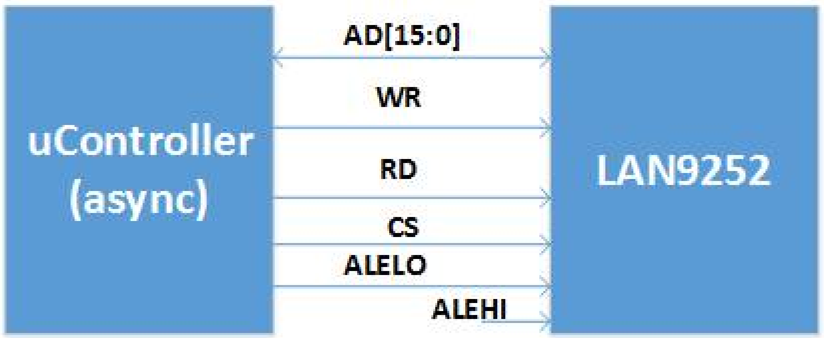
1. **HBI Multiplexed Mode**
   - 1 Phase 8-bit
   - 1-phase 16-bit
   - 2-phase 8-bit
   - 2-phase 16-bit

2. **HBI Indexed Mode**
   - 8-bit
   - 16-bit

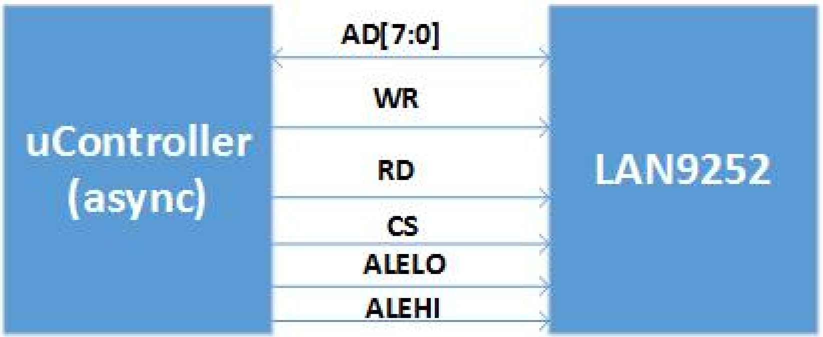
HBI Multiplexed mode – Connections

- **Connections between uController and LAN9252 for 1 Phase and 2 Phase Multiplexed modes are shown below**

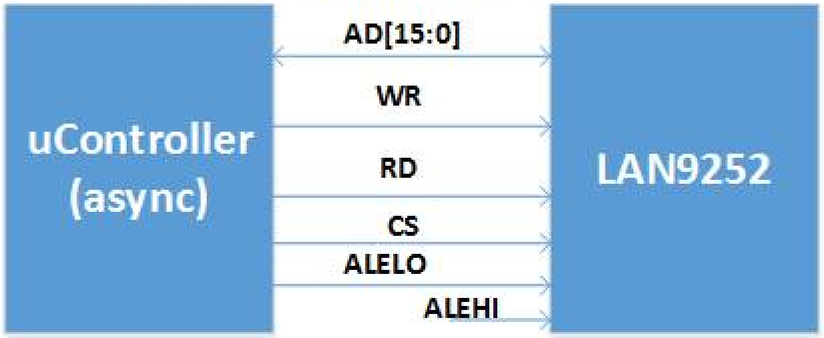
8-bit Multiplexed HBI mode: 1 Phase



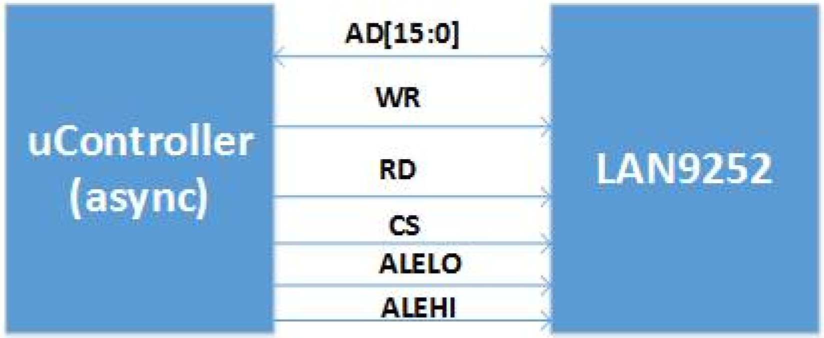
8-bit Multiplexed HBI mode: 2 Phase



16-bit Multiplexed HBI mode : 1 Phase



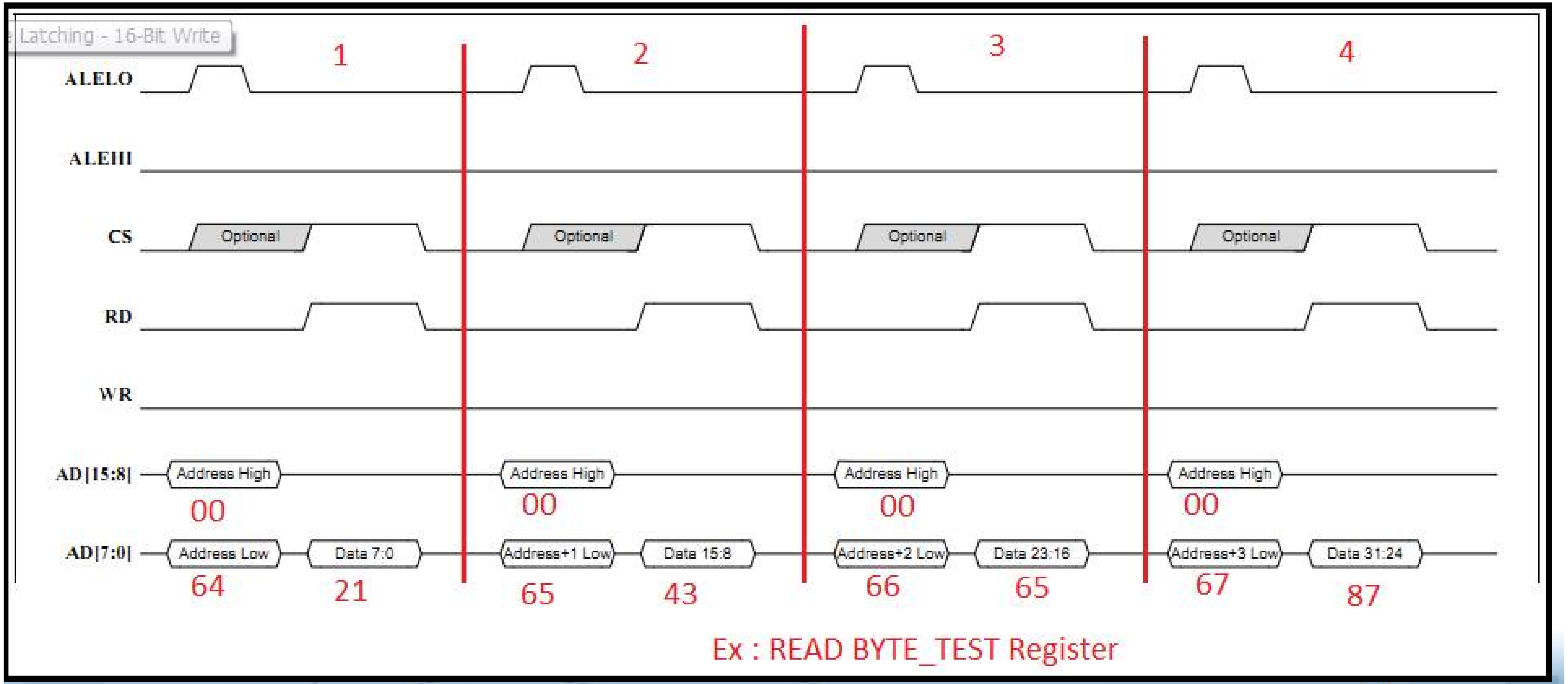
16-bit Multiplexed HBI mode : 2 Phase



Note: The POLARITY of WR, RD, CS, ALELO and ALEHI can be CONTROLLED

1-Phase 8bit Multiplexed mode

- 4 cycles needed for 32 bit Data Read/Write
- ALELO is only used , ALEHI is not used for Address latching
- 16 AD lines are required in 1-Phase 8-bit mode
- Eg:“BYTE_TEST” Offset : 064h, Default vale : 87654321

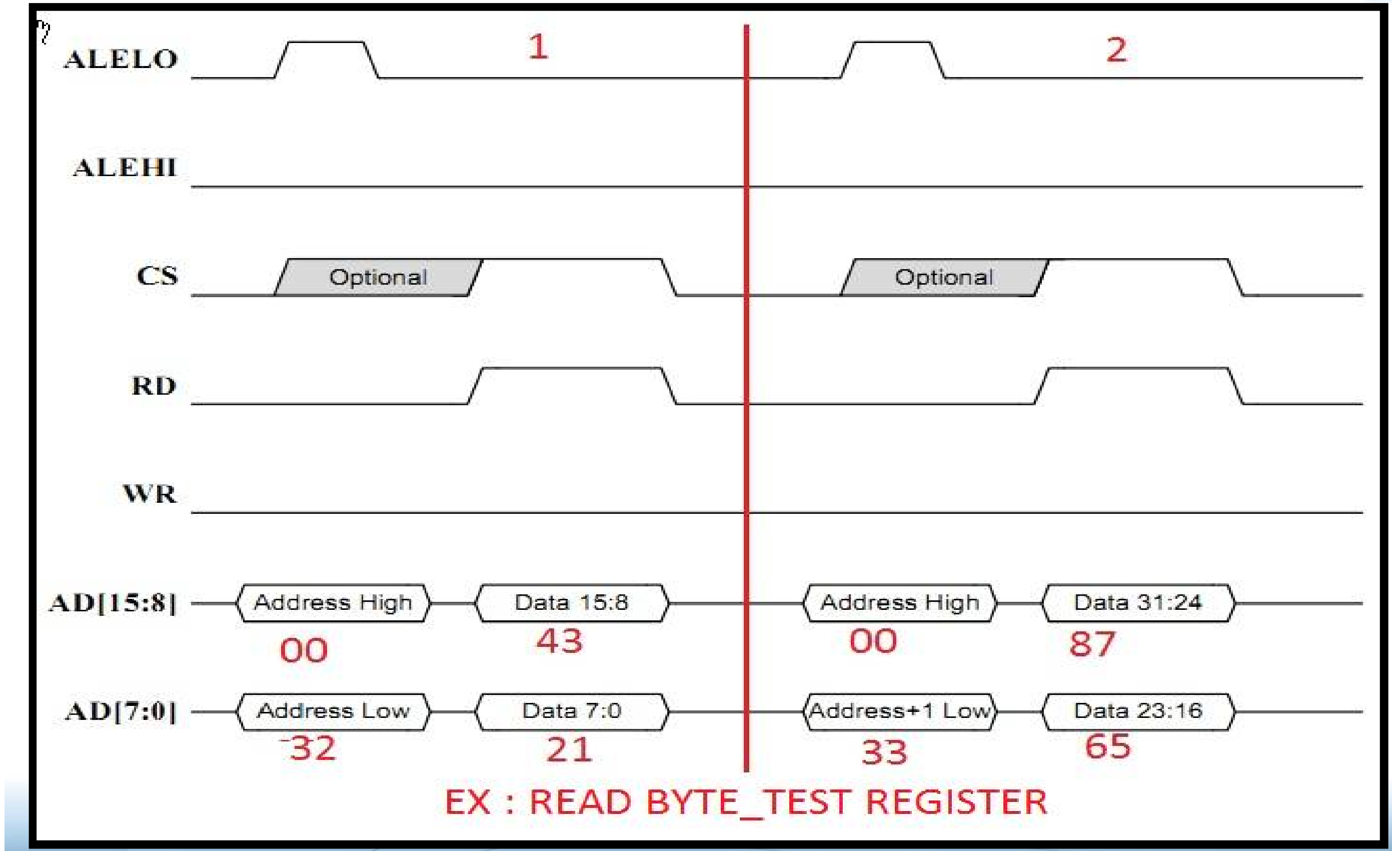


Ex : READ BYTE_TEST Register

1-Phase 16bit Multiplexed mode

- **2 cycles needed for 32 bit Data Read/Write**
- **ALELO is only used , ALEHI is not used for Address latching**
- **Address0 is ignored and 1-bit Right shift is required by host**
- **Eg:“BYTE_TEST” Offset : 064h, Default vale : 87654321**

064h = 0000 0000 0110 0100
Right shift >> by 1bit
032h = 0000 0000 0011 0010

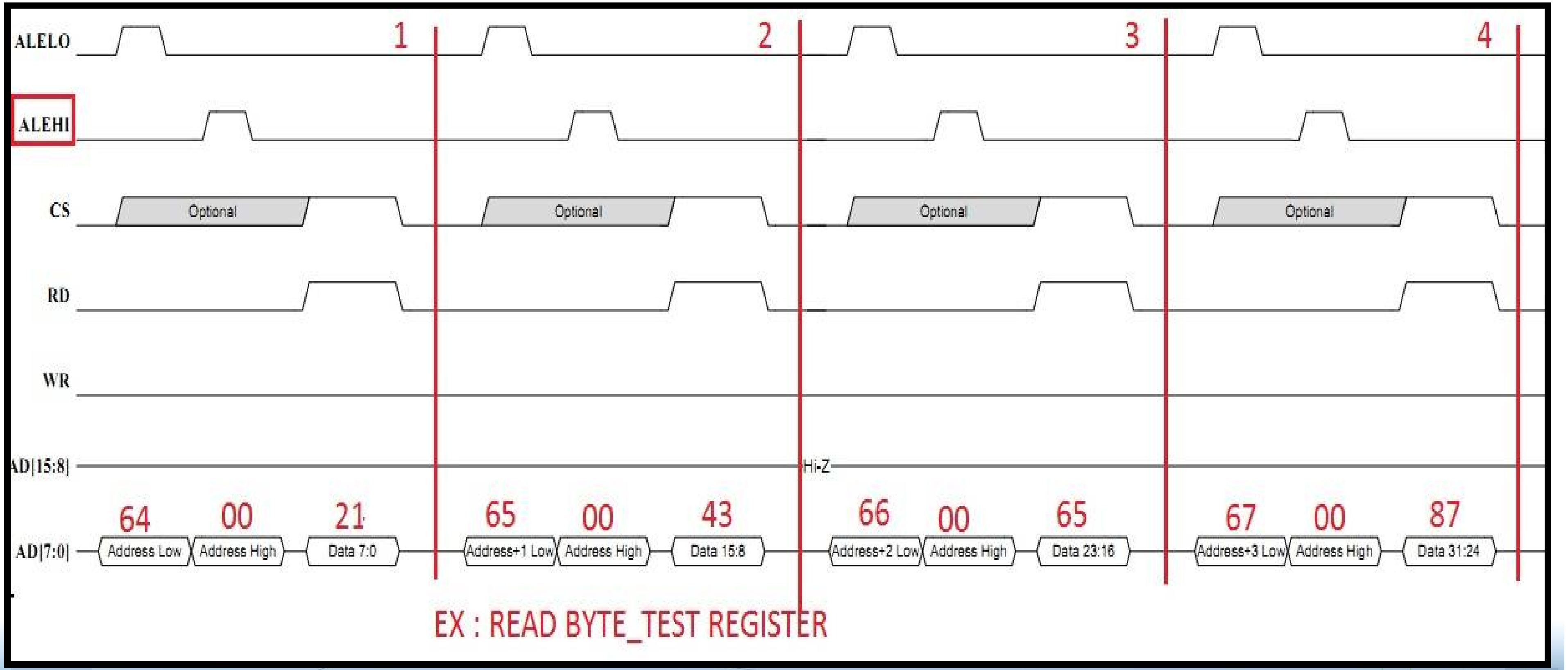


EX : READ BYTE_TEST REGISTER

MICROCHIP
Regional Training Centers

2-Phase 8bit Multiplexed mode

- 4 cycles needed for 32 bit Data Read/Write
- ALELO/ALEHI used for Address latching
- 8 AD lines are required in 2-Phase 8-bit mode, unlike 1-phase 8-bit
- Eg:“BYTE_TEST” Offset : 064h, Default vale : 87654321

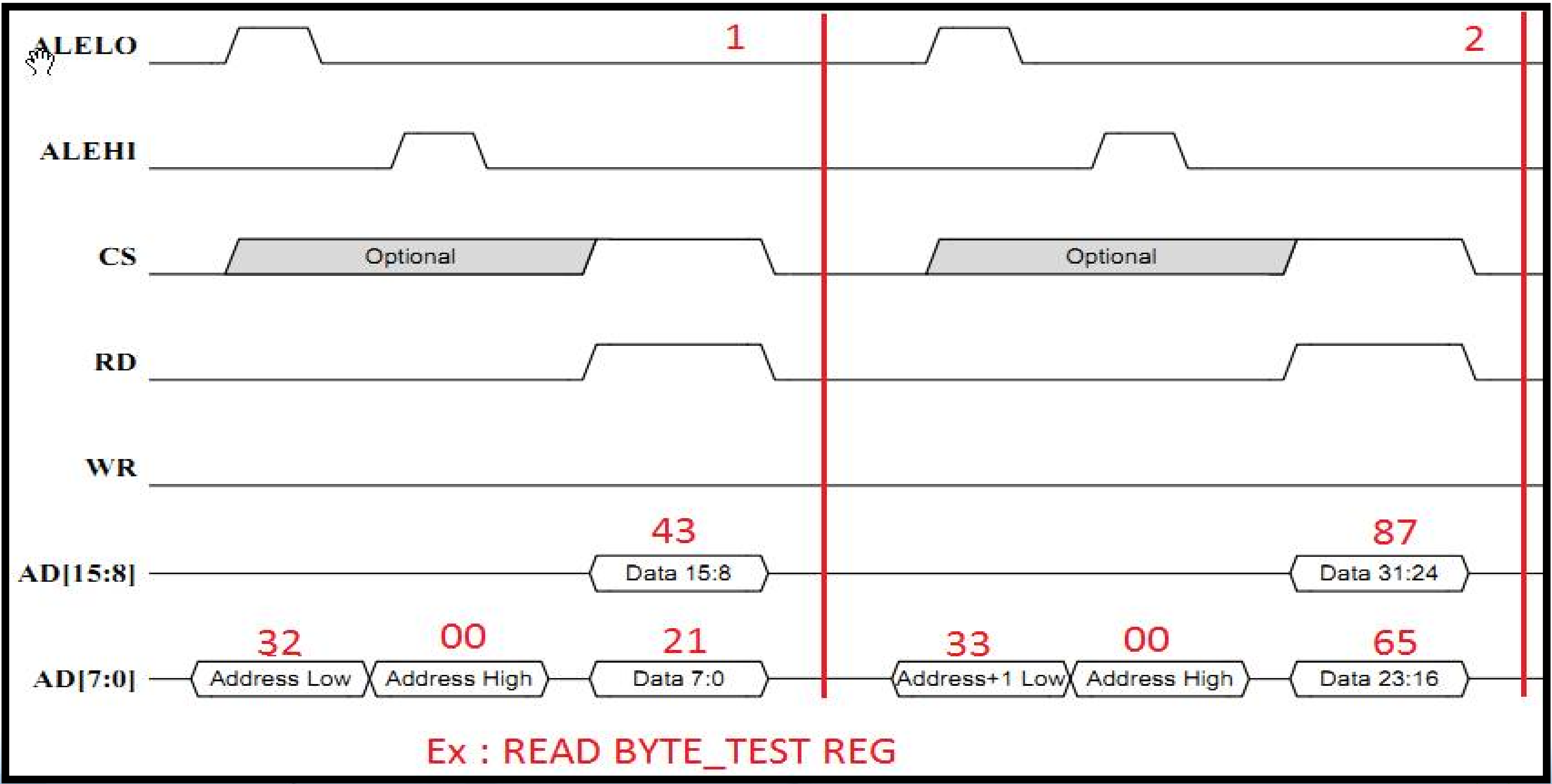


EX : READ BYTE_TEST REGISTER

2-Phase 16bit Multiplexed Mode

- **2 cycles needed for 32 bit Data Read/Write**
- **ALELO/ALEHI used used for Address latching**
- **Address0 is ignored and 1-bit Right shift is required by host**
- **Eg:"BYTE_TEST" Offset : 064h, Default vale : 87654321**

064h = 0000 0000 0110 0100
Right shift >> by 1bit
032h = 0000 0000 0011 0010



Ex : READ BYTE_TEST REG

MICROCHIP

Regional Training Centers

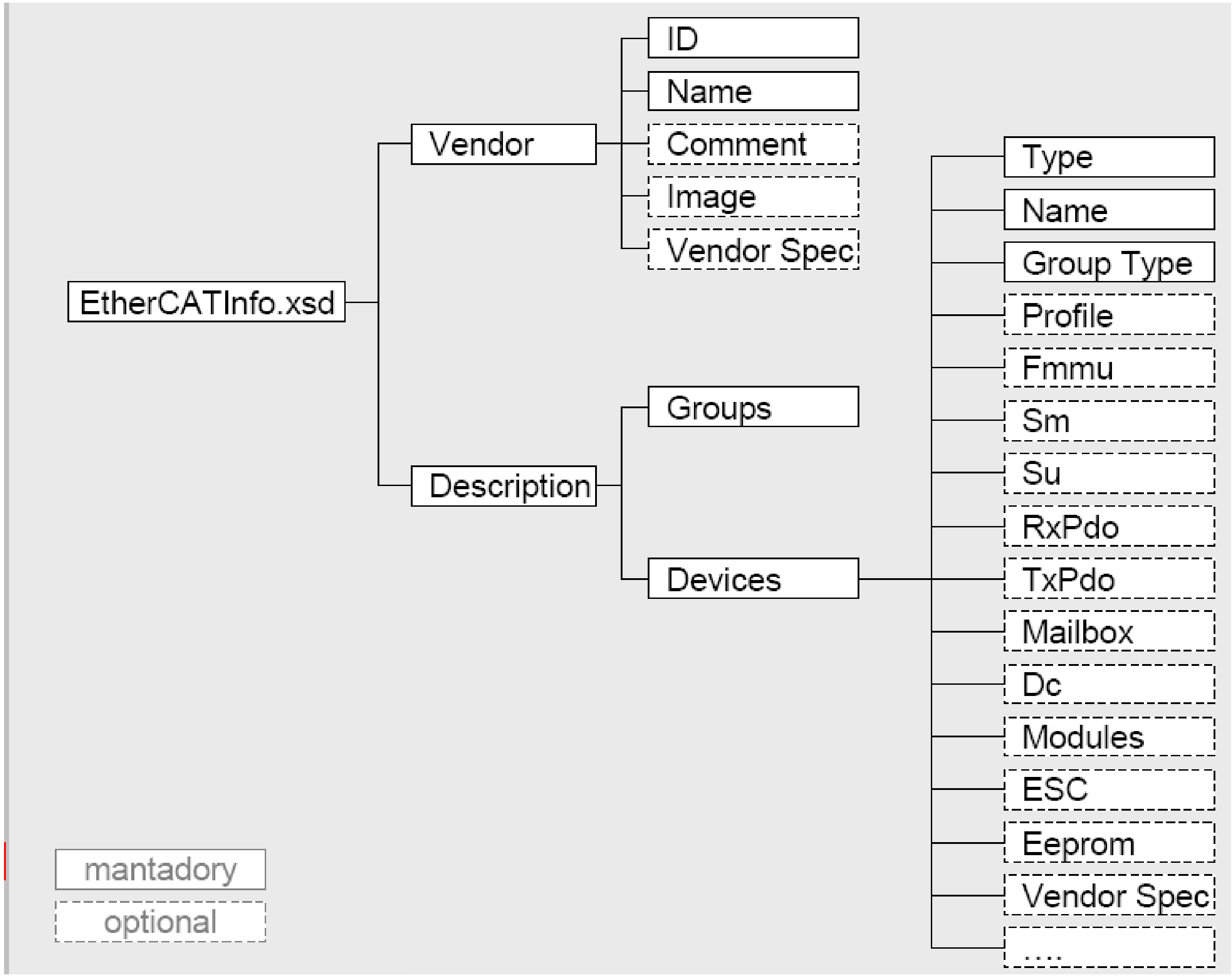
LAN9252介紹

ESI

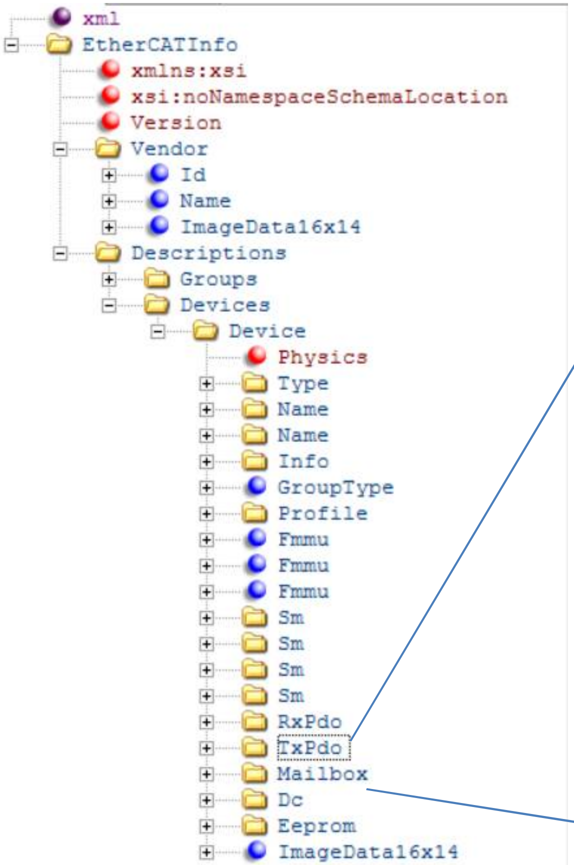
ESI overview

- **ESI 詳細規範 : ETG.2000 S (R) V1.0.7**
- 以**XML**形式存在
- **ESI** 告訴主**/**從站　從站的架構為何
    - Vendor
    - Device group
    - Device
    - PDO mapping
    - FMMU/Sync manager information
- 用 **XMLNOTEPAD** 比較好觀察
- **SSC** 可以產生**ESI**
- 透過**TWINCAT or SSC**寫到**EEPROM**
- **MASTER** 端也必須有一份**ESI copy**

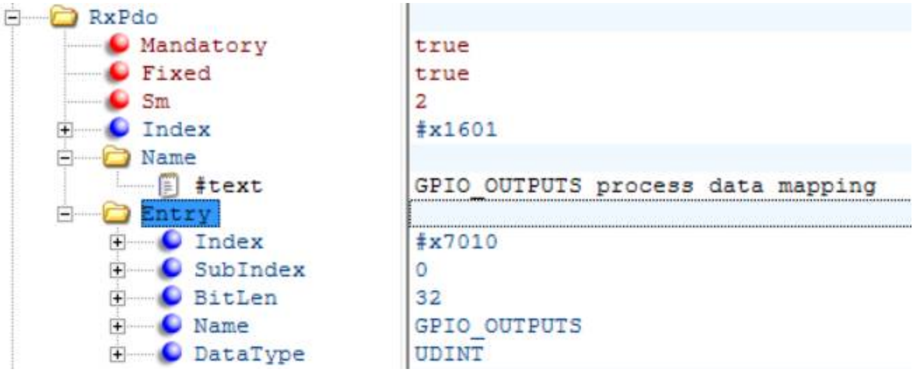
Typical ESI format



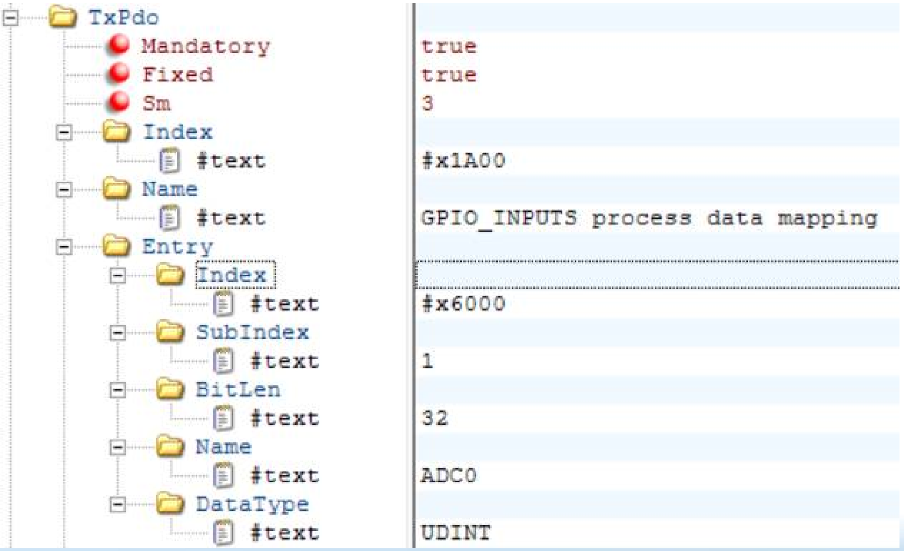
ESI PDO mapping



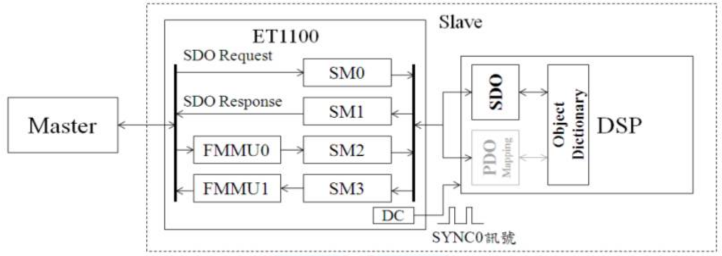
```
xml
EtherCATInfo
    xmlns:xsi
    xsi:noNamespaceSchemaLocation
    Version
    Vendor
        Id
        Name
        ImageData16x14
    Descriptions
        Groups
        Devices
            Device
                Physics
                Type
                Name
                Name
                Info
                GroupType
                Profile
                Fmmu
                Fmmu
                Fmmu
                Sm
                Sm
                Sm
                Sm
                RxPdo
                TxPdo
                Mailbox
                Dc
                Eeprom
                ImageData16x14
```



RxPdo	
Mandatory	true
Fixed	true
Sm	2
Index	#x1601
Name	
#text	GPIO_OUTPUTS process data mapping
Entry	
Index	#x7010
SubIndex	0
BitLen	32
Name	GPIO_OUTPUTS
DataType	UDINT



TxPdo	
Mandatory	true
Fixed	true
Sm	3
Index	
#text	#x1A00
Name	
#text	GPIO_INPUTS process data mapping
Entry	
Index	
#text	#x6000
SubIndex	
#text	1
BitLen	
#text	32
Name	
#text	ADC0
DataType	
#text	UDINT



Example

- **In 3 port application, the Physics need modify to enable MII**

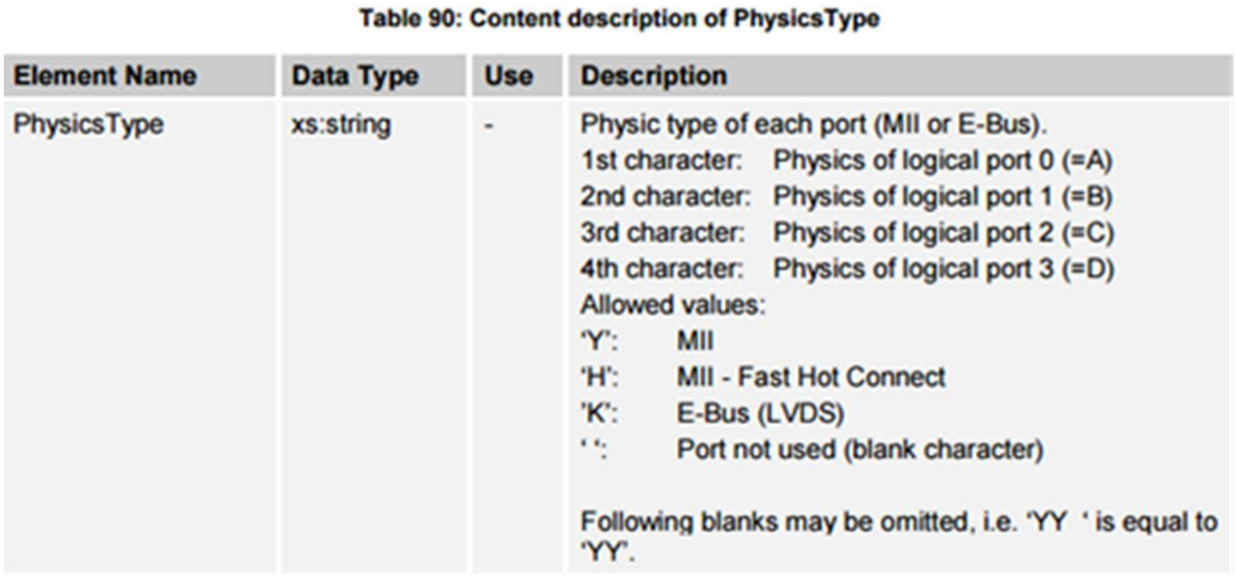


Table 90: Content description of PhysicsType

Element Name	Data Type	Use	Description
PhysicsType	xs:string	-	Physic type of each port (MII or E-Bus). 1st character: Physics of logical port 0 (=A) 2nd character: Physics of logical port 1 (=B) 3rd character: Physics of logical port 2 (=C) 4th character: Physics of logical port 3 (=D) Allowed values: 'Y': MII 'H': MII - Fast Hot Connect 'K': E-Bus (LVDS) ' ': Port not used (blank character) Following blanks may be omitted, i.e. 'YY ' is equal to 'YY'.

Regional Training Centers

LAN9252介紹

TWINCAT 端的設定/MASTER端網卡尋找

PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

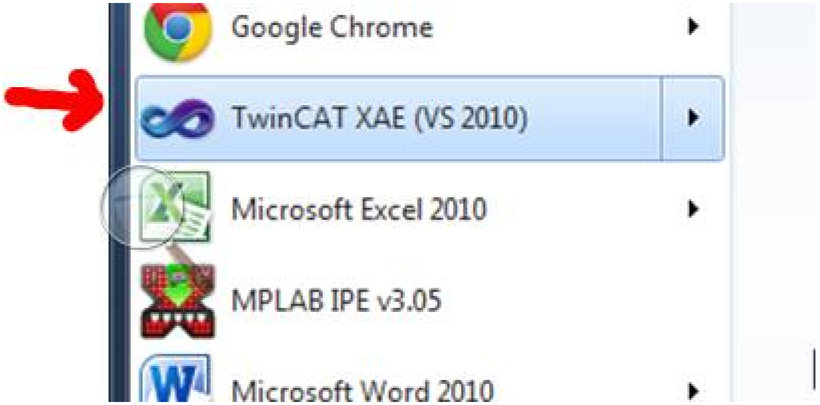
Regional Training Centers

TWINCAT3 (TC3)

- **TC3 是本課程中之　“主站”**
  - 有許多主站可選擇
  - TC3支援較多功能
  - 一般Debug 用TC3做功能確定
- 可至倍福官網下載
- **TC3必須與相容的網卡一起工作**
- 並收集所有從站之**ESI,** 置於特殊目錄

工作流程

- 打開 **TWINCAT XAE (VS2010)**



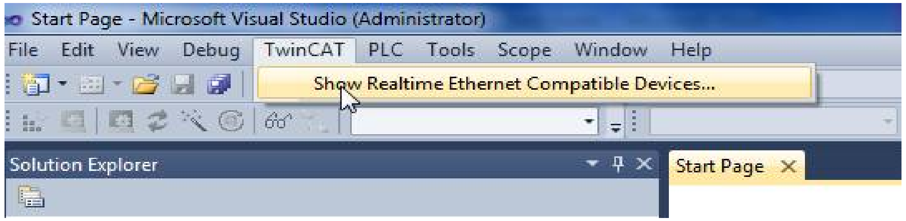
- **將ESI檔 (from SSC generated) Copy到 “C:\TwinCAT\3.1\Config\Io\EtherCAT”**

確認網卡相容性

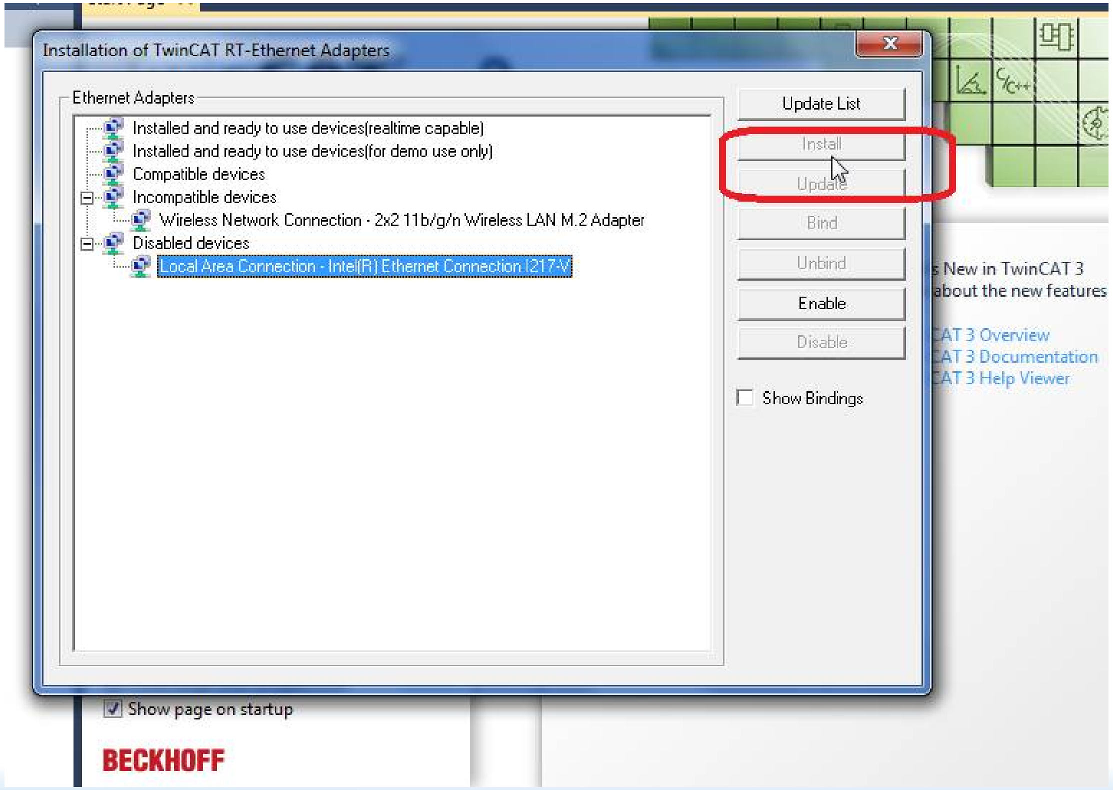
- 檢查網卡是否相容
- 若不相容則將無法與從站通訊
- 必須把**TCP/IP** 設定**disable** 掉

Microchip Regional Training Centers

確認網卡相容性



Start Page - Microsoft Visual Studio (Administrator)
File
Edit
View
Debug
TwinCAT
PLC
Tools
Scope
Window
Help
Show Realtime Ethernet Compatible Devices...
Solution Explorer
Start Page



Installation of TwinCAT RT-Ethernet Adapters

Ethernet Adapters

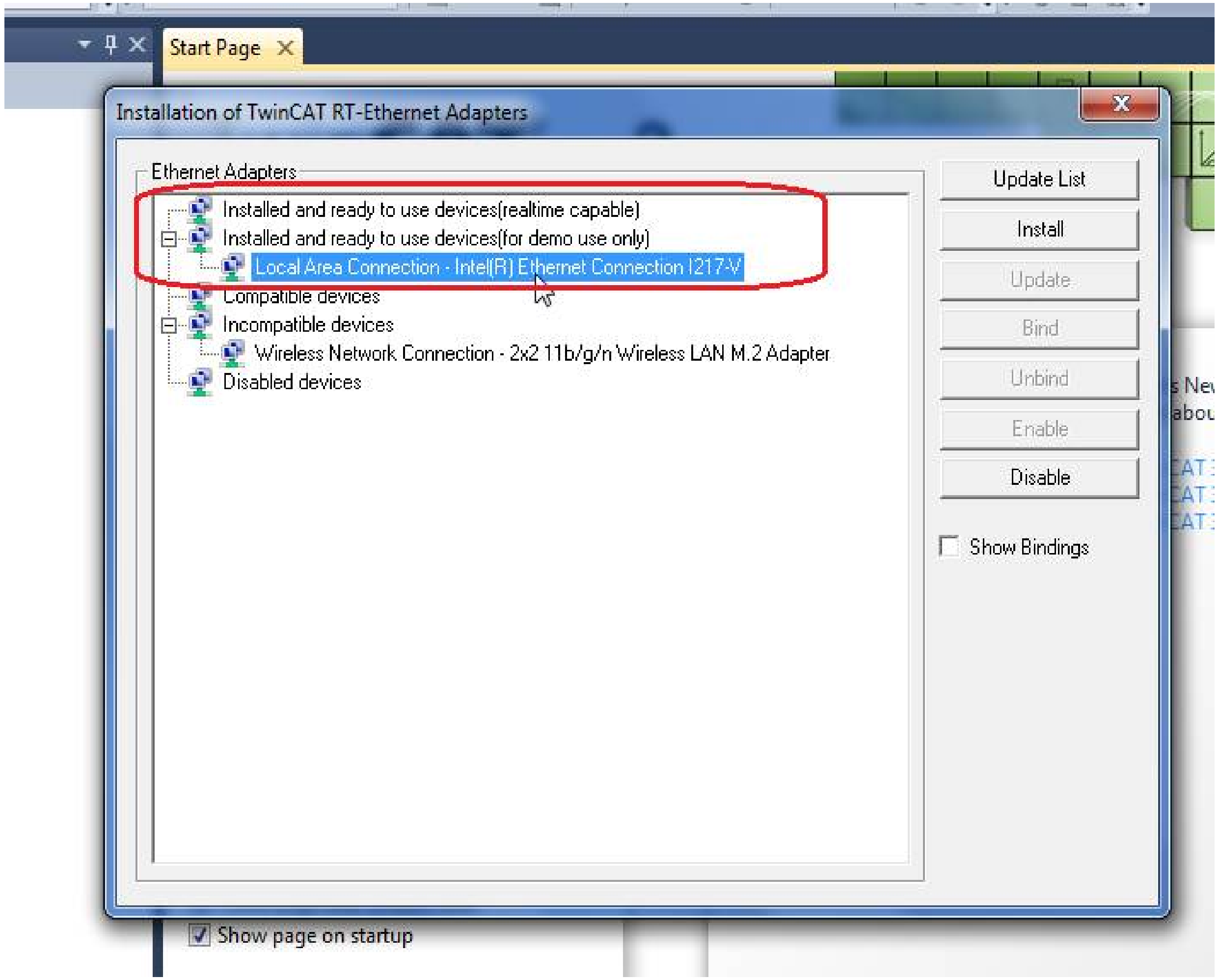
- Installed and ready to use devices(realtime capable)
- Installed and ready to use devices(for demo use only)
- Compatible devices
- Incompatible devices
  - Wireless Network Connection - 2x2 11b/g/n Wireless LAN M.2 Adapter
- Disabled devices
  - Local Area Connection - Intel(R) Ethernet Connection I217-V

☐ Show Bindings

☑ Show page on startup

Select the Network adaptor and install the TwinCAT driver

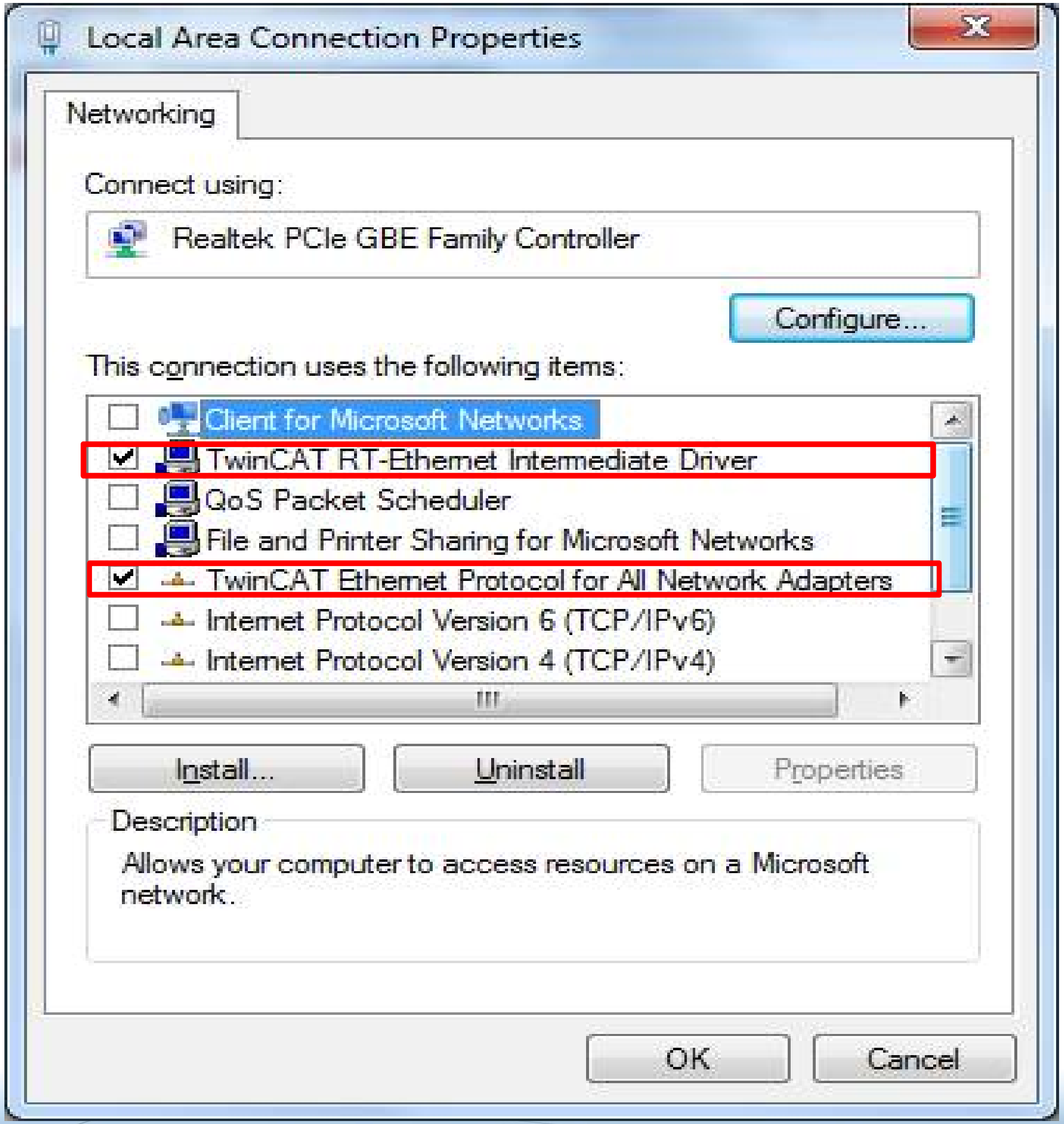
確認網卡相容性


Start Page
Installation of TwinCAT RT-Ethernet Adapters
Ethernet Adapters
Installed and ready to use devices(realtime capable)
Installed and ready to use devices(for demo use only)
Local Area Connection - Intel(R) Ethernet Connection I217-V
Compatible devices
Incompatible devices
Wireless Network Connection - 2x2 11b/g/n Wireless LAN M.2 Adapter
Disabled devices
Update List
Install
Update
Bind
Unbind
Enable
Disable
☐ Show Bindings
☑ Show page on startup

Once the TwinCAT driver is installed successfully, the driver is compatible with the TwinCAT master. Now the network adaptor will be moved to "Installed and ready to use devices"

Regional Training Centers

網卡設定



Local Area Connection Properties

Networking

Connect using:

Realtek PCIe GBE Family Controller

This connection uses the following items:

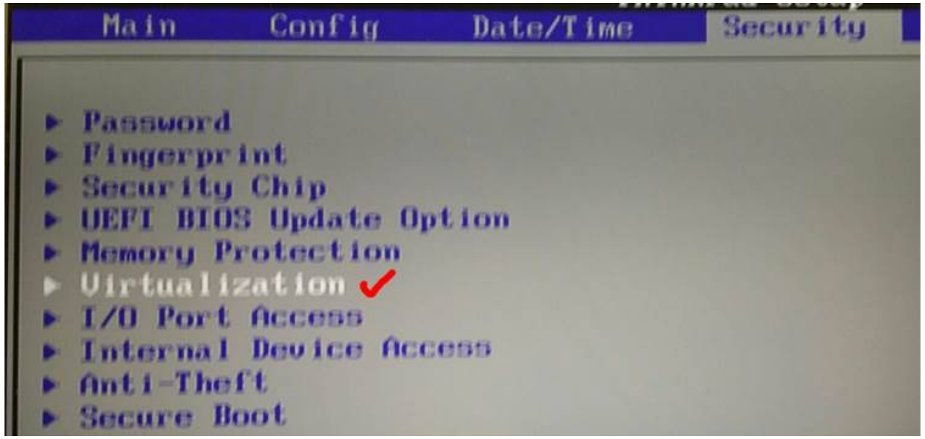
- ☐ Client for Microsoft Networks
- ☑ TwinCAT RT-Ethernet Intermediate Driver
- ☐ QoS Packet Scheduler
- ☐ File and Printer Sharing for Microsoft Networks
- ☑ TwinCAT Ethernet Protocol for All Network Adapters
- ☐ Internet Protocol Version 6 (TCP/IPv6)
- ☐ Internet Protocol Version 4 (TCP/IPv4)

Description

Allows your computer to access resources on a Microsoft network.

若無法順利安裝

- **Try BIOS setting in “security” → “virtualization” → enable**



- 若還是無法連線 只好換網卡或電腦

MICROCHIP

Regional Training Centers

LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找

PDO mapping excel and SSC flow

EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

MICROCHIP

Regional Training Centers

PDO mapping excel and SSC flow

PDO mapping concept

PDO Excel 的重要性

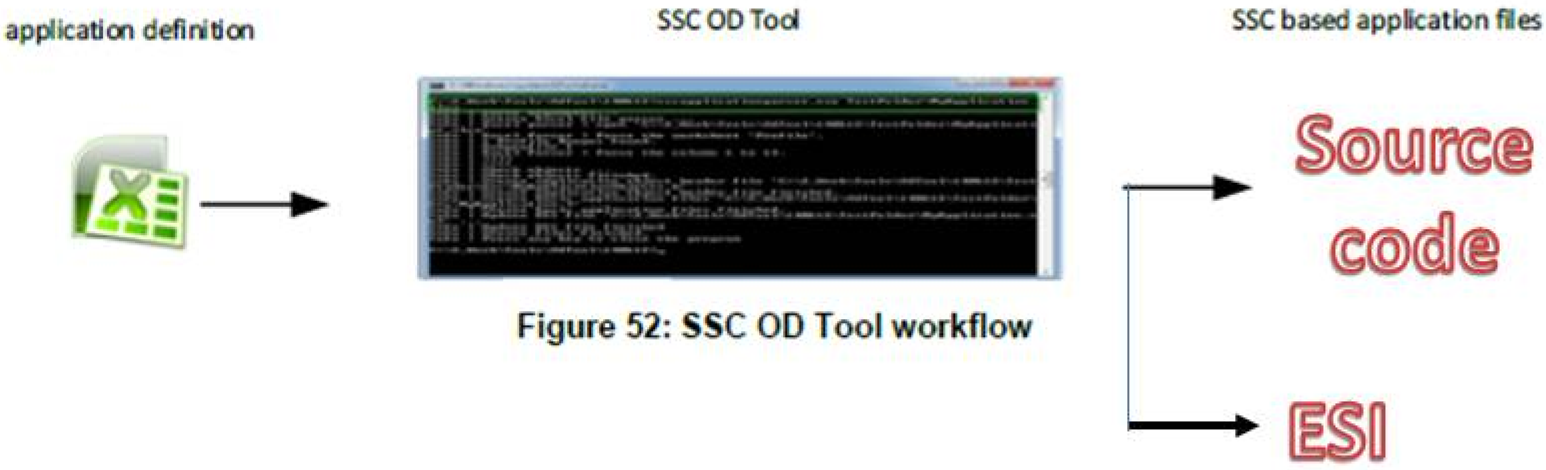


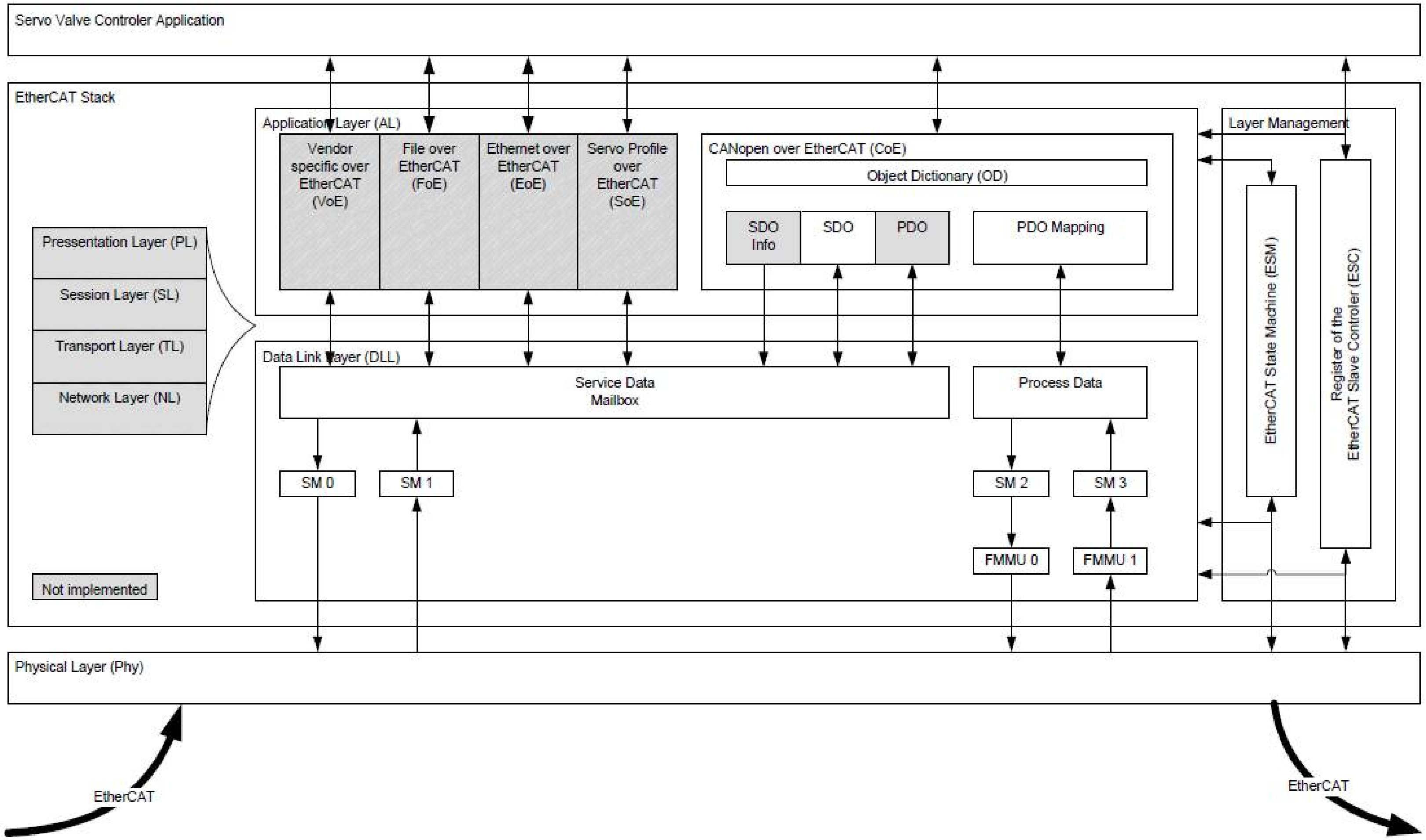
Figure 52: SSC OD Tool workflow

Microchip Regional Training Centers

Entire flow

- **Excel PDO definition → Generate ESI & SRC for MPLAB X →**
  - SRC → Modify AAPL_ input, output and others mapping → MPLABX tool flow & programming
  - Put ESI(s) into TWINCAT → Run TWINCAT → Configure Device → Variable link to PLC → PLC ST programming

Communication model



Servo Valve Controler Application

EtherCAT Stack

Application Layer (AL)

Vendor specific over EtherCAT (VoE)

File over EtherCAT (FoE)

Ethernet over EtherCAT (EoE)

Servo Profile over EtherCAT (SoE)

CANopen over EtherCAT (CoE)

Object Dictionary (OD)

SDO Info

SDO

PDO

PDO Mapping

Layer Management

EtherCAT State Machine (ESM)

Register of the EtherCAT Slave Controler (ESC)

Pressentation Layer (PL)

Session Layer (SL)

Transport Layer (TL)

Network Layer (NL)

Data Link Layer (DLL)

Service Data Mailbox

Process Data

SM 0

SM 1

SM 2

SM 3

FMMU 0

FMMU 1

Not implemented

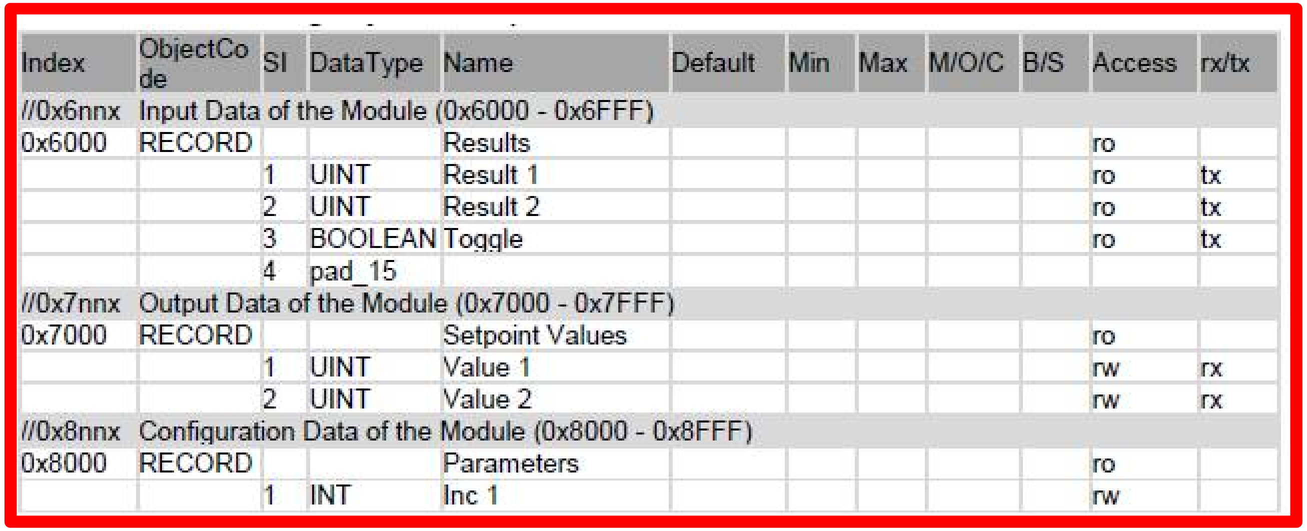
Physical Layer (Phy)

EtherCAT

EtherCAT

Figure 3: EtherCAT field bus communication layers

PDO excel



Index	ObjectCode	SI	DataType	Name	Default	Min	Max	M/O/C	B/S	Access	rx/tx
//0x6nnx	Input Data of the Module (0x6000 - 0x6FFF)										
0x6000	RECORD			Results						ro	
		1	UINT	Result 1						ro	tx
		2	UINT	Result 2						ro	tx
		3	BOOLEAN	Toggle						ro	tx
		4	pad_15								
//0x7nnx	Output Data of the Module (0x7000 - 0x7FFF)										
0x7000	RECORD			Setpoint Values						ro	
		1	UINT	Value 1						rw	rx
		2	UINT	Value 2						rw	rx
//0x8nnx	Configuration Data of the Module (0x8000 - 0x8FFF)										
0x8000	RECORD			Parameters						ro	
		1	INT	Inc 1						rw	

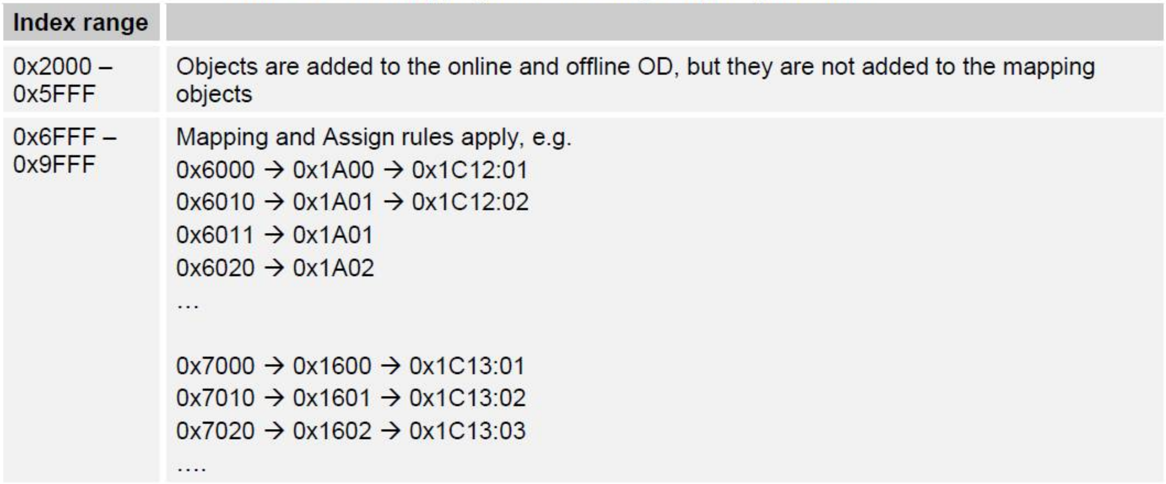
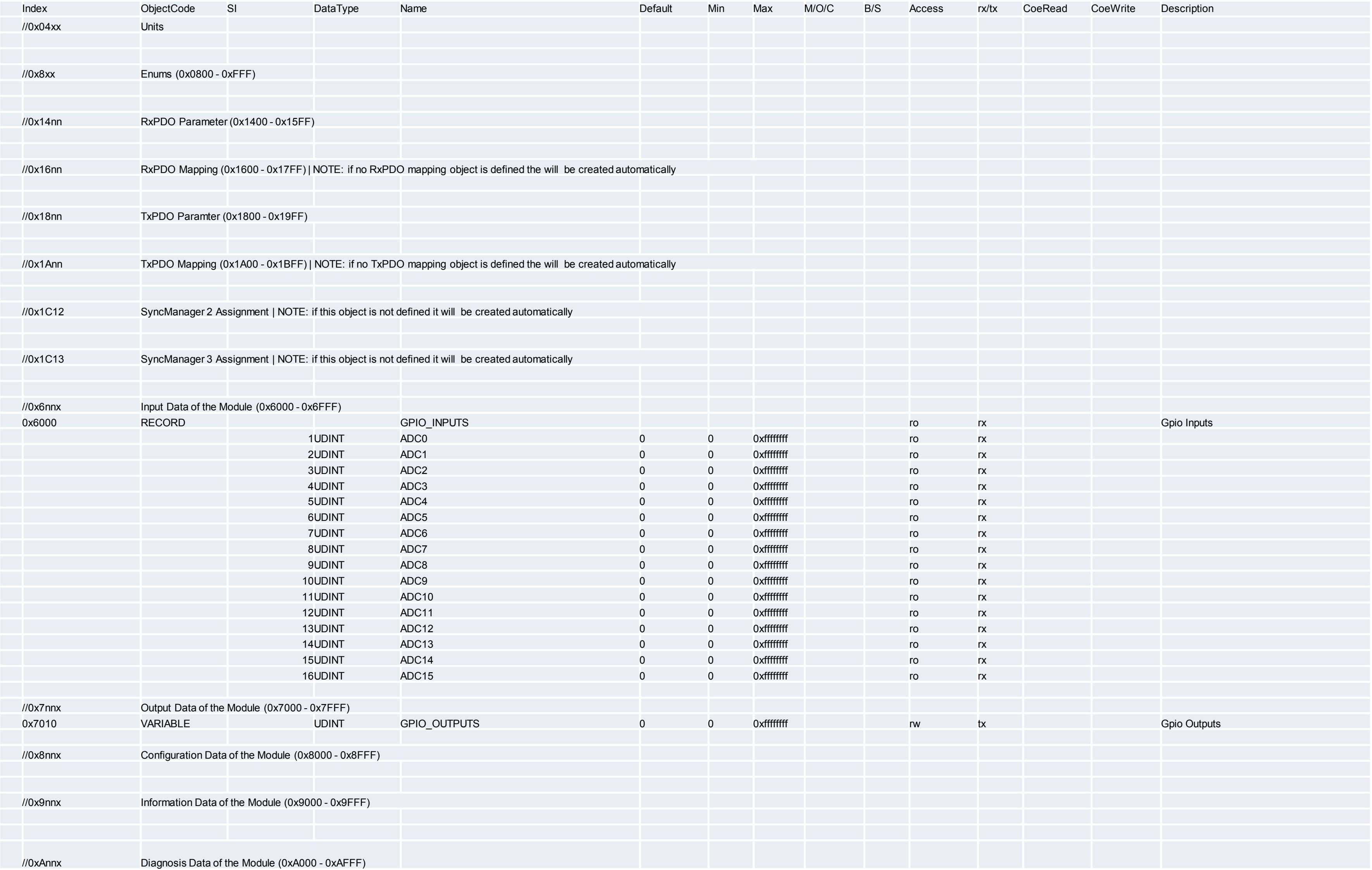


Table 21: PDO mapping and SM assign object generation

Index range	
0x2000 – 0x5FFF	Objects are added to the online and offline OD, but they are not added to the mapping objects
0x6FFF – 0x9FFF	Mapping and Assign rules apply, e.g. 0x6000 → 0x1A00 → 0x1C12:01 0x6010 → 0x1A01 → 0x1C12:02 0x6011 → 0x1A01 0x6020 → 0x1A02 … 0x7000 → 0x1600 → 0x1C13:01 0x7010 → 0x1601 → 0x1C13:02 0x7020 → 0x1602 → 0x1C13:03 ….

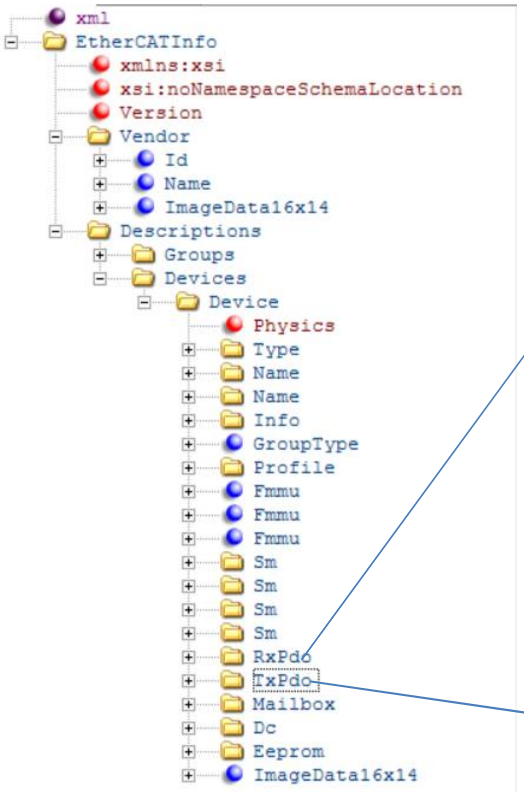
Application GPIO excel



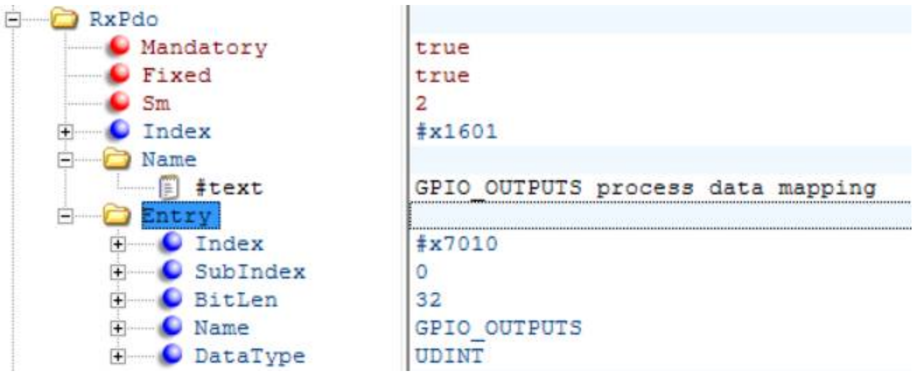
Index	ObjectCode	SI	DataType	Name	Default	Min	Max	M/O/C	B/S	Access	rx/tx	CoeRead	CoeWrite	Description
//0x04xx	Units													
//0x8xx	Enums (0x0800 - 0xFFF)													
//0x14nn	RxPDO Parameter (0x1400 - 0x15FF)													
//0x16nn	RxPDO Mapping (0x1600 - 0x17FF) | NOTE: if no RxPDO mapping object is defined the will be created automatically													
//0x18nn	TxPDO Paramter (0x1800 - 0x19FF)													
//0x1Ann	TxPDO Mapping (0x1A00 - 0x1BFF) | NOTE: if no TxPDO mapping object is defined the will be created automatically													
//0x1C12	SyncManager 2 Assignment | NOTE: if this object is not defined it will be created automatically													
//0x1C13	SyncManager 3 Assignment | NOTE: if this object is not defined it will be created automatically													
//0x6nnx	Input Data of the Module (0x6000 - 0x6FFF)													
0x6000	RECORD			GPIO_INPUTS						ro	rx			Gpio Inputs
		1	UDINT	ADC0	0	0	0xffffffff			ro	rx			
		2	UDINT	ADC1	0	0	0xffffffff			ro	rx			
		3	UDINT	ADC2	0	0	0xffffffff			ro	rx			
		4	UDINT	ADC3	0	0	0xffffffff			ro	rx			
		5	UDINT	ADC4	0	0	0xffffffff			ro	rx			
		6	UDINT	ADC5	0	0	0xffffffff			ro	rx			
		7	UDINT	ADC6	0	0	0xffffffff			ro	rx			
		8	UDINT	ADC7	0	0	0xffffffff			ro	rx			
		9	UDINT	ADC8	0	0	0xffffffff			ro	rx			
		10	UDINT	ADC9	0	0	0xffffffff			ro	rx			
		11	UDINT	ADC10	0	0	0xffffffff			ro	rx			
		12	UDINT	ADC11	0	0	0xffffffff			ro	rx			
		13	UDINT	ADC12	0	0	0xffffffff			ro	rx			
		14	UDINT	ADC13	0	0	0xffffffff			ro	rx			
		15	UDINT	ADC14	0	0	0xffffffff			ro	rx			
		16	UDINT	ADC15	0	0	0xffffffff			ro	rx			
//0x7nnx	Output Data of the Module (0x7000 - 0x7FFF)													
0x7010	VARIABLE		UDINT	GPIO_OUTPUTS	0	0	0xffffffff			rw	tx			Gpio Outputs
//0x8nnx	Configuration Data of the Module (0x8000 - 0x8FFF)													
//0x9nnx	Information Data of the Module (0x9000 - 0x9FFF)													
//0xAnnx	Diagnosis Data of the Module (0xA000 - 0xAFFF)													

RxPDO (Output) 0x16xx	0x1600	0x1601		0x160n
Output Entries (0x7xx)	0x7000 – 0x700F	0x7010 – 0x701F		0x7nn0 – 0x7nnF
TxPDO (Input) 0x1Axx	0x1A00	0x1A01		0x1Ann
Input Entries (0x7xx)	0x6000 – 0x600F	0x6010 – 0x601F		0x6nn0 – 0x6nnF
Configuration Parameter	0x8000 – 0x800F	0x8010 – 0x801F		0x8nn0 – 0x8nnF
Information	0x9000 – 0x900F	0x9010 – 0x901F		0x9nn0 – 0x9nnF
Configuration Area 0x1000 – 0x1FFF				
Device Parameter 0xF000 – 0xFFFF	Module 0	Module 1	…	Module nn
MDP-Gerät (Gateway)	**Feldbus-Slave 0**	**Feldbus-Slave 1**		**Feldbus-Slave nn**

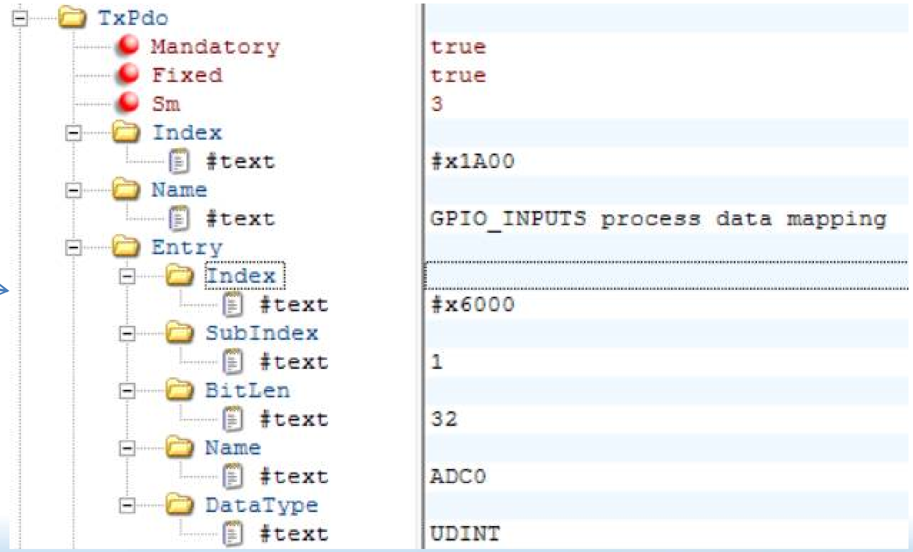
ESI PDO mapping



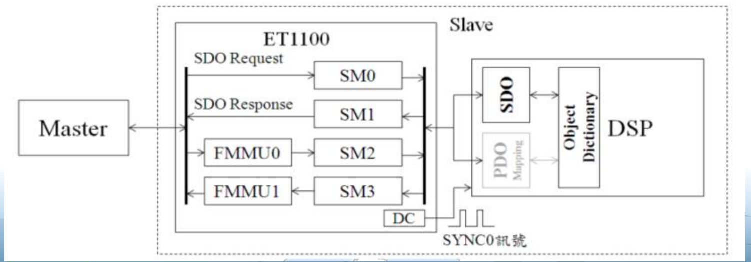
```
xml
EtherCATInfo
  xmlns:xsi
  xsi:noNamespaceSchemaLocation
  Version
  Vendor
    Id
    Name
    ImageData16x14
  Descriptions
    Groups
    Devices
      Device
        Physics
        Type
        Name
        Name
        Info
        GroupType
        Profile
        Fmmu
        Fmmu
        Fmmu
        Sm
        Sm
        Sm
        Sm
        RxPdo
        TxPdo
        Mailbox
        Dc
        Eeprom
        ImageData16x14
```



```
RxPdo
  Mandatory          true
  Fixed              true
  Sm                 2
  Index              #x1601
  Name
    #text            GPIO_OUTPUTS process data mapping
  Entry
    Index            #x7010
    SubIndex         0
    BitLen           32
    Name             GPIO_OUTPUTS
    DataType         UDINT
```



```
TxPdo
  Mandatory          true
  Fixed              true
  Sm                 3
  Index
    #text            #x1A00
  Name
    #text            GPIO_INPUTS process data mapping
  Entry
    Index
      #text          #x6000
    SubIndex
      #text          1
    BitLen
      #text          32
    Name
      #text          ADC0
    DataType
      #text          UDINT
```

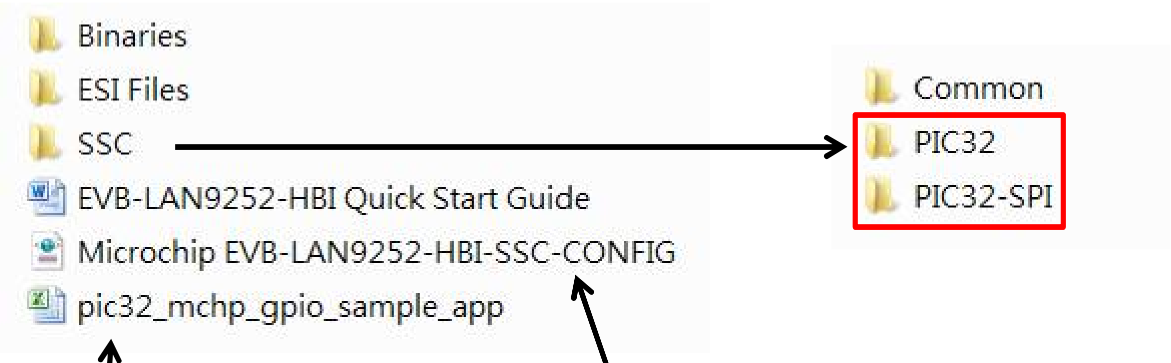


Regional Training Centers

PDO mapping excel and SSC flow

SSC flow

Starting from SDK



Binaries
ESI Files
SSC
EVB-LAN9252-HBI Quick Start Guide
Microchip EVB-LAN9252-HBI-SSC-CONFIG
pic32_mchp_gpio_sample_app

Common
PIC32
PIC32-SPI

PDO mapping excel

SDK ESI

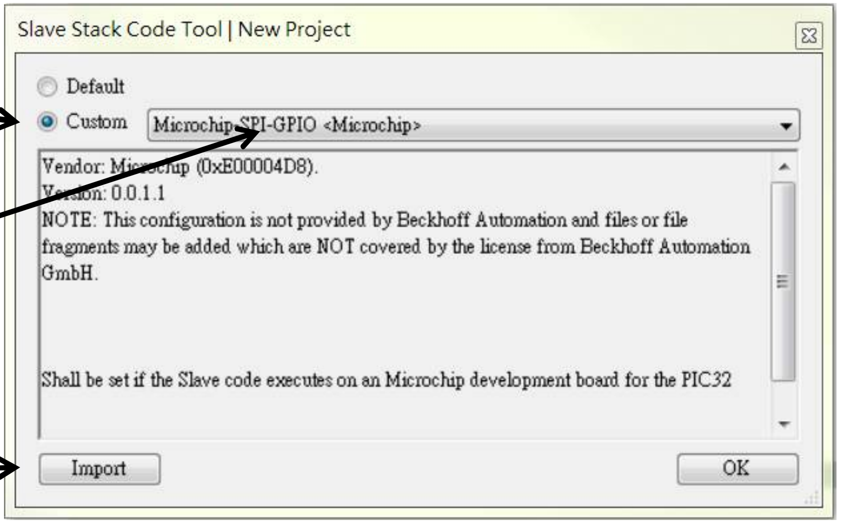
SSC 工具

1. 選 CUSTOM ＆ HW SETTING

1 Custom

2, select hardware setting

3 import XML

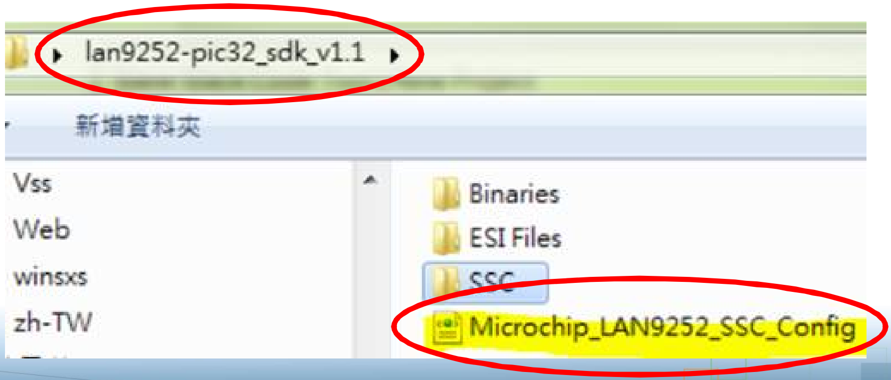


Microchip SPI-GPIO <Microchip>

Vendor: Microchip (0xE00004D8).
Version: 0.0.1.1
NOTE: This configuration is not provided by Beckhoff Automation and files or file fragments may be added which are NOT covered by the license from Beckhoff Automation GmbH.

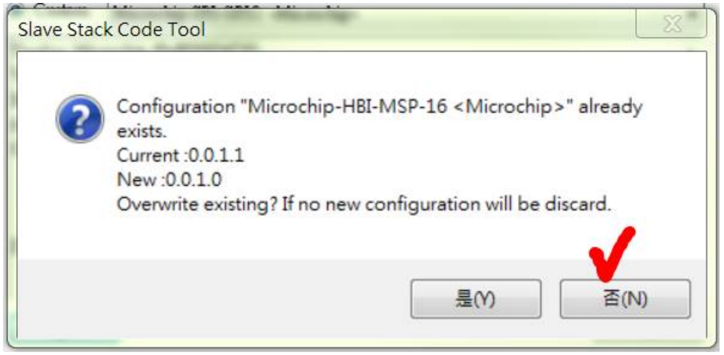
Shall be set if the Slave code executes on an Microchip development board for the PIC32

2. 選SDK 內之XML



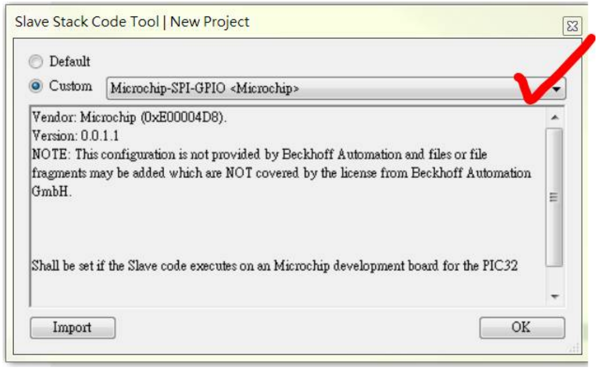
SSC 工具

3. **System will response you following and select “N”**



Configuration "Microchip-HBI-MSP-16 <Microchip>" already exists.
Current :0.0.1.1
New :0.0.1.0
Overwrite existing? If no new configuration will be discard.

4. **Re-select the interface**



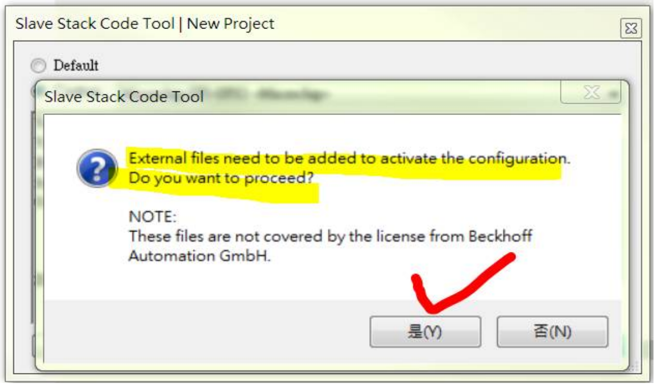
● Custom Microchip-SPI-GPIO <Microchip>

Vendor: Microchip (0xE00004D8).
Version: 0.0.1.1
NOTE: This configuration is not provided by Beckhoff Automation and files or file fragments may be added which are NOT covered by the license from Beckhoff Automation GmbH.

Shall be set if the Slave code executes on an Microchip development board for the PIC32

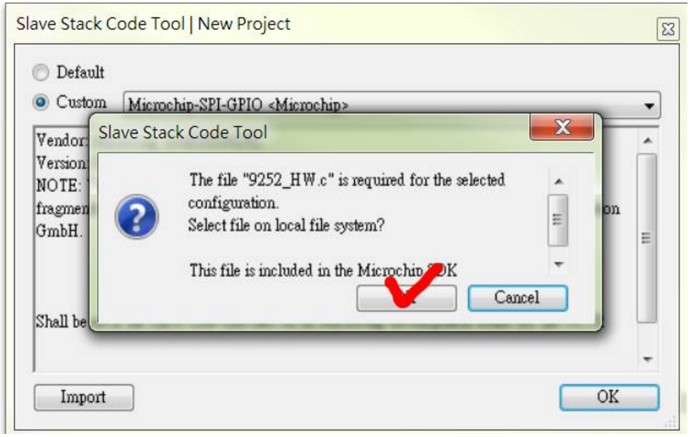
SSC 工具

5. **U will see following pages, (VERY IMPORTANT)**



External files need to be added to activate the configuration.
Do you want to proceed?

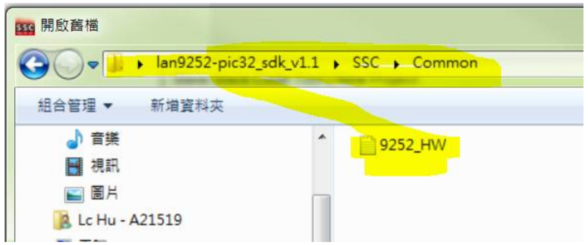
NOTE:
These files are not covered by the license from Beckhoff Automation GmbH.



The file "9252_HW.c" is required for the selected configuration.
Select file on local file system?

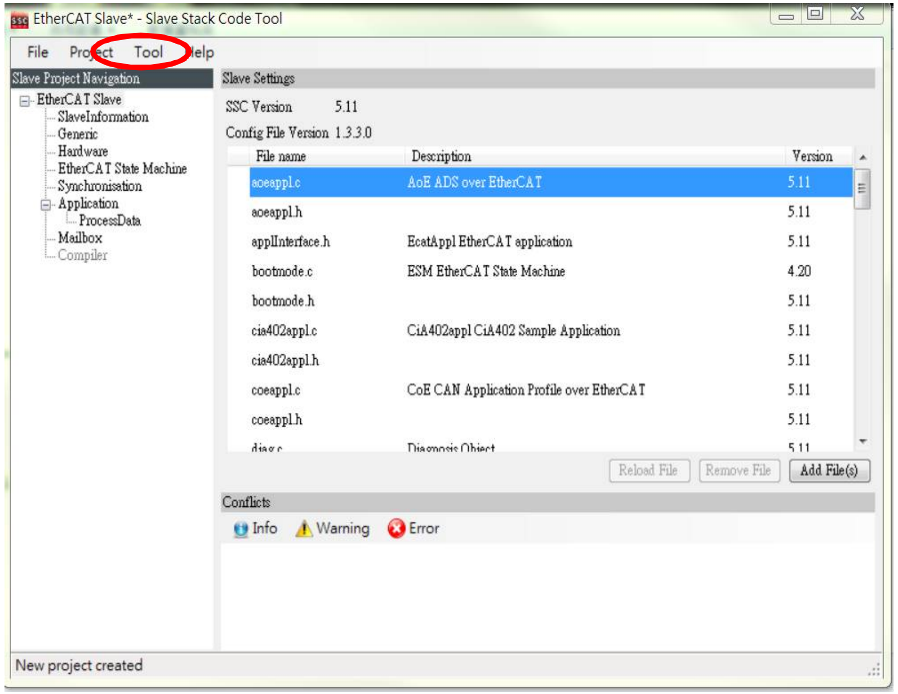
This file is included in the Microchip SDK

5. **找到9252_HW directory and double lick it**



SSC 工具

7. **Go Tool → Application → “IMPORT”**



SSC Version 5.11

Config File Version 1.3.3.0

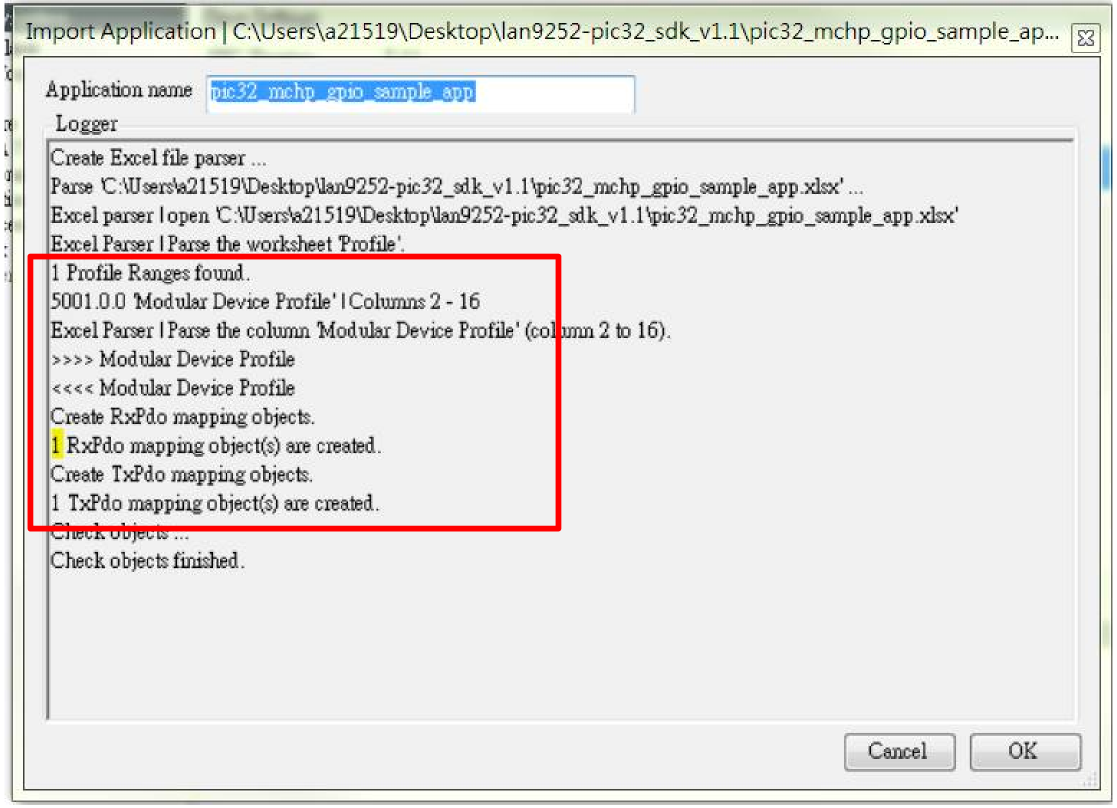
File name	Description	Version
aoeappl.c	AoE ADS over EtherCAT	5.11
aoeappl.h		5.11
applInterface.h	EcatAppl EtherCAT application	5.11
bootmode.c	ESM EtherCAT State Machine	4.20
bootmode.h		5.11
cia402appl.c	CiA402appl CiA402 Sample Application	5.11
cia402appl.h		5.11
coeappl.c	CoE CAN Application Profile over EtherCAT	5.11
coeappl.h		5.11
diag.c	Diagnosis Object	5.11

New project created

8. **Import the Excel PDO mapping @ SDK first layer “pic32_mchp_gpio_sample_app.xls”, then “OK”**

SSC 工具

9. **You should see following**



Import Application | C:\Users\a21519\Desktop\lan9252-pic32_sdk_v1.1\pic32_mchp_gpio_sample_ap...

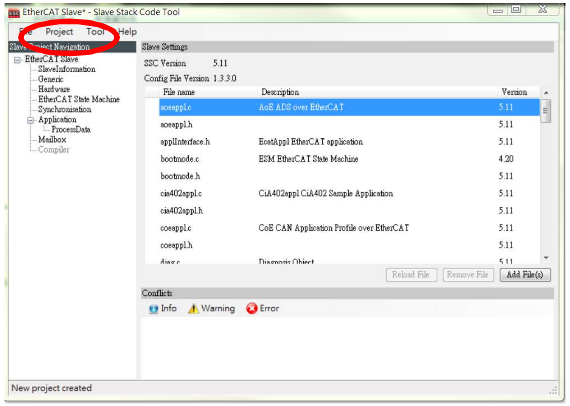
Application name: pic32_mchp_gpio_sample_app

Logger

```
Create Excel file parser ...
Parse 'C:\Users\a21519\Desktop\lan9252-pic32_sdk_v1.1\pic32_mchp_gpio_sample_app.xlsx' ...
Excel parser | open 'C:\Users\a21519\Desktop\lan9252-pic32_sdk_v1.1\pic32_mchp_gpio_sample_app.xlsx'
Excel Parser | Parse the worksheet 'Profile'.
1 Profile Ranges found.
5001.0.0 'Modular Device Profile' | Columns 2 - 16
Excel Parser | Parse the column 'Modular Device Profile' (column 2 to 16).
>>>> Modular Device Profile
<<<< Modular Device Profile
Create RxPdo mapping objects.
1 RxPdo mapping object(s) are created.
Create TxPdo mapping objects.
1 TxPdo mapping object(s) are created.
Check objects ...
Check objects finished.
```

SSC 工具

11. **At SSC tool → Project → create new slave file**



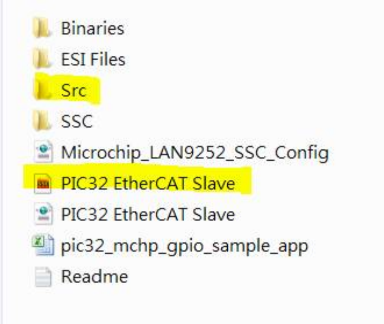
EtherCAT Slave* - Slave Stack Code Tool

SSC Version 5.11
Config File Version 1.3.3.0

File name	Description	Version
aoeappl.c	AoE ADS over EtherCAT	5.11
aoeappl.h		5.11
applInterface.h	EcatAppl EtherCAT application	5.11
bootmode.c	ESM EtherCAT State Machine	4.20
bootmode.h		5.11
cia402appl.c	CiA402appl CiA402 Sample Application	5.11
cia402appl.h		5.11
coeappl.c	CoE CAN Application Profile over EtherCAT	5.11
coeappl.h		5.11
diag.c	Diagnosis Object	5.11

New project created

12. **Original file will be saved at first layer, and a dialogs box will show up. New SRC directory generated and new ESI too**



Binaries
ESI Files
Src
SSC
Microchip_LAN9252_SSC_Config
PIC32 EtherCAT Slave
PIC32 EtherCAT Slave
pic32_mchp_gpio_sample_app
Readme

SSC 工具

12. GOTO SRC, copy all but **deselected** following files (將SRC目錄內之所有 .c/.h copy 但以下幾個檔案不要選)
    - 9252_HW.c & .h
    - pic32_mchp_gpio_sample_app.c & .h
13. Copy all files to SSC/COMMON expect above files
14. Go to MPLAB X flow

MICROCHIP

Regional Training Centers

LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow

EEPROM programming

MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

EEPROM 燒錄

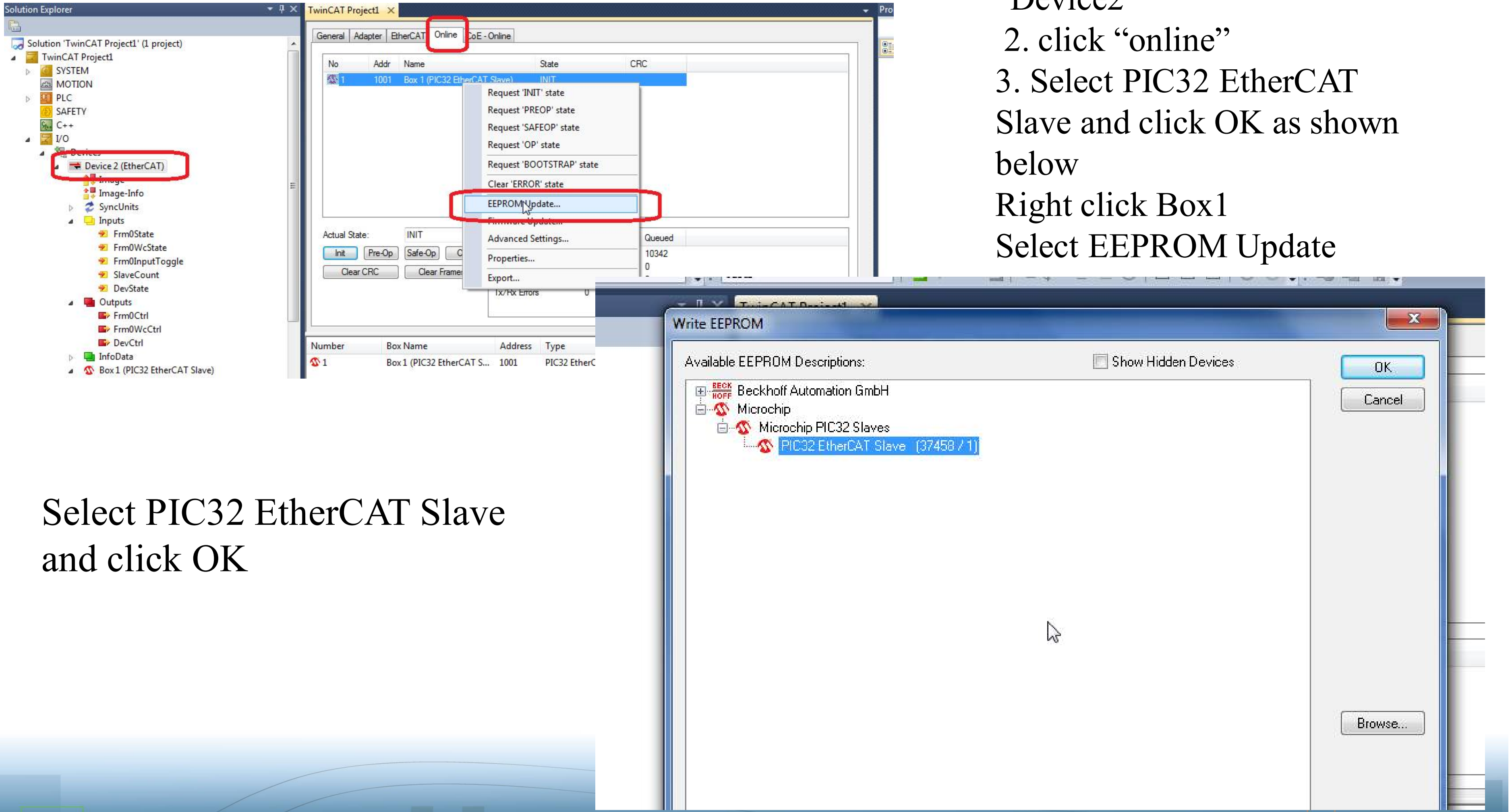
- **9252**
  - 透過TWINCAT燒錄ESI 檔
- **PIC**
  - 透過PIC KIT3燒錄MPLAB X編譯之HEX檔

9252 via TWINCAT

- **SSC 產生之ESI.xml 位於SSC root**

1. Double click menu “Device2”
2. click “online”
3. Select PIC32 EtherCAT Slave and click OK as shown below

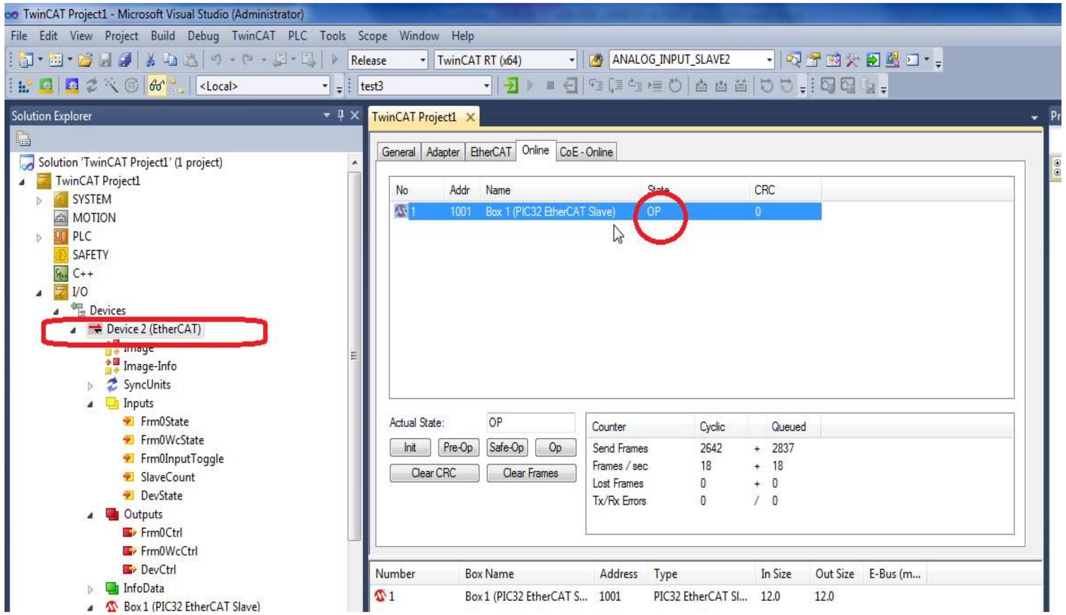
Right click Box1
Select EEPROM Update



Select PIC32 EtherCAT Slave and click OK

9252 via TWINCAT

- Once EEPROM is Programmed, Power off EVB and power ON again.
- Double click menu “Device2”, click “online” and check device status should be in OP as shown below



No	Addr	Name	State	CRC
1	1001	Box 1 (PIC32 EtherCAT Slave)	OP	0

Actual State: OP

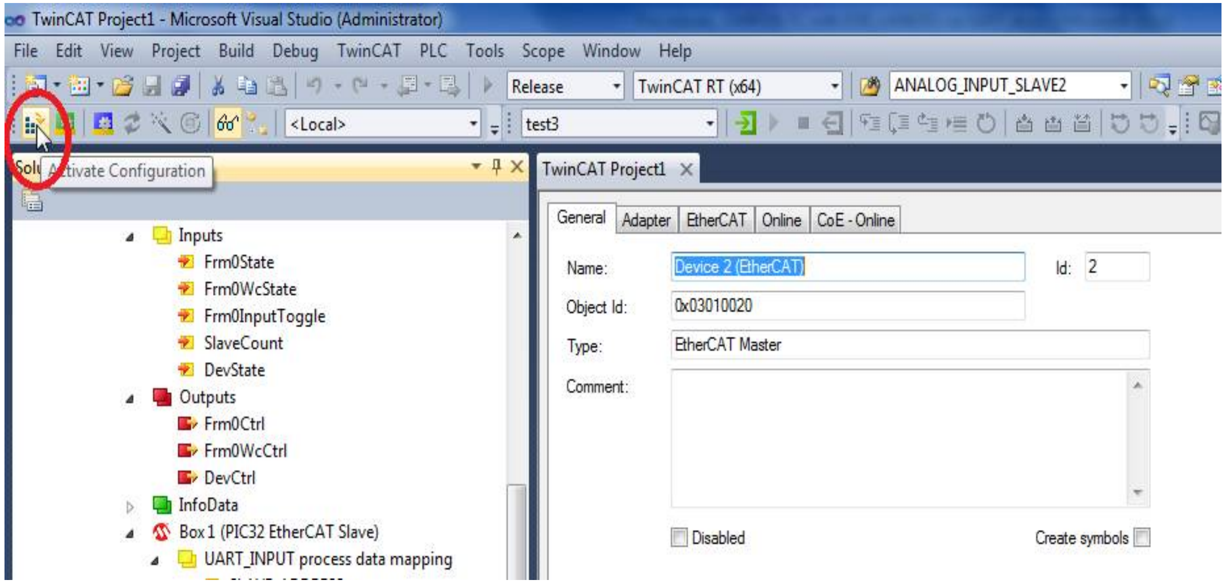
Counter	Cyclic		Queued
Send Frames	2642	+	2837
Frames / sec	18	+	18
Lost Frames	0	+	0
Tx/Rx Errors	0	/	0

Number	Box Name	Address	Type	In Size	Out Size	E-Bus (m...
1	Box 1 (PIC32 EtherCAT S...	1001	PIC32 EtherCAT Sl...	12.0	12.0	

Regional Training Centers

9252 via TWINCAT

- **Click Activate Configuration button and select OK as shown below**
- **Copy xml file into C:\TwinCAT\3.1\Config\Io\EtherCAT directory. After copying, “Reload Device Descriptions”**
- **Scan again**



Name: Device 2 (EtherCAT)

Id: 2

Object Id: 0x03010020

Type: EtherCAT Master

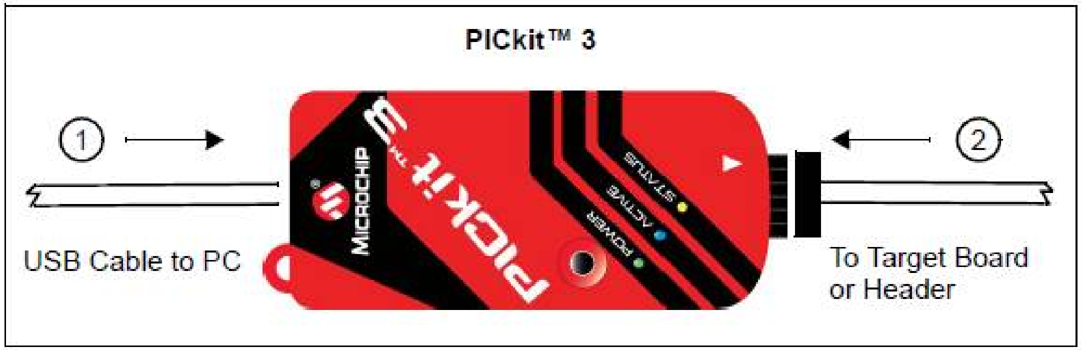
Comment:

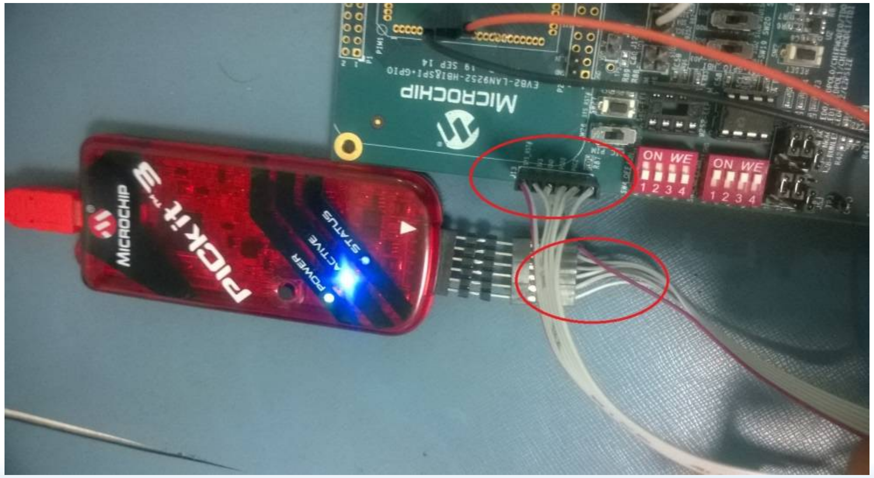
☐ Disabled

Create symbols ☐

PIC via PIC KIt 3

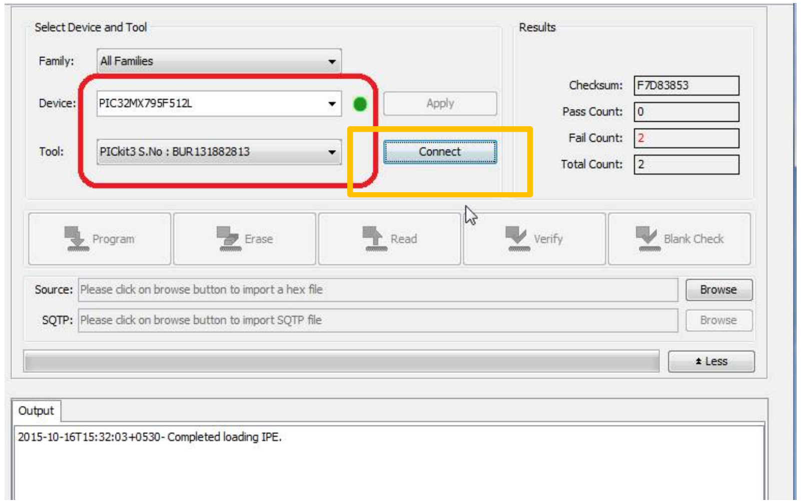
- SSC 產生之HEX file 位置: \SSC\PIC32 or PIC32-SPI \dist\HBI_MSP_16BIT_XC32_PIC32MX795F512L\production
- 使用　PIC Kit3





PIC via PIC KIt 3

- **Open MPLAB IPE and Select Target Device as shown below and then click connect button**



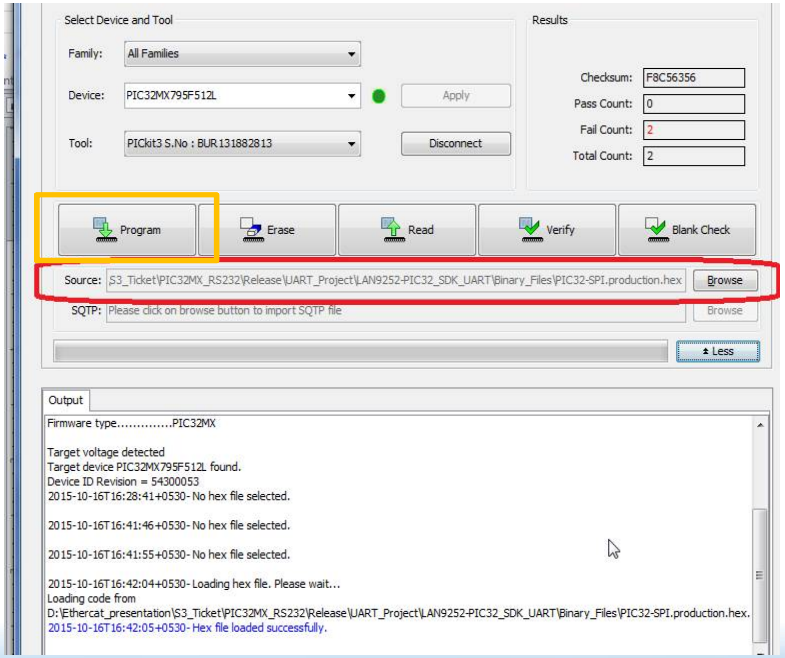
Family: All Families
Device: PIC32MX795F512L
Tool: PICkit3 S.No : BUR131882813

Checksum: F7D83853
Pass Count: 0
Fail Count: 2
Total Count: 2

Source: Please click on browse button to import a hex file
SQTP: Please click on browse button to import SQTP file

```
2015-10-16T15:32:03+0530- Completed loading IPE.
```

- **Locate the HEX source, then “program”**



Family: All Families
Device: PIC32MX795F512L
Tool: PICkit3 S.No : BUR131882813

Checksum: F8C56356
Pass Count: 0
Fail Count: 2
Total Count: 2

Source: S3_Ticket\PIC32MX_RS232\Release\UART_Project\LAN9252-PIC32_SDK_UART\Binary_Files\PIC32-SPI.production.hex
SQTP: Please click on browse button to import SQTP file

```
Firmware type..............PIC32MX

Target voltage detected
Target device PIC32MX795F512L found.
Device ID Revision = 54300053
2015-10-16T16:28:41+0530- No hex file selected.

2015-10-16T16:41:46+0530- No hex file selected.

2015-10-16T16:41:55+0530- No hex file selected.

2015-10-16T16:42:04+0530- Loading hex file. Please wait...
Loading code from
D:\Ethercat_presentation\S3_Ticket\PIC32MX_RS232\Release\UART_Project\LAN9252-PIC32_SDK_UART\Binary_Files\PIC32-SPI.production.hex.
2015-10-16T16:42:05+0530- Hex file loaded successfully.
```

MICROCHIP

Regional Training Centers

LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

After SSC flow

- Refer to previous SSC section, u will copy all files expect the 9252_HW.c/h and PIC32_mchp_gpio_sample_appl.c/h into SSC/COMMON
- Decide running HBI mode or SPI mode
- Run MPLAB X by importing the new source
- HEX file will store in : C:\Users\a21519\Documents\A21519\DATA_BASE\SMSC_ETHERCAT\twincat_projects\2195LAN9252-PIC32_SDK_V1.0.1_ADC\SSC\PIC32 or PIC32-SPI \dist\HBI_MSP_16BIT_XC32_PIC32MX795F512L\production
- Warming are fine, u only need fix Errors

MICROCHIP

Regional Training Centers

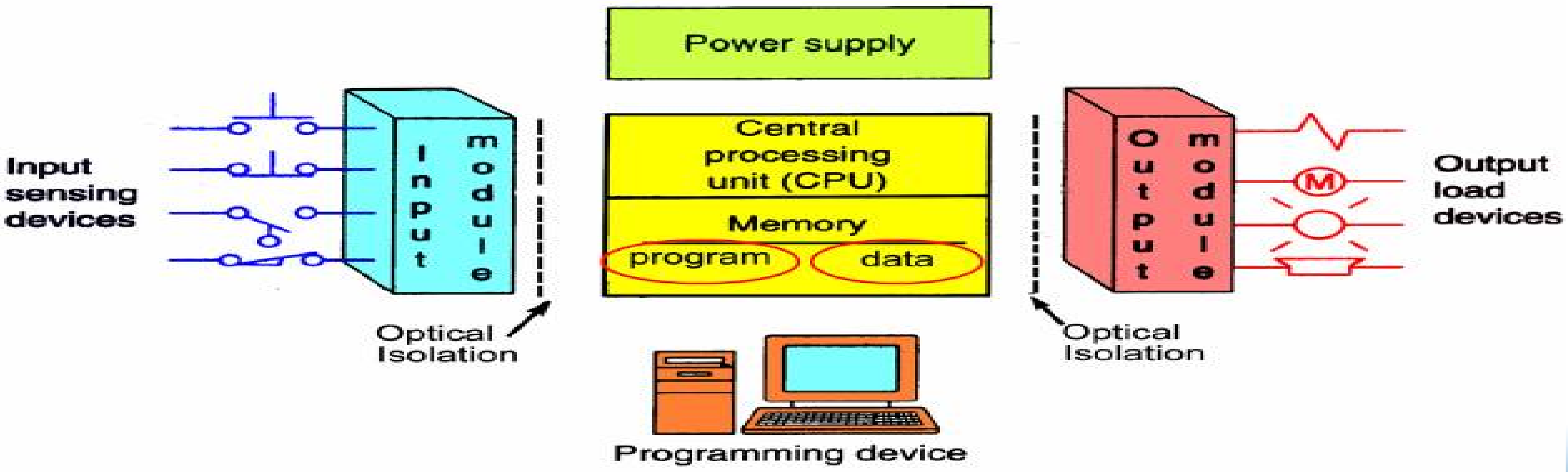
LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程

PLC Structure text code basic

UART/MIO/ADC application
APPL_ application code briefing
Hand on
Q&A , dismiss

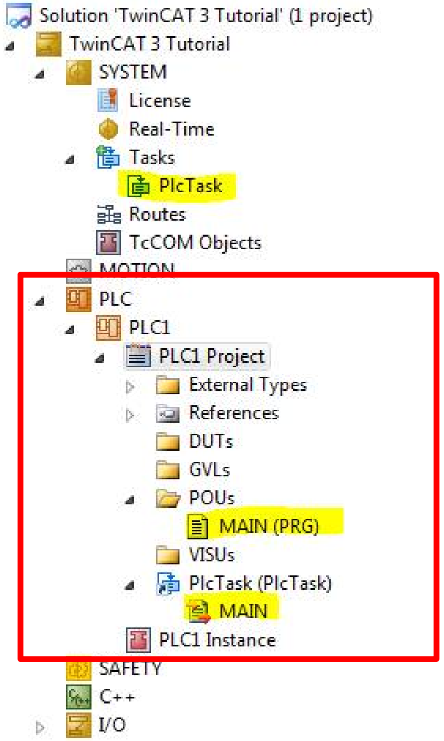
PLC : Introduction

- A PROGRAMMABLE LOGIC CONTROLLER (PLC) is an industrial computer control system that continuously monitors the state of input devices and makes decisions based upon a custom program to control the state of output devices.
- Made up of two basic components : input/output (I/O) system and CPU
- Input Interface is a Bank of terminals that Physically connects input devices (like Push buttons, Limited switches) to CPU
- Output Interface is a Bank of terminals that Physically connects Output devices (such as solenoids and motor starters) to CPU



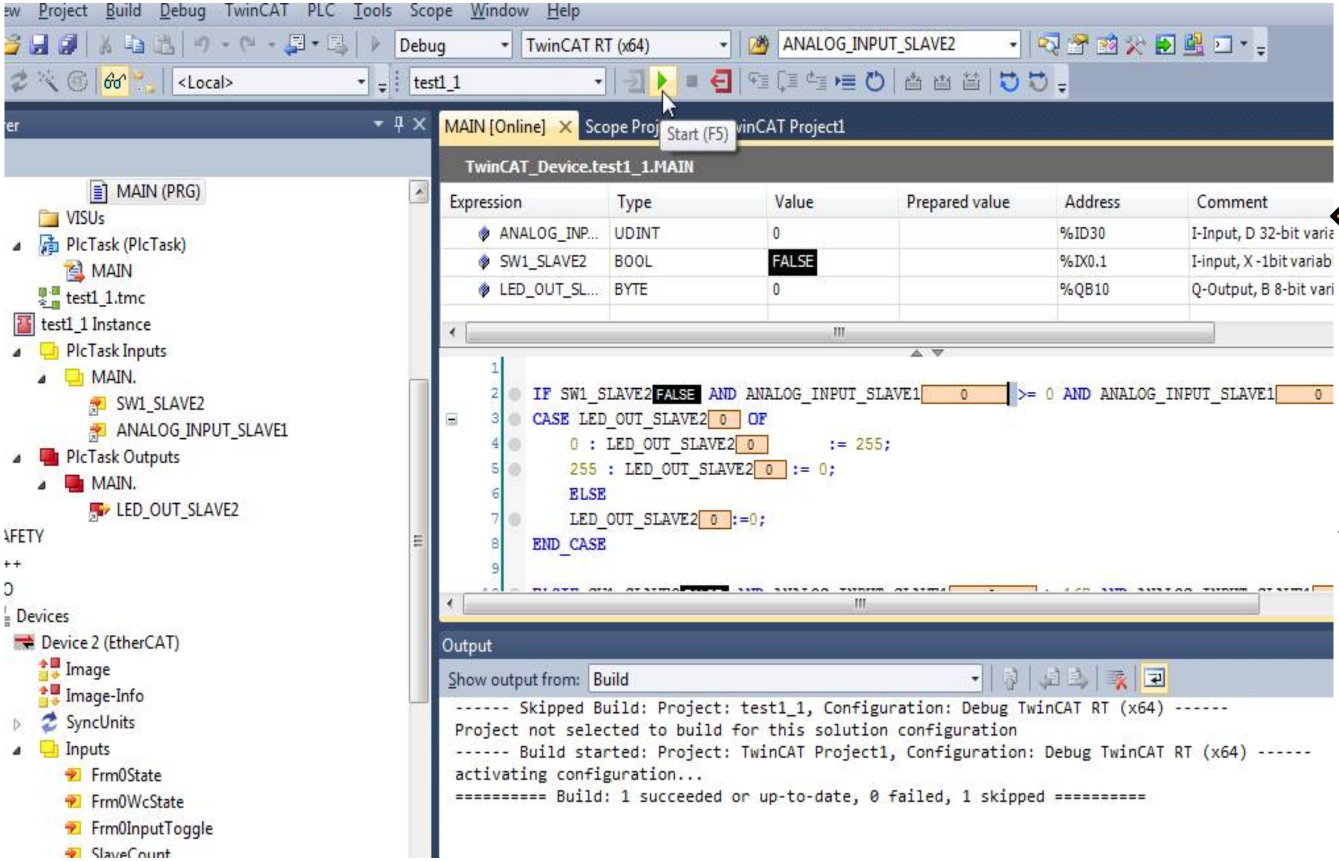
PLC code 格式

- **Follow IEC 61131-3**
  - ◆ ***Structured Text***
- **Create a PLC program using TwinCAT PLC**
- **Link the PLC program to the I/O configured in TwinCAT System Manager**



Regional Training Centers

ST code in TWINCAT



TwinCAT_Device.test1_1.MAIN

Expression	Type	Value	Prepared value	Address	Comment
ANALOG_INP...	UDINT	0		%ID30	I-Input, D 32-bit varia
SW1_SLAVE2	BOOL	FALSE		%IX0.1	I-input, X -1bit variab
LED_OUT_SL...	BYTE	0		%QB10	Q-Output, B 8-bit vari

```
IF SW1_SLAVE2 FALSE  AND ANALOG_INPUT_SLAVE1[   0   ] >= 0 AND ANALOG_INPUT_SLAVE1[   0
CASE LED_OUT_SLAVE2[ 0 ] OF
    0 : LED_OUT_SLAVE2[ 0 ]        := 255;
    255 : LED_OUT_SLAVE2[ 0 ] := 0;
    ELSE
    LED_OUT_SLAVE2[ 0 ]:=0;
END_CASE
```

Show output from: Build

```
------ Skipped Build: Project: test1_1, Configuration: Debug TwinCAT RT (x64) ------
Project not selected to build for this solution configuration
------ Build started: Project: TwinCAT Project1, Configuration: Debug TwinCAT RT (x64) ------
activating configuration...
========== Build: 1 succeeded or up-to-date, 0 failed, 1 skipped ==========
```

變數區

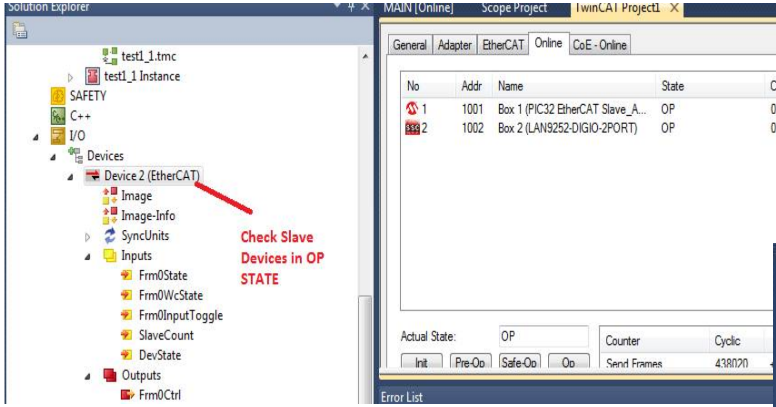
程式區

PLC
ST
IO/變
數對
應區

從站端IO資訊

PLC ST flow

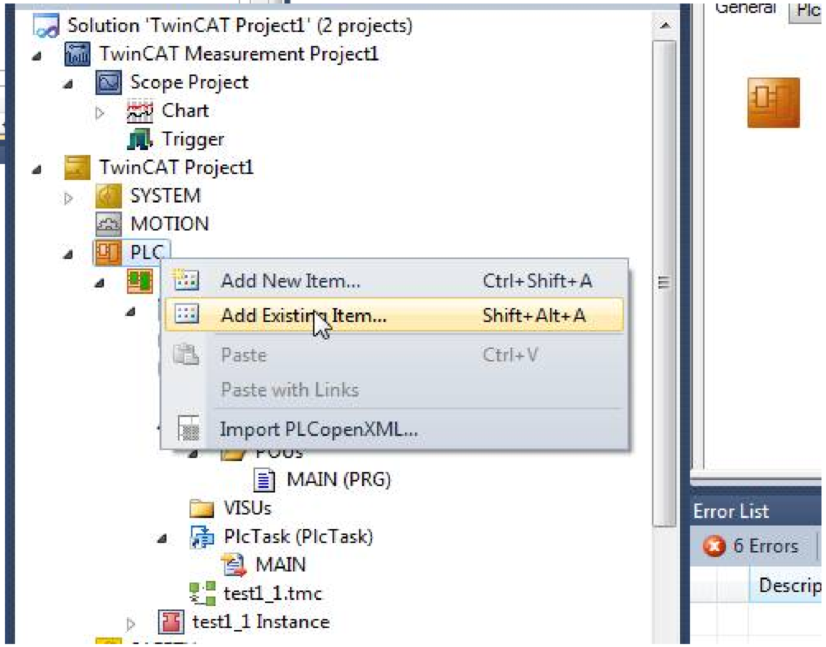
- **Twincat Scan, Check Device status should be in OP**



Check Slave Devices in OP STATE

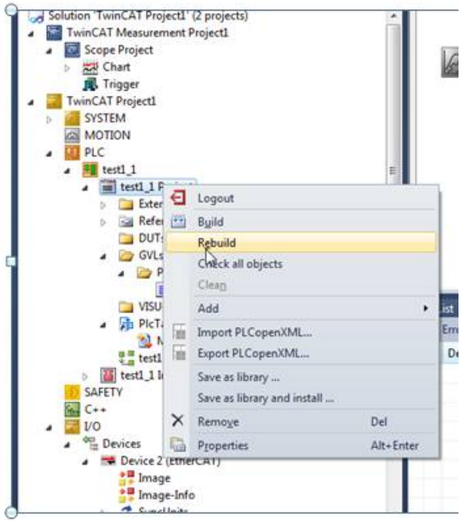
No	Addr	Name	State	CRC
1	1001	Box 1 (PIC32 EtherCAT Slave_A...	OP	0, 0
2	1002	Box 2 (LAN9252-DIGIO-2PORT)	OP	0

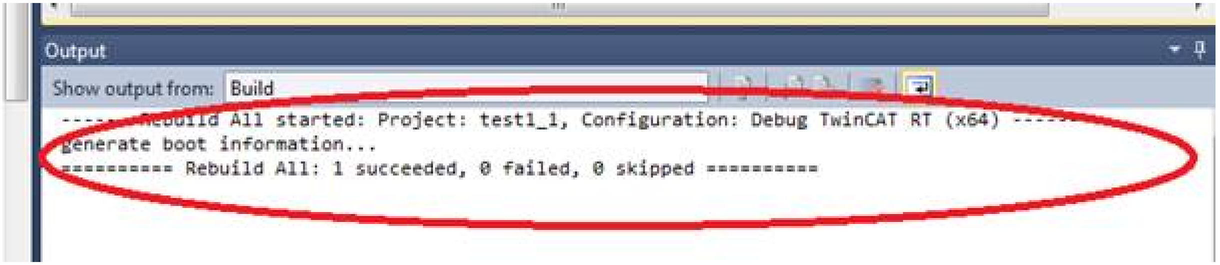
- **Add an existing PLC Program**



PLC ST flow

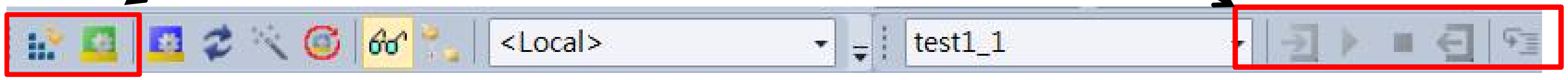
- Build and check if any error



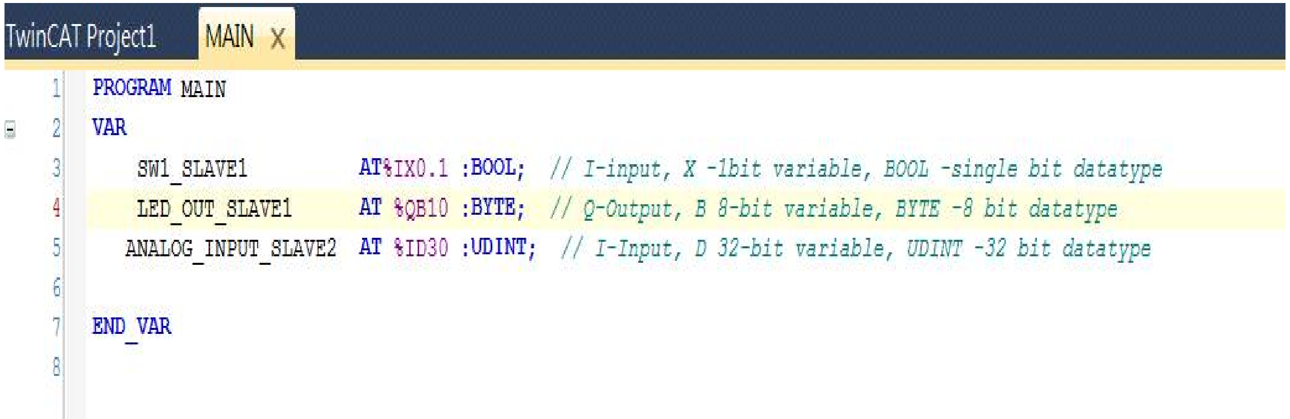


```
------ Rebuild All started: Project: test1_1, Configuration: Debug TwinCAT RT (x64) ------
generate boot information...
========== Rebuild All: 1 succeeded, 0 failed, 0 skipped ==========
```

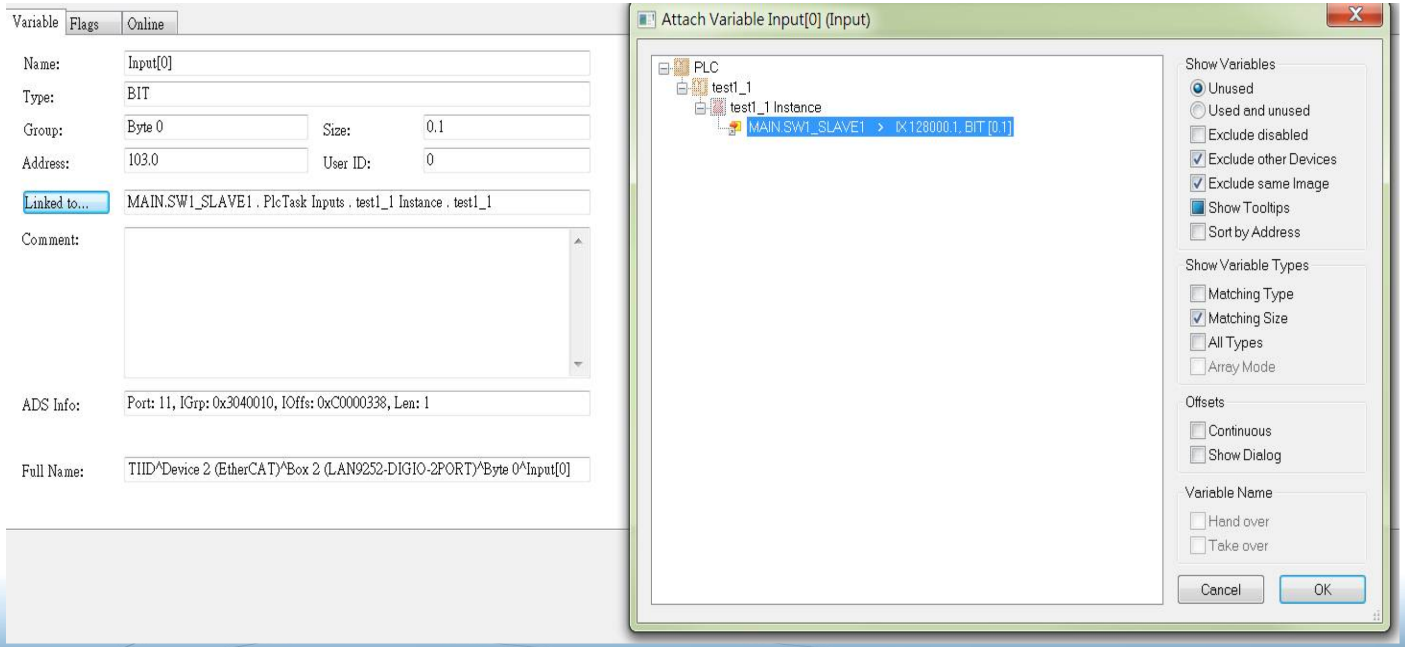
- All IOs make change link
- Activated, Restart, login in and Start
- PLC program should run



Change link in detail



```
PROGRAM MAIN
VAR
    SW1_SLAVE1          AT%IX0.1 :BOOL;  // I-input, X -1bit variable, BOOL -single bit datatype
    LED_OUT_SLAVE1      AT %QB10 :BYTE;  // Q-Output, B 8-bit variable, BYTE -8 bit datatype
   ANALOG_INPUT_SLAVE2  AT %ID30 :UDINT;  // I-Input, D 32-bit variable, UDINT -32 bit datatype

END_VAR
```



Name: Input[0]
Type: BIT
Group: Byte 0
Size: 0.1
Address: 103.0
User ID: 0
Linked to... MAIN.SW1_SLAVE1 . PlcTask Inputs . test1_1 Instance . test1_1
Comment:
ADS Info: Port: 11, IGrp: 0x3040010, IOffs: 0xC0000338, Len: 1
Full Name: TIID^Device 2 (EtherCAT)^Box 2 (LAN9252-DIGIO-2PORT)^Byte 0^Input[0]

PLC
test1_1
test1_1 Instance
MAIN.SW1_SLAVE1 > IX 128000.1, BIT [0.1]

Show Variables
- ● Unused
- ○ Used and unused
- ☐ Exclude disabled
- ☑ Exclude other Devices
- ☑ Exclude same Image
- ☐ Show Tooltips
- ☐ Sort by Address

Show Variable Types
- ☐ Matching Type
- ☑ Matching Size
- ☐ All Types
- ☐ Array Mode

Offsets
- ☐ Continuous
- ☐ Show Dialog

Variable Name
- ☐ Hand over
- ☐ Take over

MICROCHIP

Regional Training Centers

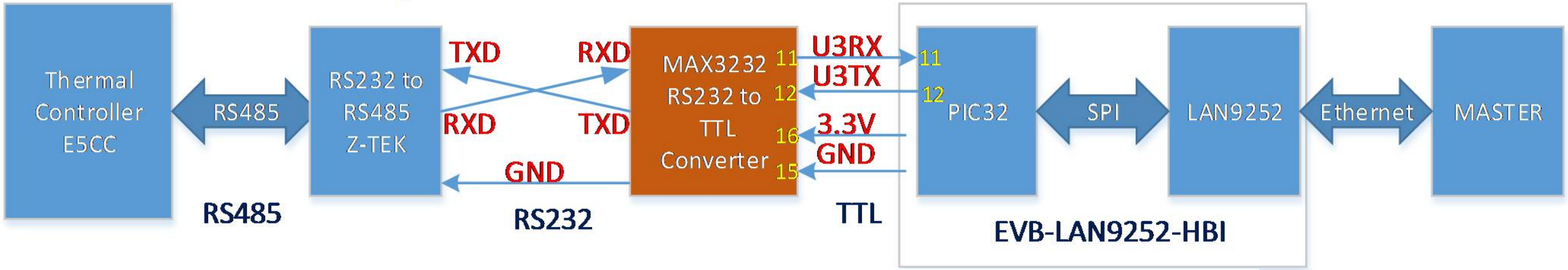
LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic

UART/MIO/ADC application

APPL_ application code briefing
Hand on
Q&A , dismiss

UART application (to 485)

Setup : MASTER to Thermal Controller



Thermal Controller E5CC

RS485

RS485

RS232 to RS485 Z-TEK

TXD

RXD

RXD

TXD

GND

RS232

MAX3232 RS232 to TTL Converter

11

12

16

15

U3RX

U3TX

3.3V

GND

TTL

11

12

PIC32

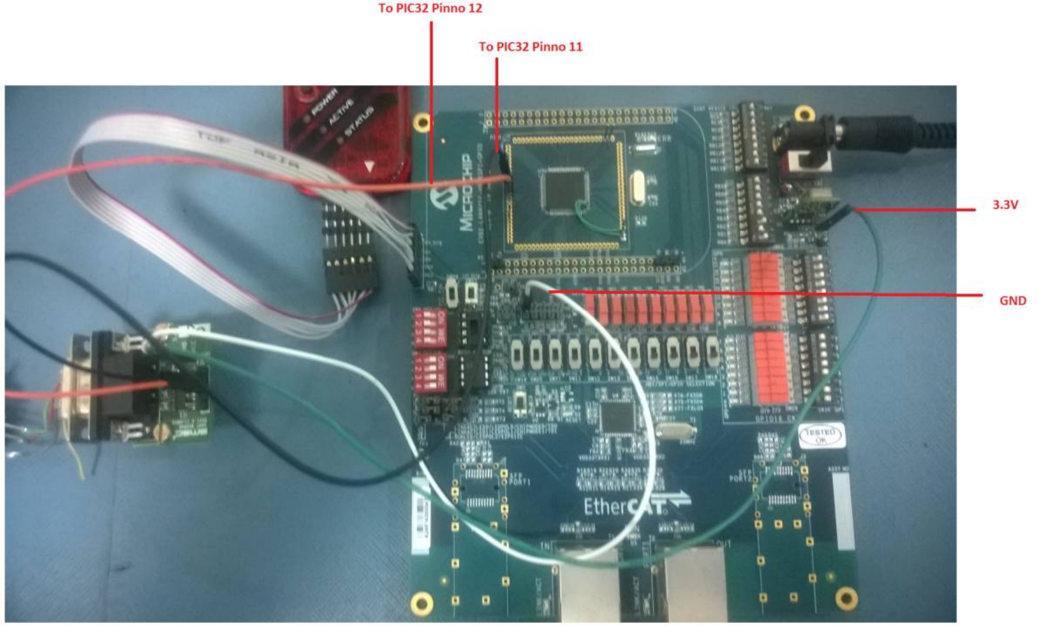
SPI

LAN9252

EVB-LAN9252-HBI

Ethernet

MASTER



To PIC32 Pinno 12

To PIC32 Pinno 11

3.3V

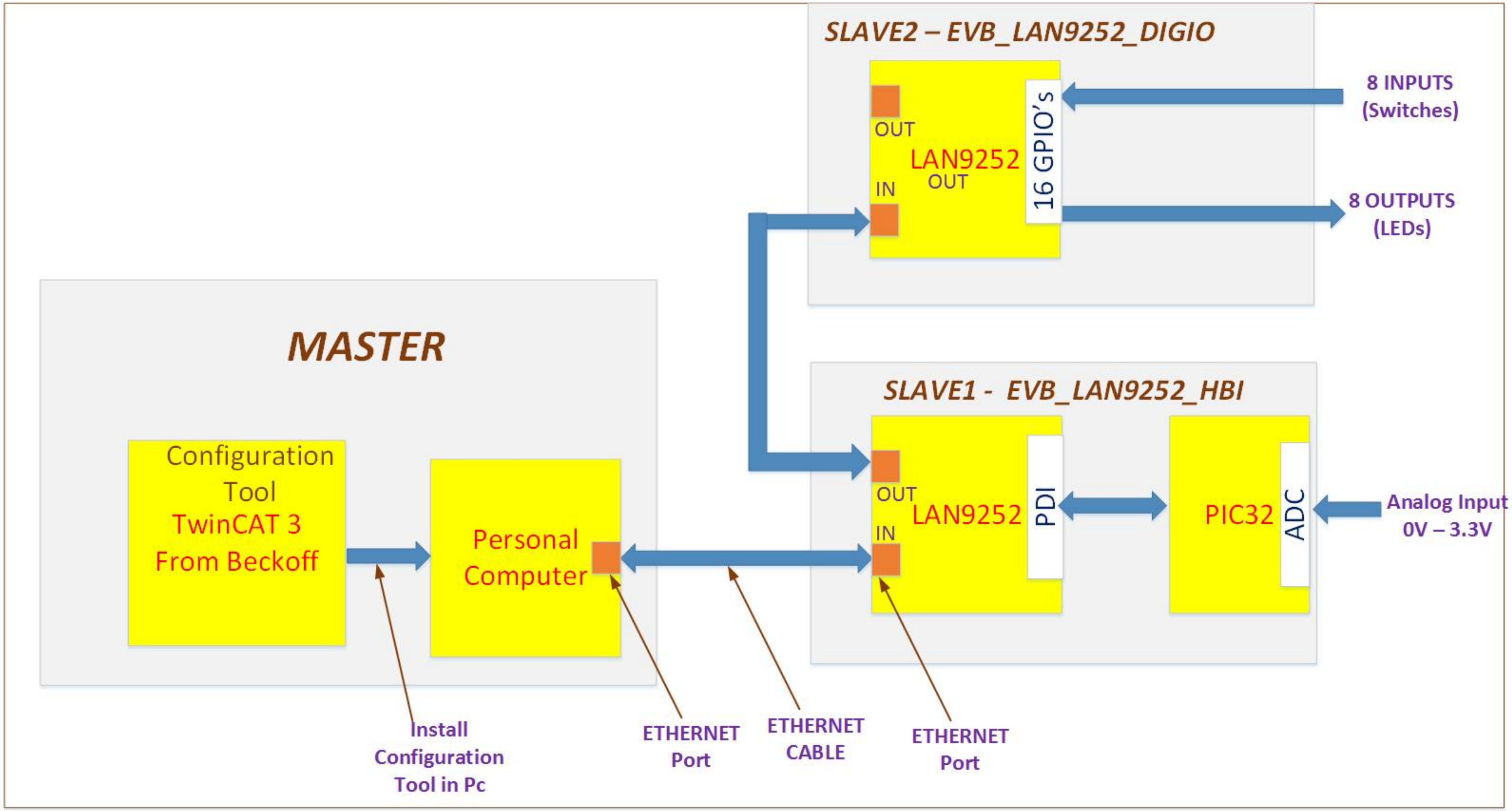
GND

SDK-32-in-32 out

- **LAN9252** 只有**16**個**IO**接口
- 客戶要**32-In,32-Out** 怎麼辦
- 透過**SPI**跟**PIC**連接 長出其他**IO**
-

Regional Training Centers

EtherCAT® Demo: Controlling GPIO's using ADC



Microchip
Regional Training Centers

PLC: Truth Table

INPUTS			OUTPUTS
Slave 1		Slave2	Slave2
Analog input Voltage	Equivalent Decimal (32Bits)	SW1 (1 Bit)	Transition using LEDs (8 Bits)
0V to 0.5V	0 to 167	ON	LED Blinking
0.5V to 1V	167 to 333	ON	<-----
1V to 1.5V	333 to 500	ON	----->
1.5V to 2V	500 to 667	ON	<-- -->
2V to 2.5V	667 to 833	ON	--> <--
2.5V to 3.3V	822 to 1024	ON	<----- LED Blinking
XX	XX	OFF	LED OFF

MICROCHIP

Regional Training Centers

LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application

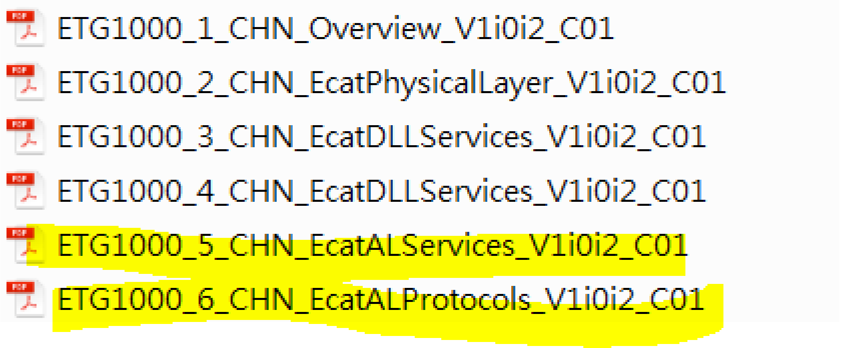
APPL_ application code briefing

Hand on
Q&A , dismiss

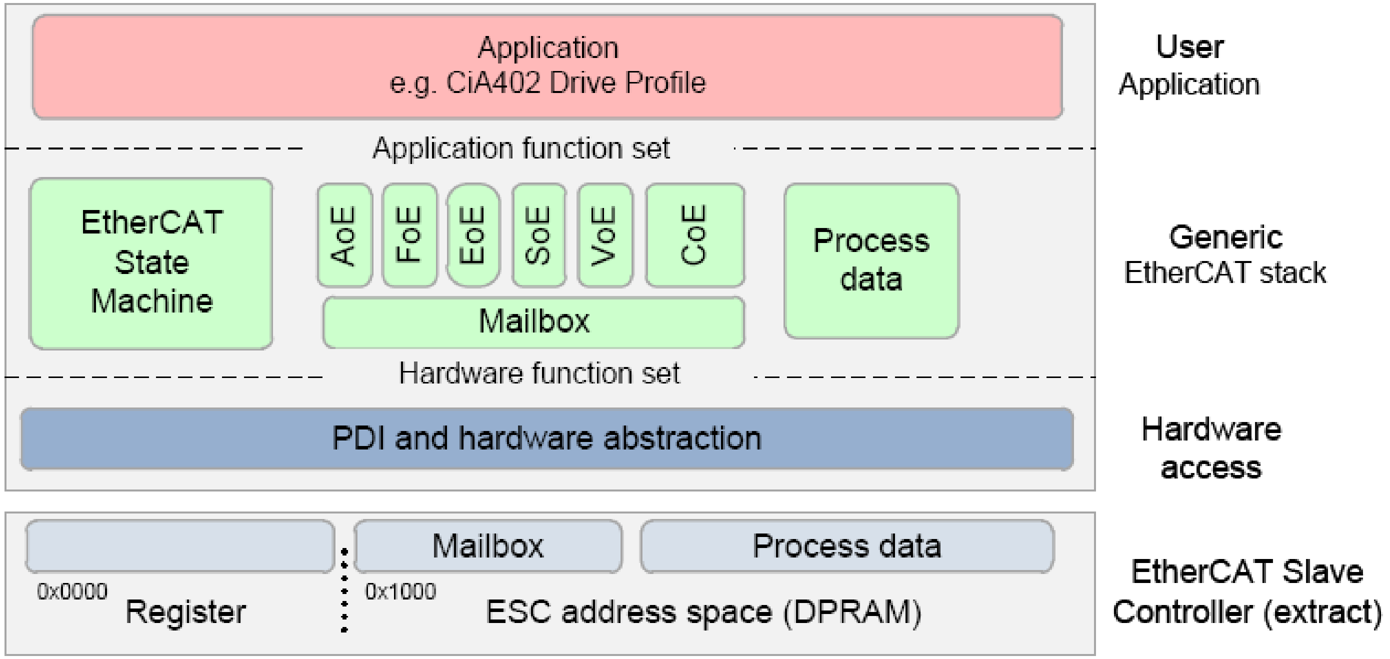
Microchip
Regional Training Centers

General code structure

- **SSC**



ETG1000_1_CHN_Overview_V1i0i2_C01
ETG1000_2_CHN_EcatPhysicalLayer_V1i0i2_C01
ETG1000_3_CHN_EcatDLLServices_V1i0i2_C01
ETG1000_4_CHN_EcatDLLServices_V1i0i2_C01
ETG1000_5_CHN_EcatALServices_V1i0i2_C01
ETG1000_6_CHN_EcatALProtocols_V1i0i2_C01



Application
e.g. CiA402 Drive Profile

User
Application

Application function set

EtherCAT
State
Machine

AoE
FoE
EoE
SoE
VoE
CoE

Mailbox

Process
data

Generic
EtherCAT stack

Hardware function set

PDI and hardware abstraction

Hardware
access

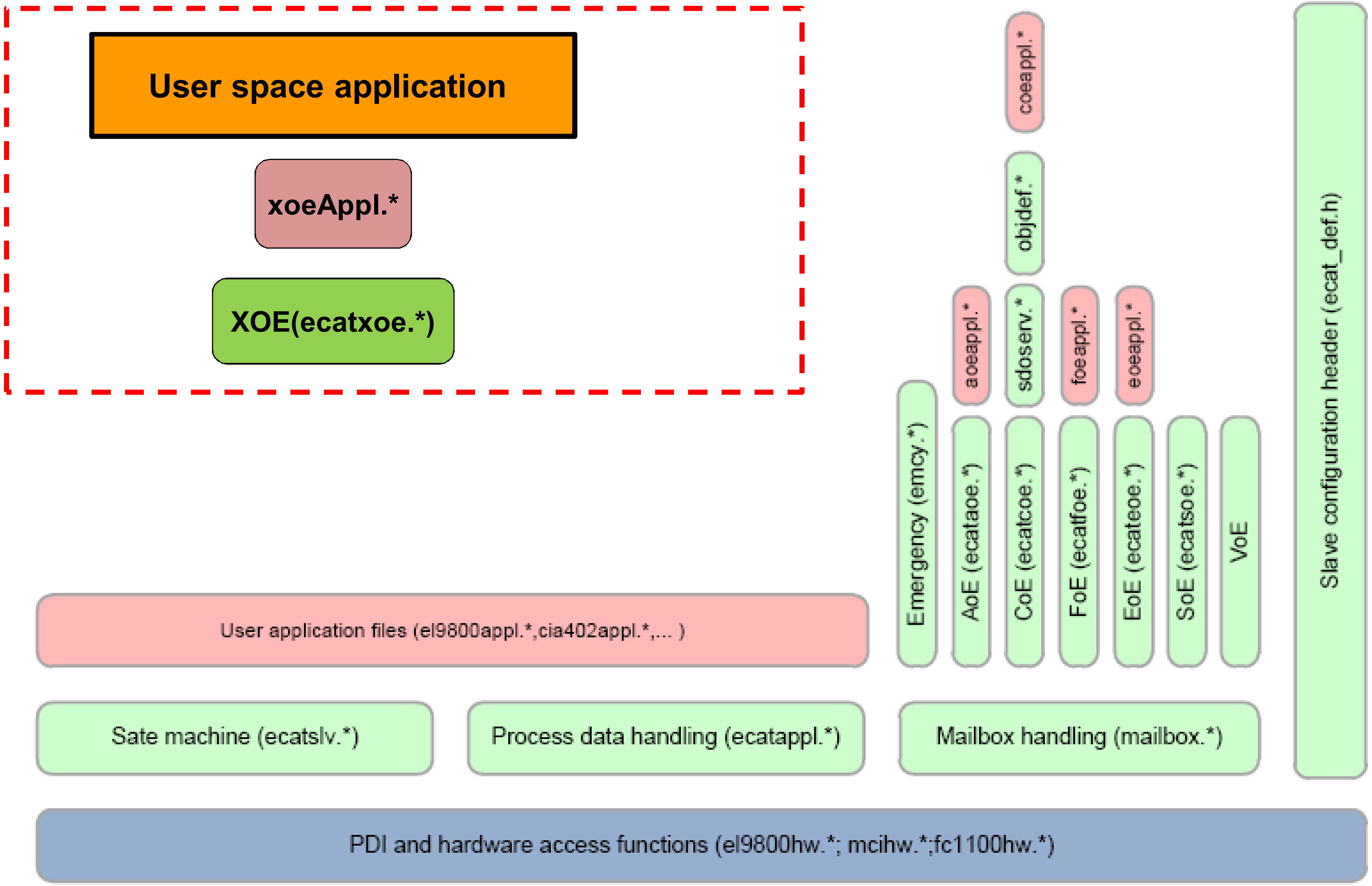
Mailbox
Process data

0x0000
Register

0x1000
ESC address space (DPRAM)

EtherCAT Slave
Controller (extract)

File stack association



User space application

xoeAppl.*

XOE(ecatxoe.*)

coeappl.*

objdef.*

aoeappl.*

sdoserv.*

foeappl.*

eoeappl.*

Emergency (emcy.*)

AoE (ecataoe.*)

CoE (ecatcoe.*)

FoE (ecatfoe.*)

EoE (ecateoe.*)

SoE (ecatsoe.*)

VoE

Slave configuration header (ecat_def.h)

User application files (el9800appl.*,cia402appl.*,...)

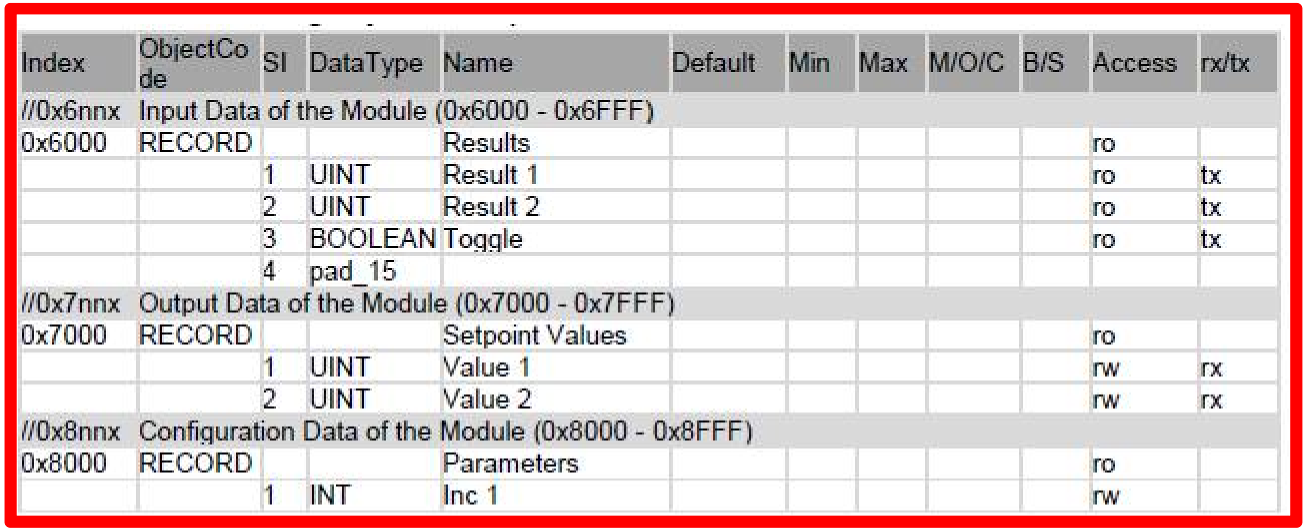
Sate machine (ecatslv.*)

Process data handling (ecatappl.*)

Mailbox handling (mailbox.*)

PDI and hardware access functions (el9800hw.*; mcihw.*;fc1100hw.*)

PDO excel



Index	ObjectCode	SI	DataType	Name	Default	Min	Max	M/O/C	B/S	Access	rx/tx
//0x6nnx	Input Data of the Module (0x6000 - 0x6FFF)										
0x6000	RECORD			Results						ro	
		1	UINT	Result 1						ro	tx
		2	UINT	Result 2						ro	tx
		3	BOOLEAN	Toggle						ro	tx
		4	pad_15								
//0x7nnx	Output Data of the Module (0x7000 - 0x7FFF)										
0x7000	RECORD			Setpoint Values						ro	
		1	UINT	Value 1						rw	rx
		2	UINT	Value 2						rw	rx
//0x8nnx	Configuration Data of the Module (0x8000 - 0x8FFF)										
0x8000	RECORD			Parameters						ro	
		1	INT	Inc 1						rw	

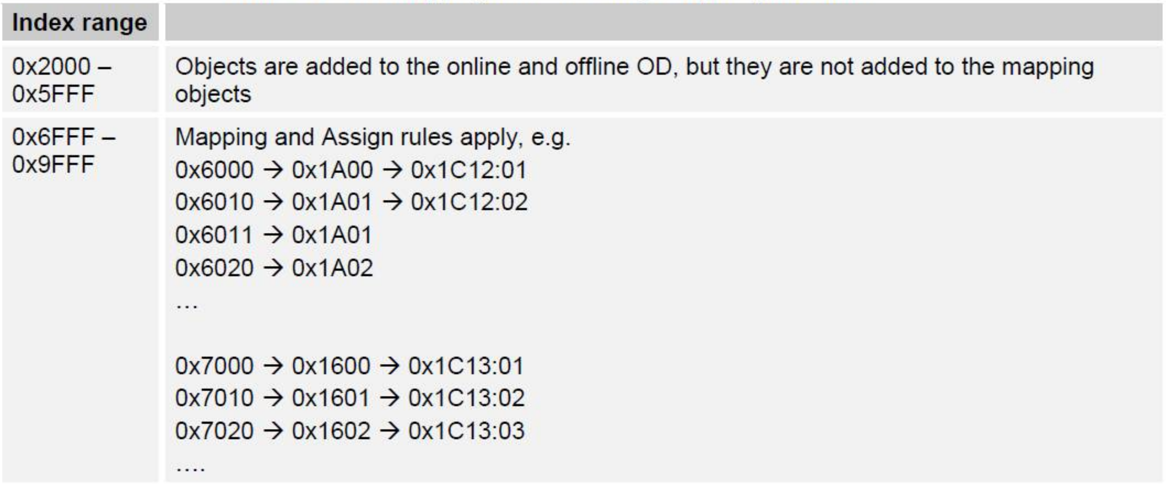


Table 21: PDO mapping and SM assign object generation

Index range	
0x2000 – 0x5FFF	Objects are added to the online and offline OD, but they are not added to the mapping objects
0x6FFF – 0x9FFF	Mapping and Assign rules apply, e.g. 0x6000 → 0x1A00 → 0x1C12:01 0x6010 → 0x1A01 → 0x1C12:02 0x6011 → 0x1A01 0x6020 → 0x1A02 … 0x7000 → 0x1600 → 0x1C13:01 0x7010 → 0x1601 → 0x1C13:02 0x7020 → 0x1602 → 0x1C13:03 ….

Table 4: Object Dictionary Structure

Index	Object Dictionary Area	Description / Value
EtherCAT Communication Area, see 4.3.1		
0x1000 - 0x1FFF	Communication Area	Standard communication area
Object Area of the Modules, see 4.3.2		
0x2000 - 0x5FFF	Manufacturer Specific Area	
0x6000 - 0x6FFF	Input Area	Objects that can be mapped to TxPDOs
0x7000 - 0x7FFF	Output Area	Objectsthat can be mapped to RxPDOs
0x8000 - 0x8FFF	Configuration Area	Configuration and setting objects
0x9000 - 0x9FFF	Information Area	Scanned information from the modules
0xA000 - 0xAFFF	Diagnosis Area	Diagnostic, status, statistic or other information
0xB000 - 0xBFFF	Service Transfer Area	Service objects
0xC000 - 0xEFFF	*Reseved Area*	
Object Area of the Device, see 4.3.3		
0xF000 - 0xFFFF	Device Area	Parameters belonging to the device

CIA profile (402)

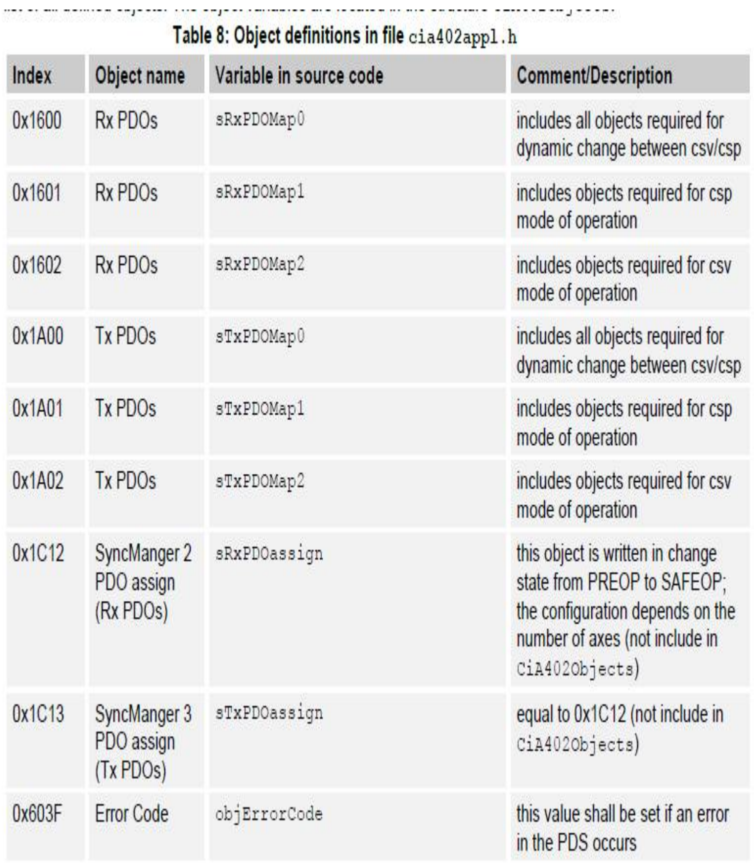
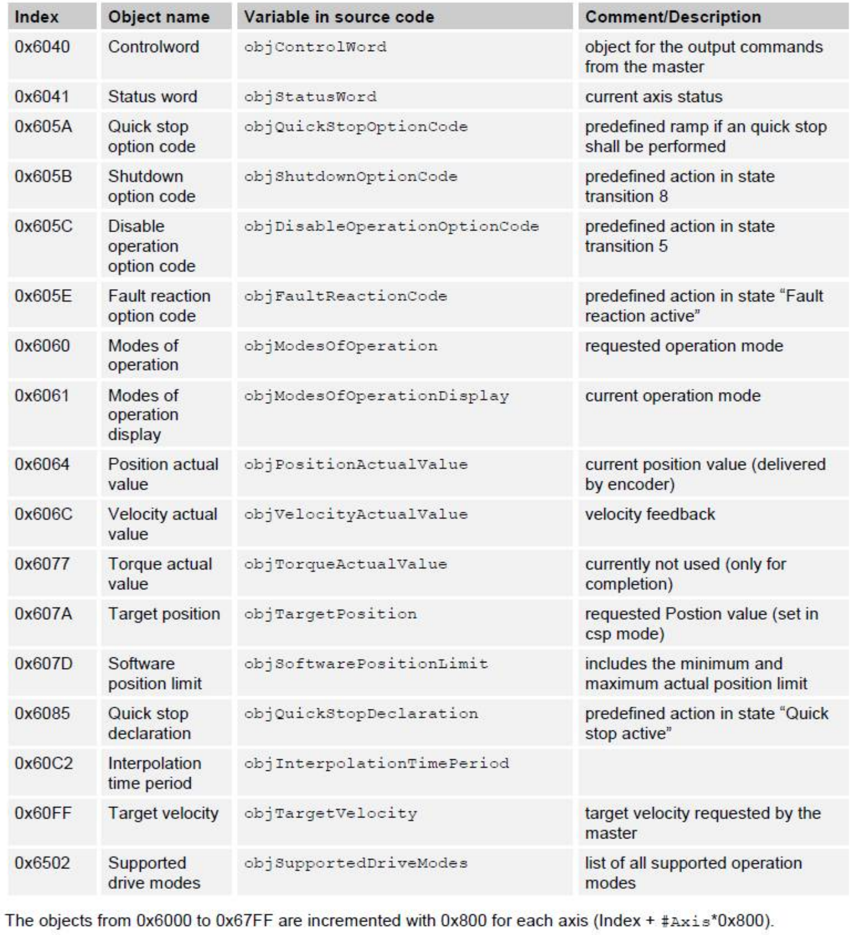


Table 8: Object definitions in file `cia402appl.h`

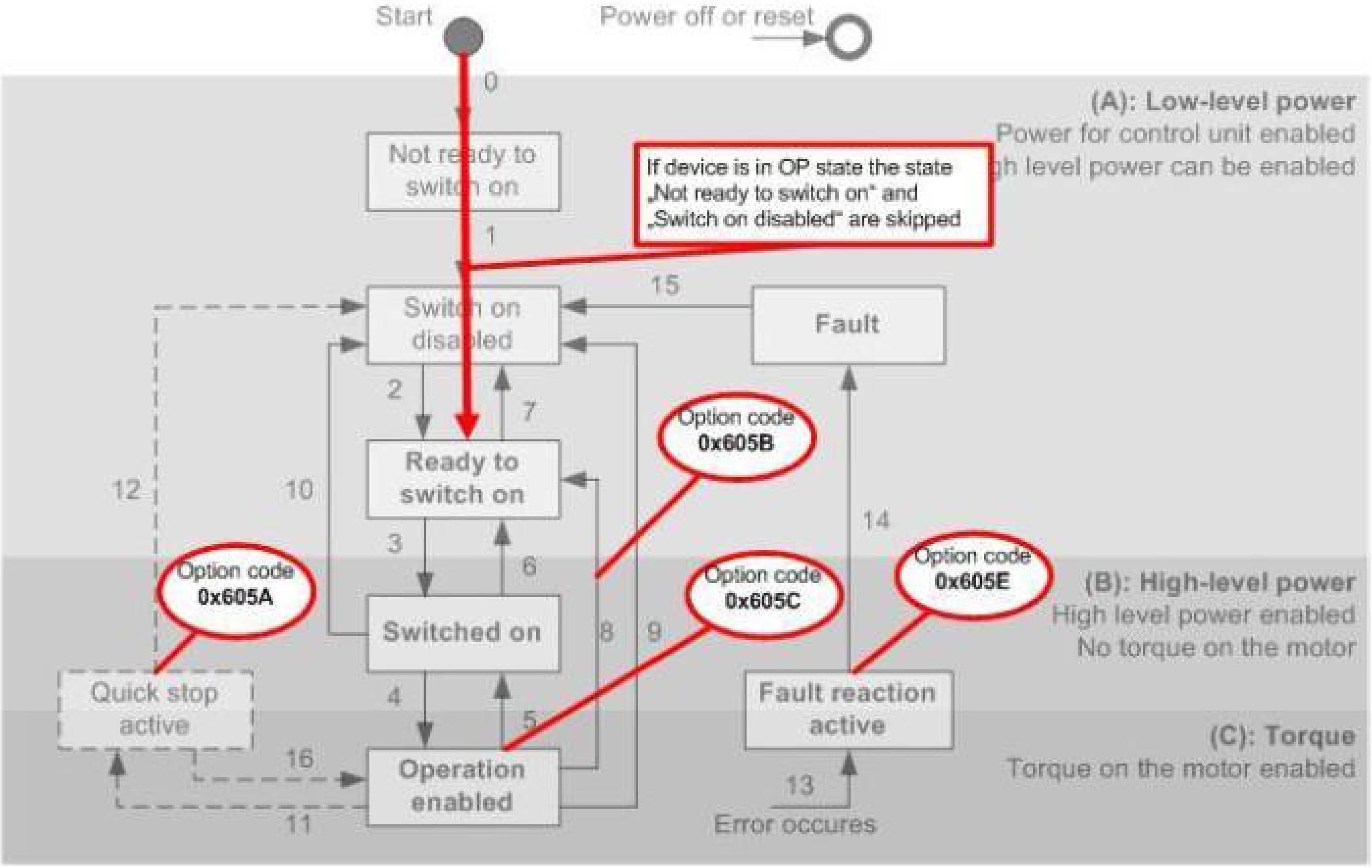
Index	Object name	Variable in source code	Comment/Description
0x1600	Rx PDOs	`sRxPDOMap0`	includes all objects required for dynamic change between csv/csp
0x1601	Rx PDOs	`sRxPDOMap1`	includes objects required for csp mode of operation
0x1602	Rx PDOs	`sRxPDOMap2`	includes objects required for csv mode of operation
0x1A00	Tx PDOs	`sTxPDOMap0`	includes all objects required for dynamic change between csv/csp
0x1A01	Tx PDOs	`sTxPDOMap1`	includes objects required for csp mode of operation
0x1A02	Tx PDOs	`sTxPDOMap2`	includes objects required for csv mode of operation
0x1C12	SyncManger 2 PDO assign (Rx PDOs)	`sRxPDOassign`	this object is written in change state from PREOP to SAFEOP; the configuration depends on the number of axes (not include in `CiA402Objects`)
0x1C13	SyncManger 3 PDO assign (Tx PDOs)	`sTxPDOassign`	equal to 0x1C12 (not include in `CiA402Objects`)
0x603F	Error Code	`objErrorCode`	this value shall be set if an error in the PDS occurs



Index	Object name	Variable in source code	Comment/Description
0x6040	Controlword	`objControlWord`	object for the output commands from the master
0x6041	Status word	`objStatusWord`	current axis status
0x605A	Quick stop option code	`objQuickStopOptionCode`	predefined ramp if an quick stop shall be performed
0x605B	Shutdown option code	`objShutdownOptionCode`	predefined action in state transition 8
0x605C	Disable operation option code	`objDisableOperationOptionCode`	predefined action in state transition 5
0x605E	Fault reaction option code	`objFaultReactionCode`	predefined action in state “Fault reaction active”
0x6060	Modes of operation	`objModesOfOperation`	requested operation mode
0x6061	Modes of operation display	`objModesOfOperationDisplay`	current operation mode
0x6064	Position actual value	`objPositionActualValue`	current position value (delivered by encoder)
0x606C	Velocity actual value	`objVelocityActualValue`	velocity feedback
0x6077	Torque actual value	`objTorqueActualValue`	currently not used (only for completion)
0x607A	Target position	`objTargetPosition`	requested Postion value (set in csp mode)
0x607D	Software position limit	`objSoftwarePositionLimit`	includes the minimum and maximum actual position limit
0x6085	Quick stop declaration	`objQuickStopDeclaration`	predefined action in state “Quick stop active”
0x60C2	Interpolation time period	`objInterpolationTimePeriod`	
0x60FF	Target velocity	`objTargetVelocity`	target velocity requested by the master
0x6502	Supported drive modes	`objSupportedDriveModes`	list of all supported operation modes

The objects from 0x6000 to 0x67FF are incremented with 0x800 for each axis (Index + `#Axis`*0x800).

State machine + PDO mapping



If device is in OP state the state „Not ready to switch on" and „Switch on disabled" are skipped

Option code 0x605A

Option code 0x605B

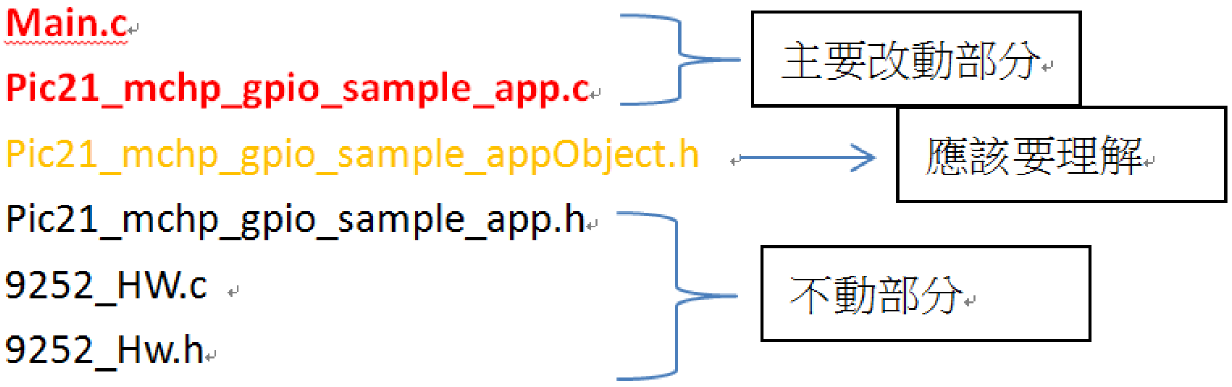
Option code 0x605C

Option code 0x605E

Figure 23: CiA402 state transitions and option codes

源碼之分析

- 主要是要架構下列之關係
  - Main 之形成 在不同應用上的差異
  - Object.h的解構與分析
  - APPL_inputmapping, outputmapping generatemapping 分析



Main.c
Pic21_mchp_gpio_sample_app.c
Pic21_mchp_gpio_sample_appObject.h
Pic21_mchp_gpio_sample_app.h
9252_HW.c
9252_Hw.h

主要改動部分
應該要理解
不動部分

Regional Training Centers

Tasks

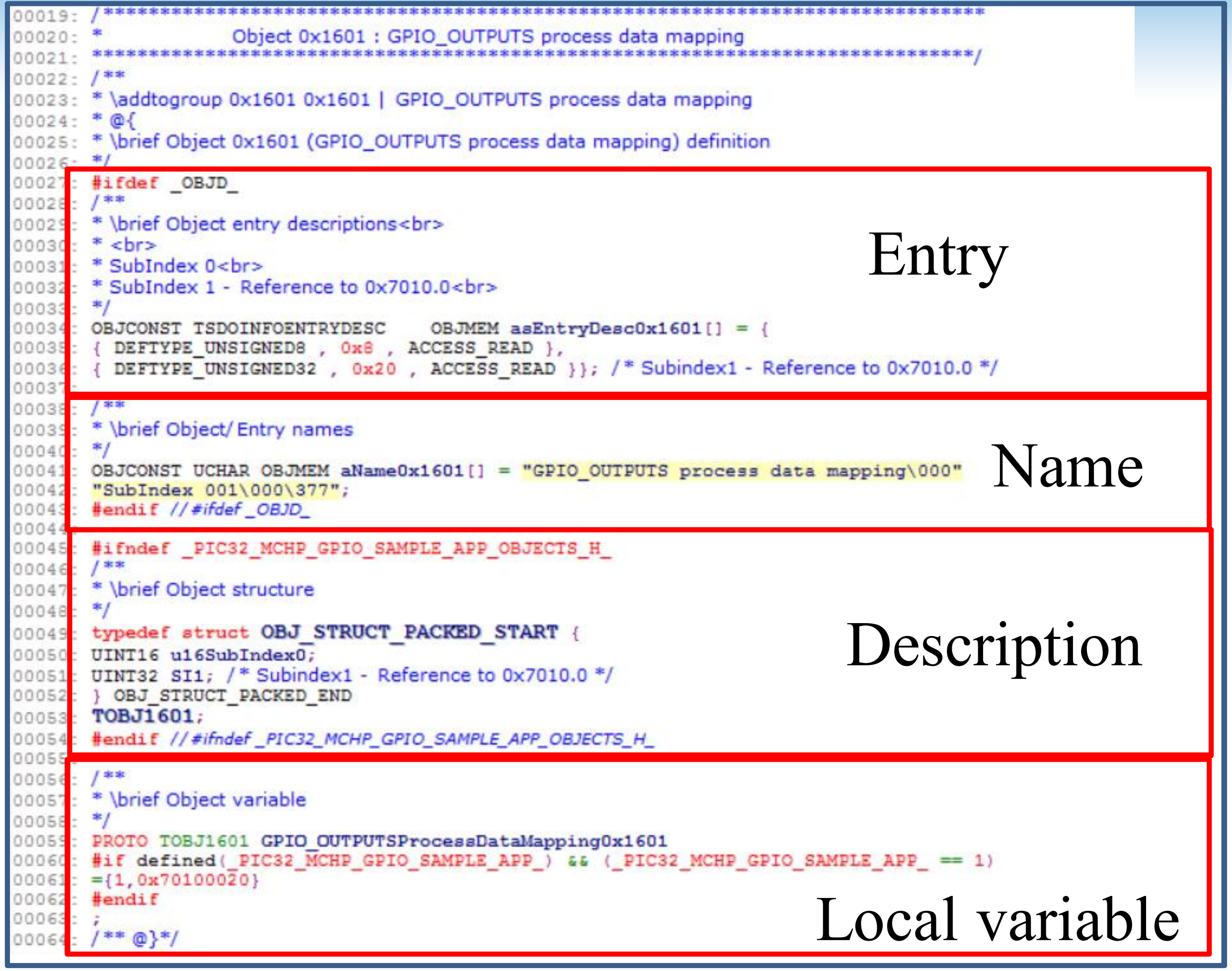
1. **The relationship between object, main and APPL_**
2. **Object, its structure, naming rule**
3. **DPRAM & Object’s link-list relation**
4. **Struct array index and members**
5. **Not including following topic : Mail box and synchronization 及 XOE 應用**

幾個C 的Trick

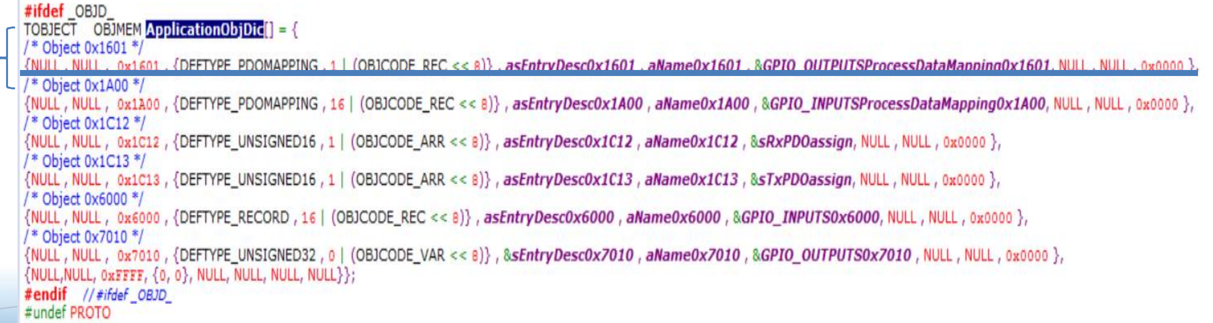
- **Pointer and variable address**
  - *P : 取得”指標變數P“ 這個位置的資料(內容)
  - &K:取得K變數的位置
  - 取得變數位置後想要存於 address_of_x　int *address_of_x= & X;
  - 取位置之內容 int value_stored= *address_of_x
  - 改變位置內容 *address_of_x=99;

OD 物件字典

- **Refer to Chapter 7 of SSC AN**
- 所有的物件字典分類成三種不同的類型，
    - VARIABLE的資料物件僅僅包括一個基本資料類型作為物件。
    - ARRAY的資料物件把不同的基本資料類型的集合作為物件。
    - RECORD的資料物件暴扣多種不同的基本資料類型作為物件。
    - 物件字典的物件的資料結構是採用鏈表的形式組成整個物件字典。其中，在物件裡面定義了索引，物件的描述，SDO入口指標的描述，物件字典的名稱，變數的指標，還定義了讀和寫兩個虛函數本地內存
- **所有資料物件的描述被收集在一個框架上即是物件字典,這個物件字典展現了給EtherCAT主站的介面**
    - Define local memory
    - Entry description 入口的描述（是入口地址的描述）
    - Object name 数据对象名称（是数据对象名称的描述）
    - Objection description 数据对象的描述（是数据对象的描述）



```
/***********************************************************************************
*                 Object 0x1601 : GPIO_OUTPUTS process data mapping
**********************************************************************************/
/**
* \addtogroup 0x1601 0x1601 | GPIO_OUTPUTS process data mapping
* @{
* \brief Object 0x1601 (GPIO_OUTPUTS process data mapping) definition
*/
#ifdef _OBJD_
/**
* \brief Object entry descriptions<br>
* <br>
* SubIndex 0<br>
* SubIndex 1 - Reference to 0x7010.0<br>
*/
OBJCONST TSDOINFOENTRYDESC    OBJMEM asEntryDesc0x1601[] = {
{ DEFTYPE_UNSIGNED8 , 0x8 , ACCESS_READ },
{ DEFTYPE_UNSIGNED32 , 0x20 , ACCESS_READ }}; /* Subindex1 - Reference to 0x7010.0 */

/**
* \brief Object/ Entry names
*/
OBJCONST UCHAR OBJMEM aName0x1601[] = "GPIO_OUTPUTS process data mapping\000"
"SubIndex 001\000\377";
#endif //#ifdef _OBJD_

#ifndef _PIC32_MCHP_GPIO_SAMPLE_APP_OBJECTS_H_
/**
* \brief Object structure
*/
typedef struct OBJ_STRUCT_PACKED_START {
UINT16 u16SubIndex0;
UINT32 SI1; /* Subindex1 - Reference to 0x7010.0 */
} OBJ_STRUCT_PACKED_END
TOBJ1601;
#endif //#ifndef _PIC32_MCHP_GPIO_SAMPLE_APP_OBJECTS_H_

/**
* \brief Object variable
*/
PROTO TOBJ1601 GPIO_OUTPUTSProcessDataMapping0x1601
#if defined(_PIC32_MCHP_GPIO_SAMPLE_APP_) && (_PIC32_MCHP_GPIO_SAMPLE_APP_ == 1)
={1,0x70100020}
#endif
;
/** @}*/
```



```
#ifdef _OBJD_
TOBJECT   OBJMEM ApplicationObjDic[] = {
/* Object 0x1601 */
{NULL , NULL , 0x1601 , {DEFTYPE_PDOMAPPING , 1 | (OBJCODE_REC << 8)} , asEntryDesc0x1601 , aName0x1601 , &GPIO_OUTPUTSProcessDataMapping0x1601, NULL , NULL , 0x0000 },
/* Object 0x1A00 */
{NULL , NULL , 0x1A00 , {DEFTYPE_PDOMAPPING , 16 | (OBJCODE_REC << 8)} , asEntryDesc0x1A00 , aName0x1A00 , &GPIO_INPUTSProcessDataMapping0x1A00, NULL , NULL , 0x0000 },
/* Object 0x1C12 */
{NULL , NULL , 0x1C12 , {DEFTYPE_UNSIGNED16 , 1 | (OBJCODE_ARR << 8)} , asEntryDesc0x1C12 , aName0x1C12 , &sRxPDOassign, NULL , NULL , 0x0000 },
/* Object 0x1C13 */
{NULL , NULL , 0x1C13 , {DEFTYPE_UNSIGNED16 , 1 | (OBJCODE_ARR << 8)} , asEntryDesc0x1C13 , aName0x1C13 , &sTxPDOassign, NULL , NULL , 0x0000 },
/* Object 0x6000 */
{NULL , NULL , 0x6000 , {DEFTYPE_RECORD , 16 | (OBJCODE_REC << 8)} , asEntryDesc0x6000 , aName0x6000 , &GPIO_INPUTS0x6000, NULL , NULL , 0x0000 },
/* Object 0x7010 */
{NULL , NULL , 0x7010 , {DEFTYPE_UNSIGNED32 , 0 | (OBJCODE_VAR << 8)} , &sEntryDesc0x7010 , aName0x7010 , &GPIO_OUTPUTS0x7010 , NULL , NULL , 0x0000 },
{NULL,NULL, 0xFFFF, {0, 0}, NULL, NULL, NULL, NULL}};
#endif   //#ifdef _OBJD_
#undef PROTO
```

TSDOINFOENTRYDESC

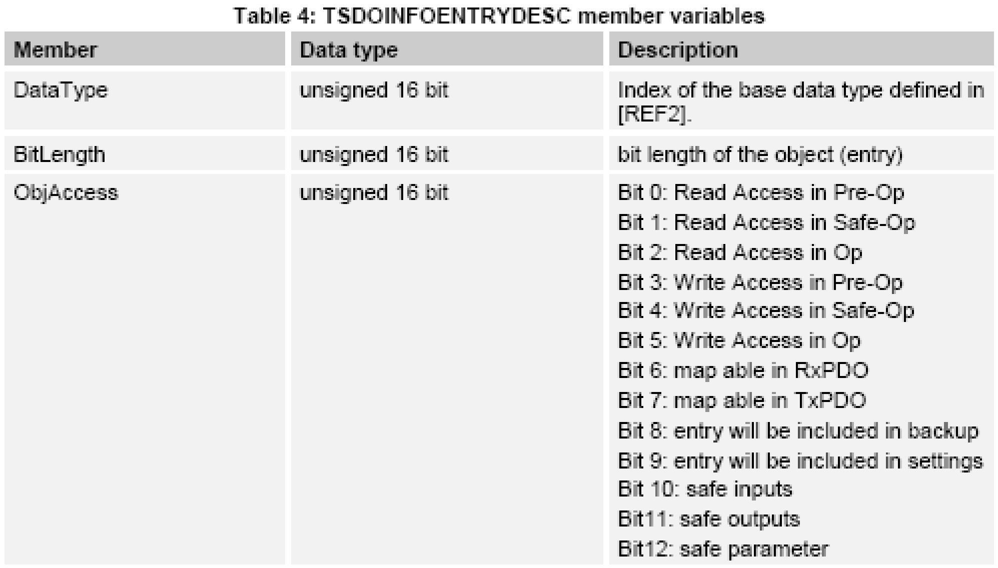


Table 4: TSDOINFOENTRYDESC member variables

Member	Data type	Description
DataType	unsigned 16 bit	Index of the base data type defined in [REF2].
BitLength	unsigned 16 bit	bit length of the object (entry)
ObjAccess	unsigned 16 bit	Bit 0: Read Access in Pre-Op Bit 1: Read Access in Safe-Op Bit 2: Read Access in Op Bit 3: Write Access in Pre-Op Bit 4: Write Access in Safe-Op Bit 5: Write Access in Op Bit 6: map able in RxPDO Bit 7: map able in TxPDO Bit 8: entry will be included in backup Bit 9: entry will be included in settings Bit 10: safe inputs Bit11: safe outputs Bit12: safe parameter

TOBJECT

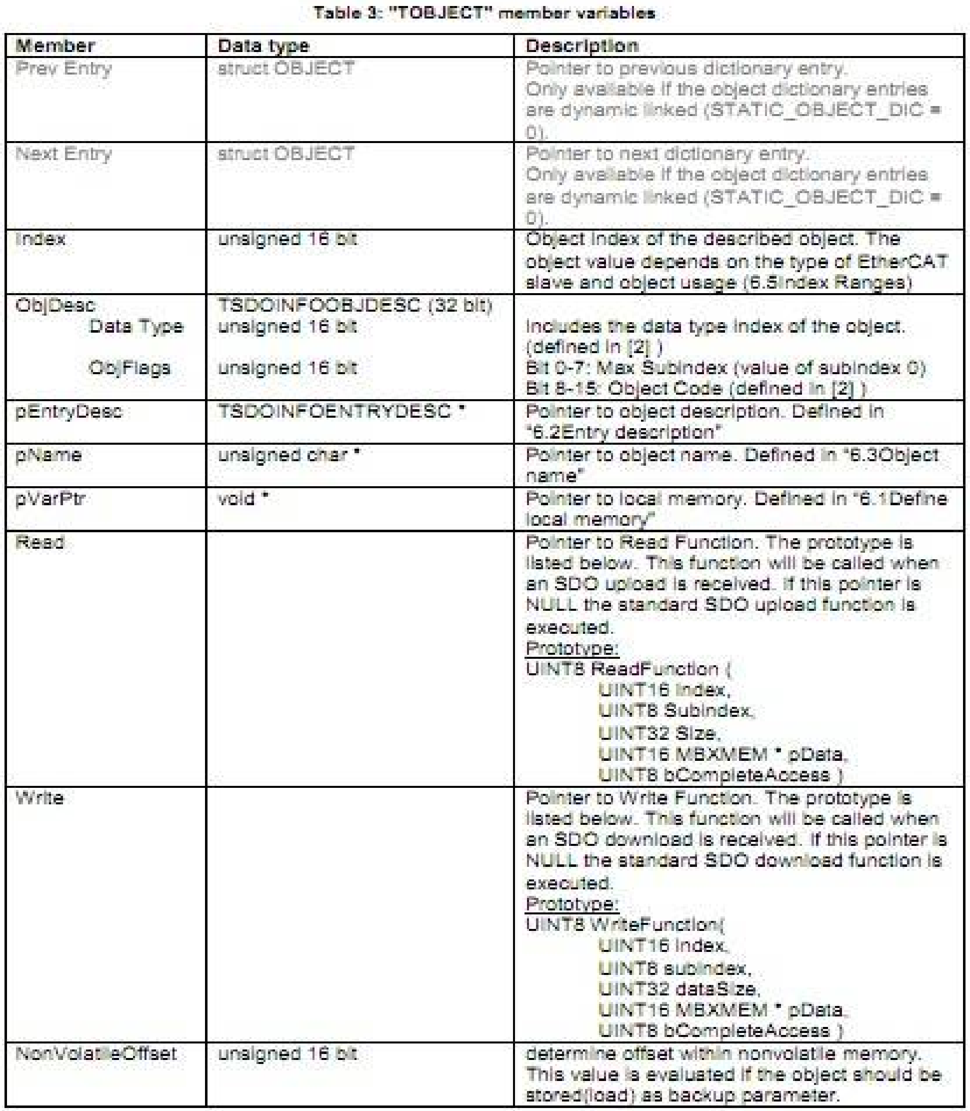
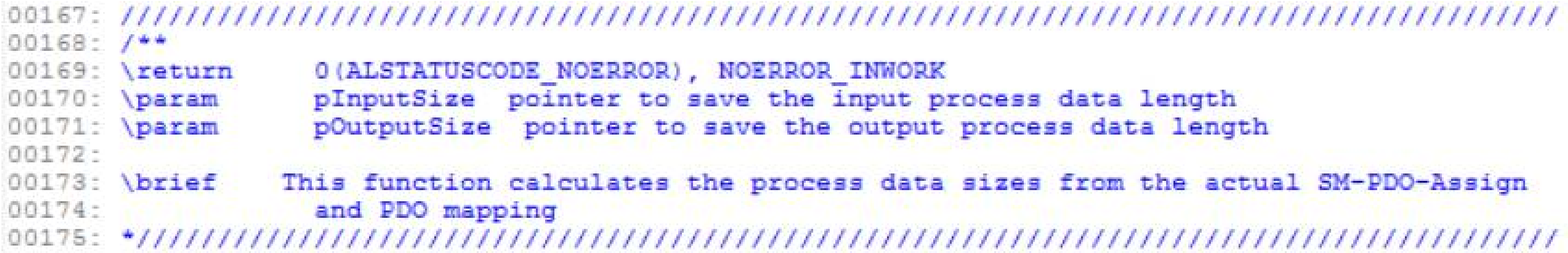


Table 3: "TOBJECT" member variables

Member	Data type	Description
Prev Entry	struct OBJECT	Pointer to previous dictionary entry. Only available if the object dictionary entries are dynamic linked (STATIC_OBJECT_DIC = 0).
Next Entry	struct OBJECT	Pointer to next dictionary entry. Only available if the object dictionary entries are dynamic linked (STATIC_OBJECT_DIC = 0).
Index	unsigned 16 bit	Object index of the described object. The object value depends on the type of EtherCAT slave and object usage (6.5Index Ranges)
ObjDesc	TSDOINFOOBJDESC (32 bit)	
Data Type	unsigned 16 bit	Includes the data type index of the object. (defined in [2])
ObjFlags	unsigned 16 bit	Bit 0-7: Max Subindex (value of subindex 0) Bit 8-15: Object Code (defined in [2])
pEntryDesc	TSDOINFOENTRYDESC *	Pointer to object description. Defined in "6.2Entry description"
pName	unsigned char *	Pointer to object name. Defined in "6.3Object name"
pVarPtr	void *	Pointer to local memory. Defined in "6.1Define local memory"
Read		Pointer to Read Function. The prototype is listed below. This function will be called when an SDO upload is received. If this pointer is NULL the standard SDO upload function is executed. Prototype: UINT8 ReadFunction (UINT16 Index, UINT8 Subindex, UINT32 Size, UINT16 MBXMEM * pData, UINT8 bCompleteAccess)
Write		Pointer to Write Function. The prototype is listed below. This function will be called when an SDO download is received. If this pointer is NULL the standard SDO download function is executed. Prototype: UINT8 WriteFunction(UINT16 Index, UINT8 subindex, UINT32 dataSize, UINT16 MBXMEM * pData, UINT8 bCompleteAccess)
NonVolatileOffset	unsigned 16 bit	determine offset within nonvolatile memory. This value is evaluated if the object should be stored(load) as backup parameter.

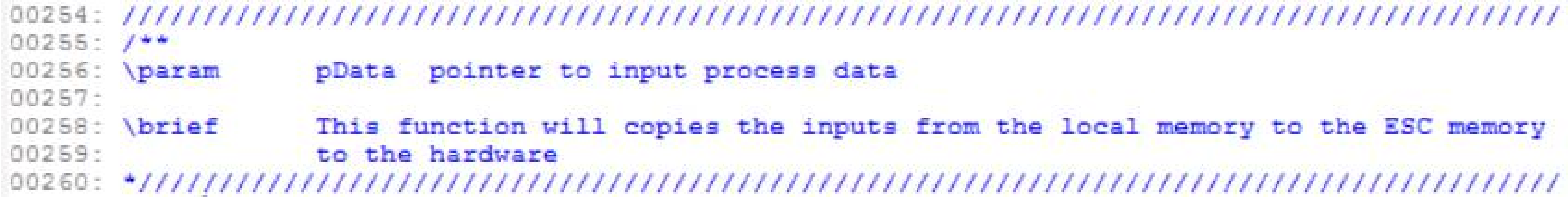
APPL_ function

- APPL_Generatemapping



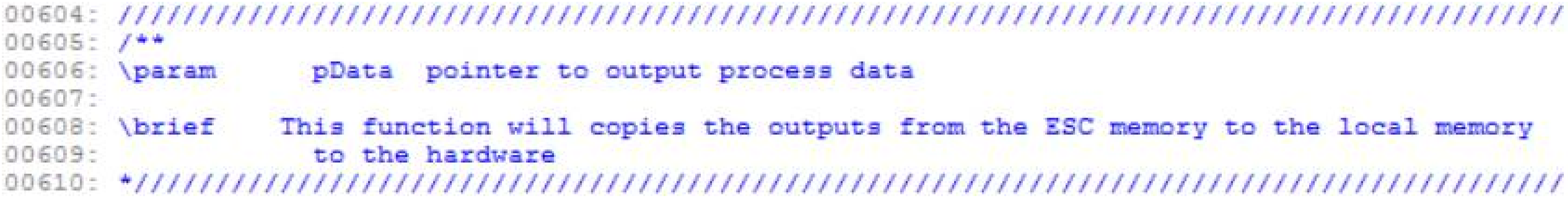
```
////////////////////////////////////////////////////////////////////////////////////////
/**
\return     0(ALSTATUSCODE_NOERROR), NOERROR_INWORK
\param      pInputSize  pointer to save the input process data length
\param      pOutputSize  pointer to save the output process data length

\brief    This function calculates the process data sizes from the actual SM-PDO-Assign
            and PDO mapping
*////////////////////////////////////////////////////////////////////////////////////////
```

- APPL_Inputmapping

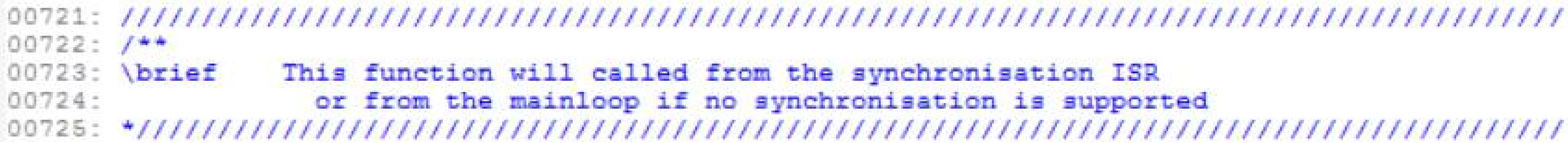


```
////////////////////////////////////////////////////////////////////////////////////////
/**
\param      pData  pointer to input process data

\brief      This function will copies the inputs from the local memory to the ESC memory
            to the hardware
*////////////////////////////////////////////////////////////////////////////////////////
```

Appl_ function

- APPL_outputmapping
- 

```
////////////////////////////////////////////////////////////////////////////////////////
/**
\param      pData  pointer to output process data

\brief     This function will copies the outputs from the ESC memory to the local memory
             to the hardware
*///////////////////////////////////////////////////////////////////////////////////////
```

- APPL_Application
- 

```
////////////////////////////////////////////////////////////////////////////////////////
/**
\brief     This function will called from the synchronisation ISR
             or from the mainloop if no synchronisation is supported
*///////////////////////////////////////////////////////////////////////////////////////
```

Main

- Check the difference and relations between Appl_ object to "user space" entry at Main

Code comparing

比對報告UART_APPL_C.

比對報告UART_object.

比對報告UART_MAIN.

MICROCHIP

Regional Training Centers

LAN9252介紹
TWINCAT 端的設定/MASTER端網卡尋找
PDO mapping excel and SSC flow
EEPROM programming
MPLABX 流程
PLC Structure text code basic
UART/MIO/ADC application
APPL_ application code briefing

Hand on

Q&A , dismiss

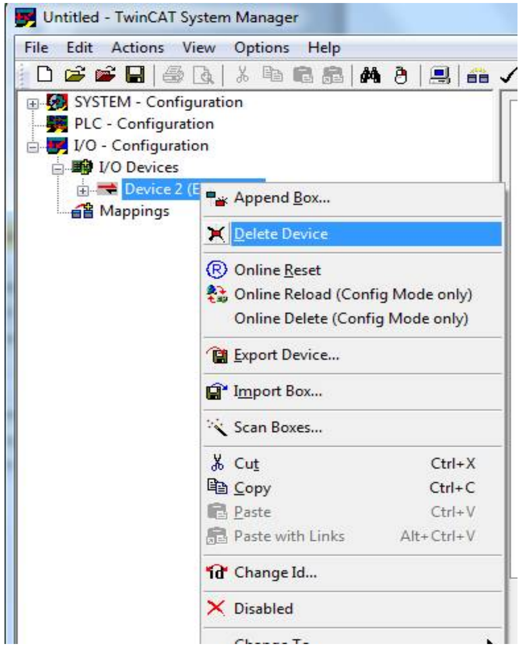
MICROCHIP

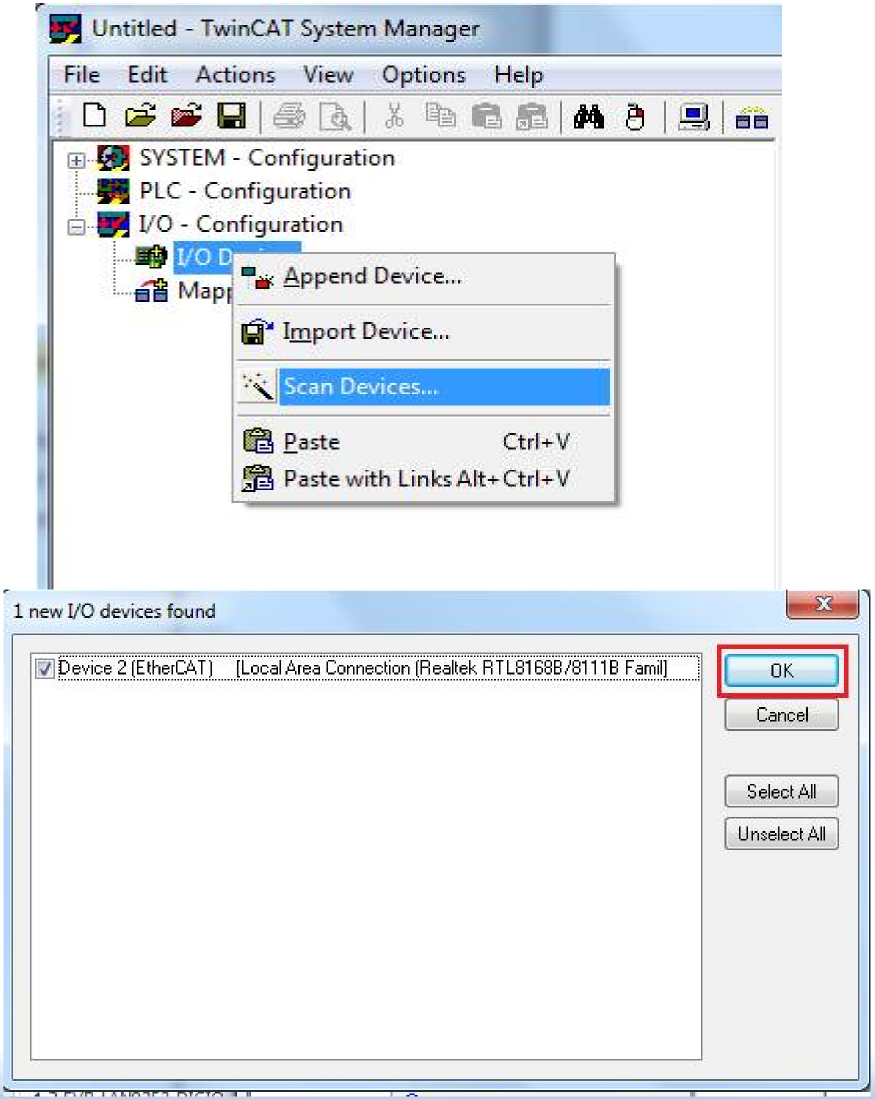
Regional Training Centers

Hand on

TWINCAT 幾個重要的操作

Just check in

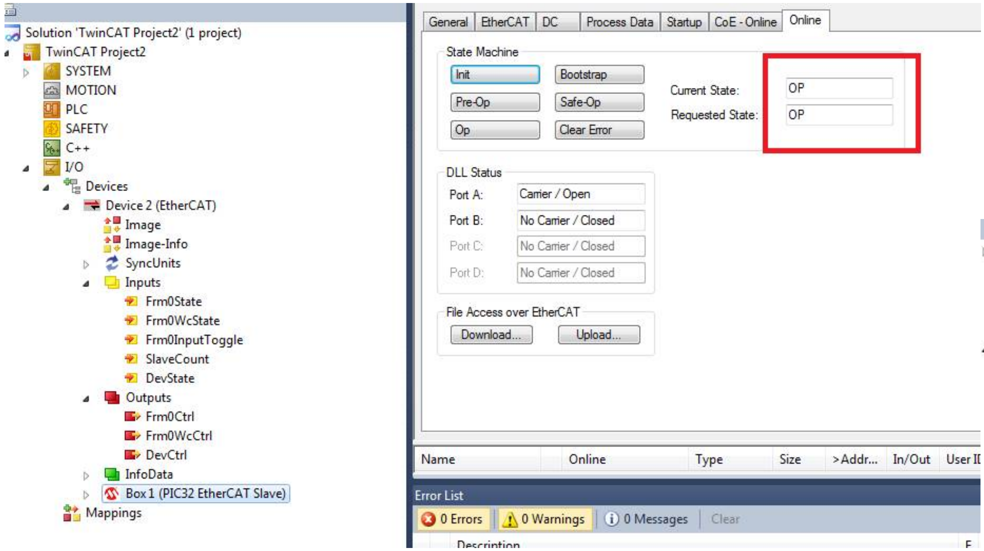




1 new I/O devices found

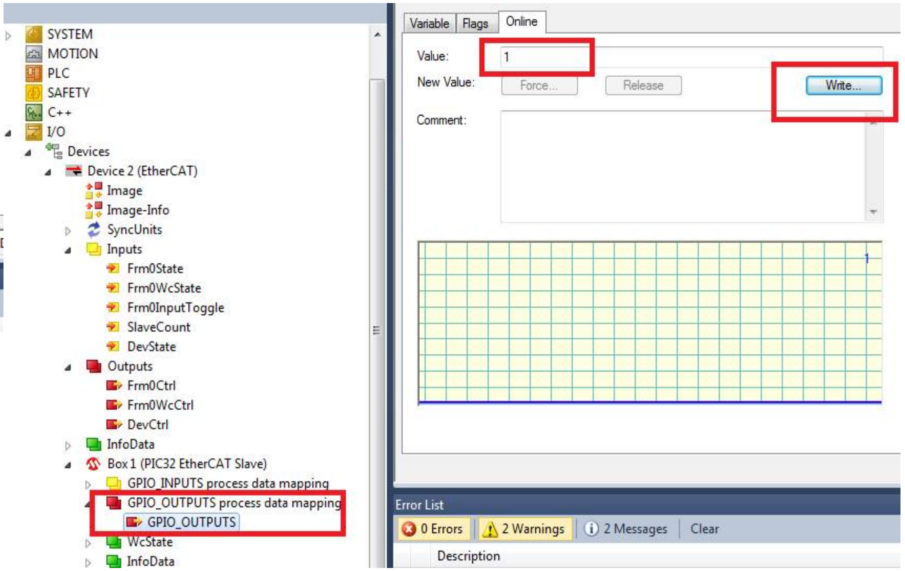
☑ Device 2 (EtherCAT) [Local Area Connection (Realtek RTL8168B/8111B Famil]

After device in

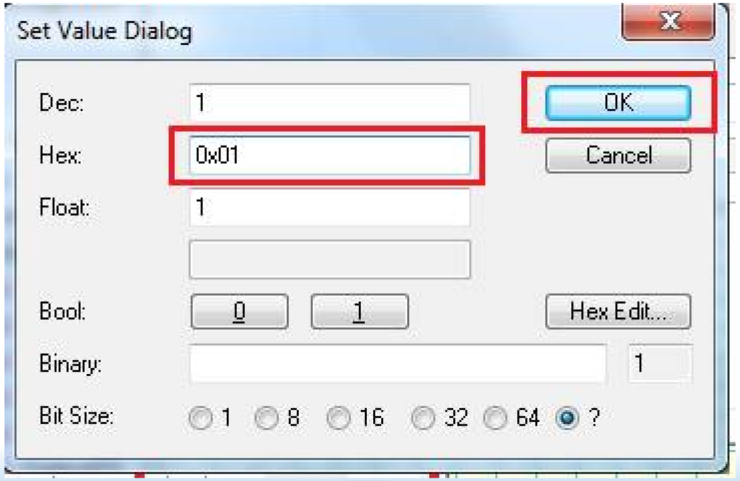


Current State: OP
Requested State: OP

Port A: Carrier / Open
Port B: No Carrier / Closed
Port C: No Carrier / Closed
Port D: No Carrier / Closed



Value: 1
New Value:



Dec: 1
Hex: 0x01
Float: 1
Binary: 1
Bit Size: ○ 1 ○ 8 ○ 16 ○ 32 ○ 64 ● ?

MICROCHIP

Regional Training Centers

Hand on

動手做

- 使用**32_IN_OUT SDK**
- 編譯**SSC**
- 設定**TWINCAT**
- 編譯**MPLABX**
- 燒錄**EEPROM (TWINCAT AND PICKIT 3)**
- 利用**TWINCAT**測試**,**介紹**TWINCAT** 的操作

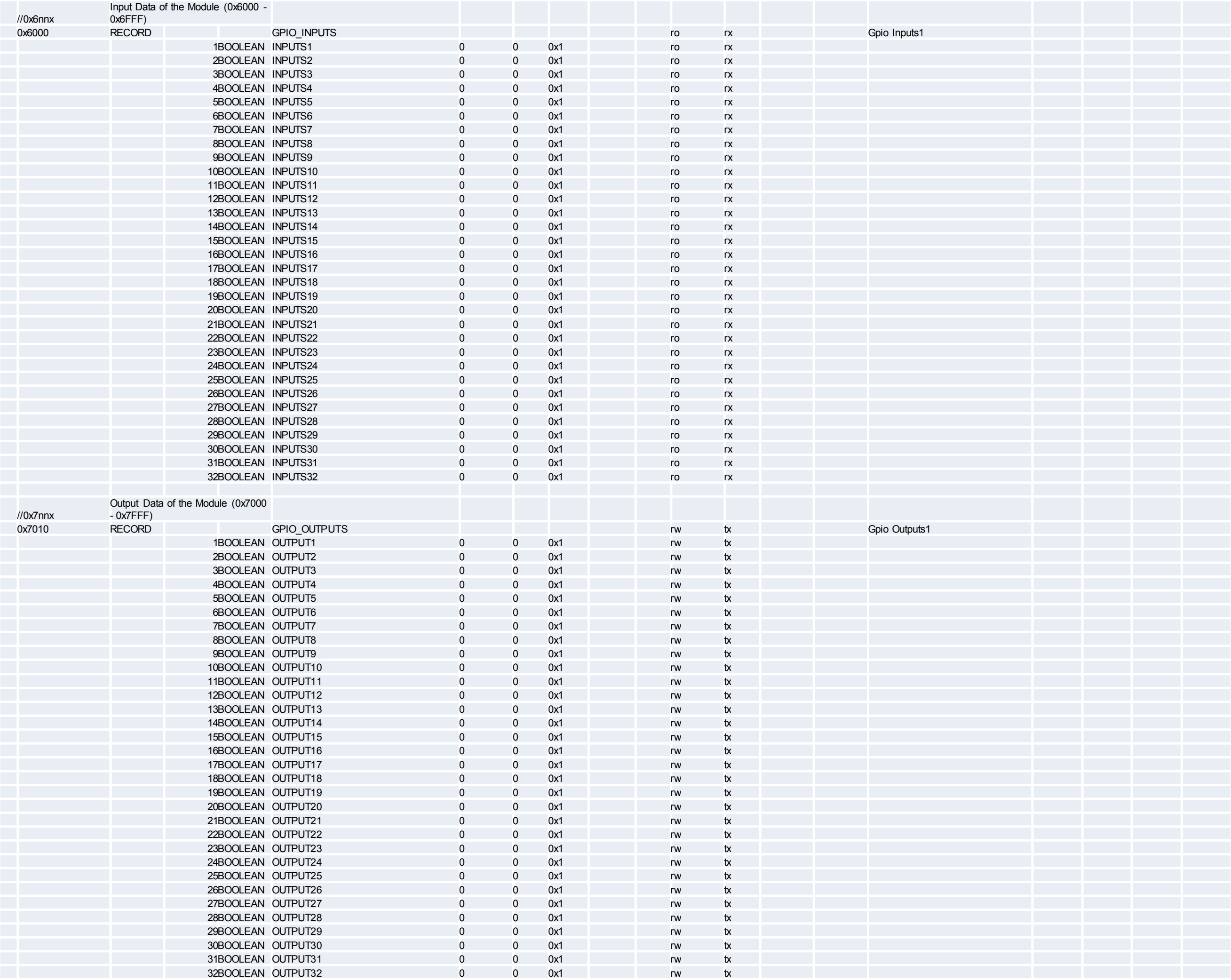
SDK-32-in-32 out

- **LAN9252 只有16個IO接口**
- **客戶要32-In,32-Out 怎麼辦**
- **透過SPI跟PIC連接 長出其他IO**
-

Define IO in PIC

New Variable Name	PIC32 Pin Name	PIC32 Pin direction	PIC32 Pin Name	PIC32 Pin no	PIM (pin no) Connected to PIC32	Test Status with respect to current EVB-LAN9252-HBI	Comments
INPUT1	TMS/RA0	I/P	RA0	17	17	OK	
INPUT2	AN5/C1IN+/VBUSON/CN7/RB5	I/P	RB5	20	20	OK	Determined by SW46
INPUT3	AN4/C1IN-/CN6/RB4	I/P	RB4	21	21	OK	Determined by SW46
INPUT4	AN3/C2IN+/CN5/RB3	I/P	RB3	22	22	OK	Determined by SW46
INPUT5	AN2/C2IN-/CN4/RB2	I/P	RB2	23	23	OK	Determined by SW46
INPUT6	PGEC1/AN1/CN3/RB1	I/P	RB1	24	24	OK	Determined by SW46
INPUT7	PGED1/AN0/CN2/RB0	I/P	RB0	25	25	OK	Determined by SW46
INPUT8	VREF-/CVREF-/AERXD2/PMA7/RA9	I/P	RA9	28	NC	Not Teseted	NC
INPUT9	VREF+/CVREF+/AERXD3/PMA6/RA10	I/P	RA10	29	NC	Not Teseted	NC
INPUT21	ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7	I/P	RG7	11	11	OK	PIM
INPUT22	ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/'U3TX/PMA3/CN10/RG8	I/P	RG8	12	12	OK	PIM
INPUT10	AN8/C1OUT/RB8	I/P	RB8	32	32	OK	
INPUT11	AN9/C2OUT/RB9	I/P	RB9	33	33	OK	
INPUT12	AN10/CVREFOUT/PMA13/RB10	I/P	RB10	34	34	OK	Determined by SW47
INPUT13	AN11/ERXERR/AETXERR/PMA12/RB11	I/P	RB11	35	35	OK	Determined by SW47
INPUT14	TCK/RA1	I/P	RA1	38	38	OK	
INPUT15	AN12/ERXD0/AECRS/PMA11/RB12	I/P	RB12	41	41	OK	Determined by SW47
INPUT16	AN13/ERXD1/AECOL/PMA10/RB13	I/P	RB13	42	42	OK	Determined by SW47
INPUT17	AN14/ERXD2/AETXD3/PMALH/PMA1/RB14	I/P	RB14	43	43	OK	ALEHI
INPUT18	AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15	I/P	RB15	44	44	OK	ALELO
INPUT19	AETXD0/SS3/U4RX/U1CTS/CN20/RD14	I/P	RD14	47	NC	Not Teseted	NC
INPUT20	AETXD1/SCK3/U4TX/U1RTS/CN21/RD15	I/P	RD15	48	NC	Not Teseted	NC
INPUT23	SCL2/RA2	I/P	RA2	58	58	OK	I2C1_SDA
INPUT24	SDA2/RA3	I/P	RA3	59	59	OK	I2C1_SCL
INPUT25	TDI/RA4	I/P	RA4	60	NC	Not Teseted	NC
INPUT26	TDO/RA5	I/P	RA5	61	NC	Not Teseted	NC
INPUT27	AETXCLK/SCL1/INT3/RA14	I/P	RA14	66	NC	Not Teseted	NC
INPUT28	AETXEN/SDA1/INT4/RA15	I/P	RA15	67	NC	Not Teseted	NC
INPUT29	RTCC/EMDIO/AEMDIO/IC1/RD8	I/P	RD8	68	NC	Not Teseted	NC
INPUT30	SS1/IC2/RD9	I/P	RD9	69	NC	Not Teseted	NC
INPUT31	SCK1/IC3/PMCS2/PMA15/RD10	I/P	RD10	70	70	OK	
INPUT32	EMDC/AEMDC/IC4/PMCS1/PMA14/RD11	I/P	RD11	71	71	OK	
OUTPUT1	AERXERR/RG15	O/P	RG15	1	NC	Not Teseted	NC
OUTPUT2	PMD5/RE5	O/P	RE5	3	3	OK	
OUTPUT3	PMD6/RE6	O/P	RE6	4	4	OK	
OUTPUT4	PMD7/RE7	O/P	RE7	5	5	OK	
OUTPUT5	T2CK/RC1	O/P	RC1	6	6	OK	SW47 - OFF Position
OUTPUT6	T3CK/AC2TX/RC2	O/P	RC2	7	7	OK	SW47 - OFF Position
OUTPUT7	T4CK/AC2RX/RC3	O/P	RC3	8	8	OK	SW47 - OFF Position
OUTPUT8	T5CK/SDI1/RC4	O/P	RC4	9	9	OK	SW47 - OFF Position
OUTPUT9	ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6	O/P	RG6	10	NC	Not Teseted	NC
OUTPUT10	OC2/RD1	O/P	RD1	76	76	OK	
OUTPUT11	OC3/RD2	O/P	RD2	77	77	OK	
OUTPUT12	OC4/RD3	O/P	RD3	78	78	OK	
OUTPUT13	ETXD2/IC5/PMD12/RD12	O/P	RD12	79	79	OK	
OUTPUT14	ETXD3/PMD13/CN19/RD13	O/P	RD13	80	80	OK	
OUTPUT15	OC5/PMWR/CN13/RD4	O/P	RD4	81	81	OK	
OUTPUT16	PMRD/CN14/RD5	O/P	RD5	82	82	OK	
OUTPUT17	ETXEN/PMD14/CN15/RD6	O/P	RD6	83	83	OK	
OUTPUT18	ETXCLK/PMD15/CN16/RD7	O/P	RD7	84	84	OK	
OUTPUT19	C1RX/ETXD1/PMD11/RF0	O/P	RF0	87	87	OK	
OUTPUT20	C1TX/ETXD0/PMD10/RF1	O/P	RF1	88	88	OK	
OUTPUT21	C2TX/ETXERR/PMD9/RG1	O/P	RG1	89	89	OK	
OUTPUT22	C2RX/PMD8/RG0	O/P	RG0	90	90	OK	
OUTPUT23	TRCLK/RA6	O/P	RA6	91	NC	Not Teseted	NC
OUTPUT24	TRD3/RA7	O/P	RA7	92	NC	Not Teseted	NC
OUTPUT25	PMD0/RE0	O/P	RE0	93	93	OK	
OUTPUT26	PMD1/RE1	O/P	RE1	94	94	OK	
OUTPUT27	TRD2/RG14	O/P	RG14	95	95	OK	
OUTPUT28	TRD1/RG12	O/P	RG12	96	96	OK	
OUTPUT29	TRD0/RG13	O/P	RG13	97	97	OK	
OUTPUT30	PMD2/RE2	O/P	RE2	98	98	OK	
OUTPUT31	PMD3/RE3	O/P	RE3	99	99	OK	
OUTPUT32	PMD4/RE4	O/P	RE4	100	100	OK	

And PDO mapping



//0x6nnx	Input Data of the Module (0x6000 - 0x6FFF)									
0x6000	RECORD			GPIO_INPUTS				ro	rx	Gpio Inputs1
		1	BOOLEAN	INPUTS1	0	0	0x1	ro	rx	
		2	BOOLEAN	INPUTS2	0	0	0x1	ro	rx	
		3	BOOLEAN	INPUTS3	0	0	0x1	ro	rx	
		4	BOOLEAN	INPUTS4	0	0	0x1	ro	rx	
		5	BOOLEAN	INPUTS5	0	0	0x1	ro	rx	
		6	BOOLEAN	INPUTS6	0	0	0x1	ro	rx	
		7	BOOLEAN	INPUTS7	0	0	0x1	ro	rx	
		8	BOOLEAN	INPUTS8	0	0	0x1	ro	rx	
		9	BOOLEAN	INPUTS9	0	0	0x1	ro	rx	
		10	BOOLEAN	INPUTS10	0	0	0x1	ro	rx	
		11	BOOLEAN	INPUTS11	0	0	0x1	ro	rx	
		12	BOOLEAN	INPUTS12	0	0	0x1	ro	rx	
		13	BOOLEAN	INPUTS13	0	0	0x1	ro	rx	
		14	BOOLEAN	INPUTS14	0	0	0x1	ro	rx	
		15	BOOLEAN	INPUTS15	0	0	0x1	ro	rx	
		16	BOOLEAN	INPUTS16	0	0	0x1	ro	rx	
		17	BOOLEAN	INPUTS17	0	0	0x1	ro	rx	
		18	BOOLEAN	INPUTS18	0	0	0x1	ro	rx	
		19	BOOLEAN	INPUTS19	0	0	0x1	ro	rx	
		20	BOOLEAN	INPUTS20	0	0	0x1	ro	rx	
		21	BOOLEAN	INPUTS21	0	0	0x1	ro	rx	
		22	BOOLEAN	INPUTS22	0	0	0x1	ro	rx	
		23	BOOLEAN	INPUTS23	0	0	0x1	ro	rx	
		24	BOOLEAN	INPUTS24	0	0	0x1	ro	rx	
		25	BOOLEAN	INPUTS25	0	0	0x1	ro	rx	
		26	BOOLEAN	INPUTS26	0	0	0x1	ro	rx	
		27	BOOLEAN	INPUTS27	0	0	0x1	ro	rx	
		28	BOOLEAN	INPUTS28	0	0	0x1	ro	rx	
		29	BOOLEAN	INPUTS29	0	0	0x1	ro	rx	
		30	BOOLEAN	INPUTS30	0	0	0x1	ro	rx	
		31	BOOLEAN	INPUTS31	0	0	0x1	ro	rx	
		32	BOOLEAN	INPUTS32	0	0	0x1	ro	rx	
//0x7nnx	Output Data of the Module (0x7000 - 0x7FFF)									
0x7010	RECORD			GPIO_OUTPUTS				rw	tx	Gpio Outputs1
		1	BOOLEAN	OUTPUT1	0	0	0x1	rw	tx	
		2	BOOLEAN	OUTPUT2	0	0	0x1	rw	tx	
		3	BOOLEAN	OUTPUT3	0	0	0x1	rw	tx	
		4	BOOLEAN	OUTPUT4	0	0	0x1	rw	tx	
		5	BOOLEAN	OUTPUT5	0	0	0x1	rw	tx	
		6	BOOLEAN	OUTPUT6	0	0	0x1	rw	tx	
		7	BOOLEAN	OUTPUT7	0	0	0x1	rw	tx	
		8	BOOLEAN	OUTPUT8	0	0	0x1	rw	tx	
		9	BOOLEAN	OUTPUT9	0	0	0x1	rw	tx	
		10	BOOLEAN	OUTPUT10	0	0	0x1	rw	tx	
		11	BOOLEAN	OUTPUT11	0	0	0x1	rw	tx	
		12	BOOLEAN	OUTPUT12	0	0	0x1	rw	tx	
		13	BOOLEAN	OUTPUT13	0	0	0x1	rw	tx	
		14	BOOLEAN	OUTPUT14	0	0	0x1	rw	tx	
		15	BOOLEAN	OUTPUT15	0	0	0x1	rw	tx	
		16	BOOLEAN	OUTPUT16	0	0	0x1	rw	tx	
		17	BOOLEAN	OUTPUT17	0	0	0x1	rw	tx	
		18	BOOLEAN	OUTPUT18	0	0	0x1	rw	tx	
		19	BOOLEAN	OUTPUT19	0	0	0x1	rw	tx	
		20	BOOLEAN	OUTPUT20	0	0	0x1	rw	tx	
		21	BOOLEAN	OUTPUT21	0	0	0x1	rw	tx	
		22	BOOLEAN	OUTPUT22	0	0	0x1	rw	tx	
		23	BOOLEAN	OUTPUT23	0	0	0x1	rw	tx	
		24	BOOLEAN	OUTPUT24	0	0	0x1	rw	tx	
		25	BOOLEAN	OUTPUT25	0	0	0x1	rw	tx	
		26	BOOLEAN	OUTPUT26	0	0	0x1	rw	tx	
		27	BOOLEAN	OUTPUT27	0	0	0x1	rw	tx	
		28	BOOLEAN	OUTPUT28	0	0	0x1	rw	tx	
		29	BOOLEAN	OUTPUT29	0	0	0x1	rw	tx	
		30	BOOLEAN	OUTPUT30	0	0	0x1	rw	tx	
		31	BOOLEAN	OUTPUT31	0	0	0x1	rw	tx	
		32	BOOLEAN	OUTPUT32	0	0	0x1	rw	tx	

其他 就自己動手

- **TWINCAT 端的設定/MASTER端網卡尋找**
- **PDO mapping excel and SSC flow**
- **EEPROM programming**
- **MPLABX 流程**
- **APPL_ application code briefing**
- **Testing from TWINCAT**

MICROCHIP

Regional Training Centers

Q&A , Thank you

and

Dismissed