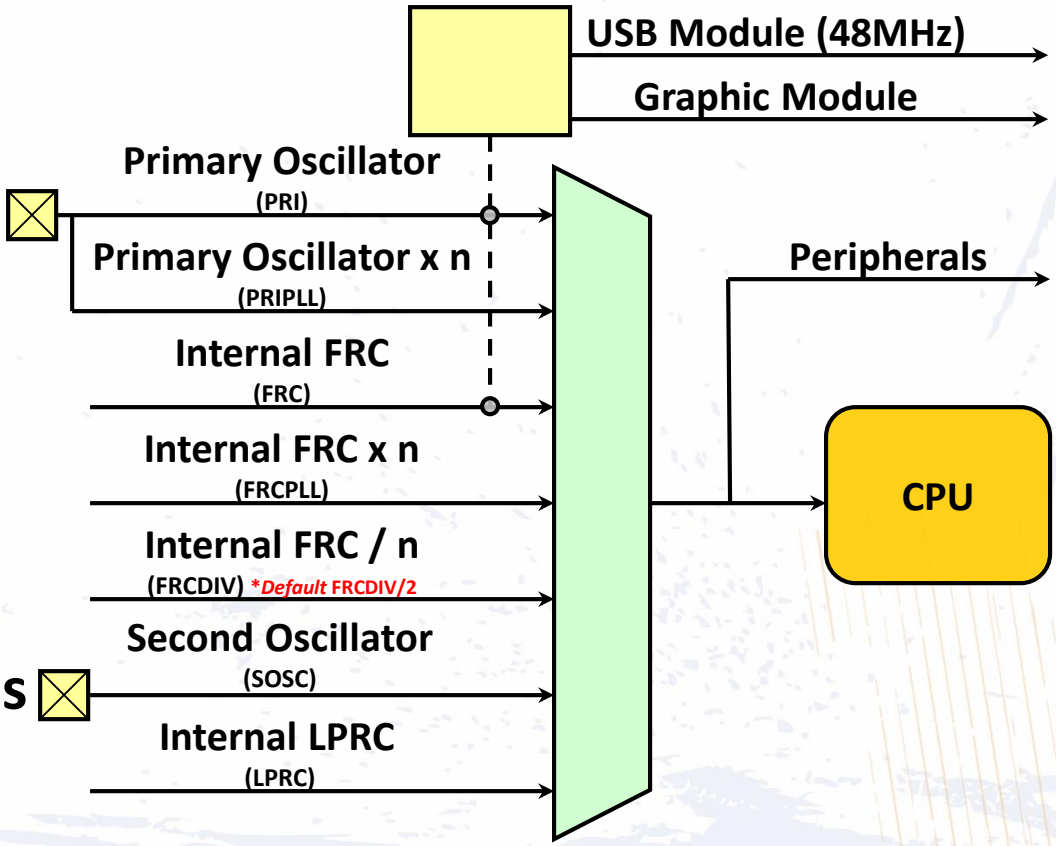
MICROCHIP

Regional Training Centers

Section 7
Oscillator and Configuration Bits

Microchip 16 Bits Clocks

- Review previous slide, Microchip 16-Bits MCU available clock sources are internal Fast RC, Low Power RC, External Crystal and Oscillator, etc..
- The clocks can be divide or multiply by PLL.
- On-chip USB PLL block to provide a stable 48 MHz clock for the USB module.
- Software-controllable switching between various clock sources.



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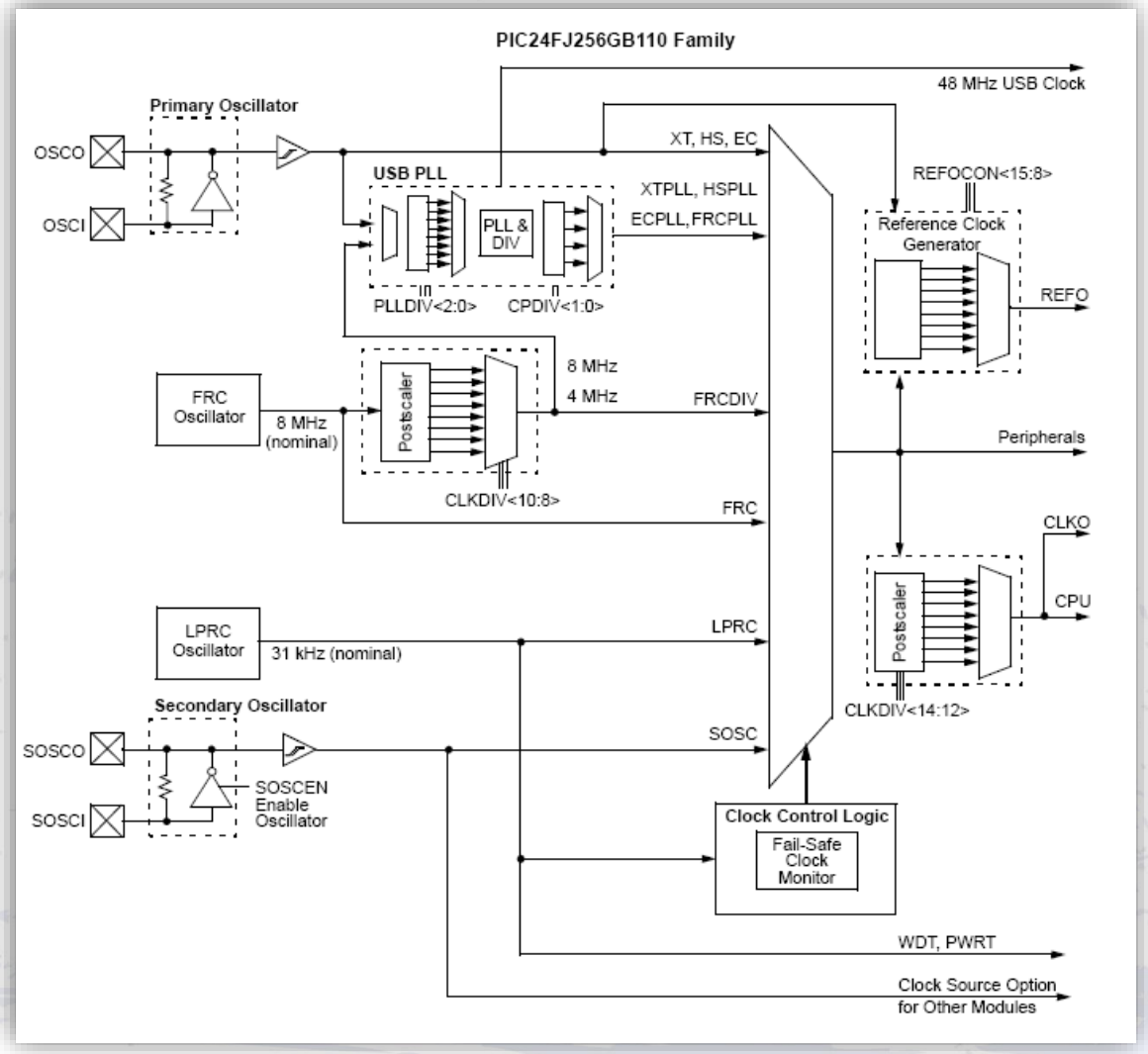
Oscillator Block Diagram



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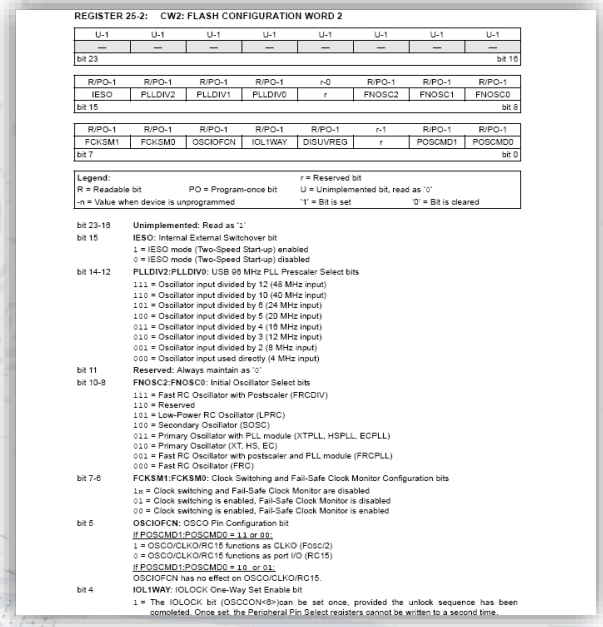
Configuration Bits

- Configuration use to set PIC24 devices several features, include clock sources, WDT, code protection and Debug interface, etc..
- You can see detail at section 26 of datasheet.



REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend:		r = Reserved bit	
R = Readable bit	PO = Program-once bit	U = Unimplemented bit, read as '0'	
-n = Value when device is unprogrammed		'1' = Bit is set	'0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) enabled
0 = IESO mode (Two-Speed Start-up) disabled

bit 14-12 **PLLDIV2:PLLDIV0:** USB 96 MHz PLL Prescaler Select bits
111 = Oscillator input divided by 12 (48 MHz input)
110 = Oscillator input divided by 10 (40 MHz input)
101 = Oscillator input divided by 6 (24 MHz input)
100 = Oscillator input divided by 5 (20 MHz input)
011 = Oscillator input divided by 4 (16 MHz input)
010 = Oscillator input divided by 3 (12 MHz input)
001 = Oscillator input divided by 2 (8 MHz input)
000 = Oscillator input used directly (4 MHz input)

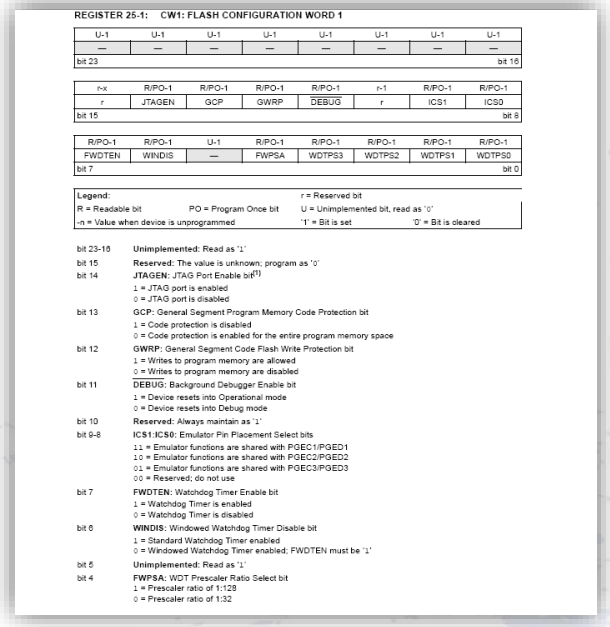
bit 11 **Reserved:** Always maintain as '0'

bit 10-8 **FNOSC2:FNOSC0:** Initial Oscillator Select bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7-6 **FCKSM1:FCKSM0:** Clock Switching and Fail-Safe Clock Monitor Configuration bits
1x = Clock switching and Fail-Safe Clock Monitor are disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **OSCIOFCN:** OSCO Pin Configuration bit
If POSCMD1:POSCMD0 = 11 or 00:
1 = OSCO/CLKO/RC15 functions as CLKO (Fosc/2)
0 = OSCO/CLKO/RC15 functions as port I/O (RC15)
If POSCMD1:POSCMD0 = 10 or 01:
OSCIOFCN has no effect on OSCO/CLKO/RC15.

bit 4 **IOL1WAY:** IOLOCK One-Way Set Enable bit
1 = The IOLOCK bit (OSCCON<6>)can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time.



REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
r	JTAGEN	GCP	GWRP	DEBUG	r	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:		r = Reserved bit	
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as '0'	
-n = Value when device is unprogrammed		'1' = Bit is set	'0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **Reserved:** The value is unknown; program as '0'

bit 14 **JTAGEN:** JTAG Port Enable bit(1)
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space

bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled

bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode

bit 10 **Reserved:** Always maintain as '1'

bit 9-8 **ICS1:ICS0:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use

bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled
0 = Watchdog Timer is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard Watchdog Timer enabled
0 = Windowed Watchdog Timer enabled; FWDTEN must be '1'

bit 5 **Unimplemented:** Read as '1'

bit 4 **FWPSA:** WDT Prescaler Ratio Select bit
1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

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XC16 Support for

Configuration Bits

- XC16 Compiler define a lot preprocessor directive to config Configuration Bits.
- E.g. : *#pragma config* ICS = PGx1
  Set debug interface to channel 1.

Watchdog Timer Enable

FWDTEN = OFF	Watchdog Timer is disabled
FWDTEN = ON	Watchdog Timer is enabled

Comm Channel Select

ICS = PGx3	Emulator functions are shared with PGEC3/PGED3
ICS = PGx2	Emulator functions are shared with PGEC2/PGED2
ICS = PGx1	Emulator functions are shared with PGEC1/PGED1

Set Clip On Emulation Mode

COE = ON	Enabled
COE = OFF	Disabled

Background Debug

BKBUG = ON	Device resets into Debug mode
BKBUG = OFF	Device resets into Operational mode

General Code Segment Write Protect

GWRP = ON	Writes to program memory are disabled
GWRP = OFF	Writes to program memory are allowed

General Code Segment Code Protect

GCP = ON	Code protection is enabled for the entire program memory space
GCP = OFF	Code protection is disabled

JTAG Port Enable

JTAGEN = OFF	JTAG port is disabled
JTAGEN = ON	JTAG port is enabled

REGISTER 26-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1
r	JTAGEN(1)	GCP	GWRP	DEBUG	—	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:	r = Reserved bit	
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed	'1' = Bit is set	'0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **Reserved:** The value is unknown; program as '0'

bit 14 **JTAGEN:** JTAG Port Enable bit(1)
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space

bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled

bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode

bit 10 **Unimplemented:** Read as '1'

bit 9-8 **ICS<1:0>:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use

bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled

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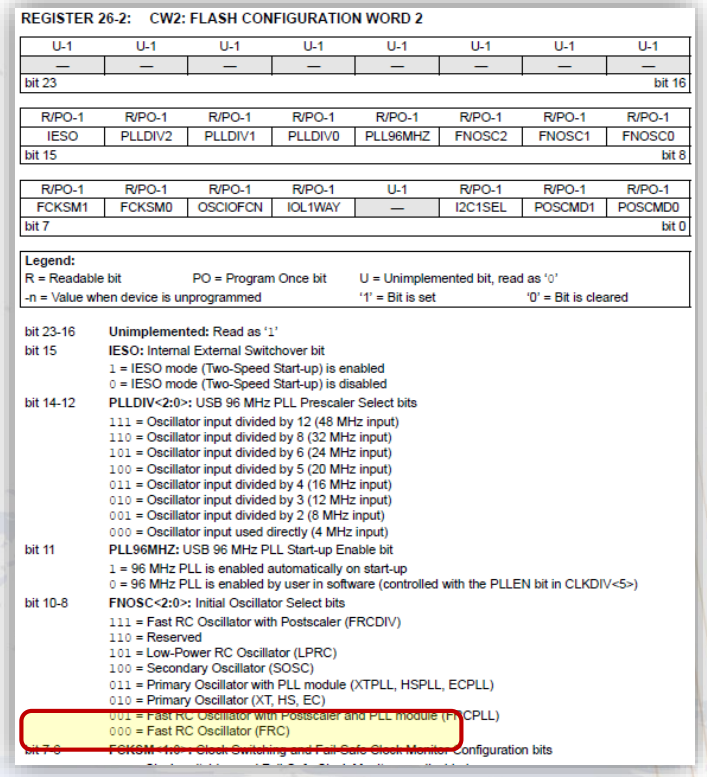
XC16 Support for

Configuration Bits

- Those preprocessor directive use to select system clock also.
- E.g. : *#pragma config FNOSC = FRC*
  Select clock source is internal Fast RC (8MHz).

Oscillator Select

FNOSC = FRC	Fast RC Oscillator (FRC)
FNOSC = FRCPLL	Fast RC oscillator with Postscaler and PLL module (FRCPLL)
FNOSC = PRI	Primary oscillator (XT, HS, EC)
FNOSC = PRIPLL	Primary oscillator (XT, HS, EC) with PLL module (XTPLL,HSPLL, ECPLL)
FNOSC = SOSC	Secondary oscillator (SOSC)
FNOSC = LPRC	Low-Power RC oscillator (LPRC)
FNOSC = FRCDIV	Fast RC oscillator with Postscaler (FRCDIV)



REGISTER 26-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	PLL96MHZ	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	—	I2C1SEL	POSCMD1	POSCMD0
bit 7							bit 0

Legend:
R = Readable bit PO = Program Once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) is enabled
0 = IESO mode (Two-Speed Start-up) is disabled
bit 14-12 **PLLDIV<2:0>:** USB 96 MHz PLL Prescaler Select bits
111 = Oscillator input divided by 12 (48 MHz input)
110 = Oscillator input divided by 8 (32 MHz input)
101 = Oscillator input divided by 6 (24 MHz input)
100 = Oscillator input divided by 5 (20 MHz input)
011 = Oscillator input divided by 4 (16 MHz input)
010 = Oscillator input divided by 3 (12 MHz input)
001 = Oscillator input divided by 2 (8 MHz input)
000 = Oscillator input used directly (4 MHz input)
bit 11 **PLL96MHZ:** USB 96 MHz PLL Start-up Enable bit
1 = 96 MHz PLL is enabled automatically on start-up
0 = 96 MHz PLL is enabled by user in software (controlled with the PLLEN bit in CLKDIV<5>)
bit 10-8 **FNOSC<2:0>:** Initial Oscillator Select bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)
bit 7-6 FCKSM<1:0>: Clock Switching and Fail-Safe Clock Monitor Configuration bits

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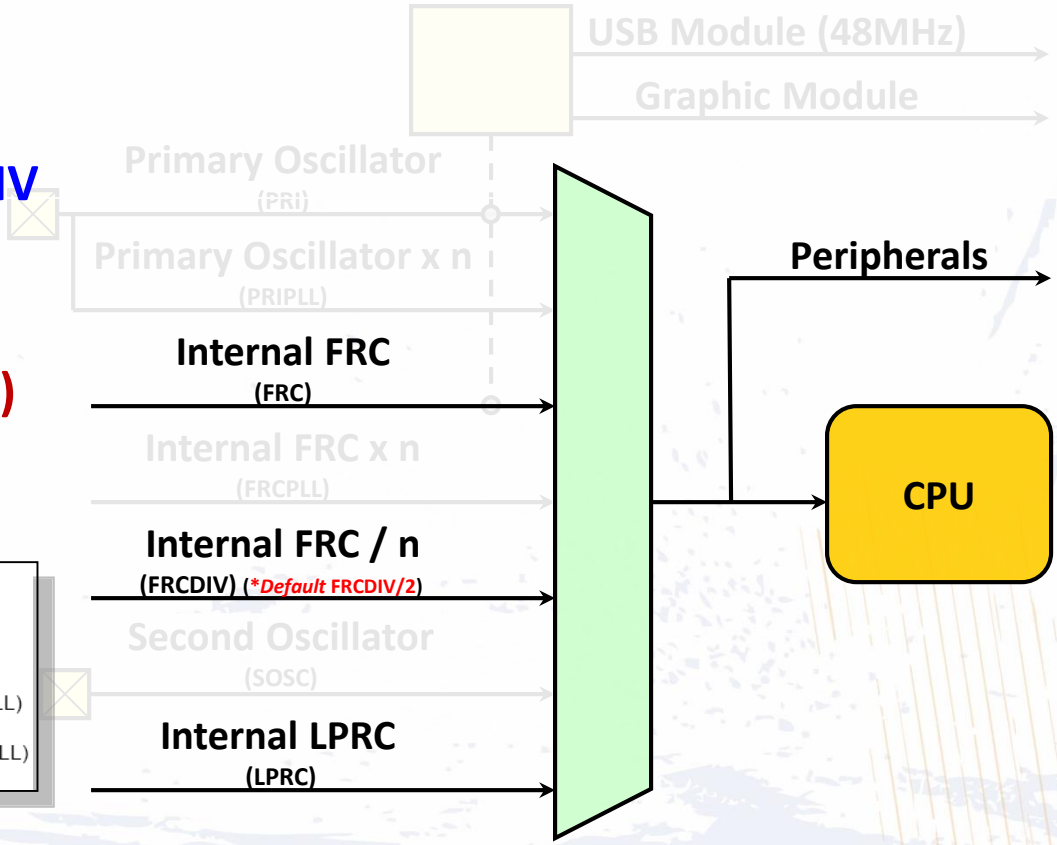
Clock Source (FRC, FRCDIV, LPRC)

- Internal FRC is 8MHz, Internal Low Power RC is 31KHz.
- Set FNOSC to FRC, FRCDIV or LPRC to select internal RC for clock source.
- *#pragma config* FNOSC = FRC
  #pragma config FNOSC = FRCDIV
  #pragma config FNOSC = LPRC
- Default clock source is
  FRCDIV = (FRC(8MHz) / RCDIV)
  *RCDIV default is 2
  *RCDIV is CLKDIV<10:8>

bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



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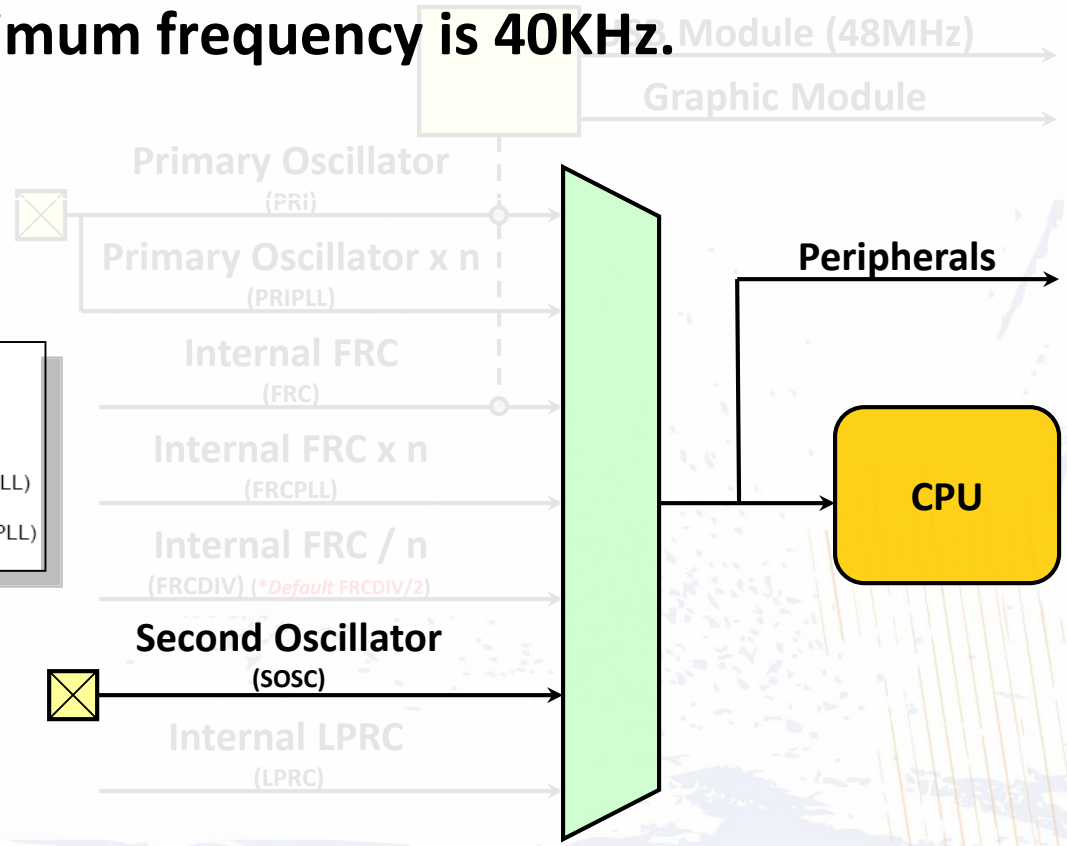
Clock Source (SOSC)

- Set FNOSC to SOSC to select secondary oscillator clock for clock source.
- Secondary oscillator maximum frequency is 40KHz.
- *#pragma config* FNOSC = SOSC

bit 10-8	**FNOSC2:FNOSC0:** Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



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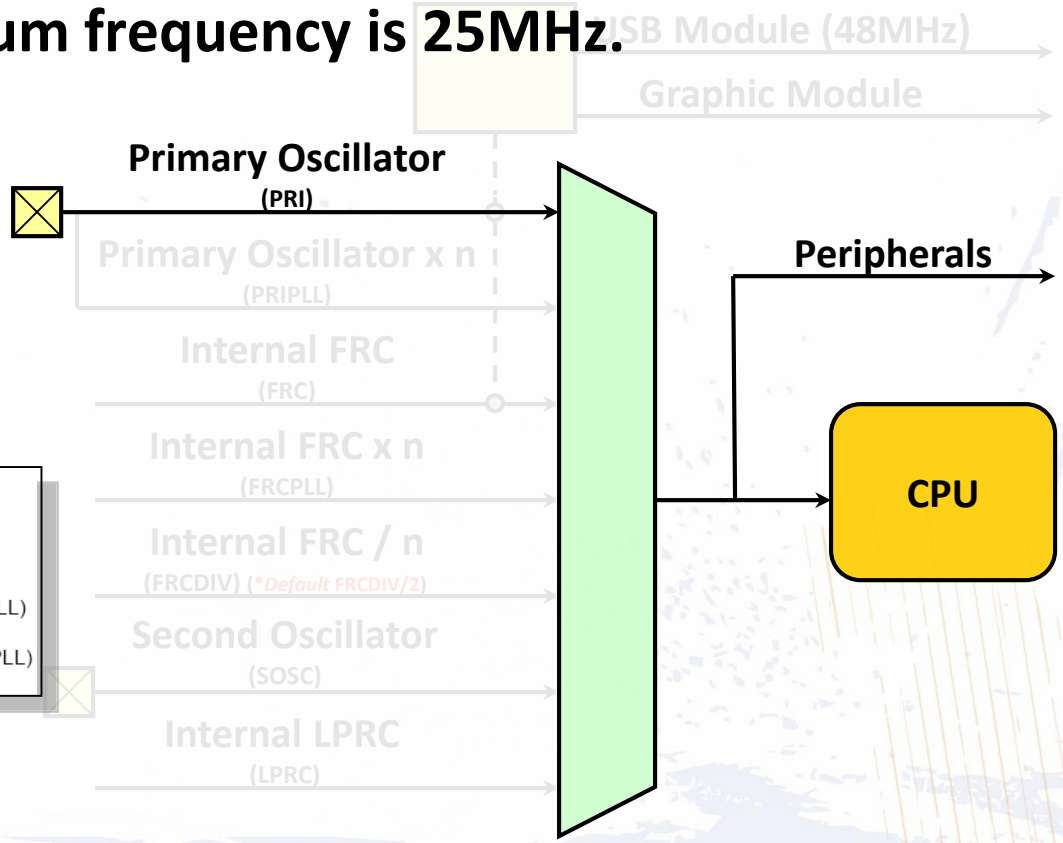
Clock Source (PRI)

- Set FNOSC to PRI to select primary oscillator clock for clock source.
- Primary oscillator maximum frequency is 25MHz.
- *#pragma config* FNOSC = PRI

bit 10-8	**FNOSC2:FNOSC0:** Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



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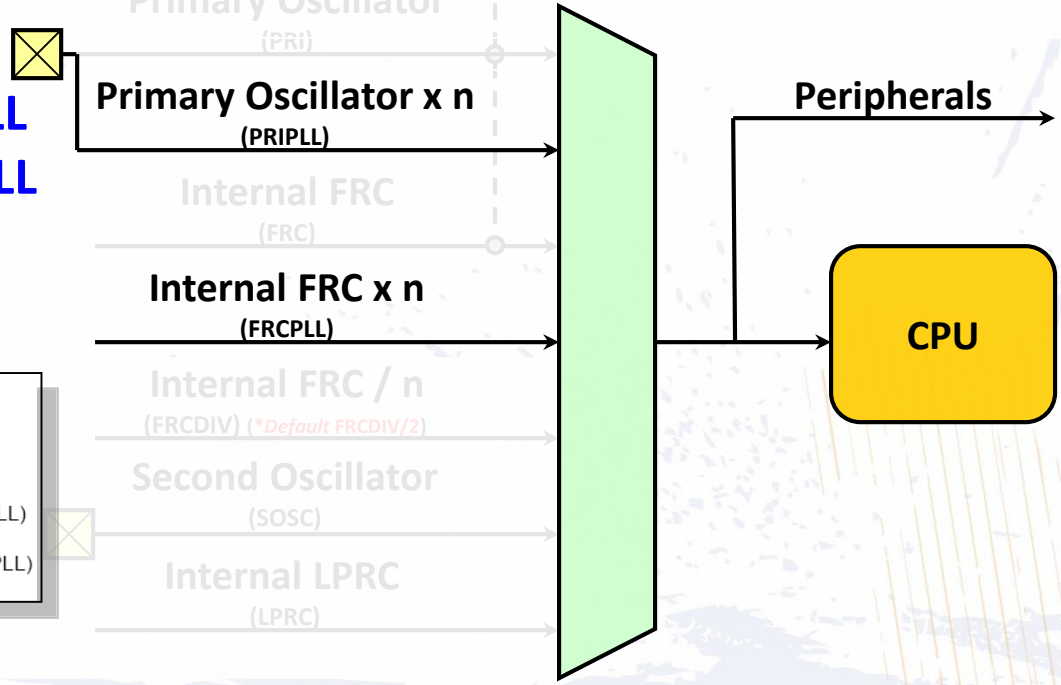
Clock Source (PRIPLL, FRCPLL)

- The system clock for all PIC24F devices includes a frequency multiplier branch built around a Phase Lock Loop (PLL). This branch allows the user to obtain a higher clock speed.
- Set FNOSC to PRIPLL or FRCPLL to get maximum frequency for clock source.
- *#pragma config* FNOSC = PRIPLL
  #pragma config FNOSC = FRCPLL



bit 10-8	**FNOSC2:FNOSC0:** Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)

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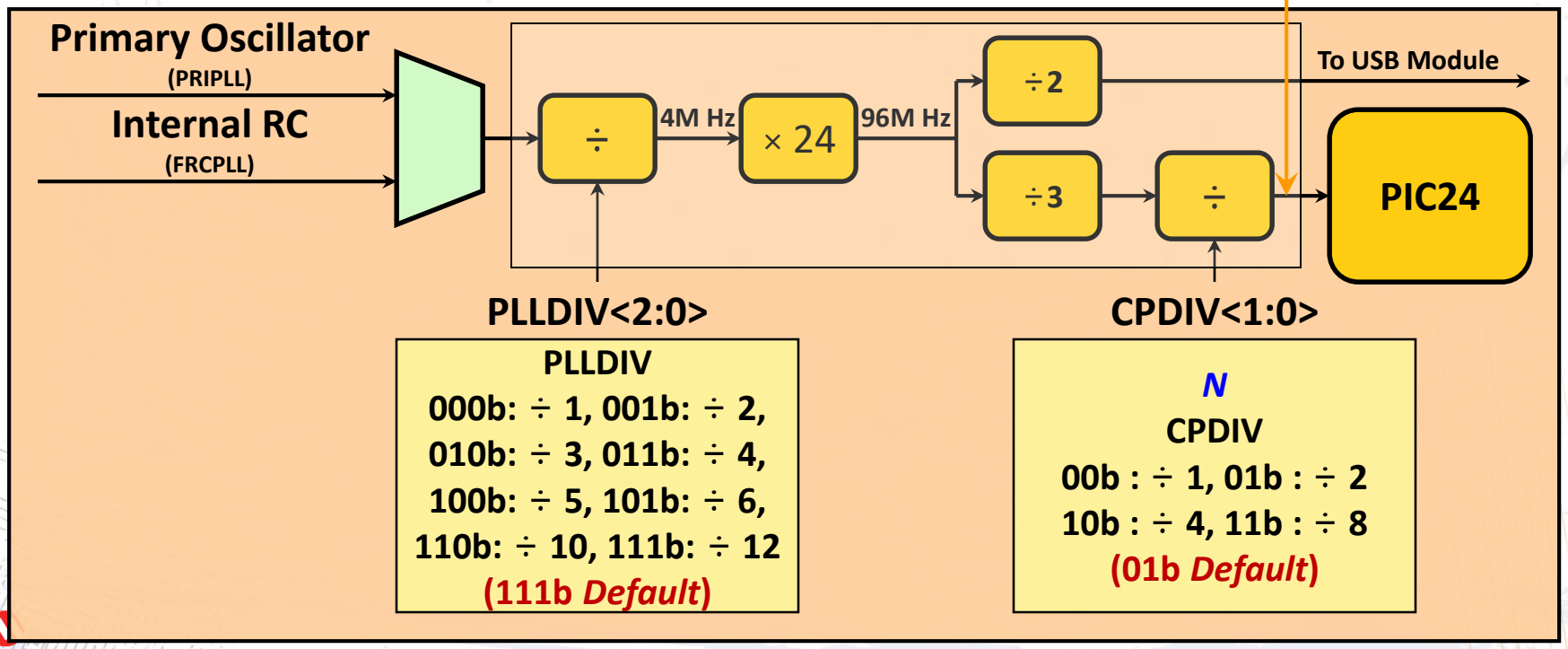
Phase Locked Loop

- PLL is a fixed 4x multiplier, which can be used with XT and EC Primary Oscillators and FRC.

$$F_{OSC} = \frac{\frac{96MHz}{3}}{N}$$



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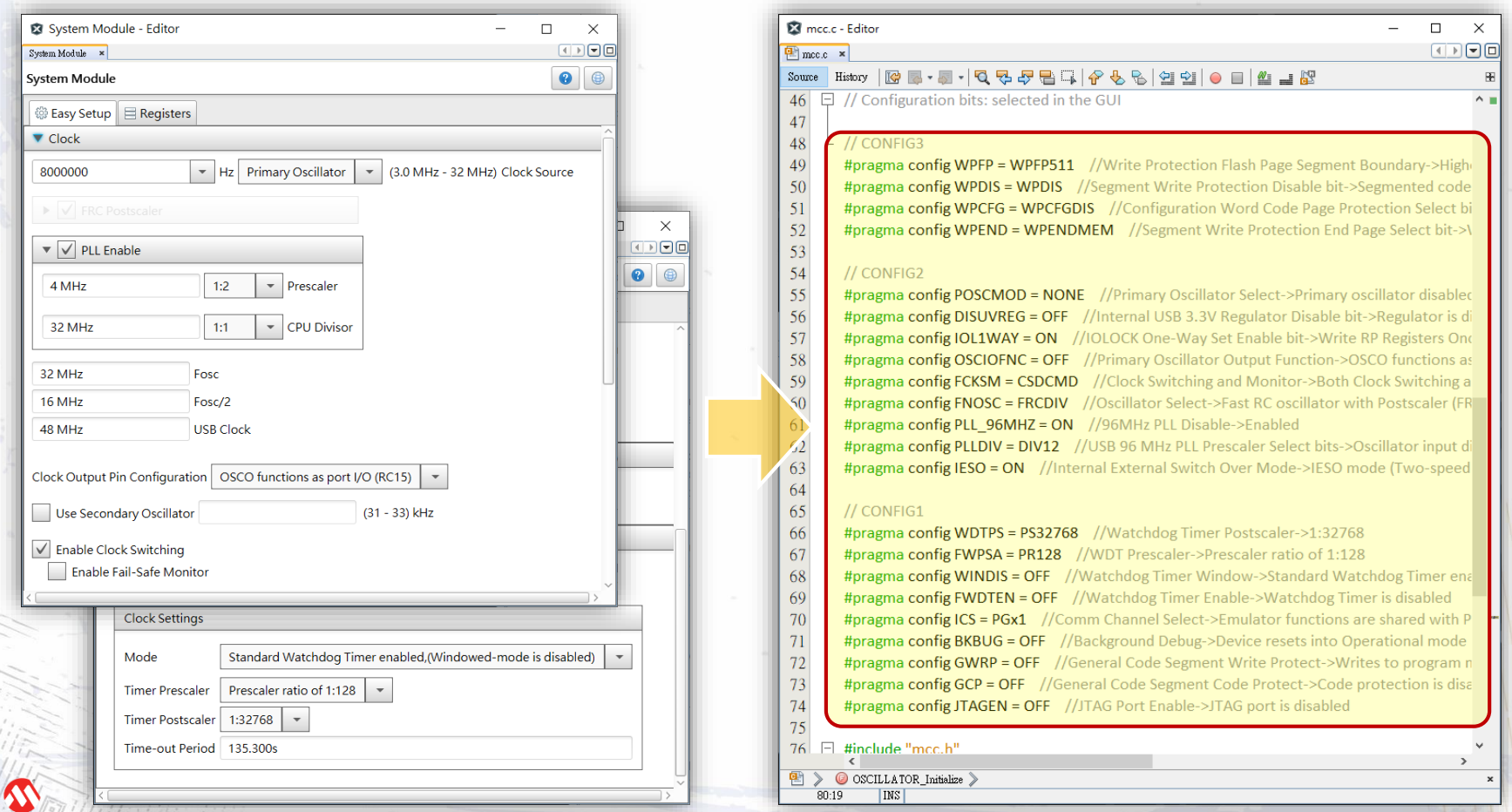
MCC's
Configuration Bits Setting

- Configuration Bits setting generate by MCC automatically.



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Lab6 System Clock PRIPLL

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Lab6 System Clock PRIPLL

- Try to change system clock from internal Fast RC to Primary Oscillator and enable PLL.
- Try to provide maximum frequency (32MHz) to MCU.

- **Let's go!**

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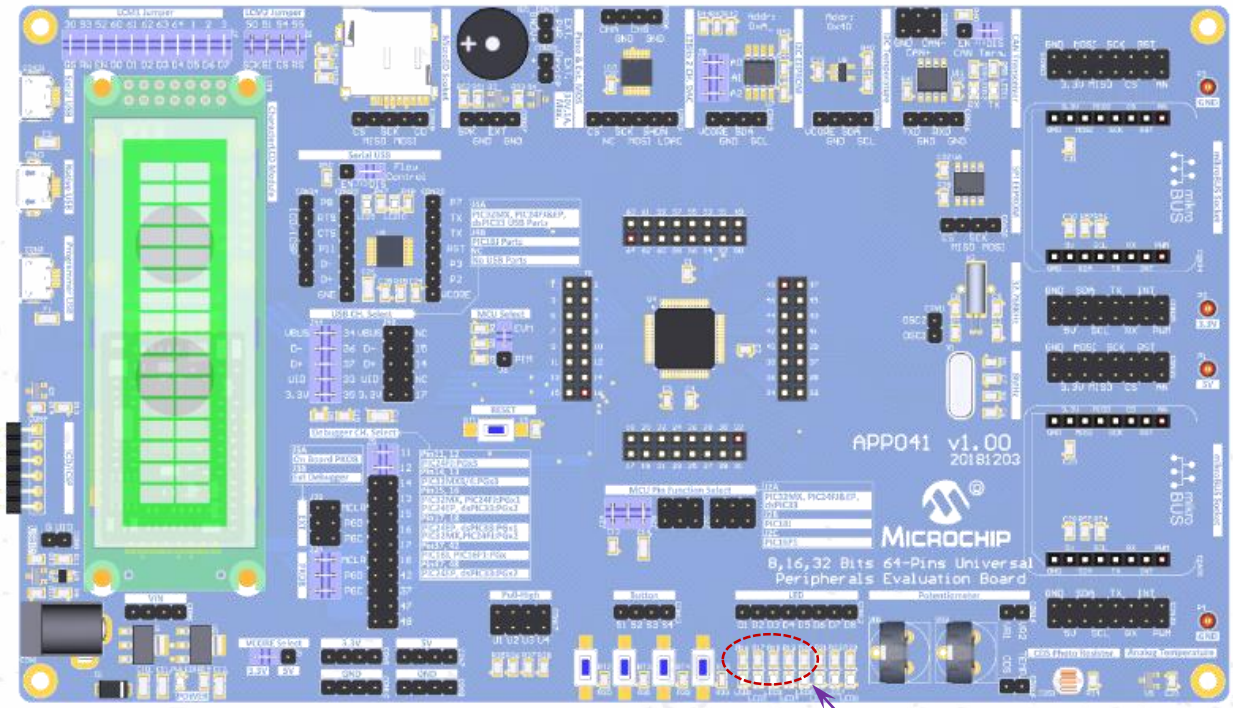
Lab6 System Clock PRIPLL

Result



LEDs Toggle same as Lab5,
But Clock source change to PRIPLL.

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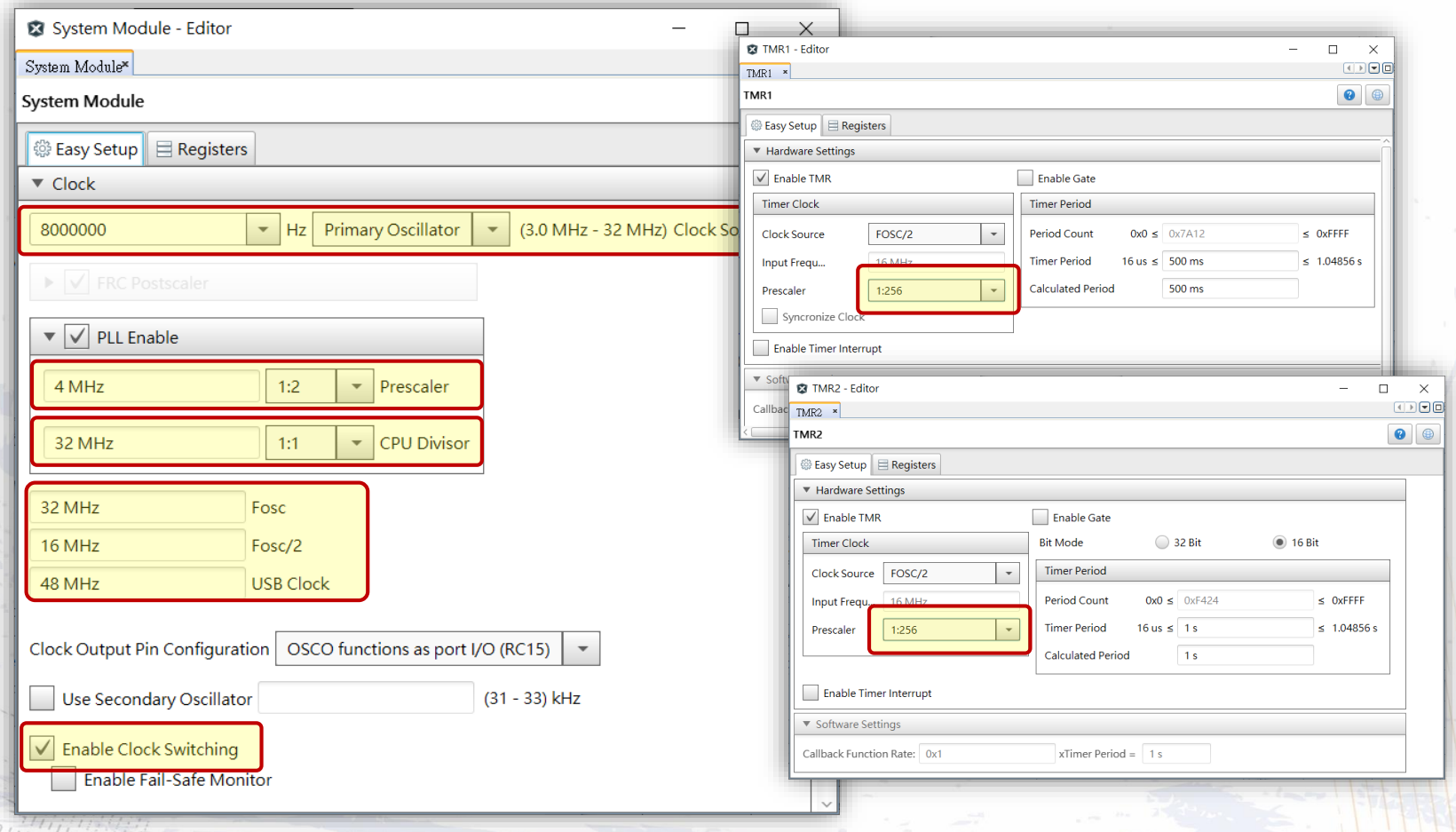
Lab6 System Clock PRIPLL

MCC's Setting



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