



MICROCHIP

Regional Training Centers

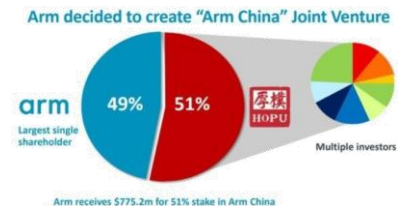
Section 1

**SAMD21 ARM Cortex-M0+
Microcontroller Introduction**

ARM's History

- **ARM (Advanced RISC Machine)** 安謀, 進階精簡指令集機器。是一個32位元精簡指令集 (RISC) 處理器架構, ARM處理器非常適用於嵌入式系統以及行動通訊領域,主要設計目標為低成本、高效能、低功耗的特性。至2009年為止, ARM架構處理器佔市面上所有32位元嵌入式RISC處理器90%的比例。
- ARM處理器從可攜式裝置 (PDA、行動電話、多媒體播放器、掌上型電玩和計算機) 到電腦週邊設備 (硬碟、桌上型路由器), 甚至在飛彈的彈載電腦等軍用設施中都有他的存在。
- 2016年7月18日, 日本軟銀集團斥資3.3萬億日元 (約合311億美元) 將設計ARM的公司ARM Holdings收購。
- 2018年6月4日, 軟銀同意旗下ARM控股的全資子公司「ARM中國」的51%股份將出售給中國的客戶企業和機構投資者。出售額為7.7520億美元。

ARM® | arm = SoftBank



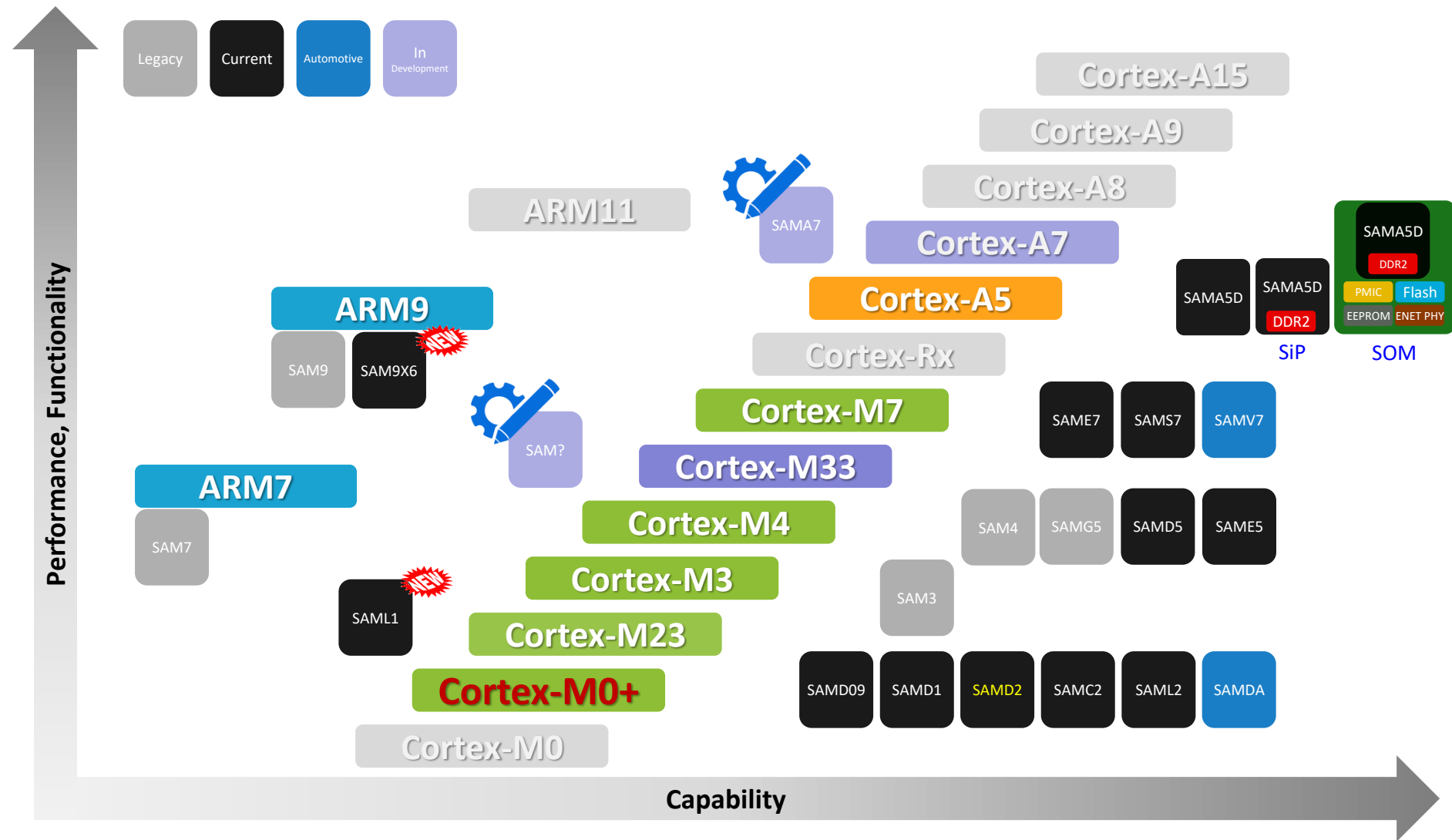
ARM in Partnership



ARM core MCU/MPU success

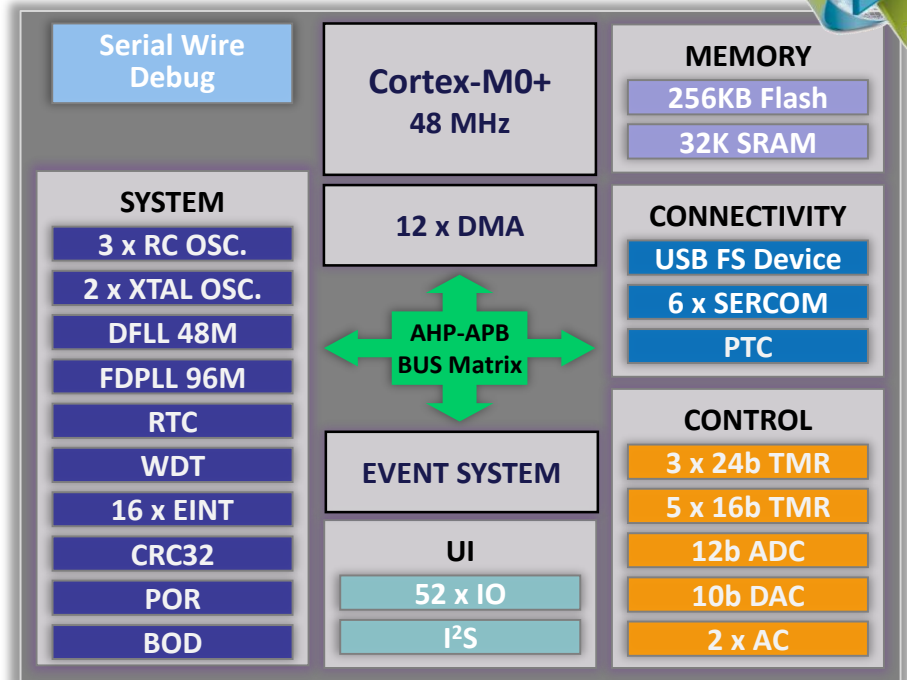


Microchip ARM Core Products



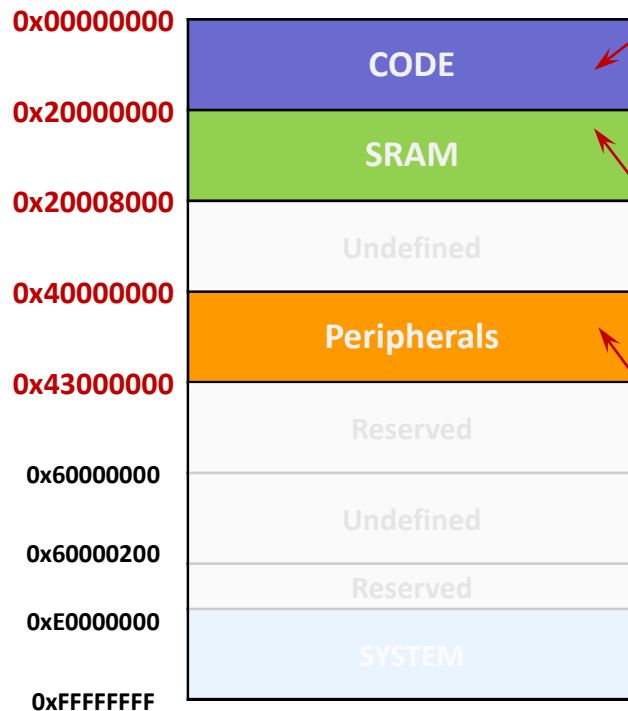
SAMD21 Block Diagram

- The SAMD21 is a series of low-power microcontrollers using the ARM® Cortex® M0+ processor (Cortexv6-M) ◦
- Maximum frequency of 48MHz and reach 2.46 CoreMark®/ MHz ◦
- All devices include intelligent and flexible peripherals, Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces ◦



SAMD21 Memory

Up to 256KB Flash and 32KB SRAM



Program Memory

The actual location of the application code.
for example,
main () is placed in this area.
The actual size depend on part number.

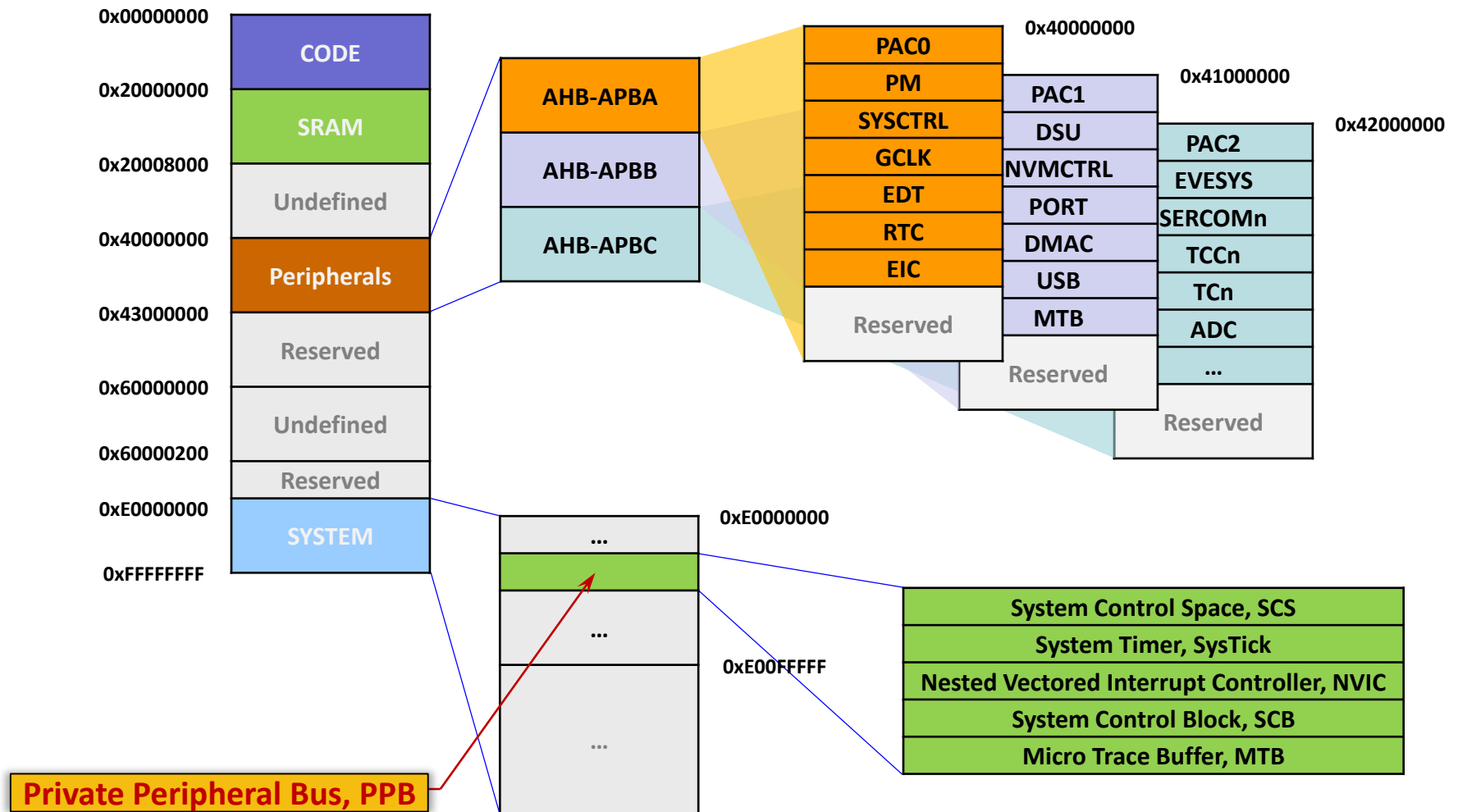
Data Memory

This area is used for storing data.
The actual size depend on part number.

Peripherals Function Registers

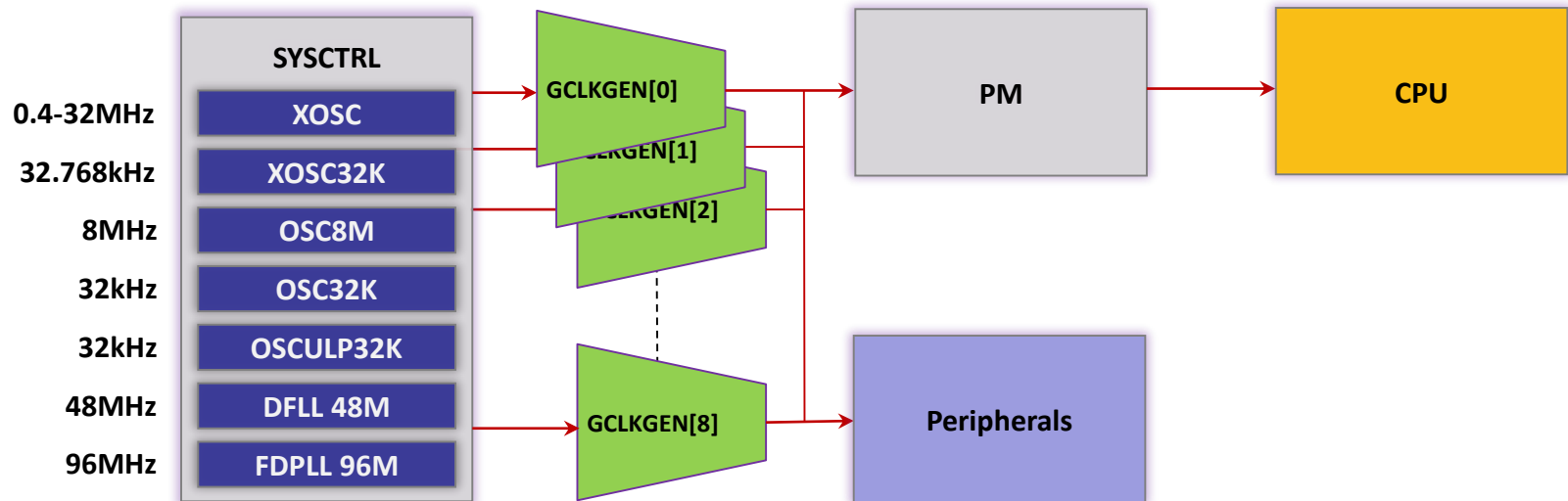
Reserved for the device
This area include control and status bits for the CPU and peripherals on the device.

SAMD21 Memory Mapping



Clock System

- **SYSCTRL provides clock sources to the Generic Clock Controller** ◦ The available clock sources are XOSC, XOSC32K, OSC32K, OSCULP32K, OSC8M, DFLL48M and FDPLL96M ◦
- **The bus clock can be enabled and disabled in the Power Manager(PM) include CPU Clock (GCLK_MAIN)** ◦



Part Number

SAMD 21 G 18 A - A U T

Product Family

SAMD = General Purpose Microcontroller

Product Series

21 = Cortex M0 + CPU, Basic Feature Set
+ DMA + USB

Pin Count

E = 32 Pins (35 Pins for WLCSP)
G = 48 Pins (45 Pins for WLCSP)
J = 64 Pins

Flash Memory Density

18 = 256KB
17 = 128KB
16 = 64KB
15 = 32KB

Device Variant

A = Default Variant
B = Added RWW support for 32KB and 64KB memory options
C = Silicon revision F for WLCSP35 package option.

Package Carrier

No character = Tray (Default)
T = Tape and Reel

Package Grade

U = -40 - 85°C Matte Sn Plating
F = -40 - 125°C Matte Sn Plating

Package Type

A = TQFP
M = QFN
U = WLCSP
C = UFBGA