



MICROCHIP

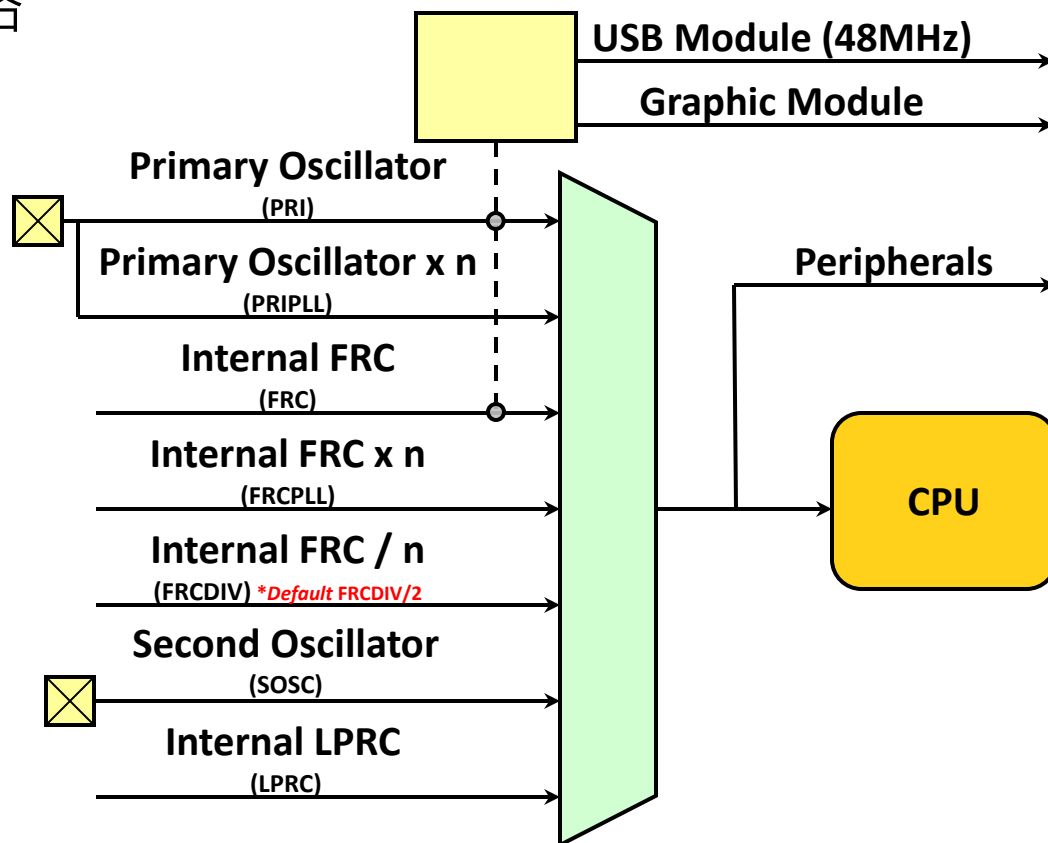
Regional Training Centers

Section 7

Oscillator and Configuration Bits

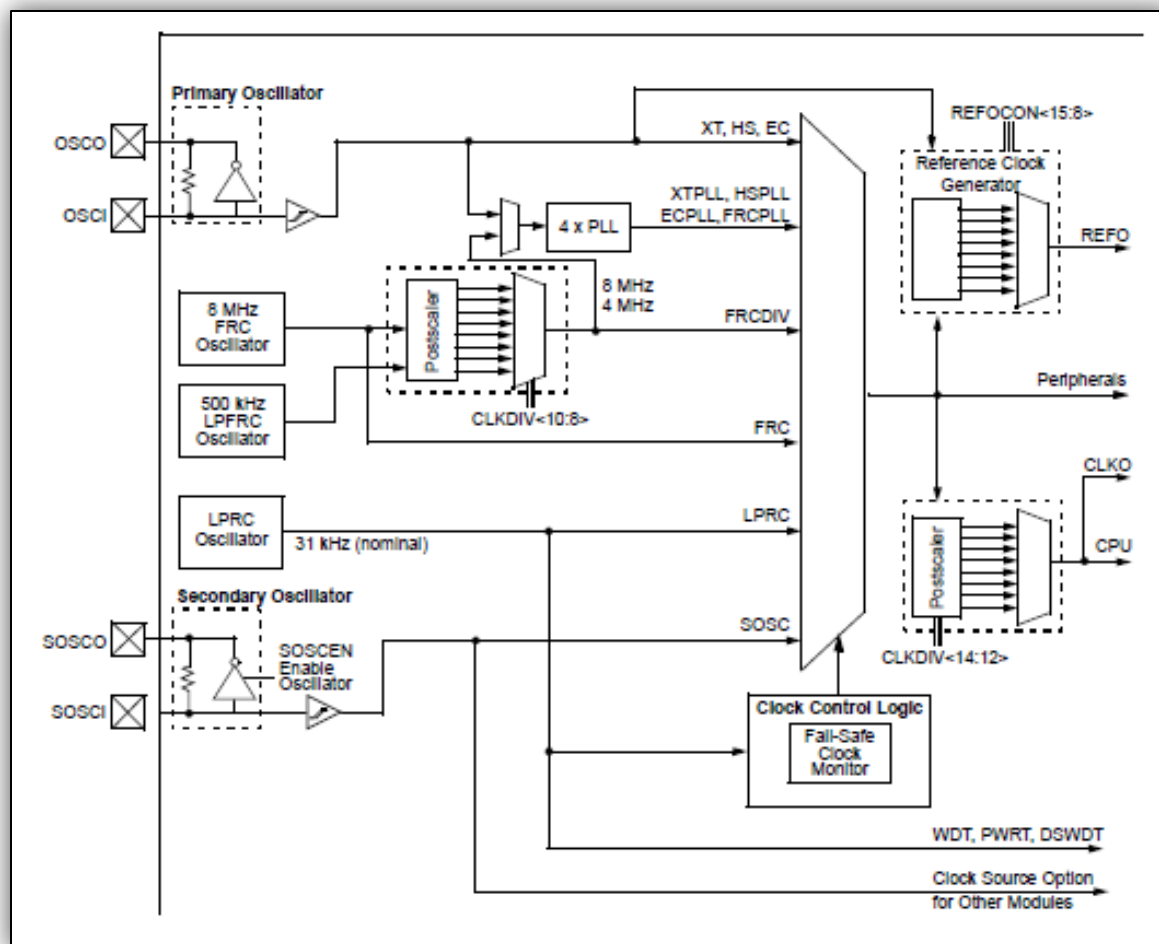
Microchip 16-Bits 時脈架構

- 回憶下前面的說明, Microchip 16-Bits MCU具有多種時脈來源可選擇。可以使用內部RC或者外部的Crystal, Oscillator。輸入的時脈也可透過內部電路進行倍頻(PLL)或者除頻。
- 時脈來源的設定, 必須正確如果設定錯誤, CPU會以不正確頻率執行, 導致程式運作上的時序不對, 或者完全沒有接收到時脈, 導致CPU無法運作。**
- 特定系列具有USB模組及LCD模組的時脈, 電路結構會更複雜。



PIC24F16KA102's Oscillator

- PIC24F16KA102的 Oscillator Block Diagram如圖所示。
- 時脈來源的設定必需透過設定 Configuration Bits。



Configuration Bits

- Configuration Bits是用來設定MCU中一些重要的模式。其中包含如:CPU的時脈來源, 除錯工具使用的接腳, Watchdog, 程式碼保護, 程式碼防寫等設定。
- 其中又以CPU的時脈來源, 除錯工具使用的接腳設定最重要, 時脈來源設定錯誤則CPU無法如預期運作, 除錯工具使用的接腳設定錯誤, 則無法開啟除錯模式。
- 參考Datasheet的Special Feature章節可以看到完整的說明。

REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16
R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8
R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend:

R = Readable bit
 PO = Program-once bit
 -n = Value when device is unprogrammed

bit 23-16 Unimplemented: Read as '1'
 bit 15 IESO: Internal External Switchover bit
 1 = IESO mode (Two-Speed Start-up)
 0 = IESO mode (Two-Speed Start-up)
 bit 14-12 PLLDIV2:PLLDIV1: USB 98 MHz PLL
 111 = Oscillator input divided by 12
 110 = Oscillator input divided by 10
 101 = Oscillator input divided by 8
 100 = Oscillator input divided by 6
 011 = Oscillator input divided by 4
 010 = Oscillator input divided by 3
 001 = Oscillator input divided by 2
 000 = Oscillator input used directly
 bit 11 Reserved: Always maintain as '0'
 bit 10-8 FNOSC2:FNOSC0: Initial Oscillator
 111 = Fast RC Oscillator with Postsc
 110 = Reserved
 101 = Low-Power RC Oscillator (LPR
 100 = Secondary Oscillator (SOSC)
 011 = Primary Oscillator with PLL m
 010 = Primary Oscillator (XT, HS, EC
 001 = Fast RC Oscillator with postsc
 000 = Fast RC Oscillator (FRC)
 bit 7-6 FCKSM1:FCKSM0: Clock Switching
 1x = Clock switching and Fail-Safe C
 01 = Clock switching is enabled, Fail
 00 = Clock switching is enabled, Fail
 bit 5 OSCIOFCN: OSCIO Pin Configuration
 1 = OSCIO/CLKO/RC15 functions as
 0 = OSCIO/CLKO/RC15 functions as
 bit 4 IOL1WAY: IOLock One-Way Set En
 1 = The IOLock bit (OSCCON<6
 completed. Once set the Periph

REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16
r-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
JTAGEN	GCP	GWRP	DEBUG	r	ICST1	ICSD0	ICSD1
bit 15							bit 8
R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWOTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:

R = Readable bit
 PO = Program Once bit
 -n = Value when device is unprogrammed

r = Reserved bit
 U = Unimplemented bit, read as '0'
 1 = Bit is set
 0 = Bit is cleared

bit 23-16 Unimplemented: Read as '1'
 bit 15 Reserved: The value is unknown; program as '0'
 bit 14 JTAGEN: JTAG Port Enable bit⁽¹⁾
 1 = JTAG port is enabled
 0 = JTAG port is disabled
 bit 13 GCP: General Segment Program Memory Code Protection bit
 1 = Code protection is disabled
 0 = Code protection is enabled for the entire program memory space
 bit 12 GWRP: General Segment Code Flash Write Protection bit
 1 = Writes to program memory are allowed
 0 = Writes to program memory are disabled
 bit 11 DEBUG: Background Debugger Enable bit
 1 = Device resets into Operational mode
 0 = Device resets into Debug mode
 bit 10 Reserved: Always maintain as '1'
 bit 9-8 ICST1:ICSD0: Emulator Pin Placement Select bits
 11 = Emulator functions are shared with PGE0/PGE1
 10 = Emulator functions are shared with PGE2/PGE3
 01 = Emulator functions are shared with PGE3/PGE0
 00 = Reserved; do not use
 bit 7 FWOTEN: Watchdog Timer Enable bit
 1 = Watchdog Timer is enabled
 0 = Watchdog Timer is disabled
 bit 6 WINDIS: Windowed Watchdog Timer Disable bit
 1 = Standard Watchdog Timer enabled
 0 = Windowed Watchdog Timer enabled; FWOTEN must be '1'
 bit 5 Unimplemented: Read as '1'
 bit 4 FWPSA: WDT Prescaler Ratio Select bit
 1 = Prescaler ratio of 1:128
 0 = Prescaler ratio of 1:32

XC16 Configuration Bits的支援

- 要設定除錯介面，則使用以下方法設定：

#pragma config ICS = PGx3

Alternate I2C1 Pin Mapping bit

I2C1SEL = SEC	Alternate location for SCL1/SDA1 pins
I2C1SEL = PRI	Default location for SCL1/SDA1 pins

Brown-out Reset Voltage bits

BORV = LPBOR	Low-power Brown-Out Reset occurs around 2.0V
BORV = V27	Brown-out Reset set to Highest Voltage (2.7V)
BORV = V20	Brown-out Reset set at 2.0V
BORV = V18	Brown-out Reset set to lowest voltage (1.8V)

MCLR Pin Enable bit

MCLRE = OFF	RA5 input pin enabled; MCLR disabled
MCLRE = ON	MCLR pin enabled; RA5 input pin disabled

ICD Pin Placement Select bits

ICS = PGx3	PGC3/PGD3 are used for programming and debugging the device
ICS = PGx2	PGC2/PGD2 are used for programming and debugging the device
ICS = PGx1	PGC1/PGD1 are used for programming and debugging the device

Set Clip On Emulation bit

COE = ON	Device will reset into Clip On Emulation Mode
COE = OFF	Device will reset into Operational Mode

Background Debugger Enable bit

BKBUG = ON	Background debugger functions enabled
BKBUG = OFF	Background debugger disabled

Deep Sleep Watchdog Timer Postscale Select bits

DSWDTPS = DSWDTPS0	1 : 2 (2.1 ms)
DSWDTPS = DSWDTPS1	1 : 8 (8.3 ms)

REGISTER 26-7: FICD: IN-CIRCUIT DEBUGGER CONFIGURATION REGISTER

R/P-1	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
DEBUG	—	—	—	—	—	FICD1	FICD0
bit 7							bit 0

Legend:

R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7	DEBUG: Background Debugger Enable bit 1 = Background debugger is disabled 0 = Background debugger functions are enabled
bit 6-2	Unimplemented: Read as '0'
bit 1-0	FICD<1:0>: ICD Pin Select bits 11 = PGC1/PGD1 are used for programming and debugging the device 10 = PGC2/PGD2 are used for programming and debugging the device 01 = PGC3/PGD3 are used for programming and debugging the device 00 = Reserved; do not use

Clock Source (FRC, FRCDIV, LPRC)

- PIC24的Oscillator來源可以選擇使用內部FRC,內部FRC/n或Low Power RC。PIC24內部的FRC,工作頻率為8MHz, LPRC為31KHz。
- 要選擇使用內部FRC/LPRC時,可以在Configuration Bits中將FNOSC <2:0>設定為111b,101b或000b。

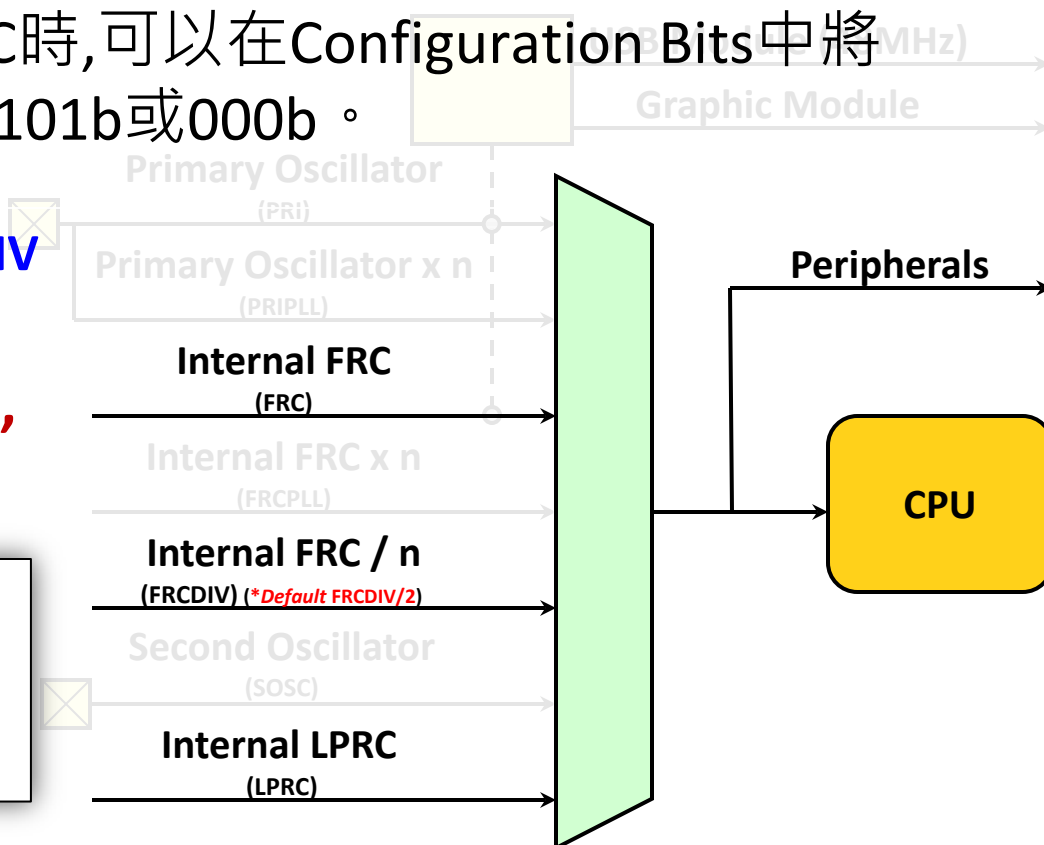
#pragma config FNOSC = FRC

#pragma config FNOSC = FRCDIV

#pragma config FNOSC = LPRC

- FNOSC預設FRCDIV(FRC/n, n(RCDIV)預設= 1 (/ 2)。**

FNOSC<2:0>: Oscillator Selection bits	
000	Fast RC Oscillator (FRC)
001	Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
010	Primary Oscillator (XT, HS, EC)
011	Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100	Secondary Oscillator (SOSC)
101	Low-Power RC Oscillator (LPRC)
110	500 kHz Low-Power FRC Oscillator with divide-by-N (LPFRCDIV)
111	8 MHz FRC Oscillator with divide-by-N (FRCDIV)



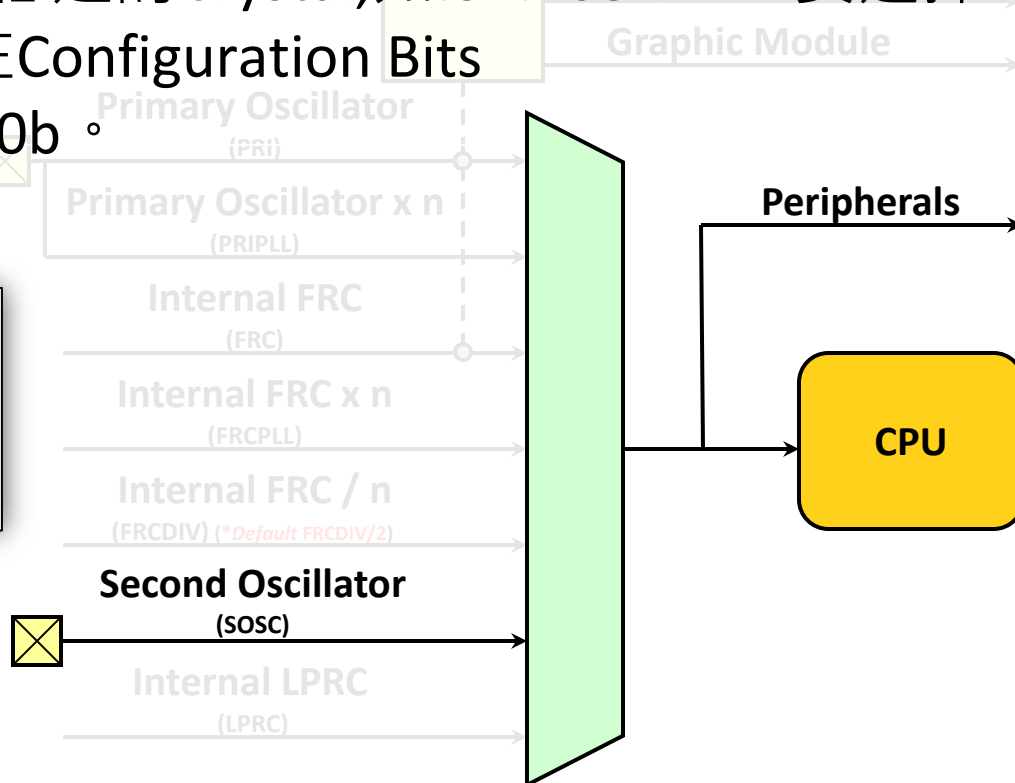
Clock Source (SOSC)

- PIC24的Oscillator來源也可以選擇透過外部的第二組時脈來源接腳(SOSC)取得。
- Second Osc.通常是用來接低速的Crystal,如:32.768KHz。要選擇使用Second Osc.時,可以在Configuration Bits中將FNOSC<2:0>設定為100b。

#pragma config FNOSC = SOSC

FNOSC<2:0>: Oscillator Selection bits

000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
010 = Primary Oscillator (XT, HS, EC)
011 = Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = 500 kHz Low-Power FRC Oscillator with divide-by-N (LPFRCDIV)
111 = 8 MHz FRC Oscillator with divide-by-N (FRCDIV)

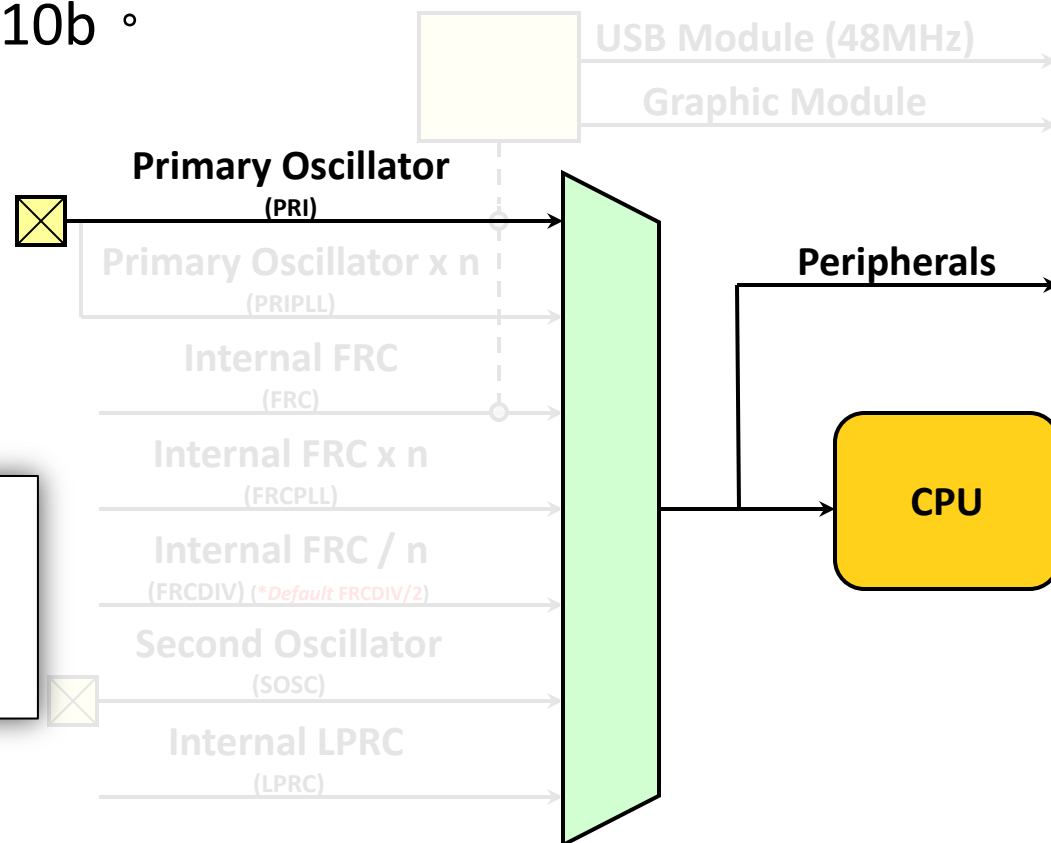


Clock Source (PRI)

- PIC24也可選擇透過外部取得時脈。直接使用Crystal的震盪頻率輸入。要選擇使用Primary Osc.時, 可以在Configuration Bits中將FNOSC<2:0>設定為010b。

#pragma config FNOSC = PRI

- Primary Osc.通常是用來連接高速的Crystal。其最高的輸入頻率被限定在25MHz以下。



FNOSC<2:0>: Oscillator Selection bits

000	= Fast RC Oscillator (FRC)
001	= Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
010	= Primary Oscillator (XT, HS, EC)
011	= Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100	= Secondary Oscillator (SOSC)
101	= Low-Power RC Oscillator (LPRC)
110	= 500 kHz Low-Power FRC Oscillator with divide-by-N (LPFRCDIV)
111	= 8 MHz FRC Oscillator with divide-by-N (FRCDIV)

Clock Source (PRIPLL, FRCPLL)

- 除了以上幾種模式,大多數的PIC24應用,都會透過內部的倍頻線路(PLL, Phase Locked Loop)來提高頻率。倍頻線路可以接受外部的震盪時脈或者內部的FRC。

要選擇使用PLL時,可以在

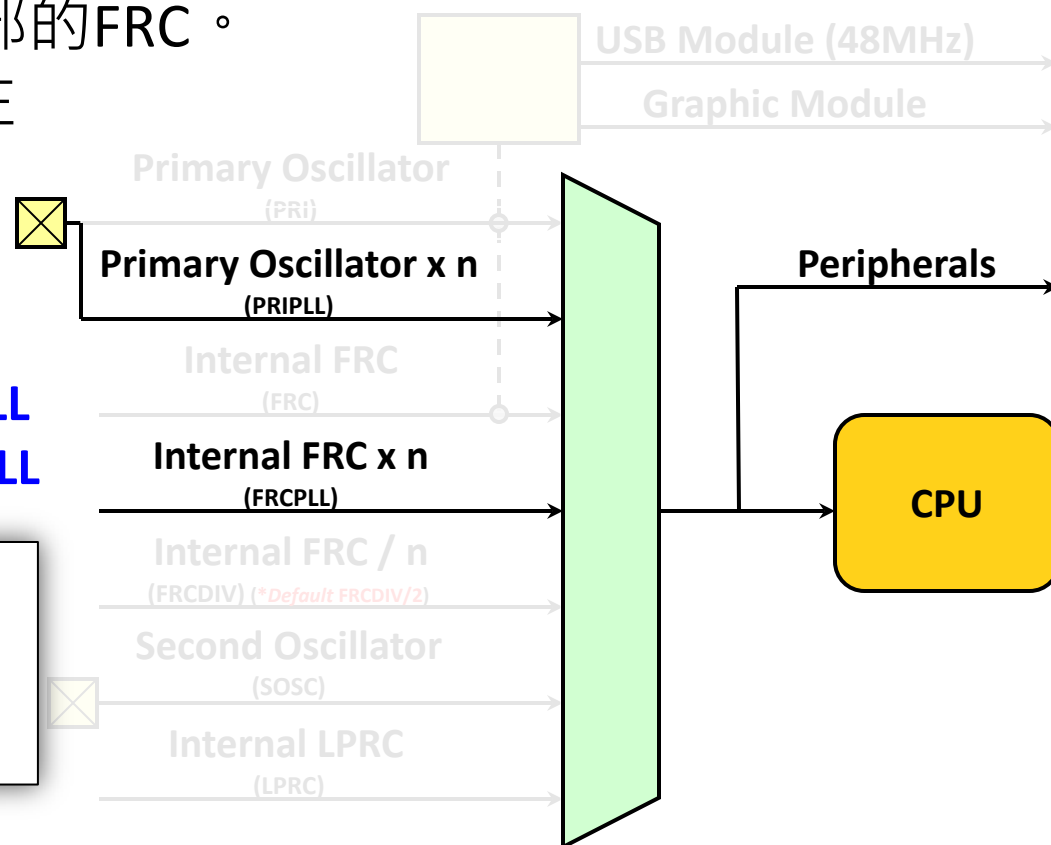
Configuration Bits中將

FNOSC<2:0>設定為

011b或001b。

#pragma config FNOSC = PRIPLL

#pragma config FNOSC = FRCPLL

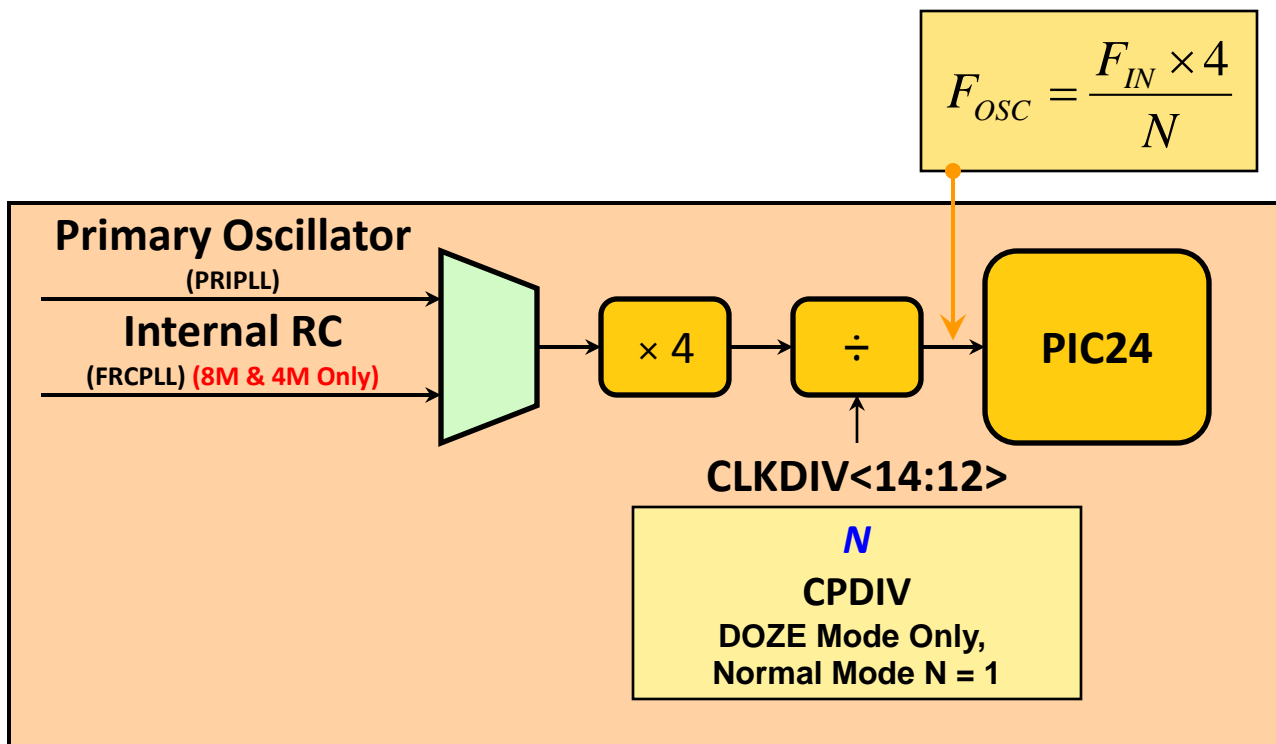


FNOSC<2:0>: Oscillator Selection bits

000	= Fast RC Oscillator (FRC)
001	= Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
010	= Primary Oscillator (XT, HS, EC)
011	= Primary Oscillator with PLL module (HS+PLL, EC+PLL)
100	= Secondary Oscillator (SOSC)
101	= Low-Power RC Oscillator (LPRC)
110	= 500 kHz Low-Power FRC Oscillator with divide-by-N (LPFRCDIV)
111	= 8 MHz FRC Oscillator with divide-by-N (FRCDIV)

Phase Locked Loop

- PIC24F16KA102的PLL的架構非常簡單, 固定4x的倍頻。

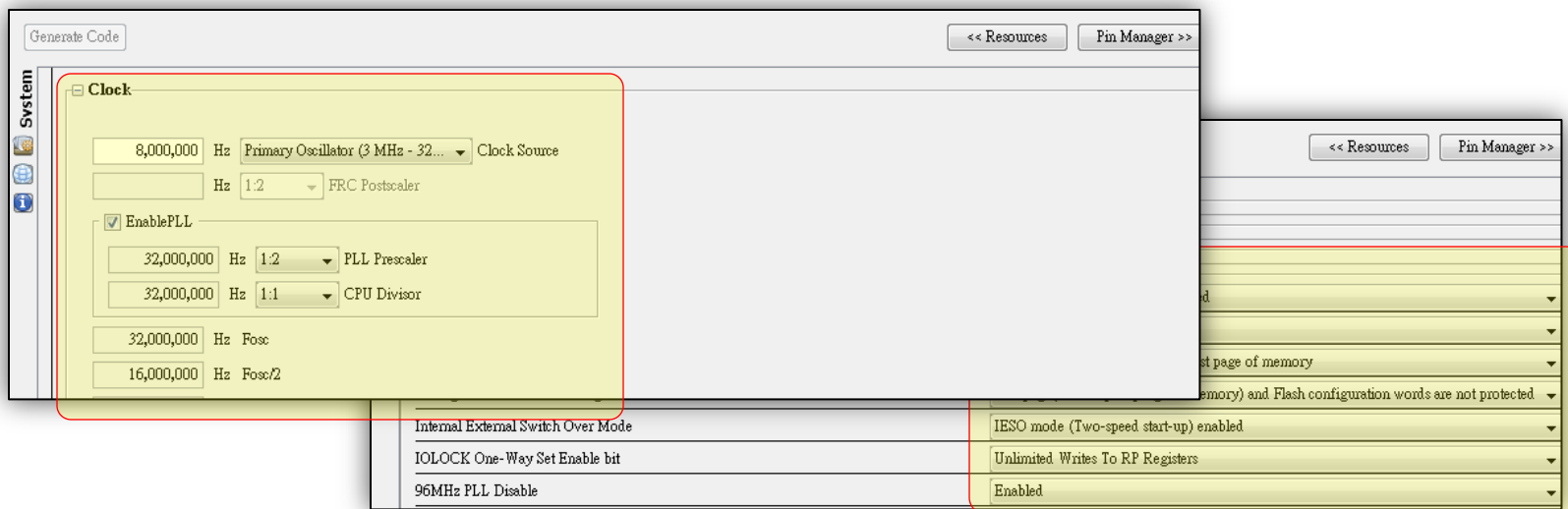


Configuration Bits Setting

- 以前我們要自己在程式中,加入各項Configuration Bits的設定。

```
#pragma config FNOSC = FRCDIV
#pragma config IESO = OFF
#pragma config ICS = PGx3
#pragma config BOREN = BOR3
#pragma config ...
#pragma config ...
```

- 現在, 透過MCC, 直接用點選的方式就能搞定。



MCC's Configuration Bits Setting

- 執行 **Generate Code** 後, MCC會自動根據選擇, 產生各項 Configuration Bits的設定。有些設定需要, 還需要使用程式填入式的數值, 這部分MCC也會一併完成。

```

49 // CONFIG3
50 #pragma config WPDIS = WPDIS // Segment Write Protection Disable bit->Segmented code protection disable
51 #pragma config WPPF = WPPF511 // Write Protection Flash Page Segment Boundary->Highest Page (same as pa
52 #pragma config WPEND = WPENDMEM // Segment W
53 #pragma config WPCFG = WPCFGDIS // Configura
54
55 // CONFIG2
56 #pragma config IESO = ON // Internal Externa
57 #pragma config IOL1WAY = OFF // IOLOCK One-W
58 #pragma config FNOSC = PRIPLL // Oscillator
59 #pragma config PLLDIV = DIV2 // USB 96 MHz P
60 #pragma config PLL_96MHZ = ON // 96MHz PLL D
61 #pragma config DISUVREG = OFF // Internal US
62 #pragma config POSCMOD = XT // Primary Oscil
63 #pragma config OSCIOFNC = OFF // Primary Osc
64 #pragma config FCKSM = CSDCMD // Clock Switch
65
66 // CONFIG1

```

```

78 #include "mcc.h"
79
80 void SYSTEM_Initialize(void)
81 {
82     OSCILLATOR_Initialize();
83     PIN_MANAGER_Initialize();
84     TMRL_Initialize();
85 }
86
87 void OSCILLATOR_Initialize(void)
88 {
89     // DOZEN disabled; DOZE 1:8; CPDIV 1:1; RCDIV FRC/2; ROI disabled;
90     CLKDIV = 0x3100;
91     // Set the secondary oscillator
92 }
93
94




```

Lab4 – Timer1 Polling PRIPLL

目標

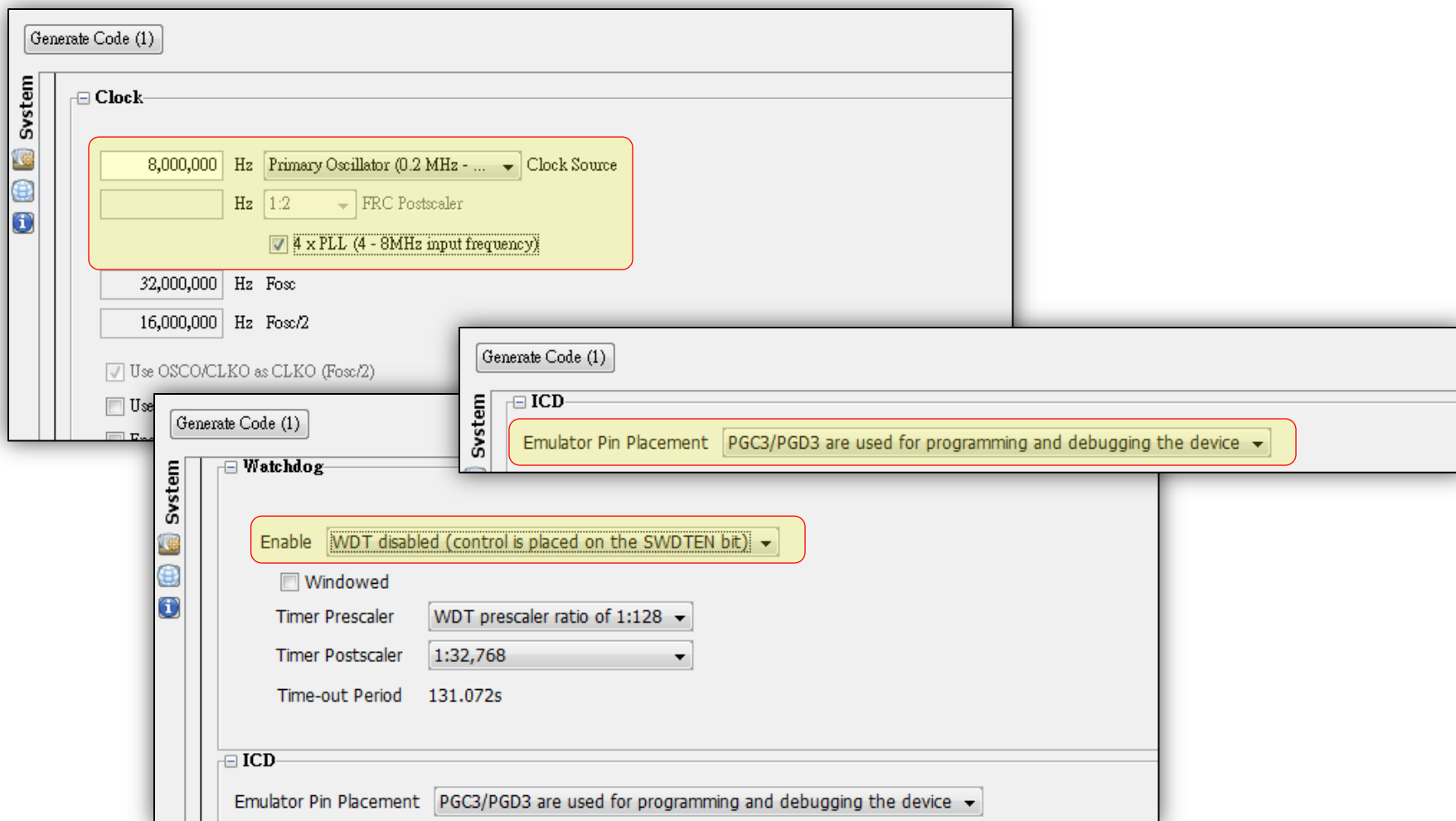
- 嘗試透過MCC的設定, 改變系統時脈為主要外部時脈輸入 (Primary Oscillator), 並開啟PLL, 將系統頻率(F_{OSC})提高到32MHz。除錯介面設定為第一組(PGEC3/PGED3), Watchdog Disable。
- 系統頻率改變後, Timer的設定, 會跟著變動。請再透過MCC調整Lab4中Timer1的設定, 讓Timer1的週期改變成100mS。
- 該如何開始？

Lab4 – Timer1 Polling PRIPLL Step

-  開啟既有專案(C:\Exercises\Exams\Lab4 Timer1 Polling PRIPLL.x)
-  接著開啟開啟MCC, 修改**System**資源, 依照題目要求設定。
-  **System**資源修改完成後, 觀察**Timer1**資源的變化, 並依照題目要求再次修改設定。

Lab4 – Timer1 Polling PRIPLL

MCC's Setting



The image displays three overlapping screenshots of the Microchip Configuration (MCC) tool interface, showing various settings for a project.

Top Screenshot (Clock Settings):

- Generate Code (1)**
- System** (left sidebar)
- Clock** (selected tab)
- 8,000,000 Hz** (Primary Oscillator (0.2 MHz - ...))
- 1:2** (FRC Postscaler)
- ☒ **4 x PLL (4 - 8MHz input frequency)**
- 32,000,000 Hz Fosc**
- 16,000,000 Hz Fosc/2**
- ☒ **Use OSCO/CLKO as CLKO (Fosc/2)**

Middle Screenshot (ICD Settings):

- Generate Code (1)**
- System** (left sidebar)
- ICD** (selected tab)
- Emulator Pin Placement** (PGC3/PGD3 are used for programming and debugging the device)

Bottom Screenshot (Watchdog Settings):

- Generate Code (1)**
- System** (left sidebar)
- Watchdog** (selected tab)
- Enable** (WDT disabled (control is placed on the SWDTEN bit))
- ☐ **Windowed**
- Timer Prescaler** (WDT prescaler ratio of 1:128)
- Timer Postscaler** (1:32,768)
- Time-out Period** (131.072s)
- ICD** (selected sub-tab)
- Emulator Pin Placement** (PGC3/PGD3 are used for programming and debugging the device)