MICROCHIP

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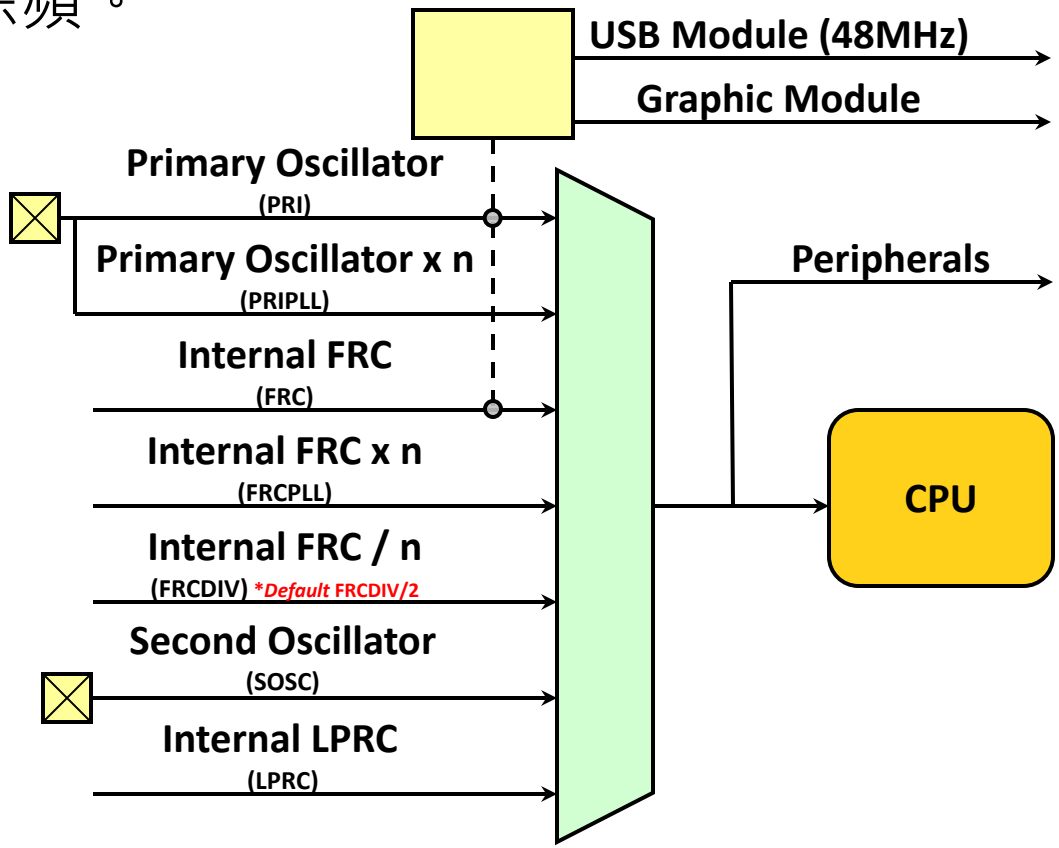
Section 7
Oscillator and Configuration Bits

Microchip 16-Bits 時脈架構

- Microchip 16-Bits MCU具有多種時脈來源可選擇。可以使用內部RC或者外部的Crystal, Oscillator。輸入的時脈也可透過內部電路進行倍頻(PLL)或者除頻。
- **時脈來源的設定, 必須正確如果設定錯誤, CPU會接收到錯誤的頻率, 導致程式運作上的時序不對, 或者完全沒有接收到時脈, 導致CPU無法運作。**
- 特定系列具有USB模組及LCD模組的時脈, 電路結構會更複雜。



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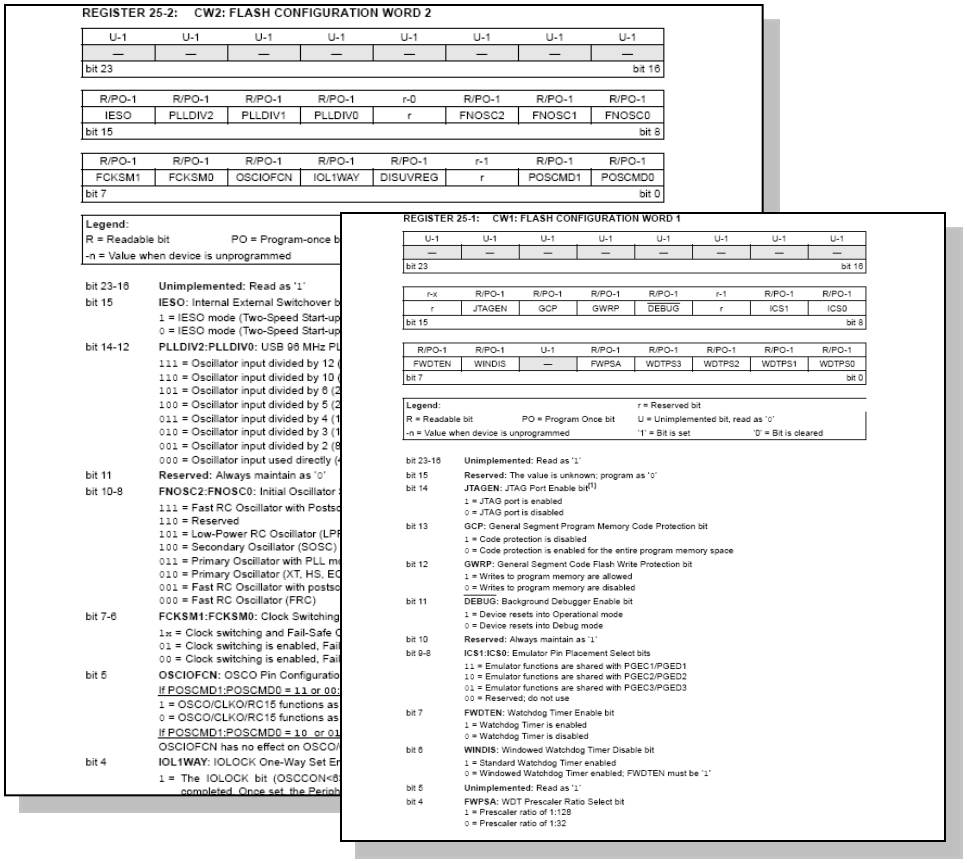
Configuration Bits

- Configuration Bits是用來設定MCU中一些重要的模式。其中包含如:CPU的時脈來源, 除錯工具使用的接腳, Watchdog, 程式碼保護, 程式碼防寫等設定。
- **其中又以CPU的時脈來源, 除錯工具使用的接腳設定最重要, 時脈來源設定錯誤CPU無法正常運作, 除錯工具使用的接腳設定錯誤, 則無法使用開啟除錯模式。**
- 參考Datasheet的Special Feature章節可以看到完整的說明。



REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend:
R = Readable bit PO = Program-once b
-n = Value when device is unprogrammed

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **IESO:** Internal External Switchover b
1 = IESO mode (Two-Speed Start-up
0 = IESO mode (Two-Speed Start-up
bit 14-12 **PLLDIV2:PLLDIV0:** USB 96 MHz PL
111 = Oscillator input divided by 12 (
110 = Oscillator input divided by 10 (
101 = Oscillator input divided by 6 (2
100 = Oscillator input divided by 5 (2
011 = Oscillator input divided by 4 (1
010 = Oscillator input divided by 3 (1
001 = Oscillator input divided by 2 (8
000 = Oscillator input used directly (
bit 11 **Reserved:** Always maintain as '0'
bit 10-8 **FNOSC2:FNOSC0:** Initial Oscillator
111 = Fast RC Oscillator with Postsc
110 = Reserved
101 = Low-Power RC Oscillator (LPF
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL m
010 = Primary Oscillator (XT, HS, EC
001 = Fast RC Oscillator with postsc
000 = Fast RC Oscillator (FRC)
bit 7-6 **FCKSM1:FCKSM0:** Clock Switching
1x = Clock switching and Fail-Safe C
01 = Clock switching is enabled, Fail
00 = Clock switching is enabled, Fail
bit 5 **OSCIOFCN:** OSCO Pin Configuratio
If POSCMD1:POSCMD0 = 11 or 00:
1 = OSCO/CLKO/RC15 functions as
0 = OSCO/CLKO/RC15 functions as
If POSCMD1:POSCMD0 = 10 or 01
OSCIOFCN has no effect on OSCO/
bit 4 **IOL1WAY:** IOLOCK One-Way Set Er
1 = The IOLOCK bit (OSCCON<6
completed. Once set, the Periph

REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
r	JTAGEN	GCP	GWRP	DEBUG	r	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend: r = Reserved bit
R = Readable bit PO = Program Once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **Reserved:** The value is unknown; program as '0'
bit 14 **JTAGEN:** JTAG Port Enable bit(1)
1 = JTAG port is enabled
0 = JTAG port is disabled
bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space
bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled
bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode
bit 10 **Reserved:** Always maintain as '1'
bit 9-8 **ICS1:ICS0:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use
bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled
0 = Watchdog Timer is disabled
bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard Watchdog Timer enabled
0 = Windowed Watchdog Timer enabled; FWDTEN must be '1'
bit 5 **Unimplemented:** Read as '1'
bit 4 **FWPSA:** WDT Prescaler Ratio Select bit
1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

XC16 Configuration Bits的支援

- 不同系列的Configuration Bits設定方法是一樣的, 但使用參數與定義可能不同。必須搭配參照Datasheet及MCU的說明檔(**config_index.html**)來設定。
- 以PICF24FJ256GB106為例,要設定為內部FRC要使用以下方法:

***#pragma config* FNOSC = FRC**

Oscillator Select

FNOSC = FRC	Fast RC Oscillator (FRC)
FNOSC = FRCPLL	Fast RC oscillator with Postscaler and PLL module (FRCPLL)
FNOSC = PRI	Primary oscillator (XT, HS, EC)
FNOSC = PRIPLL	Primary oscillator (XT, HS, EC) with PLL module (XTPLL,HSPLL, ECPLL)
FNOSC = SOSC	Secondary oscillator (SOSC)
FNOSC = LPRC	Low-Power RC oscillator (LPRC)
FNOSC = FRCDIV	Fast RC oscillator with Postscaler (FRCDIV)

REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend: r = Reserved bit
R = Readable bit PO = Program-once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) enabled
0 = IESO mode (Two-Speed Start-up) disabled

bit 14-12 **PLLDIV2:PLLDIV0:** USB 96 MHz PLL Prescaler Select bits
111 = Oscillator input divided by 12 (48 MHz input)
110 = Oscillator input divided by 10 (40 MHz input)
101 = Oscillator input divided by 6 (24 MHz input)
100 = Oscillator input divided by 5 (20 MHz input)
011 = Oscillator input divided by 4 (16 MHz input)
010 = Oscillator input divided by 3 (12 MHz input)
001 = Oscillator input divided by 2 (8 MHz input)
000 = Oscillator input used directly (4 MHz input)

bit 11 **Reserved:** Always maintain as '0'

bit 10-8 **FNOSC2:FNOSC0:** Initial Oscillator Select bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7-6 **FCKSM1:FCKSM0:** Clock Switching and Fail-Safe Clock Monitor Configuration bits

XC16 Configuration Bits的支援

- 要設定除錯介面，則使用以下方法設定:

  ***#pragma config* ICS = PGx1**

Watchdog Timer Enable

FWDTEN = OFF	Watchdog Timer is disabled
FWDTEN = ON	Watchdog Timer is enabled

Comm Channel Select

ICS = PGx3	Emulator functions are shared with PGEC3/PGED3
ICS = PGx2	Emulator functions are shared with PGEC2/PGED2
ICS = PGx1	Emulator functions are shared with PGEC1/PGED1

Set Clip On Emulation Mode

COE = ON	Enabled
COE = OFF	Disabled

Background Debug

BKBUG = ON	Device resets into Debug mode
BKBUG = OFF	Device resets into Operational mode

General Code Segment Write Protect

GWRP = ON	Writes to program memory are disabled
GWRP = OFF	Writes to program memory are allowed

General Code Segment Code Protect

GCP = ON	Code protection is enabled for the entire program memory space
GCP = OFF	Code protection is disabled

JTAG Port Enable

JTAGEN = OFF	JTAG port is disabled
JTAGEN = ON	JTAG port is enabled

REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
r	JTAGEN	GCP	GWRP	DEBUG	r	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:		r = Reserved bit
R = Readable bit	PO = Program Once bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed	'1' = Bit is set	'0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **Reserved:** The value is unknown; program as '0'

bit 14 **JTAGEN:** JTAG Port Enable bit[1]
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space

bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled

bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode

bit 10 **Reserved:** Always maintain as '1'

bit 9-8 **ICS1:ICS0:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use

bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled
0 = Watchdog Timer is disabled

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard Watchdog Timer enabled
0 = Windowed Watchdog Timer enabled; FWDTEN must be '1'

bit 5 **Unimplemented:** Read as '1'

bit 4 **FWPSA:** WDT Prescaler Ratio Select bit
1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

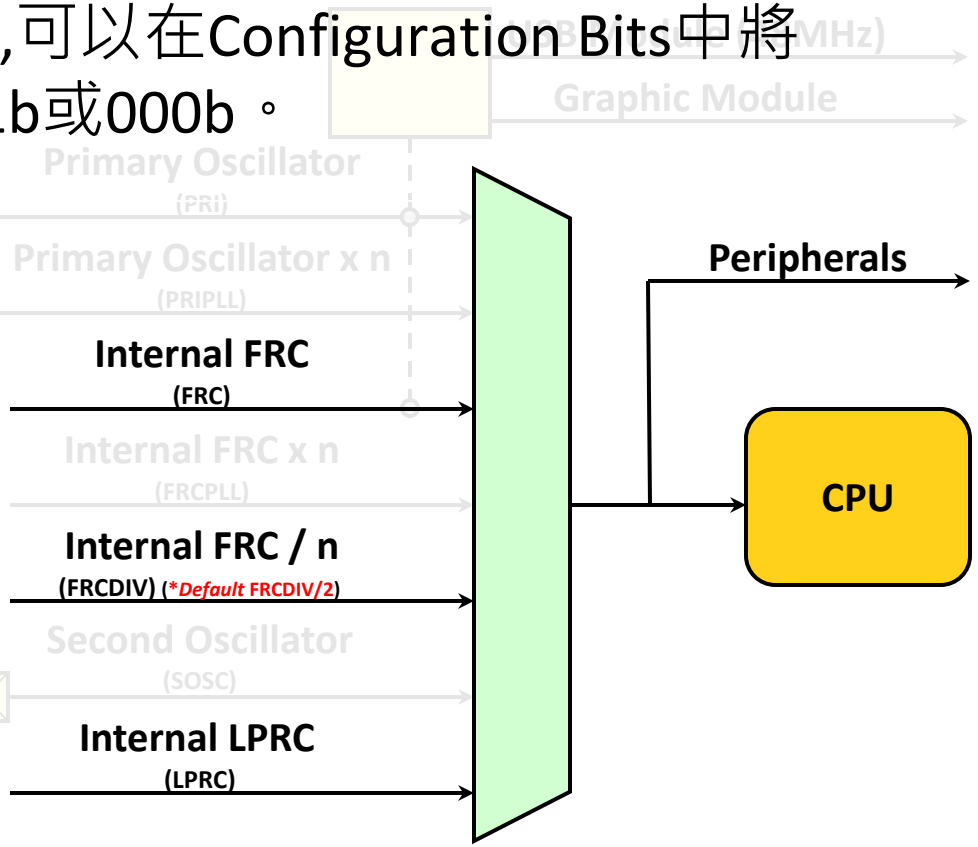
Clock Source (FRC, FRCDIV, LPRC)

- PIC24的Oscillator來源可以選擇使用內部FRC,內部FRC/n或Low Power RC。PIC24內部的FRC,工作頻率為8MHz, LPRC為31KHz。
- 要選擇使用內部FRC/LPRC時,可以在Configuration Bits中將FNOSC <2:0>設定為111b,101b或000b。

***#pragma config* FNOSC = FRC**
***#pragma config* FNOSC = FRCDIV**
***#pragma config* FNOSC = LPRC**

- **FNOSC預設FRCDIV(FRC/n, n(RCDIV)預設= 1 (/ 2)。**

bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
111	= Fast RC Oscillator with Postscaler (FRCDIV)
110	= Reserved
101	= Low-Power RC Oscillator (LPRC)
100	= Secondary Oscillator (SOSC)
011	= Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010	= Primary Oscillator (XT, HS, EC)
001	= Fast RC Oscillator with postscaler and PLL module (FRCPLL)
000	= Fast RC Oscillator (FRC)

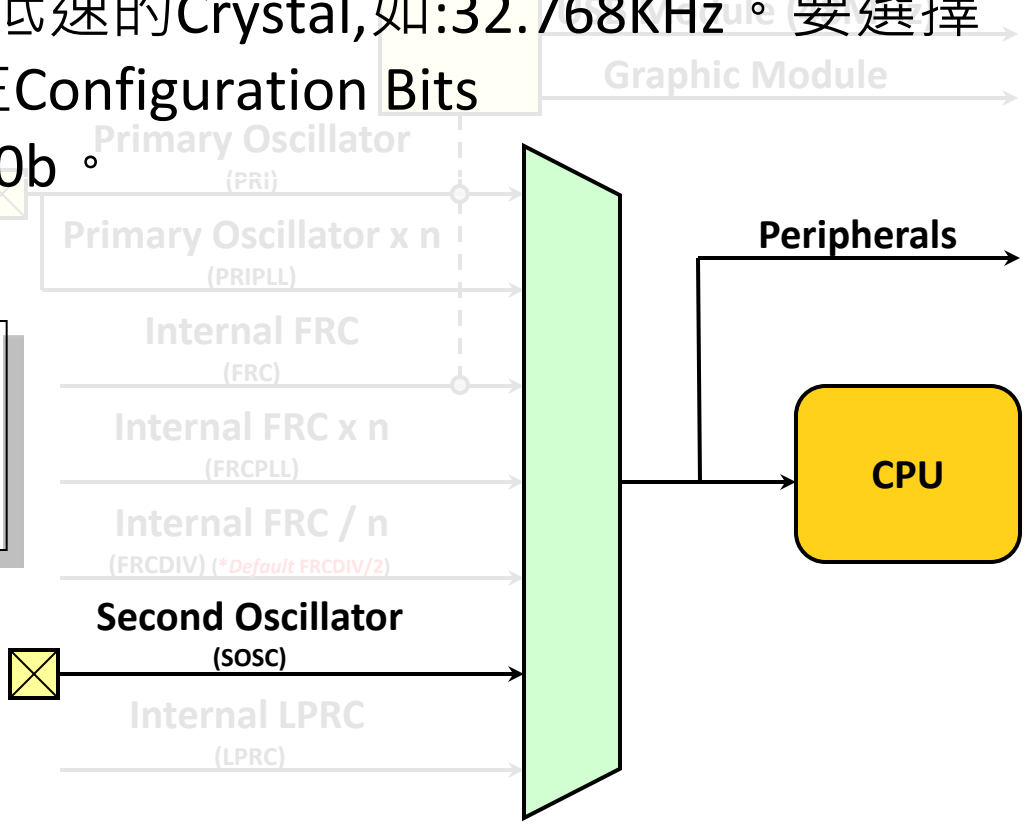


Clock Source (SOSC)

- PIC24的Oscillator來源也可以選擇透過外部的第二組時脈來源接腳(SOSC)取得。
- Second Osc.通常是用來接低速的Crystal,如:32.768KHz。要選擇使用Second Osc.時, 可以在Configuration Bits中將FNOSC<2:0>設定為100b。

***#pragma config* FNOSC = SOSC**

bit 10-8	**FNOSC2:FNOSC0:** Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



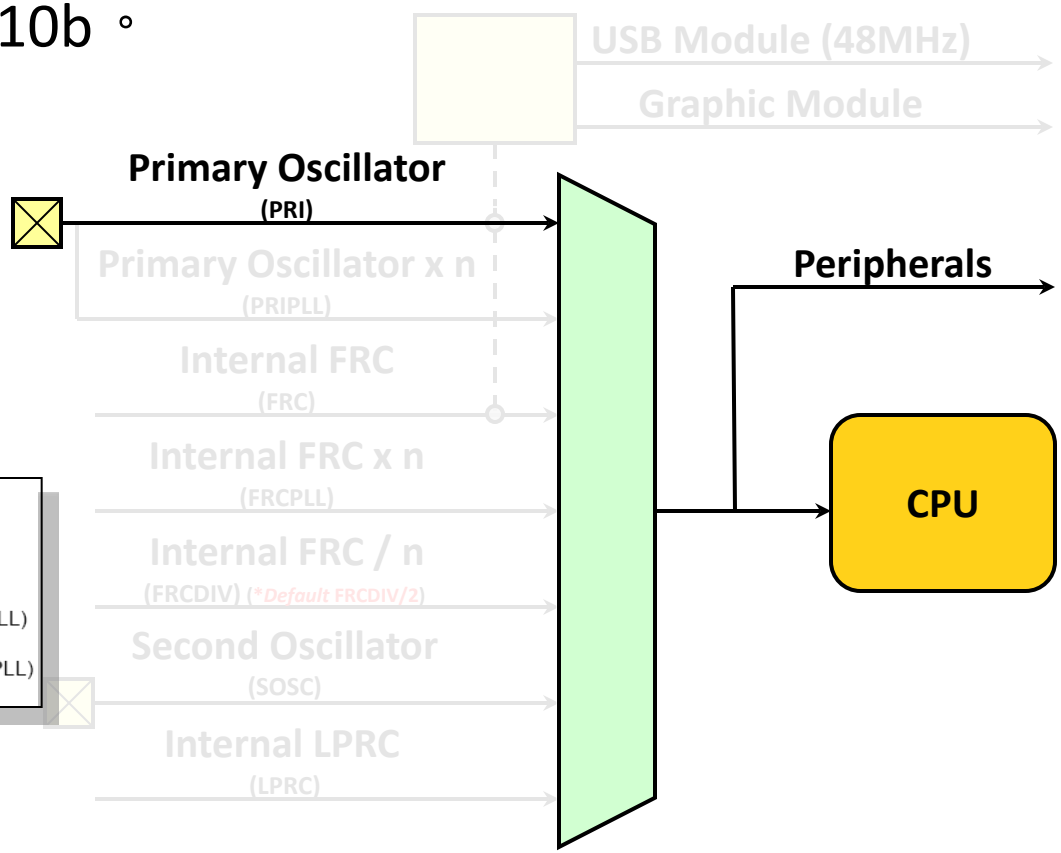
Clock Source (PRI)

- PIC24也可選擇透過外部取得時脈。直接使用Crystal的震盪頻率輸入。要選擇使用Primary Osc.時, 可以在Configuration Bits中將FNOSC<2:0>設定為010b。

  ***#pragma config* FNOSC = PRI**

- Primary Osc.通常是用來連接高速的Crystal。其最高的輸入頻率被限定在25MHz以下。

bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



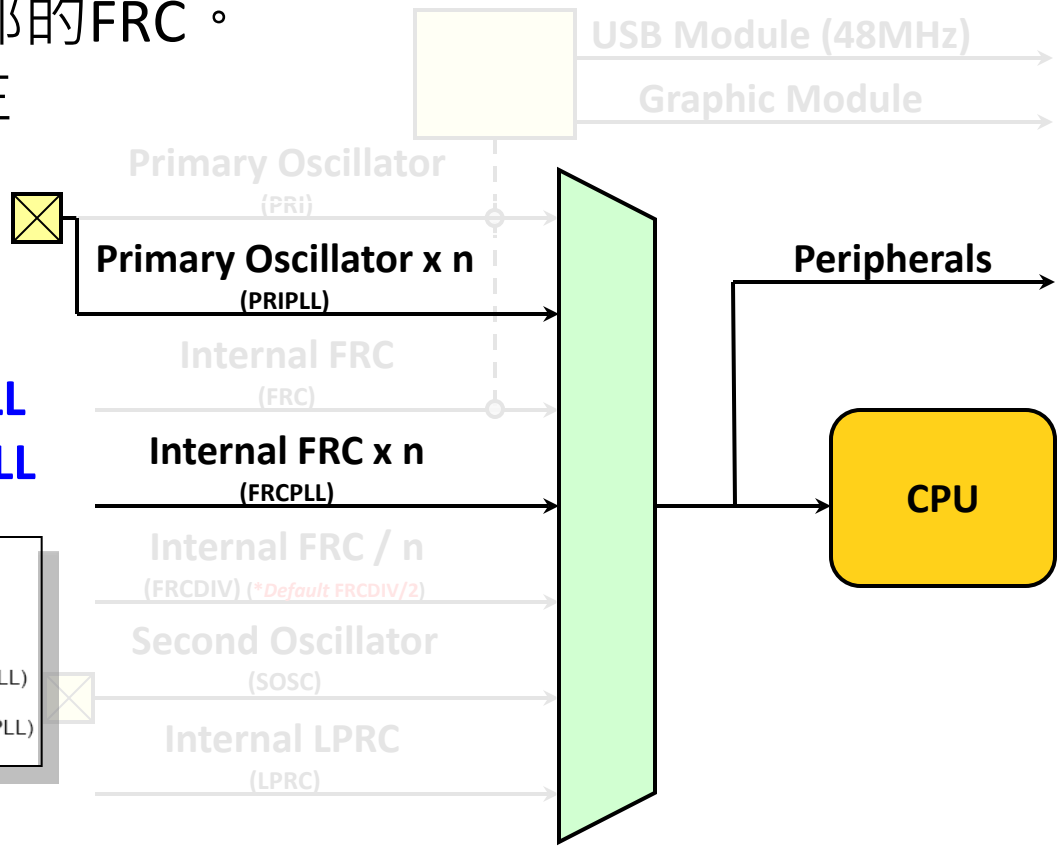
Clock Source (PRIPLL, FRCPLL)

- 除了以上幾種模式,大多數的PIC24應用, 都會透過內部的倍頻線路(PLL, Phase Locked Loop)來提高頻率。倍頻線路可以接受外部的震盪時脈或者內部的FRC。
  要選擇使用PLL時, 可以在Configuration Bits中將FNOSC<2:0>設定為011b或001b。

***#pragma config* FNOSC = PRIPLL**

***#pragma config* FNOSC = FRCPLL**

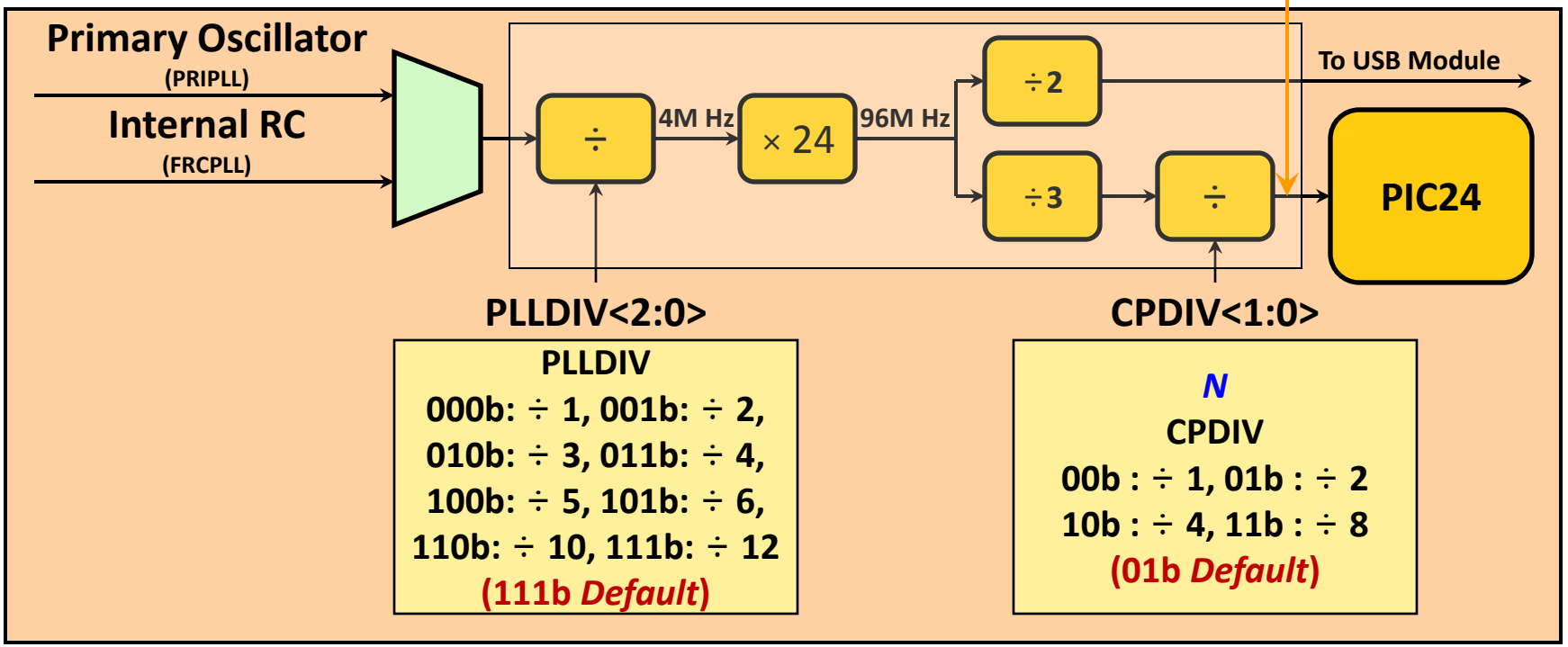
bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



Phase Locked Loop

- PLL的架構分為三個區塊:

$$F_{OSC} = \frac{\frac{96MHz}{3}}{N}$$



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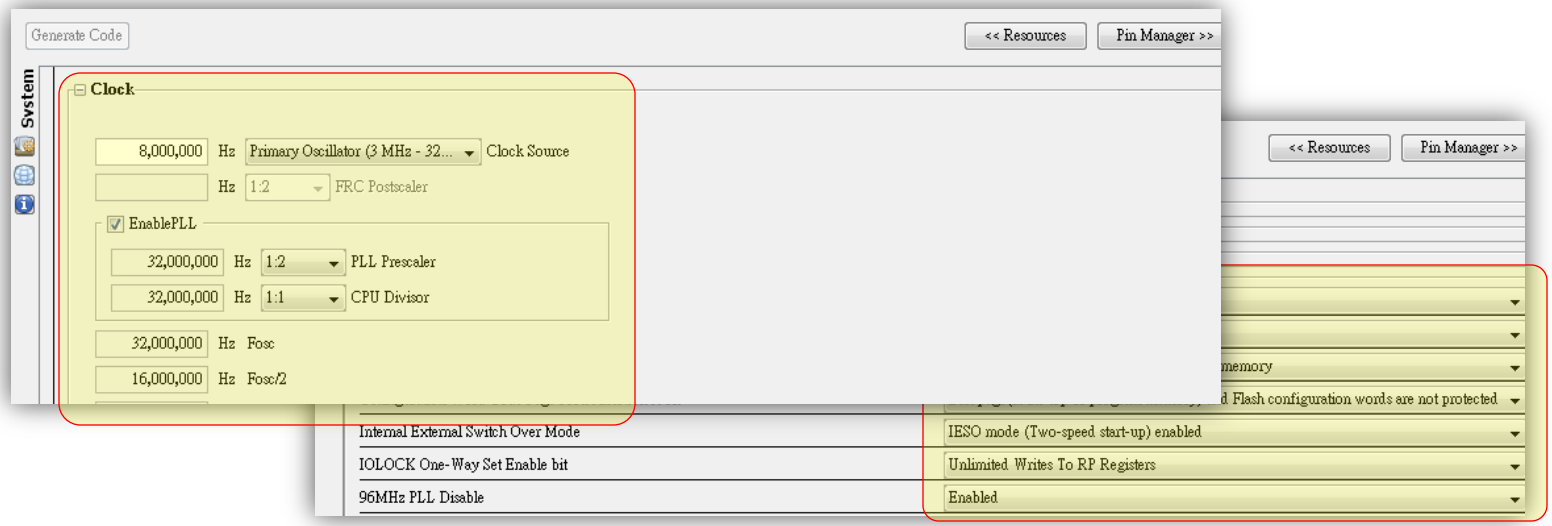
Configuration Bits Setting

- 以前我們要自己在程式中,加入各項Configuration Bits的設定。

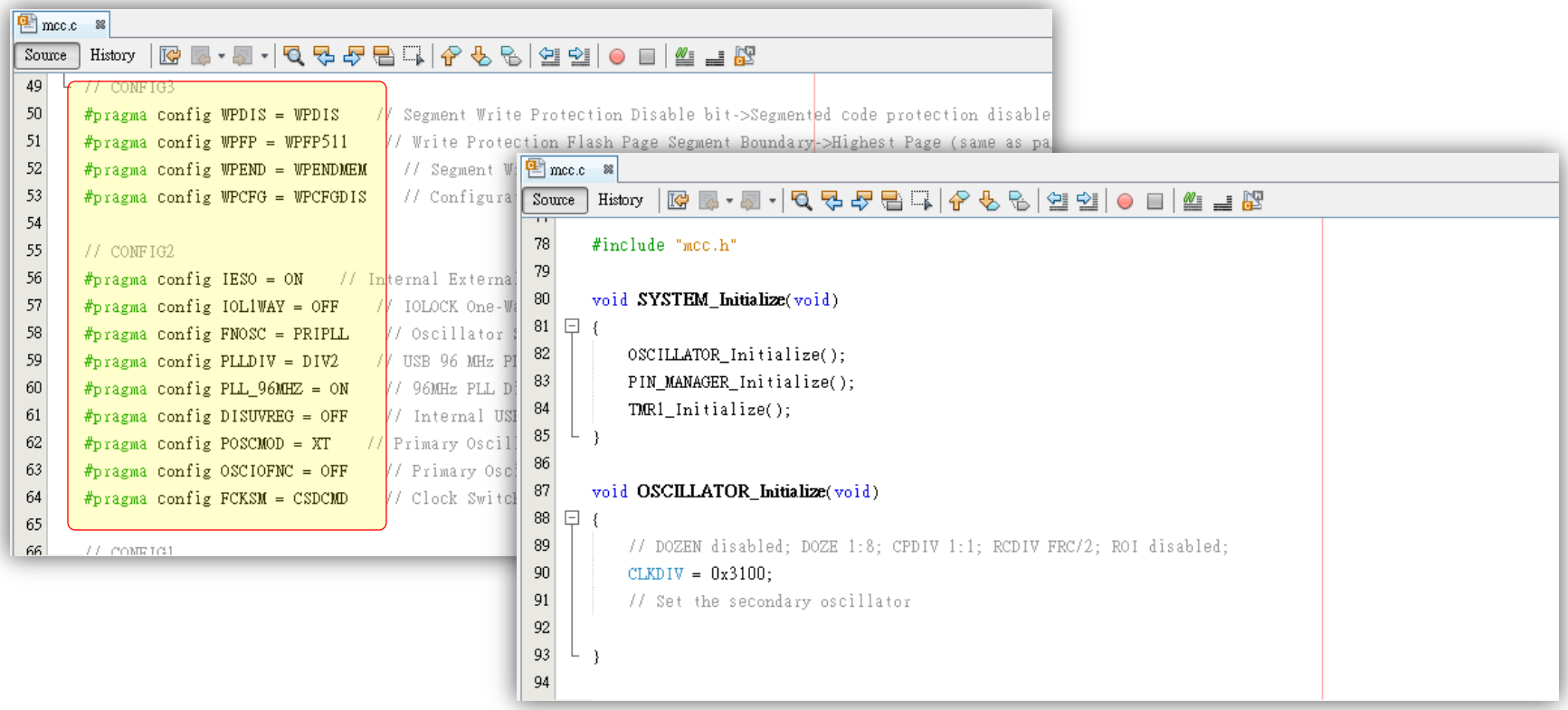
```
#pragma config FNOSC = PRIPLL
#pragma config PLLDIV = DIV2
#pragma config IESO = OFF
#pragma config ICS = PGx1
#pragma config JTAGEN = OFF
#pragma config …
```

- 現在, 透過MCC, 直接用點選的方式就能搞定。



MCC's
Configuration Bits Setting

- 執行 **Generate Code** 後, MCC會自動根據選擇, 產生各項Configuration Bits的設定。有些設定需要, 還需要使用程式填入式的的數值, 這部分MCC也會一併完成。



Lab4 – Timer1 Polling PRIPLL

目 標

- 嘗試透過MCC的設定, 改變系統時脈為主要外部時脈輸入(Primary Oscillator), 並設定PLL, 將系統頻率(F_{OSC})提高到32MHz。除錯介面設定為第一組(PGEC1/PGED1), JTAG Disable, Watchdog Disable。
- 系統頻率改變後, Timer的設定, 會跟著變動。請再透過MCC調整Lab4中Timer1的設定, 讓Timer1的週期改變成100mS。

- 該如何開始?

Lab4 – Timer1 Polling PRIPLL Step

- 開啟既有專案(C:\Exercises\Lab4 Timer1 Polling PRIPLL.x)
- 接著開啟開啟MCC, 修改**System**資源, 依照題目要求設定。
- **System**資源修改完成後, 觀察**Timer1**資源的變化, 並依照題目要求再次修改設定。

Lab4 – Timer1 Polling PRIPLL

MCC's Setting