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Section 8
Oscillator and Configuration Bit

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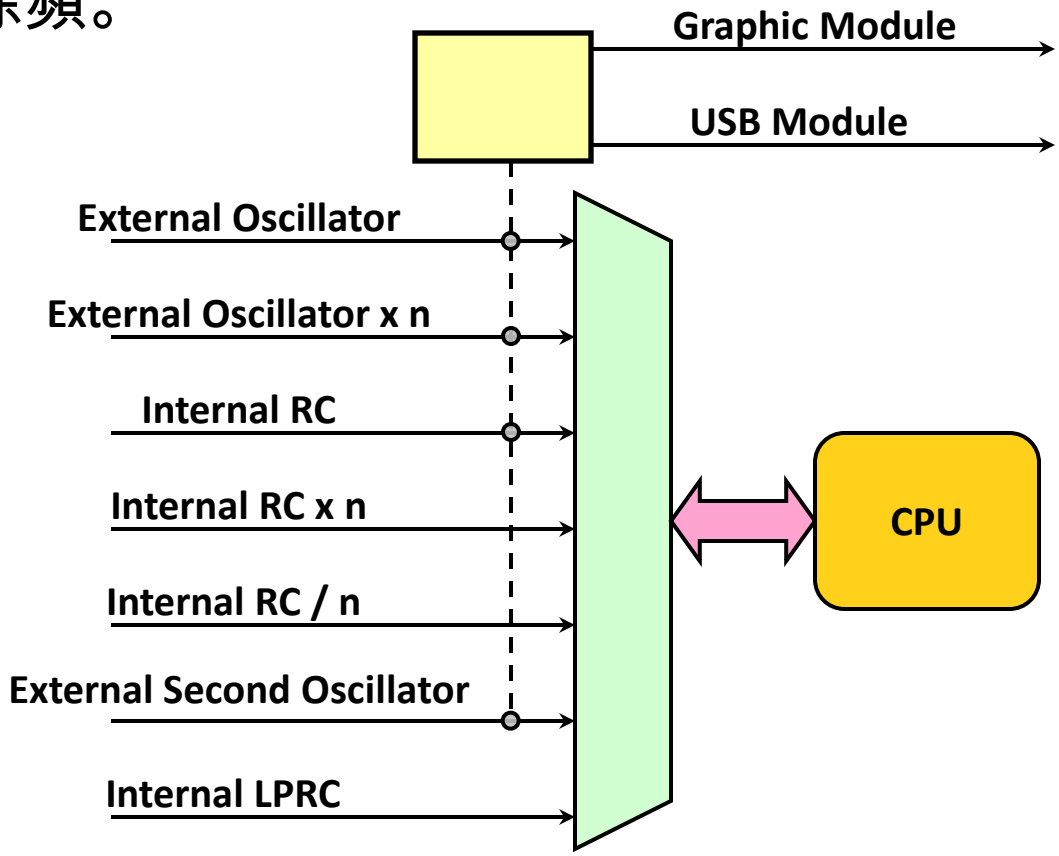
16-Bits MCU's Oscillator

- Microchip 16-Bits MCU具有多種時脈來源可選擇。可以使用內部RC或者外部的Crystal, Oscillator。輸入的時脈也可透過內部電路進行倍頻(PLL)或者除頻。
- 時脈來源的設定, 必須正確如果設定錯誤, CPU會接收到錯誤的頻率, 導致程式運作上的時序不對, 或者完全沒有接收到時脈, 導致CPU無法運作。
- 特定系列具有USB的模組及LCD的驅動模組, 時脈電路會更複雜。



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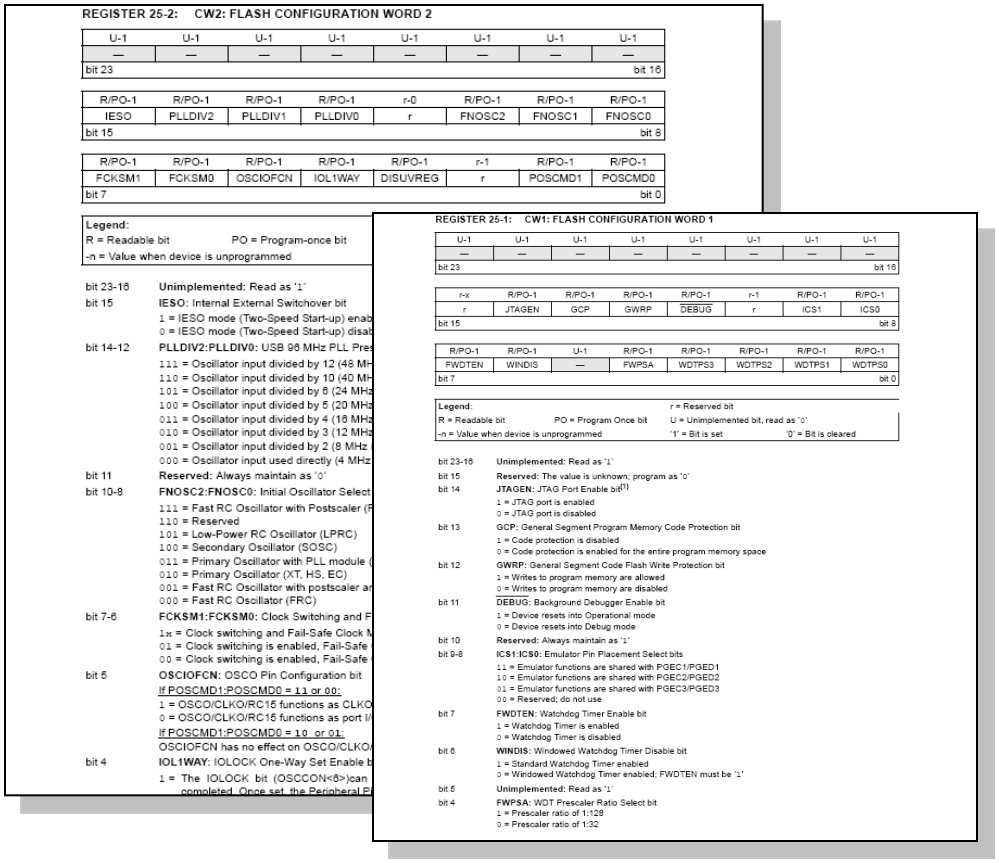
Configuration Bit

- Configuration Bit是用來設定MCU中一些重要的模式。其中包含如:CPU的時脈來源,除錯工具使用的接腳,Watchdog,程式碼保護,程式碼防寫等設定。
- 其中又以CPU的時脈來源,除錯工具使用的接腳設定最重要,時脈來源設定錯誤CPU無法正常運作,除錯工具使用的接腳設定錯誤,則無法使用硬體除錯工具。
- 參考Datasheet的Special Feature章節可以看到完整的說明。



REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend:
R = Readable bit PO = Program-once bit
-n = Value when device is unprogrammed

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) enab
0 = IESO mode (Two-Speed Start-up) disat
bit 14-12 **PLLDIV2:PLLDIV0:** USB 96 MHz PLL Pres
111 = Oscillator input divided by 12 (48 MH
110 = Oscillator input divided by 10 (40 MH
101 = Oscillator input divided by 6 (24 MHz
100 = Oscillator input divided by 5 (20 MHz
011 = Oscillator input divided by 4 (16 MHz
010 = Oscillator input divided by 3 (12 MHz
001 = Oscillator input divided by 2 (8 MHz
000 = Oscillator input used directly (4 MHz
bit 11 **Reserved:** Always maintain as '0'
bit 10-8 **FNOSC2:FNOSC0:** Initial Oscillator Select
111 = Fast RC Oscillator with Postscaler (F
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with postscaler ar
000 = Fast RC Oscillator (FRC)
bit 7-6 **FCKSM1:FCKSM0:** Clock Switching and F
1x = Clock switching and Fail-Safe Clock M
01 = Clock switching is enabled, Fail-Safe
00 = Clock switching is enabled, Fail-Safe
bit 5 **OSCIOFCN:** OSCO Pin Configuration bit
If POSCMD1:POSCMD0 = 11 or 00:
1 = OSCO/CLKO/RC15 functions as CLKO
0 = OSCO/CLKO/RC15 functions as port I/
If POSCMD1:POSCMD0 = 10 or 01:
OSCIOFCN has no effect on OSCO/CLKO
bit 4 **IOL1WAY:** IOLOCK One-Way Set Enable b
1 = The IOLOCK bit (OSCCON<6>)can
completed. Once set, the Peripheral Pi

REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
r	JTAGEN	GCP	GWRP	DEBUG	r	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend: r = Reserved bit
R = Readable bit PO = Program Once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **Reserved:** The value is unknown; program as '0'
bit 14 **JTAGEN:** JTAG Port Enable bit(1)
1 = JTAG port is enabled
0 = JTAG port is disabled
bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space
bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled
bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode
bit 10 **Reserved:** Always maintain as '1'
bit 9-8 **ICS1:ICS0:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use
bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled
0 = Watchdog Timer is disabled
bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard Watchdog Timer enabled
0 = Windowed Watchdog Timer enabled; FWDTEN must be '1'
bit 5 **Unimplemented:** Read as '1'
bit 4 **FWPSA:** WDT Prescaler Ratio Select bit
1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

C30 Configuration Bit的支援

- 不同系列的Configuration Bit設定方式是一樣的,但使用的Function Name不同。必須搭配參照Datasheet及MCU的標頭檔(p24fj256gb106.h)來設定。
- 以PICF24FJ256GB106為例,要設定為內部FRC要使用以下方法:
  _CONFIG2(*FNOSC_FRC* & … & IESO_OFF);

```
extern __attribute__((space(prog))) int _CONFIG2;
#define _CONFIG2(x) __attribute__((section("__CONFIG2.sec"),space(prog))) int _CONFIG2 = (x);
```

```
**  Oscillator Select.
**    FNOSC_FRC           Fast RC Oscillator (FRC)
**    FNOSC_FRCPLL        Fast RC oscillator with Postscaler and PLL module (FRCPLL)
**    FNOSC_PRI           Primary oscillator (XT, HS, EC)
**    FNOSC_PRIPLL        Primary oscillator (XT, HS, EC) with PLL module (XTPLL,HSPLL, ECPLL)
**    FNOSC_SOSC          Secondary oscillator (SOSC)
**    FNOSC_LPRC          Low-Power RC oscillator (LPRC)
**    FNOSC_FRCDIV        Fast RC oscillator with Postscaler (FRCDIV)
**
```

REGISTER 25-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-0	R/PO-1	R/PO-1	R/PO-1
IESO	PLLDIV2	PLLDIV1	PLLDIV0	r	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	DISUVREG	r	POSCMD1	POSCMD0
bit 7							bit 0

Legend: r = Reserved bit
R = Readable bit PO = Program-once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **IESO:** Internal External Switchover bit
1 = IESO mode (Two-Speed Start-up) enabled
0 = IESO mode (Two-Speed Start-up) disabled

PLLDIV2:PLLDIV0: USB 96 MHz PLL Prescaler Select bits
111 = Oscillator input divided by 12 (48 MHz input)
110 = Oscillator input divided by 10 (40 MHz input)
101 = Oscillator input divided by 6 (24 MHz input)
100 = Oscillator input divided by 5 (20 MHz input)
011 = Oscillator input divided by 4 (16 MHz input)
010 = Oscillator input divided by 3 (12 MHz input)
001 = Oscillator input divided by 2 (8 MHz input)
000 = Oscillator input used directly (4 MHz input)

Reserved: Always maintain as '0'

FNOSC2:FNOSC0: Initial Oscillator Select bits
111 = Fast RC Oscillator with Postscaler (FRCDIV)
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7-6 **FCKSM1:FCKSM0:** Clock Switching and Fail-Safe Clock Monitor Configuration bits

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C30 Configuration Bit的支援

- 要設定除錯介面，則使用以下方法設定:
  _CONFIG1(*ICS_PGD1* & … & JTAGEN_OFF);

```
extern __attribute__((space(prog))) int _CONFIG1;
#define _CONFIG1(x) __attribute__((section("__CONFIG1.sec"),space(prog))) int _CONFIG1 = (x);

/*
** Only one invocation of CONFIG1 should appear in a project,
** at the top of a C source file (outside of any function).
**
** The following constants can be used to set CONFIG1.
** Multiple options may be combined, as shown:
**
**     WDTPS_PS2            1:2
**     WDTPS_PS4            1:4
**
**   Comm Channel Select:
**     ICS_PGx3             Emulator functions are shared with PGEC3/PGED3
**     ICS_PGx2             Emulator functions are shared with PGEC2/PGED2
**     ICS_PGx1             Emulator functions are shared with PGEC1/PGED1
**
**     WDTPS_PS1024         1:1,024
**     WDTPS_PS2048         1:2,048
**     WDTPS_PS4096         1:4,096
**     WDTPS_PS8192         1:8,192
**     WDTPS_PS16384        1:16,384
**     WDTPS_PS32768        1:32,768
**
**   WDT Prescaler:
**     FWPSA_PR32           Prescaler ratio of 1:32
**     FWPSA_PR128          Prescaler ratio of 1:128
**
**   Watchdog Timer Window:
**     WINDIS_ON            Windowed Watchdog Timer enabled; FWDTEN must be 1
**     WINDIS_OFF           Standard Watchdog Timer enabled,(Windowed-mode is disabled)
**
**   Watchdog Timer Enable:
**     FWDTEN_OFF           Watchdog Timer is disabled
**     FWDTEN_ON            Watchdog Timer is enabled
**
```

REGISTER 25-1: CW1: FLASH CONFIGURATION WORD 1

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/PO-1	R/PO-1	R/PO-1	R/PO-1	r-1	R/PO-1	R/PO-1
r	JTAGEN	GCP	GWRP	DEBUG	r	ICS1	ICS0
bit 15							bit 8

R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	WINDIS	—	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

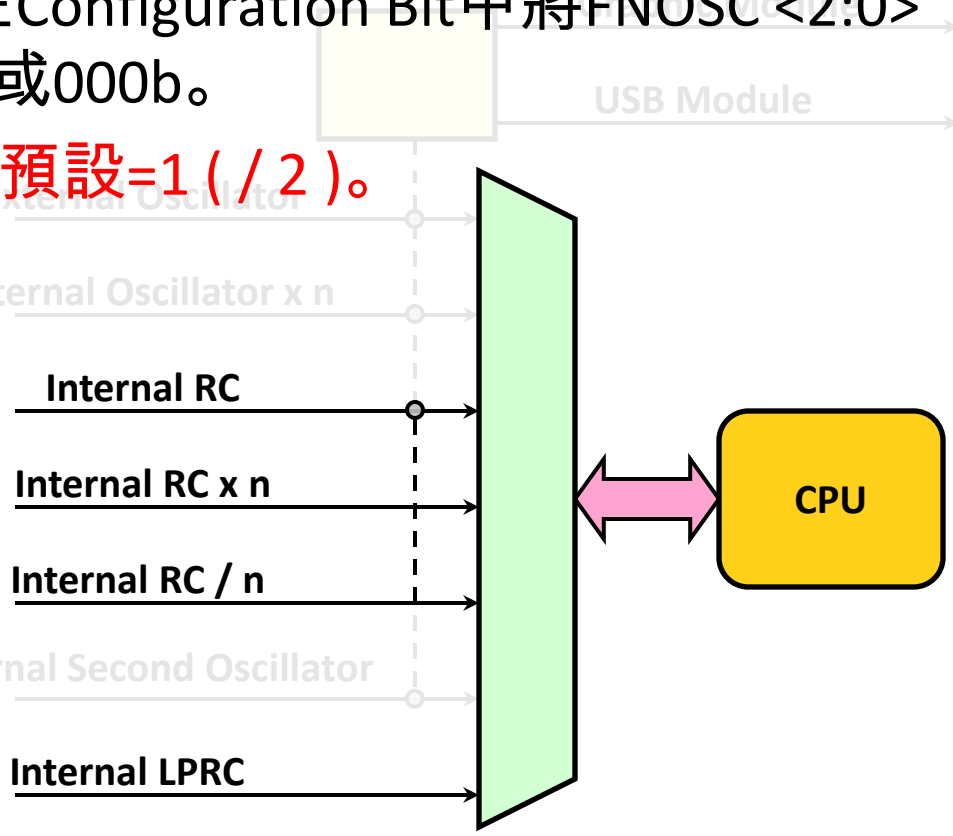
Legend: r = Reserved bit
R = Readable bit PO = Program Once bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed '1' = Bit is set '0' = Bit is cleared

bit 23-16 **Unimplemented:** Read as '1'
bit 15 **Reserved:** The value is unknown; program as '0'
bit 14 **JTAGEN:** JTAG Port Enable bit(1)
1 = JTAG port is enabled
0 = JTAG port is disabled
bit 13 **GCP:** General Segment Program Memory Code Protection bit
1 = Code protection is disabled
0 = Code protection is enabled for the entire program memory space
bit 12 **GWRP:** General Segment Code Flash Write Protection bit
1 = Writes to program memory are allowed
0 = Writes to program memory are disabled
bit 11 **DEBUG:** Background Debugger Enable bit
1 = Device resets into Operational mode
0 = Device resets into Debug mode
bit 10 **Reserved:** Always maintain as '1'
bit 9-8 **ICS1:ICS0:** Emulator Pin Placement Select bits
11 = Emulator functions are shared with PGEC1/PGED1
10 = Emulator functions are shared with PGEC2/PGED2
01 = Emulator functions are shared with PGEC3/PGED3
00 = Reserved; do not use
bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled
0 = Watchdog Timer is disabled
bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard Watchdog Timer enabled
0 = Windowed Watchdog Timer enabled; FWDTEN must be '1'
bit 5 **Unimplemented:** Read as '1'
bit 4 **FWPSA:** WDT Prescaler Ratio Select bit
1 = Prescaler ratio of 1:128
0 = Prescaler ratio of 1:32

Clock Source (FRC,LPRC)

- PIC24的Oscillator來源可以選擇使用內部RC,內部RC/n或Low Power RC。PIC24內部的FRC,工作頻率為8MHz, LPRC為31KHz。
- 要選擇使用內部RC時,可以在Configuration Bit中將FNOSC <2:0> 設定為111b,110b,101b,001b或000b。
- FNOSC預設FRC/n 。n(RCDIV)預設=1 (/ 2)。Lab0,1,2,3都是使用FRC/1 。

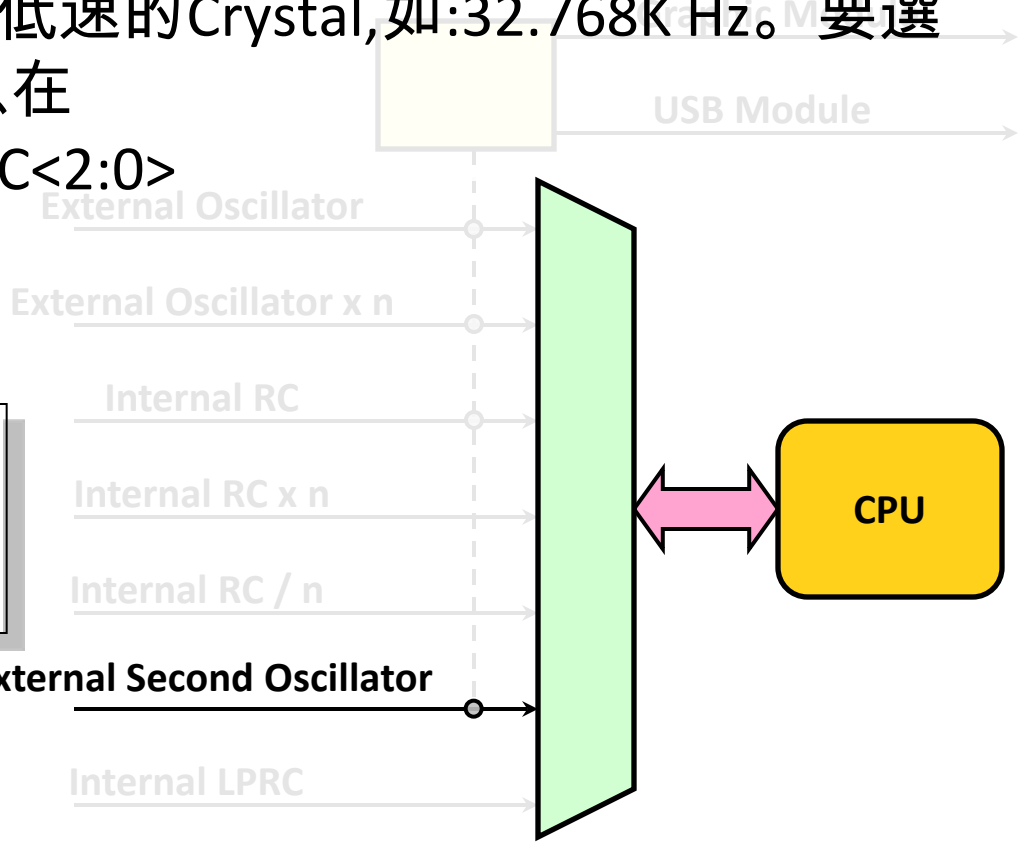
bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



Clock Source (Second OSC.)

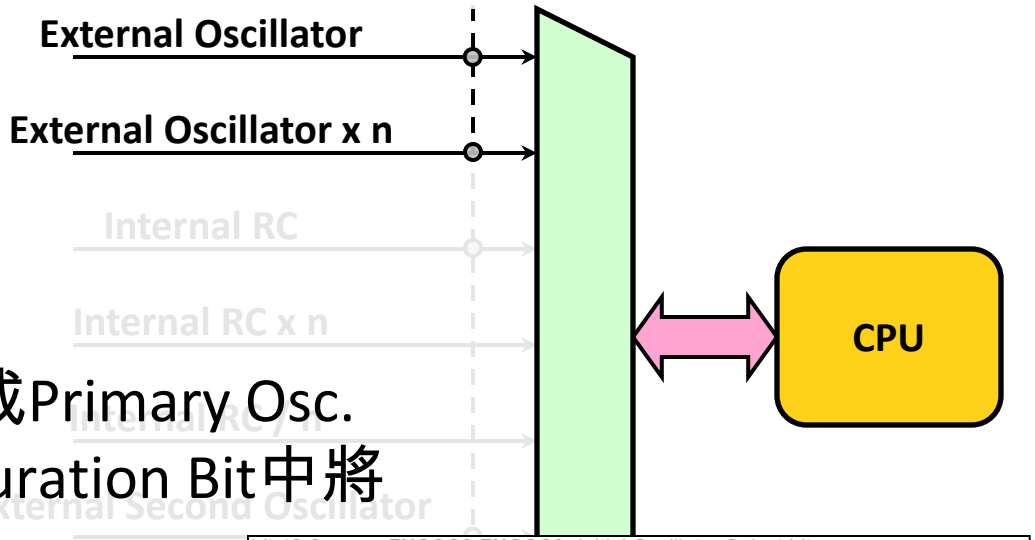
- PIC24的Oscillator來源也可以選擇透過外部的第二組時脈來源接腳(SOSC)取得。
- Second OSC.通常是用來接低速的Crystal,如:32.768K Hz。要選擇使用Second OSC.時,可以在Configuration Bit中將FNOSC<2:0>設定為100b。

bit 10-8	**FNOSC2:FNOSC0**: Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)



Clock Source (External OSC.)

- 除了以上幾種模式,PIC24也可選擇透過外部的時脈來源接腳取得(OSC)。可以選擇使用直接使用Crystal的頻率的Primary Osc. Mode(011b),或將Crystal經過PLL倍頻的Primary Osc. With PLL Mode(010b)。
- Primary Osc.通常是用來連接高速的Crystal。其最高的輸入頻率被限定在48MHz以下。
- 要選擇使用Primary Osc.或Primary Osc. With PLL時,可以在Configuration Bit中將FNOSC<2:0>設定為010b或011b。

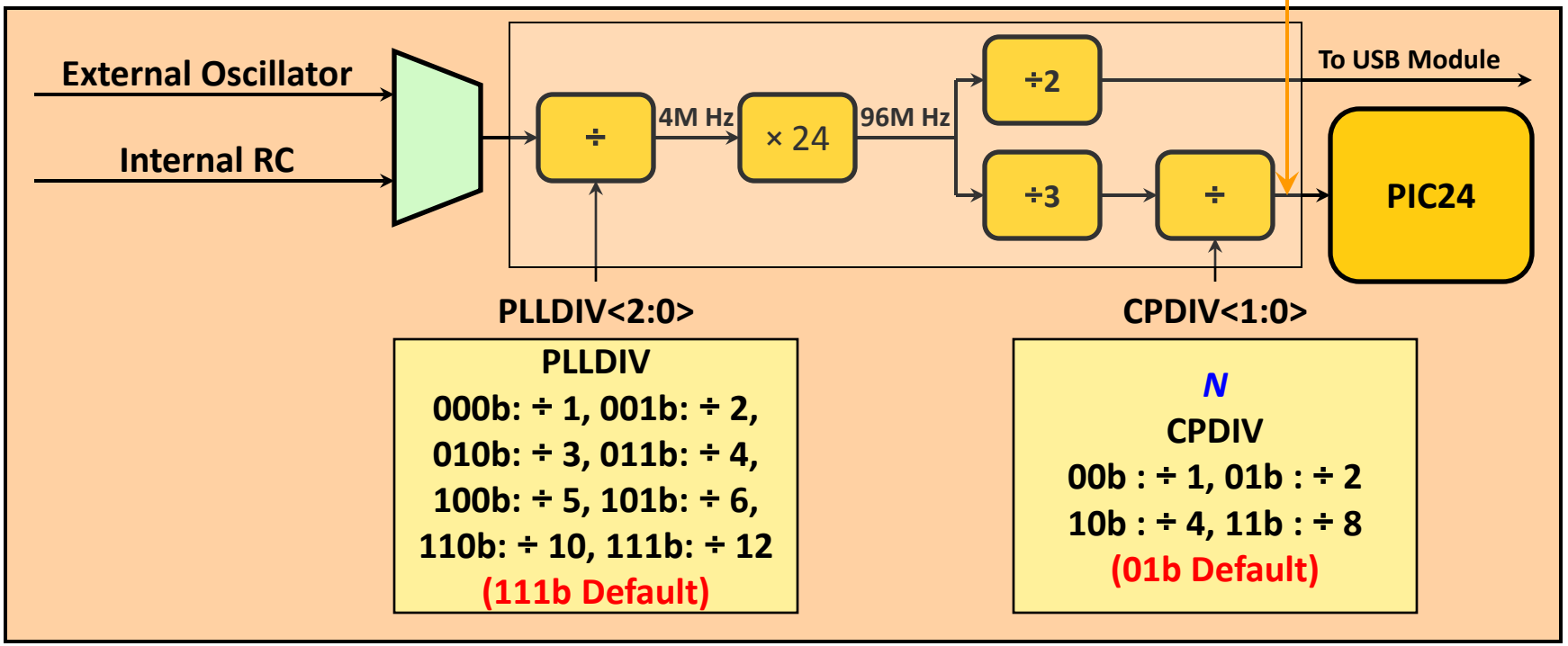


bit 10-8	**FNOSC2:FNOSC0:** Initial Oscillator Select bits
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	110 = Reserved
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XT, HS, EC)
	001 = Fast RC Oscillator with postscaler and PLL module (FRCPLL)
	000 = Fast RC Oscillator (FRC)

Phase Locked Loop

- PIC24的可以透過PLL線路,提高供給CPU的頻率(FOSC)。
- Primary Osc.跟FRC可以透過PLL線路倍頻。
- PLL的架構分為三個區塊:

$$F_{OSC} = \frac{\frac{96MHz}{3}}{N}$$



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Lab5 Configuration Bit

- 以Lab4的程式為基礎,利用MPLAB C30提供的Configuration Bits來設定Configuration Bits。將CPU時脈來源轉為Primary Osc. With PLL。CPU的工作時脈則調整為32 MHz(Fosc) ,除錯腳位設為第一組,關閉WDT,啟動時脈切換且關閉時脈監視(CSECMD)。

  Ex:

  ```
  _CONFIG1( … & … );
  _CONFIG2( … & … );
  _CONFIG3( … & … );
  ```

- 正確設定CPDIV<1:0>,讓CPU可以正常運作在32 MHz(Primary Osc. With PLL Mode)。
- 調整程式中,Timer1的設定,讓Timer1的中斷一樣維持500mS。並將程式實際燒錄到MCU中,用肉眼觀察看看程式執行的情況。

Lab5 Configuration Bit Step

- 工作頻率變快了, Timer計數值裝不下怎麼辦?

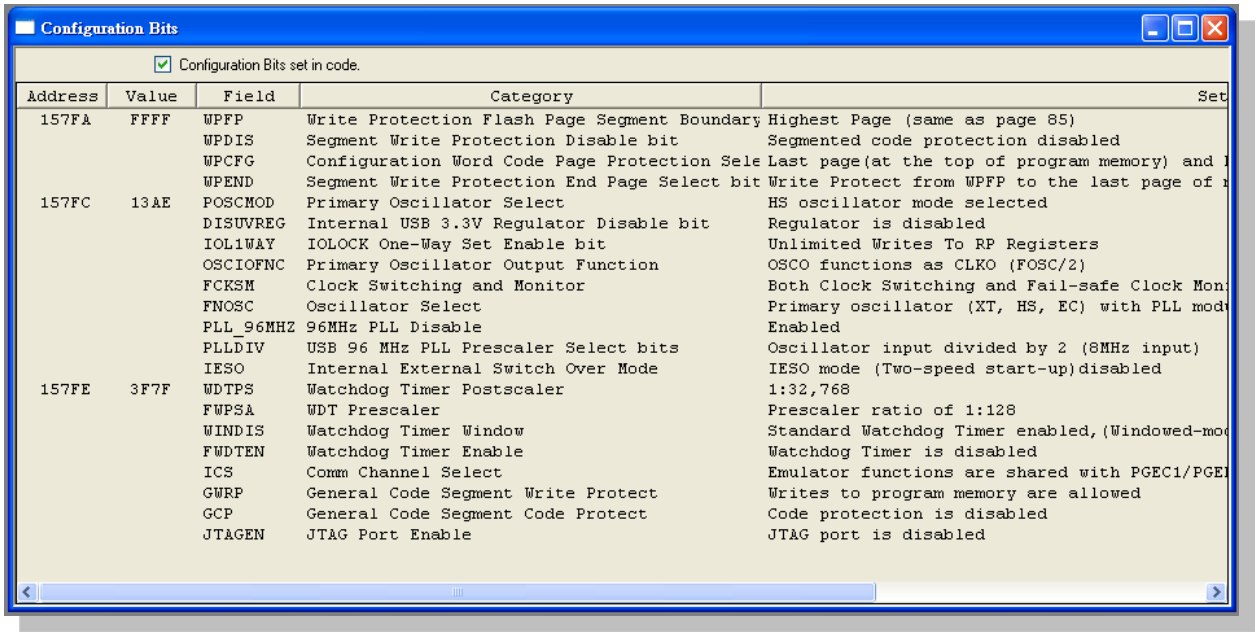
  搭配軟體技巧的手段來處理。

  Ex:

```
void __attribute__( ( interrupt , auto_psv ) ) _T1Interrupt( void ) // 100mS
{
   static unsigned int T1Tick = 0;
   IFS0bits.T1IF = 0;
   if( ++T1Tick > 4 )
   {
      T1Tick = 0;            // 500mS
       .....
   }
}
```

Configuration Bits Window

- MPLAB IDE中,功能表\Configure\Configuration Bits。也可以設定Configuration Bits。GUI的設定比較容易操作,但須注意!如果程式中跟此處有衝突時,依程式中的設定為主。
- 程式中的設定,也會反映到此處,可以觀察此視窗來確認設定是否正確。



Address	Value	Field	Category	Set
157FA	FFFF	WPFP	Write Protection Flash Page Segment Boundary	Highest Page (same as page 85)
		WPDIS	Segment Write Protection Disable bit	Segmented code protection disabled
		WPCFG	Configuration Word Code Page Protection Sele	Last page(at the top of program memory) and
		WPEND	Segment Write Protection End Page Select bit	Write Protect from WPFP to the last page of
157FC	13AE	POSCMOD	Primary Oscillator Select	HS oscillator mode selected
		DISUVREG	Internal USB 3.3V Regulator Disable bit	Regulator is disabled
		IOL1WAY	IOLOCK One-Way Set Enable bit	Unlimited Writes To RP Registers
		OSCIOFNC	Primary Oscillator Output Function	OSCO functions as CLKO (FOSC/2)
		FCKSM	Clock Switching and Monitor	Both Clock Switching and Fail-safe Clock Mon
		FNOSC	Oscillator Select	Primary oscillator (XT, HS, EC) with PLL mod
		PLL_96MHZ	96MHz PLL Disable	Enabled
		PLLDIV	USB 96 MHz PLL Prescaler Select bits	Oscillator input divided by 2 (8MHz input)
		IESO	Internal External Switch Over Mode	IESO mode (Two-speed start-up)disabled
157FE	3F7F	WDTPS	Watchdog Timer Postscaler	1:32,768
		FWPSA	WDT Prescaler	Prescaler ratio of 1:128
		WINDIS	Watchdog Timer Window	Standard Watchdog Timer enabled,(Windowed-mo
		FWDTEN	Watchdog Timer Enable	Watchdog Timer is disabled
		ICS	Comm Channel Select	Emulator functions are shared with PGEC1/PGE
		GWRP	General Code Segment Write Protect	Writes to program memory are allowed
		GCP	General Code Segment Code Protect	Code protection is disabled
		JTAGEN	JTAG Port Enable	JTAG port is disabled