



MICROCHIP

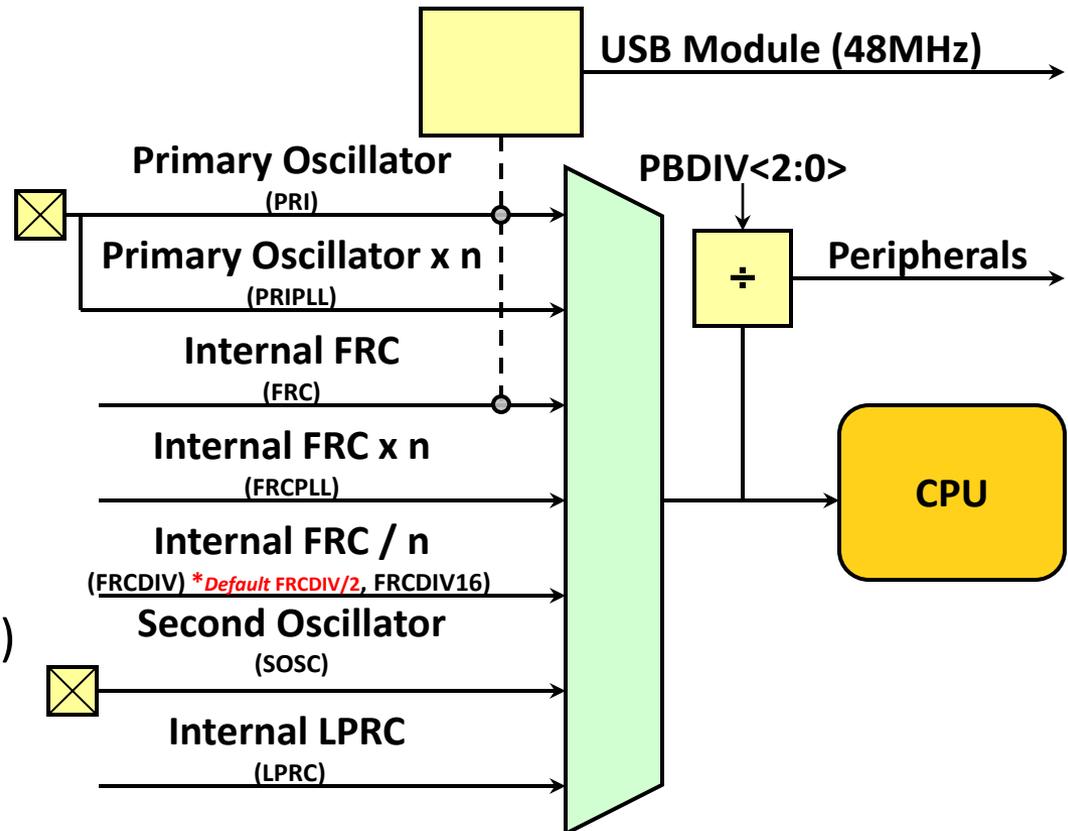
Regional Training Centers

Section 6

Oscillator and Configuration Bits

PIC32MX Oscillator Architecture

- PIC32具有多種時脈來源可選擇。可以使用內部RC或者外部的Crystal, Oscillator。輸入的時脈也可透過內部電路進行倍頻(PLL)或者除頻。
- 時脈來源的設定, 必須正確。如果設定錯誤, CPU會接收到錯誤的頻率, 導致程式運作上的時序不正確。或者完全無法運作。
- 三組時脈, 分別提供
 - CPU
 - 周邊模組(Timer, ADC, etc..)
 - USB模組使用。





MICROCHIP

Regional Training Centers

Configuration Bit

- Configuration Bit是用來設定MCU中一些重要的模式。其中包含如:CPU的時脈來源, 除錯工具使用的接腳, Watchdog, 程式碼保護, 程式碼防寫等設定。
- 其中又以CPU的時脈來源, 除錯工具使用的接腳設定最重要, 時脈來源設定錯誤CPU無法正常運作, 除錯工具使用的接腳設定錯誤, 則無法使用硬體除錯工具。
- 參考Datasheet的Special Feature章節可以看到完整的說明。

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	R-P	R-P
23:16	R-P	---	---	---	---	---	---	---	FWDTWINSZ<1:0>
15:8	R-P	R-P	R-P	R-P	R-P	r-1	---	---	---
7:0	R-P	r-1	R-P	r-1	r-1	---	---	---	---
	IESO	---	FSOSCEN	---	---	---	---	---	---

REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2									
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	R-P	R-P	R-P	R-P	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	R-P	R-P	R-P	R-P
15:8	R-P	R-P	R-P	R-P	R-P	R-P	R-P	R-P	FSRSSEL<2:0>
7:0	R-P	R-P	R-P	R-P	R-P	R-P	R-P	R-P	USERID<7:0>

REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	R-P	R-P	R-P	R-P
23:16	U-0	U-0	U-0	U-0
15:8	R-P	R-P	R-P	R-P
7:0	R-P	R-P	R-P	R-P

REGISTER 27-5: DEVCFG4: DEVICE CONFIGURATION WORD 4				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	R-P	r-1	---	---
7:0	---	---	---	FLLM

REGISTER 27-6: DEVCFG5: DEVICE CONFIGURATION WORD 5				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	UPLLEN ⁽¹⁾	---	---	---
7:0	r-1	R-P-1	---	R

REGISTER 27-7: DEVCFG6: DEVICE CONFIGURATION WORD 6				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-8: DEVCFG7: DEVICE CONFIGURATION WORD 7				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-9: DEVCFG8: DEVICE CONFIGURATION WORD 8				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-10: DEVCFG9: DEVICE CONFIGURATION WORD 9				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-11: DEVCFG10: DEVICE CONFIGURATION WORD 10				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-12: DEVCFG11: DEVICE CONFIGURATION WORD 11				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-13: DEVCFG12: DEVICE CONFIGURATION WORD 12				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-14: DEVCFG13: DEVICE CONFIGURATION WORD 13				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-15: DEVCFG14: DEVICE CONFIGURATION WORD 14				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-16: DEVCFG15: DEVICE CONFIGURATION WORD 15				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-17: DEVCFG16: DEVICE CONFIGURATION WORD 16				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-18: DEVCFG17: DEVICE CONFIGURATION WORD 17				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-19: DEVCFG18: DEVICE CONFIGURATION WORD 18				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-20: DEVCFG19: DEVICE CONFIGURATION WORD 19				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-21: DEVCFG20: DEVICE CONFIGURATION WORD 20				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-22: DEVCFG21: DEVICE CONFIGURATION WORD 21				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-23: DEVCFG22: DEVICE CONFIGURATION WORD 22				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-24: DEVCFG23: DEVICE CONFIGURATION WORD 23				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-25: DEVCFG24: DEVICE CONFIGURATION WORD 24				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-26: DEVCFG25: DEVICE CONFIGURATION WORD 25				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-27: DEVCFG26: DEVICE CONFIGURATION WORD 26				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-28: DEVCFG27: DEVICE CONFIGURATION WORD 27				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-29: DEVCFG28: DEVICE CONFIGURATION WORD 28				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-30: DEVCFG29: DEVICE CONFIGURATION WORD 29				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-31: DEVCFG30: DEVICE CONFIGURATION WORD 30				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-32: DEVCFG31: DEVICE CONFIGURATION WORD 31				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-33: DEVCFG32: DEVICE CONFIGURATION WORD 32				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-34: DEVCFG33: DEVICE CONFIGURATION WORD 33				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-35: DEVCFG34: DEVICE CONFIGURATION WORD 34				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-36: DEVCFG35: DEVICE CONFIGURATION WORD 35				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4
31:24	r-1	r-1	r-1	r-1
23:16	---	---	---	---
15:8	---	---	---	---
7:0	---	---	---	FLLM

REGISTER 27-37: DEVCFG36: DEVICE CONFIGURATION WORD 36				
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit

XC32 Configuration Bits Function

- 不同系列的Configuration Bits設定方式是一樣的,但使用的Function Name不同。必須搭配參照Datasheet及XC32的說明文件來設定。
- 以PIC32MX470F512H為例,要設定為時脈來源為內部FRC可使用以下方法:
#pragma config FNOSC = FRC

REGISTER 27-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 15-14 **FCKSM<1:0>**: Clock Switching and Monitor Selection Configuration bits
 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>**: Peripheral Bus Clock Divisor Default Value bits
 11 = PBCLK is SYSCLK divided by 8
 10 = PBCLK is SYSCLK divided by 4
 01 = PBCLK is SYSCLK divided by 2
 00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved: Write '1'**

bit 10 **OSCI0FNC**: CLK0 Enable Configuration bit
 1 = CLK0 output disabled
 0 = CLK0 output signal active on the OSC0 pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLK0 to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>**: Primary Oscillator Configuration bits
 11 = Primary Oscillator disabled
 10 = HS Oscillator mode selected
 01 = XT Oscillator mode selected
 00 = External Clock mode selected

bit 7 **IESO**: Internal External Switchover bit
 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved: Write '1'**

bit 5 **FSOSCEN**: Secondary Oscillator Enable bit
 1 = Enable Secondary Oscillator
 0 = Disable Secondary Oscillator

bit 4-3 **Reserved: Write '1'**

bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits
 111 = Fast RC Oscillator with divide-by-N (FRCDIV)
 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
 101 = Low-Power RC Oscillator (LPRC)
 100 = Secondary Oscillator (SOSC)
 011 = Primary Oscillator (POSC) with PLL module (XT+PLL, HS+PLL, EC+PLL)
 010 = Primary Oscillator (XT, HS, EC)⁽¹⁾
 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
 000 = Fast RC Oscillator (FRC)

Note 1: Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

XC32 Configuration Bits Function

- MPLAB XC32 可以在程式碼中使用特殊關鍵字 `#pragma config` 來設定 Configuration Bit。

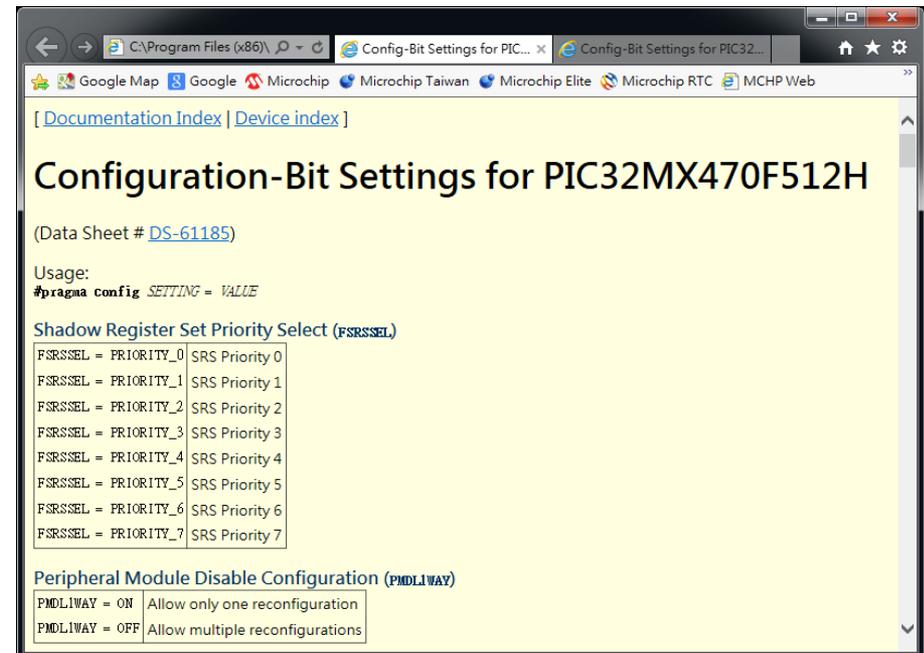
利用 `#pragma config` 在程式裡來設定, 語法如下例所示:

```
#pragma config UPLLDIV = DIV_2 , UPLEN = ON
```

```
#pragma config FPLLDIV = DIV_2 , FPLLMUL = MUL_20 , FPLLODIV = DIV_1
```

- `config` 的有效定義字與意義可參考說明文件:

C:\Program Files (x86)\Microchip\xc32\
v1.32\docs\config_docs\32mx470f512h.html



Configuration-Bit Settings for PIC32MX470F512H
(Data Sheet # [DS-61185](#))

Usage:
`#pragma config SETTING = VALUE`

Shadow Register Set Priority Select (FSRSSEL)

FSRSSEL = PRIORITY_0	SRS Priority 0
FSRSSEL = PRIORITY_1	SRS Priority 1
FSRSSEL = PRIORITY_2	SRS Priority 2
FSRSSEL = PRIORITY_3	SRS Priority 3
FSRSSEL = PRIORITY_4	SRS Priority 4
FSRSSEL = PRIORITY_5	SRS Priority 5
FSRSSEL = PRIORITY_6	SRS Priority 6
FSRSSEL = PRIORITY_7	SRS Priority 7

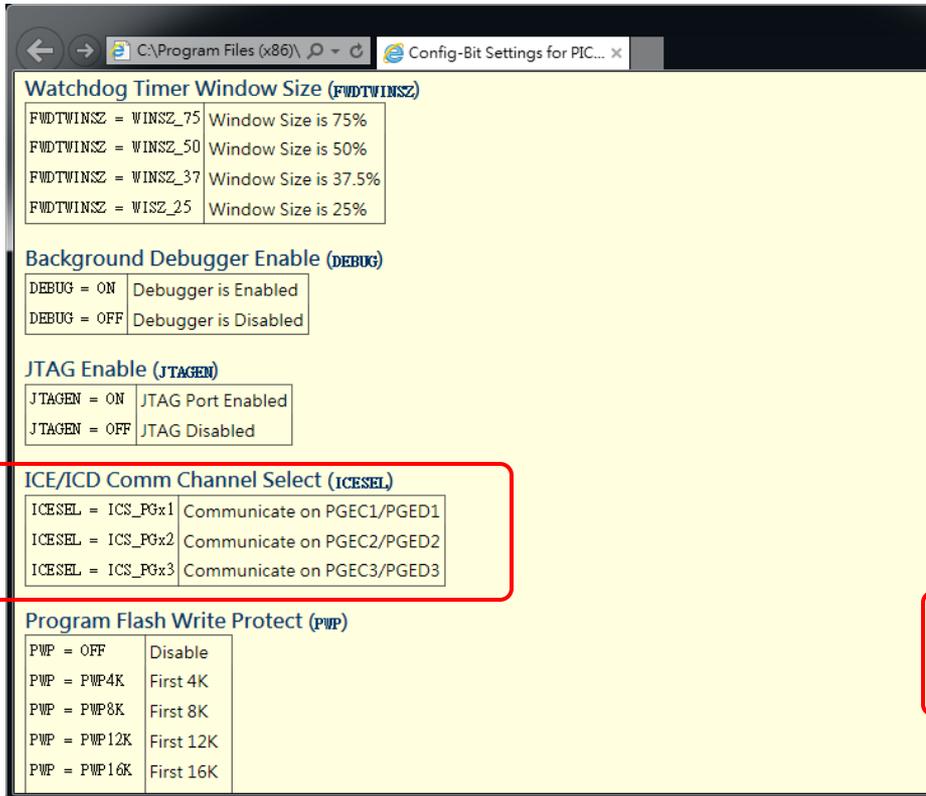
Peripheral Module Disable Configuration (PMDLIWAY)

PMDLIWAY = ON	Allow only one reconfiguration
PMDLIWAY = OFF	Allow multiple reconfigurations

XC32 Configuration Bits Function

- 要設定除錯介面，則使用以下方法設定：

#pragma config ICESEL = ICS_PGx1



Watchdog Timer Window Size (FWDTWINSZ)

FWDTWINSZ = WINSZ_75	Window Size is 75%
FWDTWINSZ = WINSZ_50	Window Size is 50%
FWDTWINSZ = WINSZ_37	Window Size is 37.5%
FWDTWINSZ = WINSZ_25	Window Size is 25%

Background Debugger Enable (DEBUG)

DEBUG = ON	Debugger is Enabled
DEBUG = OFF	Debugger is Disabled

JTAG Enable (JTAGEN)

JTAGEN = ON	JTAG Port Enabled
JTAGEN = OFF	JTAG Disabled

ICE/ICD Comm Channel Select (ICESEL)

ICESEL = ICS_PGx1	Communicate on PGEC1/PGED1
ICESEL = ICS_PGx2	Communicate on PGEC2/PGED2
ICESEL = ICS_PGx3	Communicate on PGEC3/PGED3

Program Flash Write Protect (PWP)

PWP = OFF	Disable
PWP = PWP4K	First 4K
PWP = PWP8K	First 8K
PWP = PWP12K	First 12K
PWP = PWP16K	First 16K

REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 24 **BWP**: Boot Flash Write-Protect bit
Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved**: Write '1'

bit 19-12 **PWP<7:0>**: Program Flash Write-Protect bits
Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.
11111111 = Disabled
11111110 = 0xBD00_0FFF
11111101 = 0xBD00_1FFF
11111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
11111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
11111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
.
.
01111111 = 0xBD07_FFFF

bit 11-5 **Reserved**: Write '1'

bit 4-3 **ICESEL<1:0>**: In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN**: JTAG Enable bit⁽¹⁾
1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>**: Background Debugger Enable bits (forced to '11' if code-protect is enabled)
1x = Debugger is disabled
0x = Debugger is enabled

Configuration Bits Setup

FRC & FRCDIV16 & FRCDIV

- PIC32MX的Oscillator來源可以選擇使用內部FRC,內部FRC/16或內部FRC/n。PIC32MX內部的FRC, 震盪頻率為8MHz。
- 要選擇使用內部FRC, 內部FRC/16或內部FRC/n時, Configuration Bits必須作以下設定

`#pragma config FNOSC = FRC`

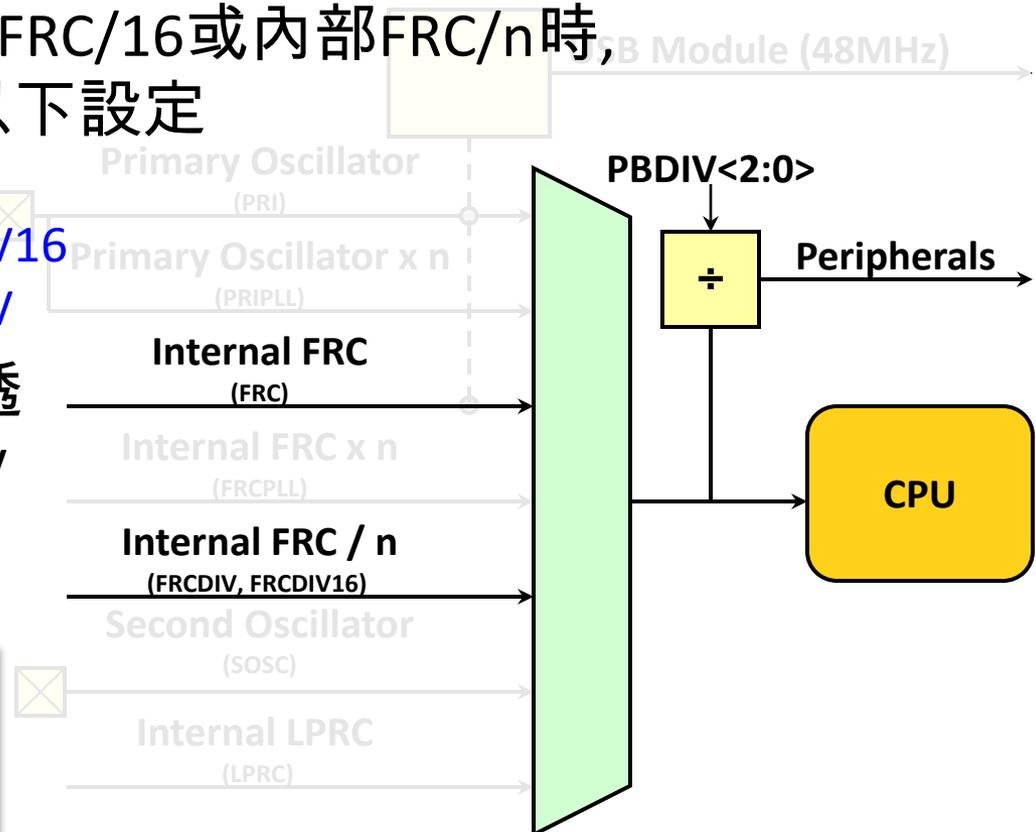
`#pragma config FNOSC = FRCDIV16`

`#pragma config FNOSC = FRCDIV`

- 如果選擇FRCDIV時, 還須透過設定OSCCONbits.FRCDIV決定n值(Default n = 2)。

Ex:OSCCONbits.FRCDIV = 0x00;

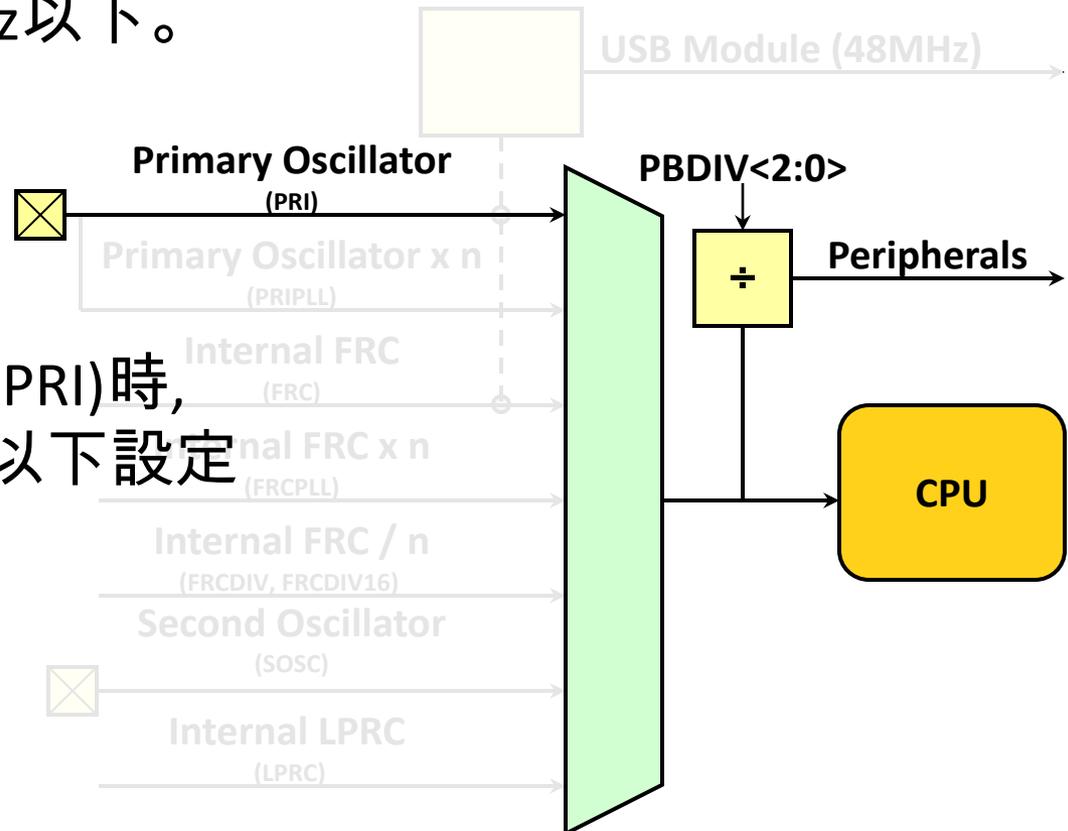
bit 26-24	FRCDIV<2:0>: Internal Fast RC (FRC) Oscillator Clock Divider bits
111	= FRC divided by 256
110	= FRC divided by 64
101	= FRC divided by 32
100	= FRC divided by 16
011	= FRC divided by 8
010	= FRC divided by 4
001	= FRC divided by 2 (default setting)
000	= FRC divided by 1



Configuration Bits Setup

PRI

- PIC32MX的Oscillator來源可以選擇使用主要外部時脈來源接腳 (PRI)。 Primary OSC.通常是用來連接高速的Crystal。其最高的輸入頻率被限定在25MHz以下。

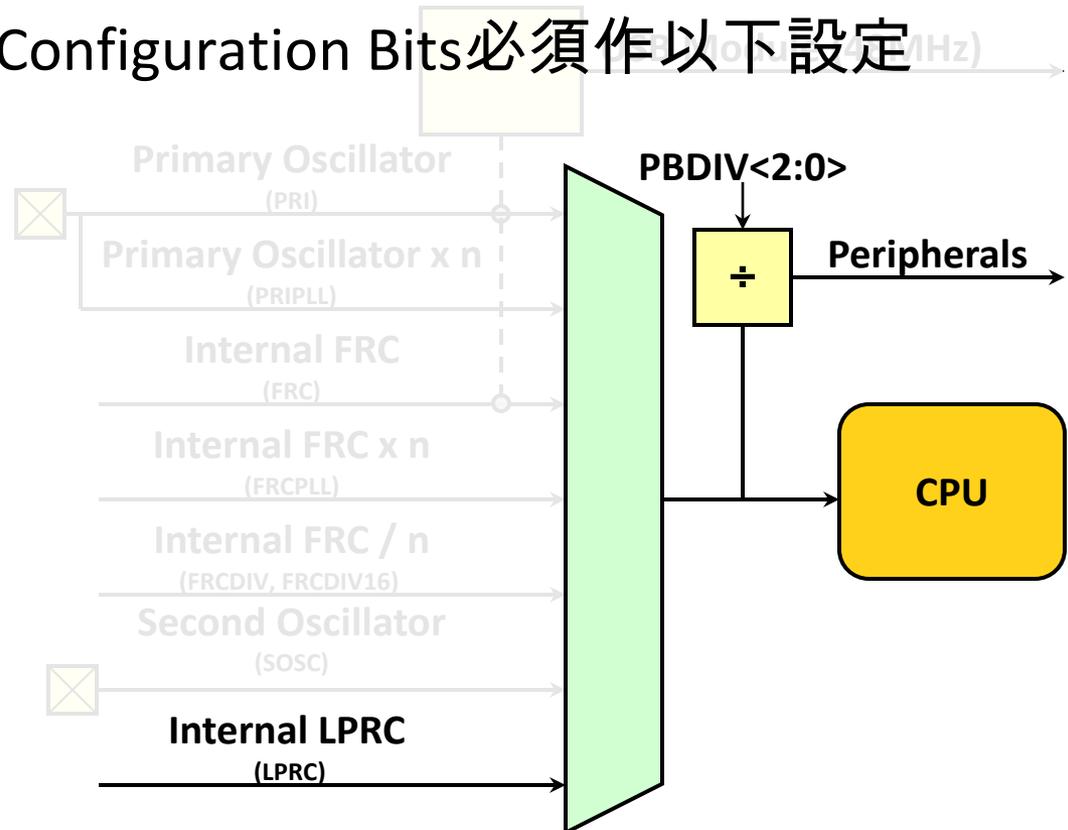


- 要選擇使用Primary OSC.(PRI)時, Configuration Bits必須作以下設定
`#pragma config FNOSC = PRI`

Configuration Bits Setup

LPRC

- PIC32MX的Oscillator來源可以選擇使用內部LPRC, PIC32MX內部的LPRC, 震盪頻率為31.25KHz。
- 要選擇使用內部LPRC時, Configuration Bits必須作以下設定
#pragma config FNOSC = LPRC



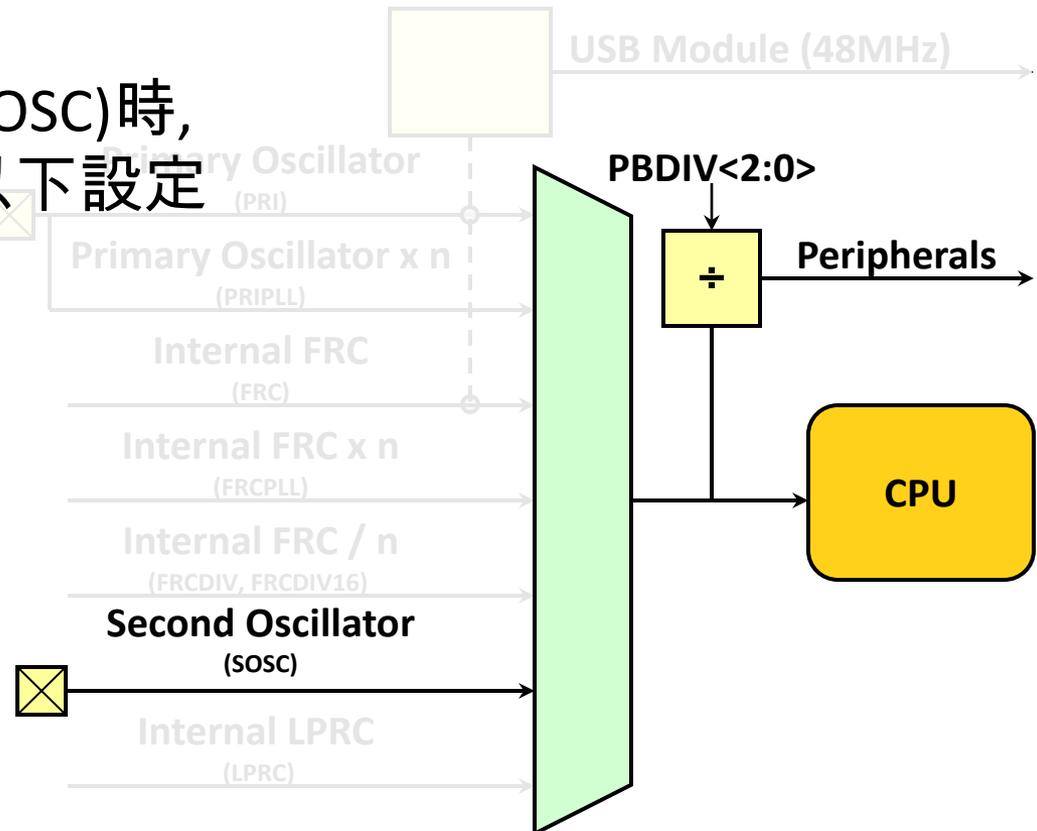
Configuration Bits Setup

SOSC

- PIC32MX的Oscillator來源可以選擇使用第二組外部時脈來源接腳(SOSC)。 Second OSC.通常是用來接低速的Crystal,如:32.768K Hz。

- 要選擇使用Second OSC.(SOSC)時, Configuration Bits必須作以下設定

`#pragma config FNOSC = SOSC`

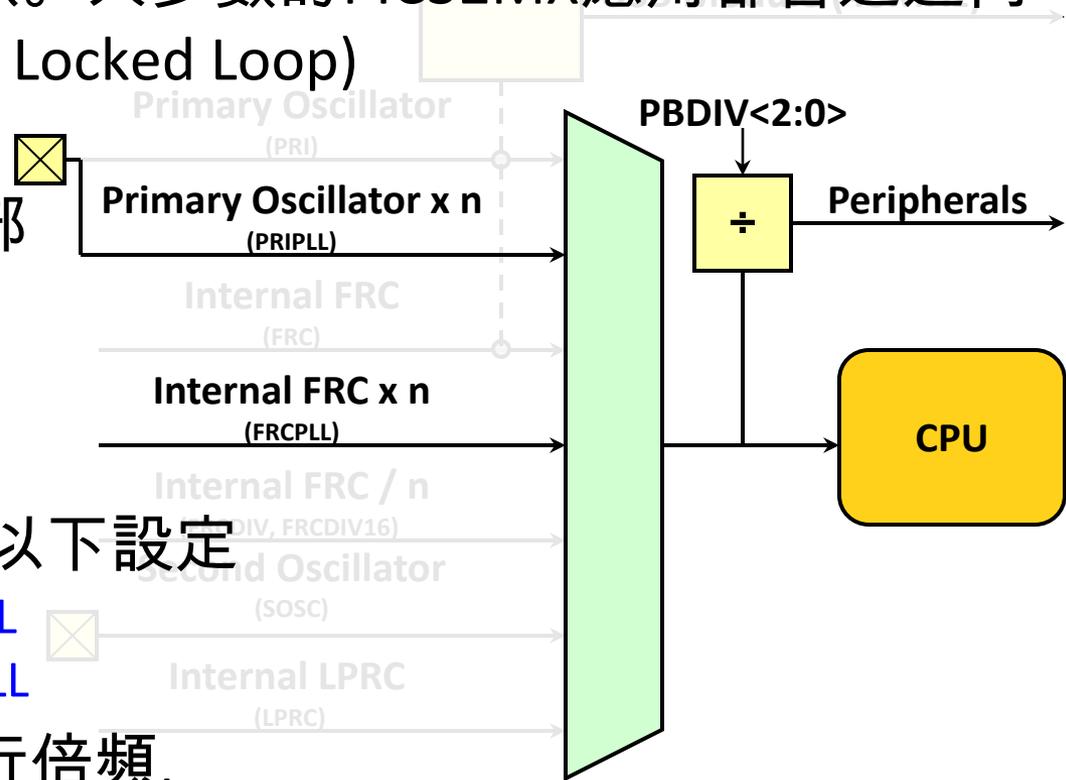


Configuration Bits Setup

PRIPLL, FRCPLL

- PICMX32最高工作頻率可以達到80MHz, 但上述幾種時脈來源都無法提供80MHz的時脈。大多數的PIC32MX應用都會透過內部的倍頻線路(PLL, Phase Locked Loop)來提高頻率。
- 主要外部時脈來源跟內部FRC都可以透過倍頻線路來提高頻率。
- 要選擇使用時, Configuration Bits必須作以下設定

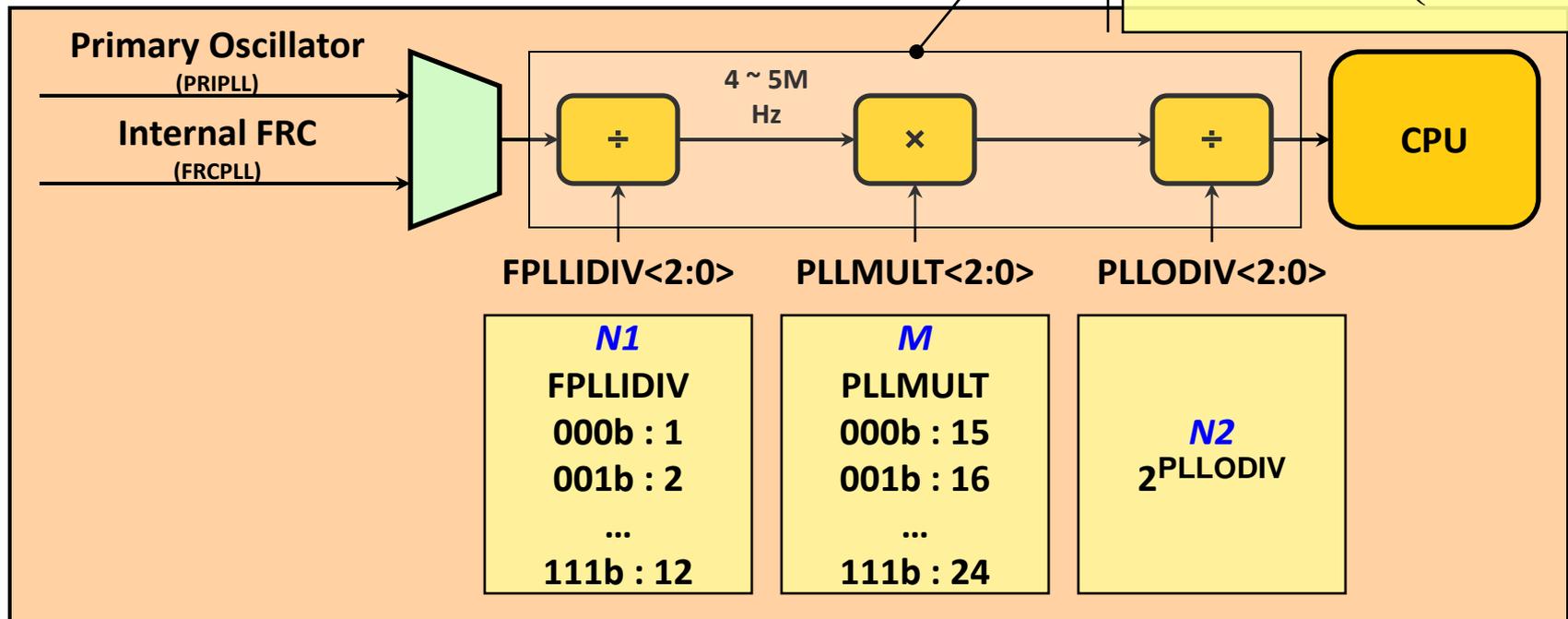
```
#pragma config FNOSC = PRIPLL
#pragma config FNOSC = FRCPLL
```
- PRIPLL, FRCPLL因為會進行倍頻, 所以還必須額外設定倍頻線路(PLL, Phase Locked Loop)的參數。



Phase Locked Loop

- PIC32可以透過PLL線路,提高供給CPU的頻率。
- Primary Osc.跟FRC可以透過PLL線路倍頻。
- PLL的架構分為三個區塊:

$$F_{OSC} = F_{IN} \times \left(\frac{M}{N1 \times N2} \right)$$



System Clock and PB Clock

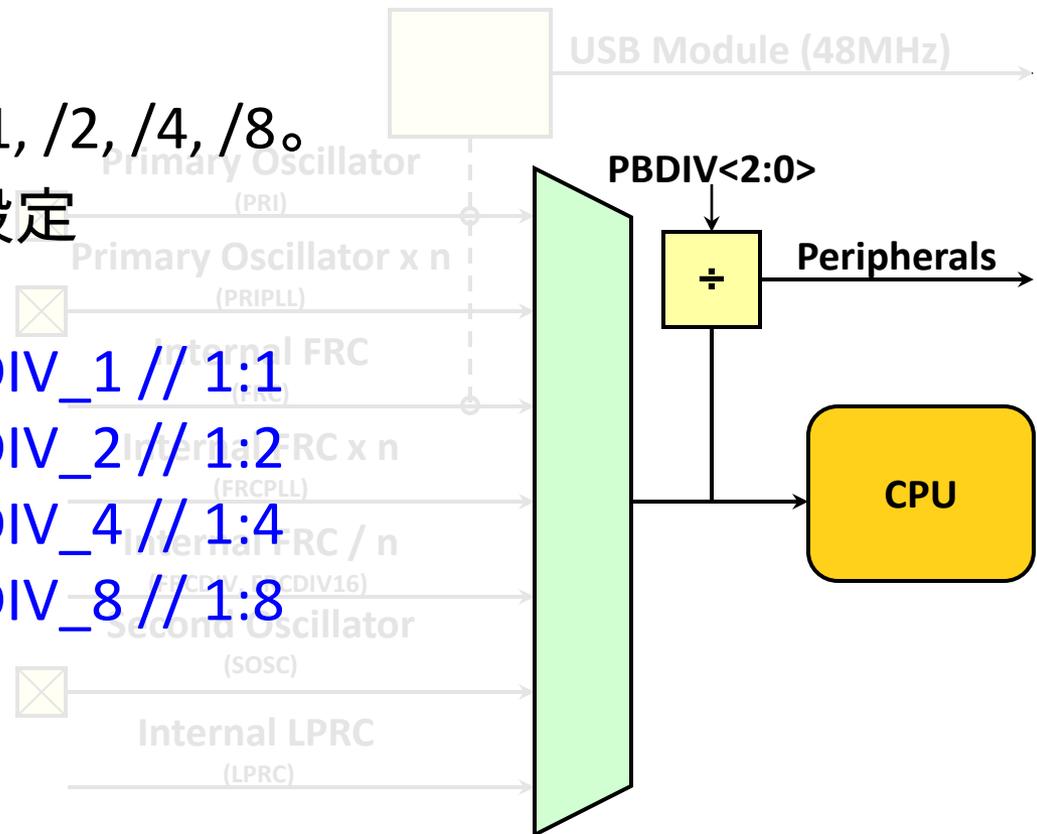
- PIC32的系統時脈(System Clock)與周邊時脈(PB Clock)可以運作不同頻率,兩者間存在一比率關係。
- 周邊時脈(PB Clock) = 系統時脈(System Clock) / 1, /2, /4, /8。
- Configuration Bits的比率設定可參考以下設定

`#pragma config FPBDIV = DIV_1 // 1:1`

`#pragma config FPBDIV = DIV_2 // 1:2`

`#pragma config FPBDIV = DIV_4 // 1:4`

`#pragma config FPBDIV = DIV_8 // 1:8`



FRCPLL, PRIPLL Setup Example

- **FRC OSC (8MHz) with PLL. $((8\text{MHz} / 2) * 15) / 1 = 60\text{MHz}$**
System Freq. / 2 = PB Freq. = 30MHz
#pragma config FNOSC = FRCPLL
#pragma config FPLLIDIV = DIV_2 , FPLLMUL = MUL_15 , FPLLODIV = DIV_1
#pragma config FPBDIV = DIV_2
- **Primary OSC (8MHz) with PLL. $((8\text{MHz} / 2) * 20) / 1 = 80\text{MHz}$**
System Freq. = PB Freq. = 80MHz
#pragma config FNOSC = PRIPLL , POSCMOD = HS
#pragma config FPLLIDIV = DIV_2 , FPLLMUL = MUL_20 , FPLLODIV = DIV_1
#pragma config FPBDIV = DIV_1
- **Primary OSC (8MHz) with PLL. $((8\text{MHz} / 2) * 20) / 2 = 40\text{MHz}$**
System Freq. / 8 = PB Freq. = 5MHz
#pragma config FNOSC = PRIPLL , POSCMOD = HS
#pragma config FPLLIDIV = DIV_2 , FPLLMUL = MUL_20 , FPLLODIV = DIV_2
#pragma config FPBDIV = DIV_8

Oscillator On-Fly-Change

- PIC32MX支援系統時脈的動態切換。程式運作時因為各種需要必須改變時脈頻率時, 就可以使用動態切換。在Bootloader架構下, 程式必須使用動態切換, 才能設定所要的系統頻率。
- 動態切換有一套很複雜的流程, 參考Datasheet可知一二。要自己手工打造太辛苦了。XC32有提供現成的函數可以支援。

Microchip PIC32MX Peripheral Library.chm。

C:\Program Files (x86)\Microchip\xc32\v1.32\docs\pic32-lib-help\

OSCConfig(Clock Source , PLL Multiplier , PLL Postscaler , FRC Divisor);

以PLLIDIV 設為除2, Primary Crystal = 8MHz為例: (*PLLIDIV無法動態修改)

```
// Sys. Clock = FRC = 8 MHz
```

```
OSCConfig( OSC_FRC , 0 , 0 , 0 );
```

```
// Sys. Clock = FRC / 2 = 4 MHz
```

```
OSCConfig( OSC_FRC_DIV , 0 , 0 , OSC_FRC_POST_2 );
```

```
// Sys. Clock = ((FRC / 2) * 20) / 2 = 40 MHz
```

```
OSCConfig( OSC_FRC_PLL , OSC_PLL_MULT_20 , OSC_PLL_POST_2 , 0 );
```

```
// Sys. Clock = ((PRI / 2) * 20) / 1 = 80 MHz
```

```
OSCConfig( OSC_POSC_PLL , OSC_PLL_MULT_20 , OSC_PLL_POST_1 , 0 );
```

Oscillator On-Fly-Change

- 周邊時脈(PB Clock)與系統時脈(System Clock)的比率也可以動態切換。

- OSCSetPBDIV (PB Divider);

Ex:

```
// System Frequency / 8 = PB Frequency
```

```
OSCSetPBDIV(OSC_PB_DIV_8);
```

```
// System Frequency / 4 = PB Frequency
```

```
OSCSetPBDIV(OSC_PB_DIV_4);
```

```
// System Frequency / 2 = PB Frequency
```

```
OSCSetPBDIV(OSC_PB_DIV_2);
```

```
// System Frequency / 1 = PB Frequency
```

```
OSCSetPBDIV(OSC_PB_DIV_1);
```

Lab3 – Oscillator On Fly Change

- 以Lab2的程式為基礎, 利用XC32提供的Oscillator On Fly Change Function來設定時脈。將CPU時脈設定為80MHz,時脈來源採用外部的Crystal(8MHz), 開啟PLL。周邊時脈與系統時脈的比率設成1:8。
- 使用Bootloader將程式燒錄進APP028-1。觀察LED的動作狀態。驗證看看D8(RD2)是否還是每500mS亮/滅一次(1 Hz)?變快或變慢多少?

Lab3 – Oscillator On Fly Change *Step1*

- 如何達成Oscillator On-Flay-Change?

透過Oscillator On-Flay-Change Function來調整Lab2的設定。將系統頻率調整為80MHz, PB Clock = Sys Clock / 8。

For Example:

```
OSCConfig( OSC_POSC_PLL , OSC_PLL_MULT_20 , OSC_PLL_POST_1 , 0 );  
// Sys. Clock = ((PRI / 2) * 20) / 1 = 80 MHz  
OSCSetPBDIV(OSC_PB_DIV_8);  
// System Freq. / 8 = PB Freq.
```

Lab3 – Oscillator On Fly Change *Step2*

- **注意！**每次調整頻率後，必須重新修正PIC32的Wait State與Prefetch的設定，才能讓系統達到最佳化的效能。
- MPLAB XC32提供的SYSTEM Config函數可以用來調整Wait State與Prefetch的設定
SYSTEMConfig(Sys Clock , Flag);
Ex:
SYSTEMConfig(8000000 , SYS_CFG_WAIT_STATES | SYS_CFG_PCACHE);
- 所以記住必須在調整頻率的程式碼後面加入
SYSTEMConfig(Sys Clock , Flag);函數。

Lab3 – Oscillator On Fly Change *Result!*

!在大部分的情形下，會設定工作時脈為最高工作時脈，以發揮出CPU的最高效率。以PIC32MX470F512H為例，最高工作時脈就是80MHz。