

## Op Amp Precision Design: DC Errors

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### INTRODUCTION

Engineers that use op amps in their circuits; especially those new to analog or op amp circuit design. Also intended for engineers that want to understand op amp DC specifications.

### Description

This application note covers the essential background information and design theory needed to design a precision DC circuit using op amps. Topics include:

- Op Amp DC Specifications
- Circuit Analysis
- Circuit Optimization
- Advanced Topics
- References

This application note is limited to voltage feedback (traditional) op amps. Those interested in current feedback op amps will benefit from the information here; the DC specifications and op amp DC model have many similarities.

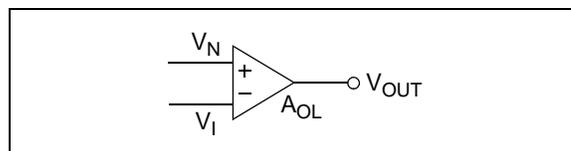
For those that are interested, a simple circuit for measuring input offset voltage has been included in **Appendix A: "Input Offset Measurement Circuit"**.

### DC SPECIFICATIONS

There are a small number of DC specifications that describe errors at the input of an op amp. This section organizes these specifications into those related to the input offset and the others related to input bias currents.

#### Ideal Op Amp

Figure 1 shows the ideal, DC model for op amps (the external circuitry is not shown). All error sources are ignored and the open-loop gain ( $A_{OL}$ ) is infinite. The output voltage is related to the input voltages as shown in Equation 1.



**FIGURE 1:** *Ideal, DC Op Amp Model.*

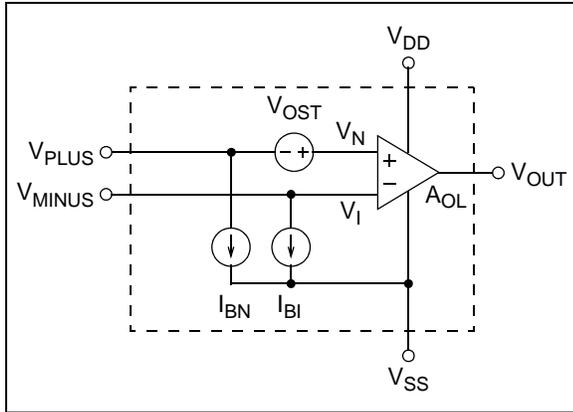
#### EQUATION 1:

$$V_{OUT} = A_{OL}(V_N - V_I)$$

When negative feedback is applied, the ideal op amp's infinite gain forces  $V_N$  and  $V_I$  to be exactly equal; this is the virtual short that some authors talk about. [ 1, 2] When positive feedback is applied (e.g., when used as a comparator),  $V_{OUT}$  swings as far negative or positive as it can (to the rails), depending on the sign of the difference ( $V_N - V_I$ ).

#### Op Amp Model with DC Errors

Figure 2 shows a physically based, DC model for op amps.  $V_{PLUS}$  and  $V_{MINUS}$  are the external input voltages, while  $V_N$  and  $V_I$  are the internal input voltages.  $V_{OST}$  represents the total input offset voltage error. The non-inverting bias current ( $I_{BN}$ ) and inverting bias current ( $I_{BI}$ ) represent the physical currents seen at each of the two input pins.  $A_{OL}$  is the finite DC open-loop gain.



**FIGURE 2:** Physically Biased, DC Op Amp Model.

## Input Offset Related Specifications

A positive  $V_{OST}$  creates a positive shift in the output voltage ( $V_{OUT}$ ). The DC voltages are:

### EQUATION 2:

$$\begin{aligned} V_N &= V_{PLUS} + V_{OST} \\ V_I &= V_{MINUS} \\ V_{OUT} &= A_{OL}(V_N - V_I) \\ &= A_{OL}((V_{PLUS} - V_{MINUS}) + V_{OST}) \end{aligned}$$

The total input offset voltage ( $V_{OST}$ ) collects the following specifications into one, easy to use parameter:

- Input Offset Voltage ( $V_{OS}$ ):
  - Specified offset
  - Describes  $V_{OST}$  at a specific bias point
- DC Open-Loop Gain ( $A_{OL}$ ):
  - $A_{OL} = \Delta V_{OUT} / \Delta V_{OST}$
- Common Mode Rejection Ratio (CMRR):
  - $CMRR = \Delta V_{CM} / \Delta V_{OST}$
  - $V_{CM}$  is the common mode input voltage (average of  $V_{PLUS}$  and  $V_{MINUS}$ )
- Power Supply Rejection Ratio (PSRR):
  - $PSRR = \Delta(V_{DD} - V_{SS}) / \Delta V_{OST}$
- Input Offset Drift with Temperature ( $\Delta V_{OS} / \Delta T_A$ ):
  - Describes how  $V_{OST}$  changes with  $T_A$ ; actually  $\Delta V_{OST} / \Delta T_A$
  - $T_A$  is the ambient temperature

It is important to understand the units for these specifications. An engineer not used to op amp data sheets may be confused by the units shown. The following list should clear up the confusion.

- $V_{OS}$  units are: mV or  $\mu V$
- $A_{OL}$  units do not usually report the relationship shown above:
  - $\mu V/V$  for  $1/A_{OL} = \Delta V_{OST} / \Delta V_{OUT}$
  - dB for  $20 \log(A_{OL})$
- CMRR units are similar to the  $A_{OL}$  units:
  - $\mu V/V$  for  $1/CMRR = \Delta V_{OST} / \Delta V_{CM}$
  - dB for  $20 \log(CMRR)$
- PSRR units are similar to the  $A_{OL}$  units:
  - $\mu V/V$  for  $1/PSRR = \Delta V_{OST} / \Delta(V_{DD} - V_{SS})$
  - dB for  $20 \log(PSRR)$

$\Delta V_{OS} / \Delta T_A$  units are:  $\mu V/^\circ C$  or  $nV/^\circ C$

**Note:** Notice that the gains  $A_{OL}$ , CMRR and PSRR, when reported in  $\mu V/V$ , are actually their reciprocals. This form of the gains is best for statistical analyses; the values tend to have a Gaussian distribution.

Sometimes PSRR is split in two pieces:  $PSRR^+$  that is related to changes in  $V_{DD}$  ( $\Delta V_{DD}$ ) and  $PSRR^-$  that is related to changes in  $V_{SS}$  ( $\Delta V_{SS}$ ).

These quantities are lumped together in the following equation, where the changes in bias voltages are from those specified for  $V_{OS}$  (all units are converted to either V or V/V):

### EQUATION 3:

$$V_{OST} = V_{OS} + \frac{\Delta V_{OUT}}{A_{OL}} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{DD}}{PSRR^+} + \frac{\Delta V_{SS}}{PSRR^-} + \Delta T_A \cdot \frac{\Delta V_{OS}}{\Delta T_A}$$

Notice that all of the specifications will give a positive change in  $V_{OST}$  when the corresponding changes are positive.

## Input Current Related Specifications

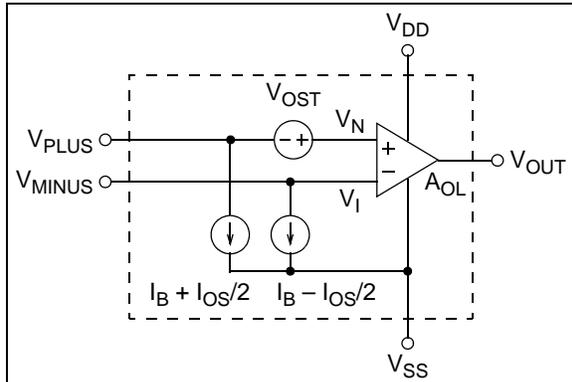
The input bias currents ( $I_{BN}$  and  $I_{BI}$ ) create voltage drops across external resistances, which cause  $V_{OUT}$  to shift. By convention, the currents going into the pins  $V_{PLUS}$  and  $V_{MINUS}$  are positive.

Traditionally, these physically based currents have been mathematically transformed into the equivalent pair of currents  $I_B$  (input bias current) and  $I_{OS}$  (input offset current). These are the average of  $I_{BN}$  and  $I_{BI}$ , and their difference, respectively:

### EQUATION 4:

$$\begin{aligned} I_B &= \frac{(I_{BN} + I_{BI})}{2} \\ I_{OS} &= I_{BN} - I_{BI} \end{aligned}$$

This model makes sense for traditional op amps that have  $I_{BN}$  and  $I_{BI}$  nearly equal. This means that, in this case,  $I_B$  is much larger than  $I_{OS}$ . This happens because these currents are caused by similar physical phenomena (e.g., matched transistor pair with similar input bias currents). [Figure 2](#) shows how these specified currents are modeled in a circuit.



**FIGURE 3:** Equivalent DC Model for Traditional Op Amps.

Some newer op amp architectures have  $I_{OS}$  near to the same magnitude as  $I_B$ . This happens because the physical causes of  $I_{BN}$  and  $I_{BI}$  are not physically related (they are independent or uncorrelated). Most data sheets still use  $I_B$  and  $I_{OS}$  as the specifications.

The input currents depend strongly on architecture, type of input transistors, and temperature. As discussed before, traditional parts have  $I_B \gg I_{OS}$ . Some of the newer architectures have  $I_{OS}$  and  $I_B$  of about the same size.

Most op amps have ESD diodes at the inputs. PN junction ESD diodes tend to have small reverse leakage at room temperature. These leakage currents increase by a factor of 2 for each 10°C increase in temperature. Since the ESD diodes tend to match well, the differences between leakage currents tend to be small. These leakage currents are a part of the input bias currents. When an input goes outside the supply voltage(s) the ESD diodes are tied to, the forward current can grow to be very large.

CMOS inputs transistors have very small input bias currents. Most of these op amps use ESD diodes at the input for protection; the reverse leakage currents of these ESD diodes are the dominant input bias currents.

Electrometer grade op amps minimize input currents. They typically use FET transistors at the input that give currents in the femto-ampere ( $10^{15}$ A) range.

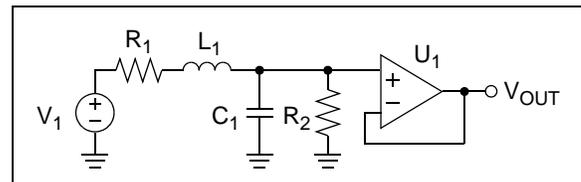
Bipolar inputs have larger input bias currents. They are the input differential pair's base currents, which do not change much with supply voltage. They will change significantly with temperature (e.g., a 4 x range between -40°C and +125°C). These op amps usually use ESD diodes, which increase the bias currents; especially at high temperatures.

## CIRCUIT ANALYSIS

Using a few simple techniques, it is easy to analyze the DC error performance of op amp circuits. Several common circuits illustrate these techniques.

### Resistance Seen by the Non-inverting Input

[Figure 4](#) is a simple circuit with a source and several impedances attached to the non-inverting input. The process of calculating the equivalent resistance seen by the non-inverting input will be described using this circuit as the starting point.

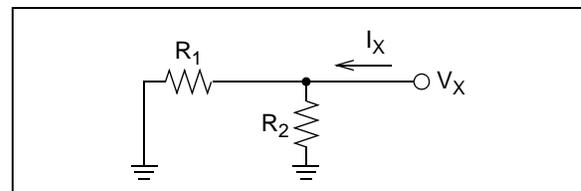


**FIGURE 4:** Simple Circuit.

The first step is to replace all external components with their DC equivalent for a Thevenin analysis:

- Voltage sources become 0V (short circuit)
- Current sources become 0A (open circuit)
- Resistors are left as is
- Capacitors become  $\infty\Omega$  (open circuit)
- Inductors become  $0\Omega$  (short circuit)

[Figure 5](#) shows the resulting circuit when this is done to those components attached to the non-inverting input of the op amp in [Figure 4](#). A test source ( $V_X$ ) has been added to help in the Thevenin analysis.



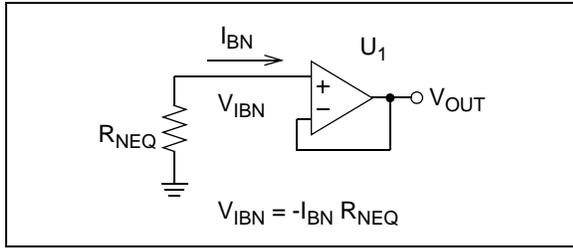
**FIGURE 5:** Equivalent DC Circuit for Non-inverting Input.

The equivalent resistance seen by the non-inverting input, for this example, is:

### EQUATION 5:

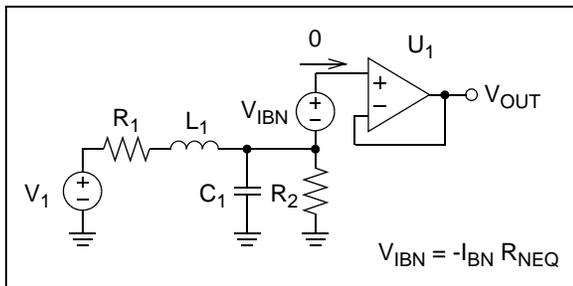
$$R_{NEQ} = \frac{V_X}{I_X} = R_1 \parallel R_2$$

This resistance is used in the error calculations for the non-inverting bias current ( $I_{BN}$ ) source. [Figure 6](#) shows how this is accomplished; the error at the op amp input is calculated at this point of the process.



**FIGURE 6:** Application to Non-inverting Bias Current Error Calculations.

The error voltage ( $V_{IBN}$ ) shown in Figure 6 can be placed in an equivalent circuit diagram that does not explicitly show the current  $I_{BN}$ . This will make the analysis easier, and more consistent, in later steps. This new equivalent circuit is shown in Figure 7 ( $I_{BN}$  is already included in  $V_{IBN}$ ). The  $V_{IBN}$  source, when it is positive, will produce a positive change in  $V_{OUT}$ .

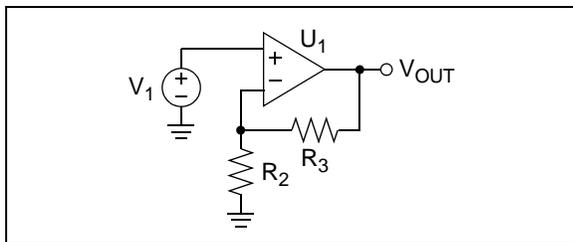


**FIGURE 7:** Application to Non-inverting Bias Current Error Calculations.

This equivalent circuit has the same connections as the original one (Figure 4) to simplify the analysis; this will be useful later on as we combine all of the error terms.

## Resistance Seen by the Inverting Input

Figure 8 is a non-inverting gain amplifier. The process discussed in the last section will be used here to calculate the resistance seen by the inverting input.

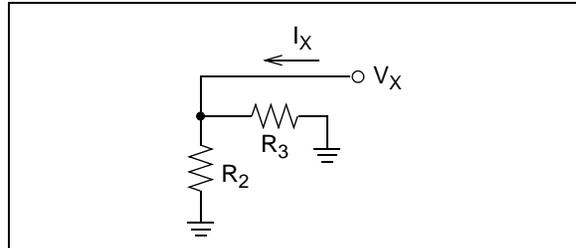


**FIGURE 8:** Non-inverting Gain Circuit.

The same process of generating a Thevenin equivalent applies here, with one short cut:

- The op amp's output ( $V_{OUT}$ ) is treated as a voltage source
  - It becomes a short to ground

Figure 9 shows the resulting circuit at the inverting input, with the test source ( $V_X$ ).



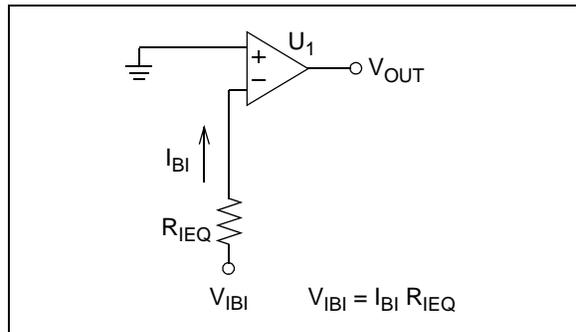
**FIGURE 9:** Equivalent DC Circuit for the Inverting Input.

The equivalent resistance seen by the inverting input, for this example, is:

## EQUATION 6:

$$R_{IEQ} = \frac{V_X}{I_X} \\ = R_2 \parallel R_3$$

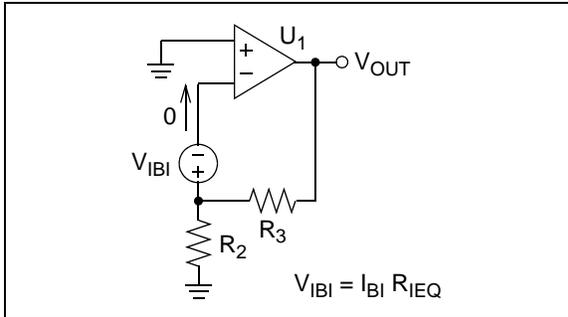
This resistance is used in the error calculations for the inverting bias current ( $I_{BI}$ ) source. Figure 10 shows how this is done for the error at the op amp output, referred to the input.



**FIGURE 10:** Application to Inverting Bias Current Error Calculations.

**Note:** Since the op amp's inverting input voltage must equal its non-inverting input voltage,  $V_{IBI}$  is shown as a change in  $V_{OUT}$  referred to the input.

The error voltage ( $V_{IB}$ ) shown in Figure 10 is placed in an equivalent circuit diagram that does not explicitly show the current  $I_{BI}$ ; see Figure 11 ( $I_{BI}$  is already included in  $V_{IBI}$ ). The  $V_{IBI}$  source, when it is positive, will produce a positive change in  $V_{OUT}$ .



**FIGURE 11:** Application to Inverting Bias Current Error Calculations.

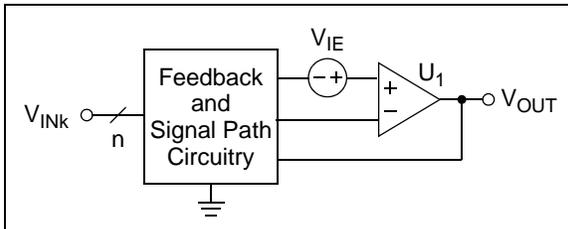
The resistors  $R_2$  and  $R_3$  are shown with the same connections as the original circuit (Figure 8) to simplify the analysis; this will be explained in the next section.

## Combined Input Voltage Errors and Noise Gain

All of the DC errors at an op amp's input ( $V_{OST}$ ,  $V_{IBN}$  and  $V_{IBI}$ ) can be combined into one equivalent voltage source ( $V_{IE}$ ) at the non-inverting input pin (see Figure 12):

### EQUATION 7:

$$V_{IE} = V_{OST} + V_{IBN} + V_{IBI}$$



**FIGURE 12:** Circuit Diagram Illustrating the Concept of Noise Gain.

Noise gain ( $G_N$ ) is the DC gain from  $V_{IE}$  (at the non-inverting input pin) to  $V_{OUT}$  when the op amp operates in a closed-loop condition, when all other (external) energy sources are zero.  $G_N$  is positive for stable feedback loops. This gain can be obtained with any reasonable circuit analysis method. In equation form, we have:

### EQUATION 8:

$$G_N = \frac{V_{OUT}}{V_{IE}}$$

Where:

$$\begin{aligned} V_{INk} &= 0V \\ k &= 1 \text{ to } n \end{aligned}$$

The following examples will show how this concept is applied in common op amp circuits.

**Note:** The concept of noise gain is central to understanding op amp behavior. For instance, it simplifies op amp bandwidth, noise and stability analyses.

## Output DC Error

Now we can quickly calculate the output error of the op amp ( $V_{OE}$ ) using the information we have developed. The principle of superposition gives:

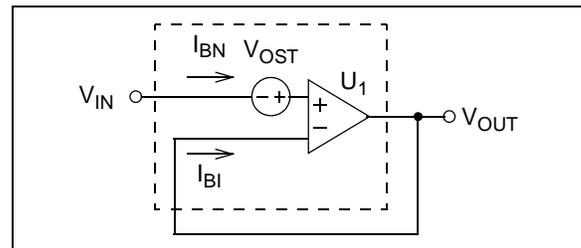
### EQUATION 9:

$$\begin{aligned} V_{OE} &= G_N V_{IE} \\ &= G_N (V_{OST} + V_{IBN} + V_{IBI}) \end{aligned}$$

## Examples

### UNITY GAIN BUFFER

Figure 13 shows a unity gain buffer using an op amp. The op amp's DC model is shown inside the dashed box.



**FIGURE 13:** Unity Gain Buffer.

Because the resistances seen by the op amp inputs are zero and  $G_N = 1$  V/V, the output voltage is simply:

### EQUATION 10:

$$V_{OUT} = V_{IN} + V_{OST}$$

Let's use Microchip's MCP601 op amp to illustrate this design. We'll assume that  $V_{CMR}$ ,  $V_{DD}$  and  $V_{OUT}$  vary across their complete ranges. We'll use an arbitrary estimate of the worst-case value for  $\Delta V_{OS}/\Delta T_A$  (see the data sheet for the official specifications).  $R_1$  and  $R_3$  will be 0.1% resistors.

**Note:** Since the MCP601's common mode input voltage range ( $V_{CMR}$ ), at +25°C, is limited to the range -0.3V and  $V_{DD} - 1.2V$ , there will be large output errors when  $V_{CM}$  approaches  $V_{DD}$ .

## EXAMPLE 1:

Maximum  $V_{OE} = V_{OST}$ :

$V_{OS} < \pm 2.00$  mV

$$\Delta V_{OUT}/A_{OL} \leq (2.65V)/(100 \text{ kV/V}) \leq 0.03 \text{ mV}$$

$$\Delta V_{DD}/PSRR \leq (1.40V)/(10.0 \text{ kV/V}) \leq 0.14 \text{ mV}$$

$$\Delta V_{CM}/CMRR \leq (4.3V - (-0.3V))/(5.62 \text{ kV/V}) \leq 0.82 \text{ mV} = \pm 0.41 \text{ mV}$$

$$\Delta T_A(\Delta V_{OS}/\Delta T_A) \leq (100^\circ\text{C})(\pm 12 \mu\text{V}/^\circ\text{C}) \leq \pm 1.20 \text{ mV}$$

$$V_{OST} \leq \pm 3.8 \text{ mV}$$

## NON-INVERTING AMPLIFIER

Figure 14 shows a non-inverting gain amplifier with an LC low-pass filter at the input. The op amp's DC model is shown inside the dashed box.

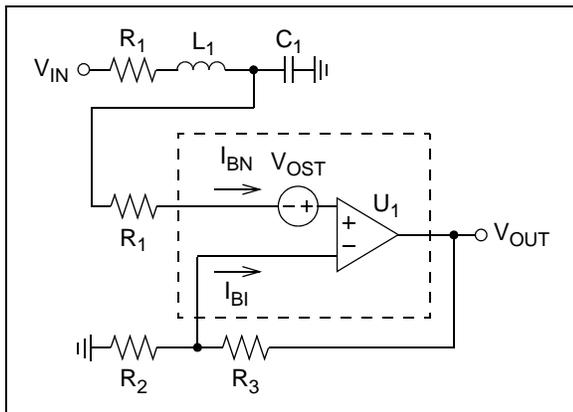


FIGURE 14: Non-inverting Gain Amplifier.

The output voltage with error is:

## EQUATION 11:

$$V_{OE} = G_N(V_{OST} + V_{IBN} + V_{IBI})$$

$$V_{OUT} = G_N V_{IN} + V_{OE}$$

Where:

$$G_N = 1 + R_3/R_2$$

$$R_{NEQ} = R_1$$

$$R_{IEQ} = R_2 || R_3$$

$$V_{IBN} = -I_{BN} R_{NEQ}$$

$$V_{IBI} = I_{BI} R_{IEQ}$$

The MCP601  $V_{OST}$  calculations in Example 1 can be used for a gain of +10 V/V example:

## EXAMPLE 2:

Maximum  $V_{OST} = \pm 3.8$  mV

Selected Resistors (see Figure 14):

$$R_3 = 20.0 \text{ k}\Omega$$

$$R_2 = 2.21 \text{ k}\Omega$$

$$R_1 = 2.00 \text{ k}\Omega$$

$$G_N = 10.05 \text{ V/V}$$

Maximum  $V_{IBN}$ :

$$R_{NEQ} = 2.00 \text{ k}\Omega$$

$$V_{IBN} \geq -(5 \text{ nA} + 0.5 \text{ nA})(2.00 \text{ k}\Omega) = -11 \mu\text{V}$$

Maximum  $V_{IBN}$ :

$$R_{IEQ} = 1.99 \text{ k}\Omega$$

$$V_{IBN} \leq (5 \text{ nA} - 0.5 \text{ nA})(1.99 \text{ k}\Omega) = 9 \mu\text{V}$$

Maximum  $V_{OE}$ :

$$V_{OE} \leq \pm 38 \text{ mV}$$

## INVERTING AMPLIFIER

Figure 15 shows an inverting gain amplifier. The op amp's DC model is shown inside the dashed box.

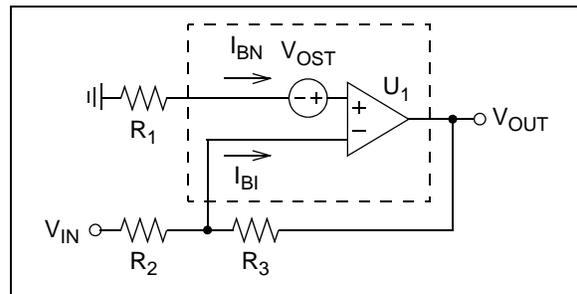


FIGURE 15: Inverting Gain Amplifier.

The output voltage with error is:

## EQUATION 12:

$$V_{OE} = G_N(V_{OST} + V_{IBN} + V_{IBI})$$

$$V_{OUT} = -(G_N - 1)V_{IN} + V_{OE}$$

Where:

$$G_N = 1 + R_3/R_2$$

$$R_{NEQ} = R_1$$

$$R_{IEQ} = R_2 || R_3$$

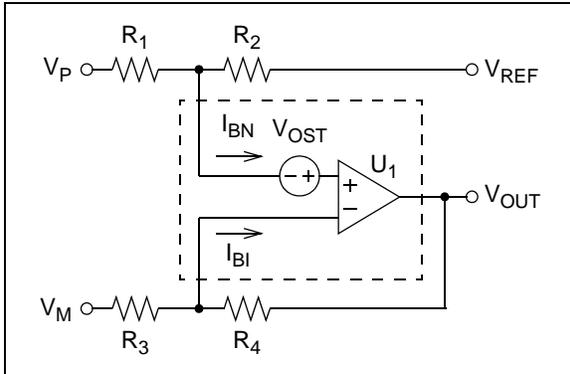
$$V_{IBN} = -I_{BN} R_{NEQ}$$

$$V_{IBI} = I_{BI} R_{IEQ}$$

Notice that Example 2 is easily modified for an inverting gain of -9 V/V; the resistors and  $V_{OE}$  are the same (only the signal gain is changed).

## DIFFERENCE AMPLIFIER

Figure 16 shows a difference amplifier. The op amp's DC model is shown inside the dashed box. Notice that this circuit can be analyzed quickly using superposition.



**FIGURE 16:** Difference Amplifier.

The output voltage with error is:

### EQUATION 13:

$$V_{OE} = G_N(V_{IE} + V_{IBN} + V_{IBI})$$

$$V_{OUT} = (G_N - 1)(V_P - V_M) + V_{REF} + V_{OE}$$

Where:

$$R_2 = R_1$$

$$R_4 = R_3$$

$$G_N = 1 + R_2/R_1 = 1 + R_4/R_3$$

$$R_{NEQ} = R_1 \parallel R_2$$

$$R_{IEQ} = R_3 \parallel R_4$$

$$V_{IBN} = -I_{BN}R_{NEQ}$$

$$V_{IBI} = I_{BI}R_{IEQ}$$

Using the MCP601 in a differential amplifier with gain 10 V/V gives (similar to Example 2):

### EXAMPLE 3:

Maximum  $V_{OST} = \pm 3.8$  mV

Selected Resistors (see Figure 16):

$$R_1 = R_3 = 2.00 \text{ k}\Omega$$

$$R_2 = R_4 = 20.0 \text{ k}\Omega$$

$$G_N = 11.00 \text{ V/V}$$

$$(G_N - 1) = 10.00 \text{ V/V, the differential gain}$$

Maximum Error Voltages:

$$V_{IBN} \geq -(5 \text{ nA} + 0.5 \text{ nA})(1.82 \text{ k}\Omega) = -10 \text{ }\mu\text{V}$$

$$V_{IBN} \leq (5 \text{ nA} - 0.5 \text{ nA})(1.82 \text{ k}\Omega) = 8 \text{ }\mu\text{V}$$

$$V_{OE} \leq \pm 42 \text{ mV}$$

## CIRCUIT OPTIMIZATION

There are a few, simple design techniques that can quickly help a designer reach an acceptable accuracy.

### Gain Selection

Set any amplifier next to a signal source (e.g., temperature sensor) to the highest reasonable gain. This will cause any later gains to be small; typically they will be at a gain of 1 V/V.

This design technique minimizes the impact most of the analog signal processing components have on the overall error. It also allows the designer to reduce cost by specifying more precise components only where they are needed.

### Minimizing Bias Current Errors

For the examples shown in Figure 13 through Figure 16, it is instructive to convert the bias current error voltages to the equivalent form using the specified currents:

### EQUATION 14:

$$V_{IBN} + V_{IBI} = -I_{BN}R_{NEQ} + I_{BI}R_{IEQ}$$

$$= I_B(R_{IEQ} - R_{NEQ}) - I_{OS}\left(\frac{R_{IEQ} + R_{NEQ}}{2}\right)$$

Minimizing the resistances helps minimize these errors for all op amps.

Many op amps' bias current ( $I_B$ ) have a much larger maximum specification than their offset current ( $I_{OS}$ ). In that case, set  $R_{N\_EQ} = R_{I\_EQ}$  for the best performance. When  $I_{OS}$  is much smaller than  $I_B$ , the resistor tolerance (RTOL) needs to be good enough to prevent  $I_B$  from becoming a significant contributor to the error:

### EQUATION 15:

$$RTOL \ll 4 \frac{I_{OS}}{I_B}$$

Large input resistances can also cause a significant shift in the input common mode voltage ( $V_{CM}$ ). In some cases, this can significantly reduce the input common mode voltage range ( $V_{CMR}$ ):

### EQUATION 16:

$$\Delta V_{CM} = -I_B \left( \frac{R_{IEQ} + R_{NEQ}}{2} \right)$$

$$V_{CMR\_EQ} = V_{CMR} + \Delta V_{CM}$$

## Op Amp Selection

The op amp needs to support the level of DC precision required by the design. Table 1 shows four general op amp architectures that give trade-offs between performance, cost and design complexity.

**TABLE 1: OP AMP CAPABILITIES<sup>(1)</sup>**

Parameter	Performance for Each Architecture			
	General Purpose	Trimmed	Auto-calibrated	Auto-zeroed
$V_{OS}$	1	2	3	4
$\Delta V_{OS}/\Delta T_A$	1	1	3	4
$V_{OS}$ Aging	1	1	3	4
$A_{OL}$	2	2	3	4
CMRR	1	1	1	4
PSRR	1	1	1	4
$I_B$	2	2	1	3
$I_{OS}$	2	2	2	2

**Note 1:** The performance numbers signify: 1 = okay, 2 = good, 3 = better and 4 = best.

## Process and Environmental Variations

Methods to evaluate a design's variation in performance are commonly understood in the industry. Examples include worst case analysis (all tolerances at minimum or maximum) and RSS (Root Sum of Squares – a statistical approach).

The following list gives important op amp behaviors to include when evaluating process and environmental changes (almost all have a Gaussian distribution):

- $V_{OS}$ 
  - All  $V_{OS}$  values for duals and quads are statistically independent (zero correlation)
- $1/A_{OL}$ ,  $1/CMRR$  and  $1/PSRR$  (in units of  $\mu V/V$ )
- $\Delta V_{OS}/\Delta T_A$
- Offset Aging
  - Increases with time
  - Only specified on auto-zeroed op amp data sheets
- $I_B$  and  $I_{OS}$ 
  - CMOS inputs (with ESD diodes) have an exponential relationship with temperature (double every 10°C increase)
  - Bipolar inputs typically double at -40°C and are halved at +125°C
  - Are typically uncorrelated

## ADVANCED TOPICS

### PCB Layout

Printed Circuit Board (PCB) layout can have a significant effect on DC precision. Effects that need to be considered include:

- Ground Loops – Poor grounding techniques and inattention to current return paths can cause significant shifts in DC voltages
- Crosstalk – Other signals on a PCB can find sneak paths through the ground, power supplies and traces

### Input Common Mode Voltage Range

A commonly overlooked error source is allowing the signal to go outside the input voltage range. This most commonly occurs when using a non-rail-to-rail input op amp in unity gain; the input will cause an output error when the  $V_{CMR}$  is exceeded; this error grows quickly.

### Output Voltage Range

There will be a significant error, that grows very quick, when the output voltage range is exceeded. The  $V_{OL}$  and  $V_{OH}$  specifications usually shown in op amp data sheets describe non-linear behavior (i.e., when used as a comparator). When the output approaches either limit,  $V_{OST}$  can increase significantly before reaching the hard limits. For the most stringent designs, keep  $V_{OUT}$  within the range that the data sheet shows for the  $A_{OL}$  specification.

### Noise

The data sheet's input noise density specifications can be used to calculate an op amp's integrated output noise (random variation in output voltage). This helps determine the range of expected errors at any point in time; it also can significantly reduce the output range when there is a very high gain.

### Non-linear Distortion

Non-linear distortion converts a sinewave at one frequency into a Fourier series of tones; the undesired tone frequencies are the harmonic distortion products. One of these undesired tones is at zero frequency (DC); non-linear distortion can produce DC shifts.

For example, a simple sinewave that is processed by an amplifier with a quadratic (polynomial) response will produce:

**EQUATION 17:**

$$\begin{aligned}
 V_{IN} &= V_M \sin(2\pi ft) \\
 V_{OUT} &= A_0 + A_1 V_{IN} + A_2 V_{IN}^2 \\
 &= A_0 + A_1 V_M \sin(2\pi ft) + A_2 (V_M \sin(2\pi ft))^2 \\
 &= B_0 + B_1 \sin(2\pi ft) + B_2 \cos(4\pi ft)
 \end{aligned}$$

Where:

$$B_0 = A_0 + \frac{A_2 V_M^2}{2}$$

$$B_1 = A_1 V_M$$

$$B_2 = \frac{-A_2 V_M^2}{2}$$

All other even order harmonic distortion terms cause a shift in DC bias too. The quadratic term, however, usually dominates.

Using mildly non-linear components in the signal path can cause this effect. The cure is to select higher quality components.

More commonly, higher frequency signals will be routed through a non-linear element. A common example is discussed in detail in the next section.

**EMI**

Electro-magnetic Interference (EMI) at high frequencies (i.e., near and above the op amp's Gain Bandwidth Product) easily couples to the inputs of any component on a PCB; op amps are no exception to this rule. Because the op amp has little control over this energy, and the ESD diodes are very fast, the latter will rectify high frequency EMI.

The rectification of the EMI energy produces both high frequency energy and a significant DC shift at the op amp inputs. This appears as an unexpectedly large  $V_{OST}$  on many measurement boxes; they average out the high frequency component. To see if this is an issue with your design, use a fast oscilloscope at short time scales.

The most effective cures for EMI problems are handled at the PCB design level. The coupling paths include power supply lines, magnetic loops and capacitive metal areas.

It is possible to improve performance with high frequency filters at the op amp inputs. Usually, however, the improvements are small. Also, the filters may affect the feedback network's stability, causing unexpected behaviors.

**Oscillations**

We sometimes see an op amp circuit that is unstable enough to oscillate. When this does happen, many puzzling symptoms appear. The supply current increases, the DC voltages in a circuit can shift, voltages can wander and intermittent glitches can be seen.

To find this problem, use a fast oscilloscope and change the time scale; it may be necessary to gain up a signal to see oscillations much smaller than 0.1V.

To verify the source of oscillation (unstable behavior), modify component values (e.g., place a capacitor in parallel) in different feedback loops. A change in oscillation frequency usually indicates that the unstable loop has been affected.

**Note:** Op amps, by themselves, cannot be either stable or unstable. The feedback loop design (interaction of op amp and passive components) sets the stability.

**SUMMARY**

This application note has covered the topic of precision design using (voltage feedback) op amps in some detail. It shows how all of the DC errors can be referred to the input; they appear as an additional change in input offset voltage. It gives results for the most common op amp circuits: unity gain buffer, non-inverting gain amplifier, inverting gain amplifier and difference amplifier. Tips on optimizing performance and coverage of advanced topics help the designer with more difficult designs. The references give additional information on related topics.

**REFERENCES****Textbook on Circuit Level Design**

- [1] Paul R. Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 2<sup>nd</sup> Ed., John Wiley & Sons, 1984.

**Textbook on Transistor Level Design**

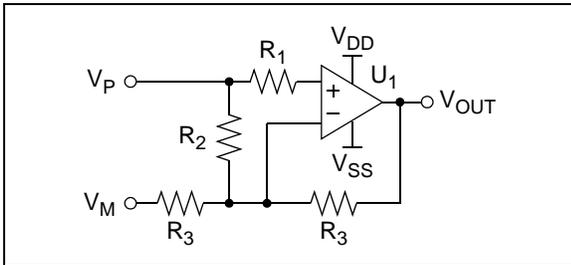
- [2] Paul R. Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 2<sup>nd</sup> Ed., John Wiley & Sons, 1984.

## APPENDIX A: INPUT OFFSET MEASUREMENT CIRCUIT

This appendix shows a simple test circuit that can be used on the bench to evaluate most op amps' input offset voltage and bias current performance. A simpler circuit is discussed first, which only measures  $V_{OST}$ . It is then expanded to include  $I_{BN}$  and  $I_{BI}$  measurements. The limitations of these circuit are also discussed.

### A.1 Basic Input Offset Test Circuit

The circuit shown in [Figure A-1](#) supports quick op amp  $V_{OST}$  measurements ( $V_{OS}$ ,  $A_{OL}$ ,  $CMRR$ ,  $PSRR$  and  $\Delta V_{OS}/\Delta T_A$ ).  $V_P$  sets the op amp's  $V_{CM}$ .  $V_M$  sets the nominal  $V_{OUT}$  value.  $R_1$  isolates  $U_1$ 's input from  $V_P$  and is used to cancel  $I_B$  induced errors. The two resistors  $R_3$  set an inverting gain of -1 V/V for  $V_M$ .  $R_2$  increases the noise gain, but does not affect the gains seen by  $V_P$  and  $V_M$ .  $V_{DD}$  and  $V_{SS}$  are the supply voltages, which can be varied for  $PSRR$  measurements.



**FIGURE A-1: Offset Test Circuit.**

The common mode input voltage and output voltage are:

#### EQUATION A-1:

$$\begin{aligned}
 V_{CM} &= V_P + \left(\frac{V_{OST}}{2}\right) - I_{BN}R_1 \\
 &= V_P + \left(\frac{V_{OST}}{2}\right) - (I_B + I_{OS})R_1 \\
 V_{OUT} &= 2V_P - V_M + V_{OST}G_N - I_{BN}G_N R_1 + I_{BI}R_3 \\
 &= 2V_P - V_M + V_{OST}G_N + I_B(R_3 - G_N R_1) \\
 &\quad - I_{OS}\left(\frac{R_3 + G_N R_1}{2}\right)
 \end{aligned}$$

Where:

$$G_N = 2 + R_3/R_2$$

**Note:**  $V_{CM}$  contains a  $V_{OST}/2$  term because it is the average of the two input voltages (one with  $V_{OST}$  and the other without). Usually, this makes only a small difference.

#### A.1.1 CIRCUIT DESIGN

The goal is to make  $G_N$  reasonably large and the error terms (with  $V_{OST}$ ,  $I_{BN}$  and  $I_{BI}$ ) as small as possible. The following design choices will give good results (since  $G_N V_{OST}$  is chosen to be so large):

#### EQUATION A-2:

$$\begin{aligned}
 G_N &\approx \frac{(25\text{mV})}{(\max|V_{OST}|)} \\
 R_3 &\approx \text{typical load resistance} \\
 R_2 &= \frac{R_3}{G_N - 2} \\
 R_1 &= \frac{R_3}{G_N}
 \end{aligned}$$

The 25 mV used to estimate  $G_N$  gives  $V_{OUT}$  a reasonable output range. For instance, the MCP601's  $A_{OL}$  specification requires  $V_{OUT}$  to be 0.1V from the rails; the  $G_N V_{OST}$  term will make this 0.05V to 0.15V from the rails.

Solving for  $V_{OST}$ , and assuming that the bias current errors are negligible, gives:

#### EQUATION A-3:

$$V_{OST} \approx \frac{V_{OUT\#1} - (2V_P - V_M)}{G_N}$$

Let's use Microchip's MCP601 op amp to illustrate this design (similar to [Example 2](#) on page 6).  $R_3$  is reduced to minimize the impact of  $I_{BN}$  and  $I_{BI}$ .

#### EXAMPLE A-1:

$$V_{OST} \leq \pm 3.8 \text{ mV}$$

Design Selections:

$$\begin{aligned}
 G_N &\approx (25 \text{ mV}) / (3.8 \text{ mV}) \\
 &= 6.6 \text{ V/V} \rightarrow 5 \text{ V/V} \\
 R_3 &= 100 \text{ k}\Omega \rightarrow 20.0 \text{ k}\Omega \\
 R_2 &= 6.65 \text{ k}\Omega \\
 R_1 &= 4.02 \text{ k}\Omega
 \end{aligned}$$

Impact on  $V_{CM}$  and  $V_{OUT}$  accuracy:

$$\begin{aligned}
 V_{CM} &= V_P \pm 1.9 \text{ mV} \\
 V_{OUT} &= 2V_P - V_M + V_{OST}G_N \pm 0.01 \text{ mV}
 \end{aligned}$$

The error in  $V_{CM}$ , divided by  $CMRR$  (5.62 kV/V), produces a  $\pm 0.3 \mu\text{V}$  error in  $V_{OUT}$ . It also reduces the input common mode voltage range by 2.0 mV, which is negligible for most purposes. Thus, the estimated  $V_{OUT}$  has errors, dominated by the bias currents, of about  $\pm 0.04\%$ .

## A.1.2 MEASUREMENT STRATEGY

Now that we have a circuit, it pays to have a strategy to measure those points needed. Let's assume the goal is to double check the MCP601's data sheet specifications at +25°C.

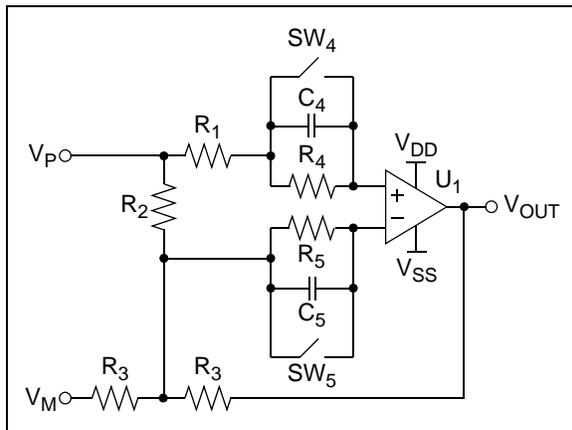
**TABLE A-1: MEASUREMENT POINTS**

Meas. No.	Nominal Bias Point			Target Parameters			
	V <sub>DD</sub> (V)	V <sub>CM</sub> (V)	V <sub>OUT</sub> (V)	V <sub>OS</sub>	A <sub>OL</sub>	CMRR	PSRR
1	2.7	1.35	1.35	X	—	—	X
2		1.35	0.1	—	X	—	—
3		1.35	2.6	—	X	—	—
4	5.0	-0.3	2.5	—	—	X	—
5		3.8	2.5	—	—	X	—
6	5.5	2.75	2.75	X	—	—	X
7		2.75	0.1	—	X	—	—
8		2.75	5.4	—	X	—	—

See Section "Input Offset Related Specifications" on page 2 for the equations relating these measurements and the specifications.

## A.2 Complete Input Offset Test Circuit

The circuit in Figure A-2 functions like Figure A-1, plus it has R<sub>4</sub> and R<sub>5</sub> to measure I<sub>BN</sub> and I<sub>BI</sub>. SW<sub>4</sub> and SW<sub>5</sub> short R<sub>4</sub> and R<sub>5</sub> for all V<sub>OST</sub> related measurements. C<sub>4</sub> and C<sub>5</sub> help maintain stability and reduce noise.



**FIGURE A-2:** Offset Test Circuit with Bias Current Capabilities.

The common mode input voltage and output voltage are:

**EQUATION A-4:**

$$\begin{aligned}
 V_{CM} &= V_P + \left(\frac{V_{OST}}{2}\right) - I_{BN}R_{NEQ} \\
 &= V_P + \left(\frac{V_{OST}}{2}\right) - (I_B + I_{OS})R_{NEQ} \\
 V_{OUT} &= 2V_P - V_M + G_N(V_{OST} - I_{BN}R_{NEQ} + I_{BI}R_{IEQ}) \\
 &= 2V_P - V_M + G_N V_{OST} + I_B G_N (R_{IEQ} - R_{NEQ}) \\
 &\quad + I_{OS} G_N \left(\frac{R_{IEQ} + R_{NEQ}}{2}\right)
 \end{aligned}$$

Where:

$$\begin{aligned}
 G_N &= 2 + R_3/R_2 \\
 R_{NEQ} &= R_1, SW_4 = \text{short} \\
 &= R_1 + R_4, SW_4 = \text{open} \\
 R_{IEQ} &= R_3/G_N, SW_5 = \text{short} \\
 &= (R_3/G_N) + R_5, SW_5 = \text{open}
 \end{aligned}$$

## A.2.1 CIRCUIT DESIGN

We now add to the design equations estimates of R<sub>4</sub>, R<sub>5</sub>, C<sub>4</sub> and C<sub>5</sub>. The capacitors are much larger than most op amps' common mode input capacitance (for stability, noise and speed).

**EQUATION A-5:**

Select G<sub>N</sub>, R<sub>3</sub>, R<sub>2</sub> and R<sub>1</sub> as before

$$\begin{aligned}
 R_4 &= (25 \text{ mV}) / (G_N \text{ max } |I_{BN}|) \\
 R_5 &= (25 \text{ mV}) / (G_N \text{ max } |I_{BI}|) \\
 C_4 &= C_5 = 100 \text{ pF}
 \end{aligned}$$

The practical way to use this circuit is as follows. Measure all of the V<sub>OST</sub> related parameters with SW<sub>4</sub> and SW<sub>5</sub> shorted; the circuit behaves exactly as described in A.1 "Basic Input Offset Test Circuit".

To measure I<sub>BN</sub> and I<sub>BI</sub>, take three measurements at a single bias point with different switch selections:

**TABLE A-2: SWITCH SELECTIONS**

Meas. No.	Switches		Emphasize
	SW <sub>1</sub>	SW <sub>2</sub>	
1	short	short	V <sub>OST</sub>
2	open	short	V <sub>OST</sub> and I <sub>BN</sub> R <sub>4</sub>
3	short	open	V <sub>OST</sub> and I <sub>BI</sub> R <sub>5</sub>

**Note 1:** The change in V<sub>CM</sub> caused by R<sub>4</sub>, in Meas. No. 2, can be substantial.

# AN1177

Subtracting these measurements gives the following simple results:

## EQUATION A-6:

$$I_{BN} = \frac{-(V_{OUT\#2} - V_{OUT\#1})}{R_4}$$

$$I_{BI} = \frac{V_{OUT\#3} - V_{OUT\#1}}{R_5}$$

$$V_{OST} = \frac{V_{OUT\#1} - (2V_P - V_M)}{G_N} + I_{BN}R_1 - I_{BI} \cdot \frac{R_3}{G}$$

$$\approx \frac{V_{OUT\#1} - (2V_P - V_M)}{G_N}$$

$$I_B = \frac{(I_{BN} + I_{BI})}{2}$$

$$I_{OS} = I_{BN} - I_{BI}$$

Let's continue [Example A-1](#), which uses the MCP601, for measurements up to +85°C:

## EXAMPLE A-2:

$$V_{OST} \leq \pm 3.8 \text{ mV}$$

$$T_A \leq +85^\circ\text{C}$$

Additional Design Selections:

$$R_4 = R_5 = (25 \text{ mV}) / ((5 \text{ V/V}) (60 \text{ pA}))$$

$$= 83.3 \text{ M}\Omega \rightarrow 20.0 \text{ M}\Omega$$

$$G_N R_4 = G_N R_5 = 100 \text{ M}\Omega$$

$$C_4 = C_5 = 100 \text{ pF}$$

Example Output Values:

$$I_{BN} G_N R_4 = 0.10 \text{ mV}, I_{BN} = 1 \text{ pA}$$

$$= 6.0 \text{ mV}, I_{BN} = 60 \text{ pA}$$

The 20 MΩ is comprised of two, easy to obtain, 10 MΩ resistors in series. Using a 18-bit ADC to measure V<sub>OUT</sub> should be adequate. Let's continue [Example A-2](#) at +125°C by using a different value for R<sub>4</sub> and R<sub>5</sub>:

## EXAMPLE A-3:

$$V_{OST} < \pm 3.8 \text{ mV}$$

$$T_A = +125^\circ\text{C}$$

Additional Design Selections:

$$R_4 = R_5 = (25 \text{ mV}) / ((5 \text{ V/V}) (5 \text{ nA}))$$

$$= 1 \text{ M}\Omega$$

$$G_N R_4 = G_N R_5 = 5 \text{ M}\Omega$$

$$C_4 = C_5 = 100 \text{ pF}$$

Example Output Values:

$$I_{BN} G_N R_4 = 0.25 \text{ mV}, I_{BN} = 50 \text{ pA}$$

$$= 25 \text{ mV}, I_{BN} = 5 \text{ nA}$$

This means that a 16-bit ADC is sufficient for this temperature.

## A.2.2 MEASUREMENT STRATEGY

Let's double check the MCP601's data sheet bias current specifications, for one temperature, at V<sub>DD</sub> = 2.7V and 5.5V.

**TABLE A-3: BIAS CURRENT MEASUREMENT POINTS**

Meas. No.	Nominal Bias Point			Switch Settings		Target Parameter
	V <sub>DD</sub> (V)	V <sub>CM</sub> (V)	V <sub>OUT</sub> (V)	SW <sub>4</sub>	SW <sub>5</sub>	
1	2.7	1.35	1.35	short	short	V <sub>OST</sub>
2				open	short	I <sub>BN</sub>
3				short	open	I <sub>BI</sub>
4	5.5	2.75	2.75	short	short	V <sub>OST</sub>
5				open	short	I <sub>BN</sub>
6				short	open	I <sub>BI</sub>

See [Equation A-6](#) for the parameter extraction equations.

## A.3 Limitations of These Test Circuits

Some of the more important limitations are:

- V<sub>CM</sub> is not accurately controlled (especially for CMRR)
- The common mode input range may be exceeded when I<sub>BN</sub>R<sub>4</sub> is very large
- The V<sub>OST</sub> resolution is not better than 10 μV to 20 μV
- Temperature gradients on the PCB cause thermo-junction voltages
- V<sub>OUT</sub> needs to be measured accurately in order to maintain reasonable accuracy on the extracted parameters. For instance, with V<sub>DD</sub> = 5.5V and a maximum V<sub>OST</sub>G<sub>N</sub> of 0.1V, an ADC at V<sub>OUT</sub> would need at least 16 bits in order to resolve V<sub>OST</sub> to 0.1%
- Measurements can be slower than with other solutions

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