AN722

Operational Amplifier Topologies and DC Specifications

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INTRODUCTION

Operational amplifiers (op amps) are as prolific in analog circuits as salt and pepper is on food. They are sprinkled throughout the sensor data acquisition system, performing a variety of functions. For instance, at the sensor interface, amplifiers are used to buffer and gain the sensor output. The current or voltage excitation to the sensor, quite often is generated by an amplifier circuit. Following the front end sensor circuitry, an op amp is used to implement a low pass, band pass or high pass filter. In this portion of the circuit, gain stages are also implemented using programmable gain amplifiers or instrumentation amplifiers whose building blocks are the op amp. Analog-to-Digital (A/D) converters are most typically driven by an amplifier in order to achieve good converter performance.

Each one of these amplifier applications place unique demands on the device, so that one performance specification may be critical in one circuit, but not necessarily in another. This application note defines the DC specifications of op amps and presents circuit applications where optimization of a particular specification is critical.

DEFINING THE OP AMP

Ideal Specifications

The op amp can be simply defined as an analog gain block with two signal inputs, two power supply connections and one output, as shown in Figure 1.

The input stage of the op amp has two terminals, the non-inverting (V_{IN+}) and inverting (V_{IN-}) inputs. For the ideal voltage feedback amplifier, both inputs are matched having no leakage current, infinite input impedance, infinite common mode rejection, zero noise and zero offset voltage (V_{OS}) between the terminals.

The power supply terminals (V_{DD} and V_{SS}) of the ideal op amp, have no minimum or maximum voltage restrictions. Additionally, the current from the power supply through the amplifier (I_{SUPPLY}, I_{DD} or I_Q) is zero and any variation in the power supply voltage does not introduce errors into the analog signal path.

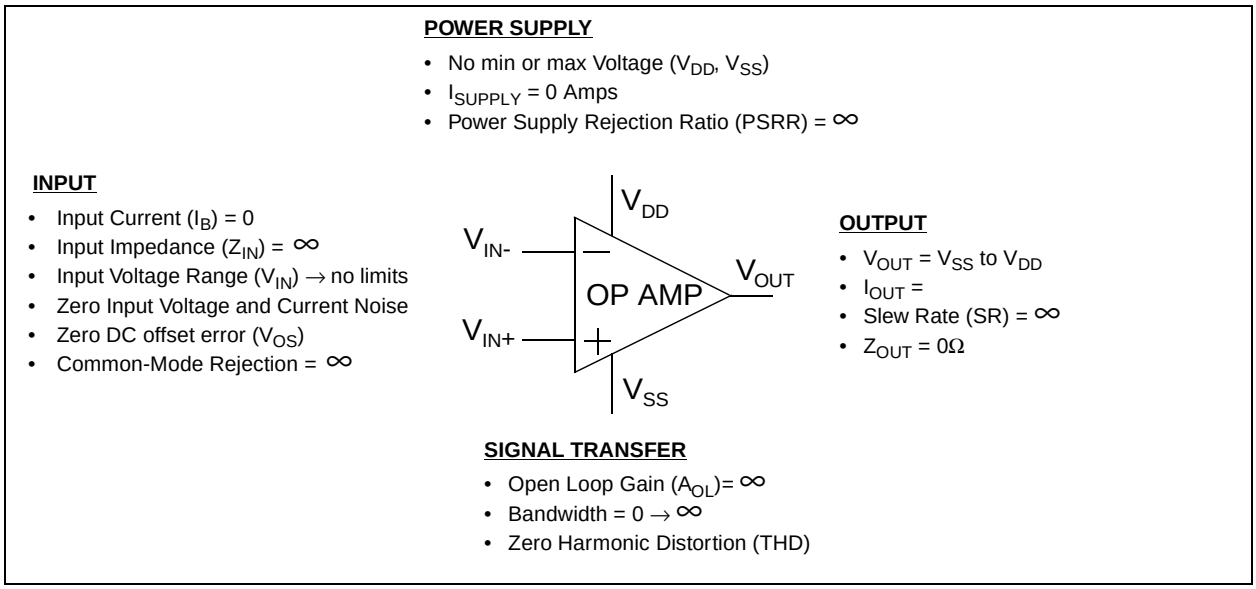

FIGURE 1: *The ideal op amp description can be separated into four basic categories: input, power supply, output, and signal transfer.*

In terms of the amplifier output, the swing capability equals or exceeds the voltage restrictions of the power supply. The output current (I_{OUT}) of this terminal can be infinite for indefinite periods of time, without causing reliability or catastrophic failures. The speed (SR) at which the output swings from rail to rail is instantaneous and the output impedance (Z_{OL} or Z_{CL}) is zero.

Finally, the open loop gain of the amplifier block is infinite and the bandwidth of the open loop gain is also infinite. To put the finishing touches on the signal transfer characteristics of the ideal amplifier, signals pass through the device without added distortion (THD) or noise.

Technology Limitations

This ideal amplifier does not exist. Consequently, performance specifications describe the amplifier so that the designer can assess the impact it will have on his circuit.

The errors that appear on the terminals of the op amp are a consequence of the semiconductor process and transistor implementation of the integrated circuit. In terms of the impact of the type of process that is used to design the amplifier, some generalities are summarized in Figure 2. These generalities are just that and not hard and fast rules.

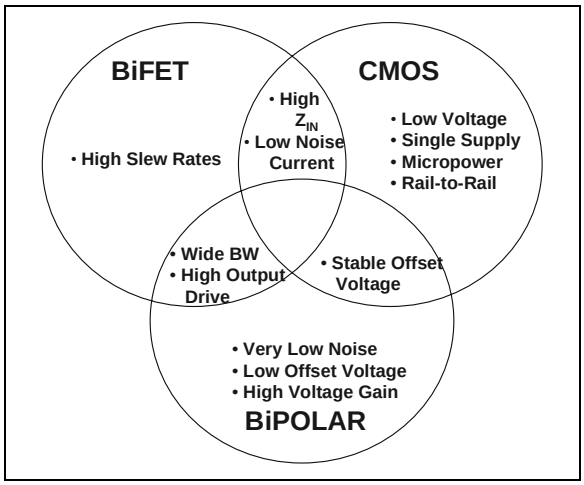

FIGURE 2: *Different IC processes render different advantages for amplifiers. The choices in processes for single supply amplifiers are Bipolar, CMOS and BiFET, which is a combination of Field Effect Transistors (FET) and Bipolar transistors.*

For instance, the BiFET op amp is designed using an FET (Field Effect Transistor) as the device at the input terminals and Bipolar for the remainder of the circuit. Op amp designed with this IC implementation have higher slew rates as compared to the pure Bipolar amplifier and CMOS amplifier.

In contrast, a pure Bipolar amplifier has NPN or PNP transistors at the input terminals. This allows the IC designer to achieve relatively low input offset voltage and voltage noise between the input terminals as well as higher open loop gains.

The commonality between the BiFET and Bipolar amplifiers are that they typically have wider bandwidths and higher output drive capability, as compared to the CMOS amplifier.

CMOS, on the other hand is well known for its low power, single supply op amps. The transistors in this style of amplifier are CMOS, allowing for an infinite input impedance and zero current leakage. This characteristic is similar in BiFET amplifiers. The degradation of these input impedances and leakage currents with the BiFET and CMOS input op amps are due to the required electrostatic discharge (ESD) cells that are added to the input terminals. CMOS amplifiers are also capable of rail-to-rail operation (in analog terms) while still having low quiescent current (current from the power supply).

The op amp specifications can be separated into two general categories, DC and AC. For the remainder of this application note, only the DC specifications will be discussed with accompanying detailed applications where that specification has an impact on the circuit performance. For discussions on AC specifications, refer to the application note from Microchip entitled “Operational Amplifier AC Specifications and Applications”, AN723. (*available December, 1999*)

DC SPECIFICATIONS

The DC specifications discussed in this application note are:

- Input Offset Voltage (V_{OS})
- Input Bias Current (I_B)
- Input Voltage Range (V_{IN} or V_{CM})
- Open Loop Gain (A_{OL})
- Power Supply Rejection (PSRR or PSR)
- Common-mode Rejection (CMRR)
- Output Voltage Swing (V_{OUT}, V_{OH}, or V_{OL})
- Output Resistance (R_{OUT}, R_{OL}, R_{CL}, Z_{OL}, or Z_{CL})
- Power Supply and Temperature Range (V_{SS}, V_{DD}, I_{DD}, and I_Q)

In Figure 3, these parameters are shown in their proper locations to allow for easy circuit evaluation and error analysis.

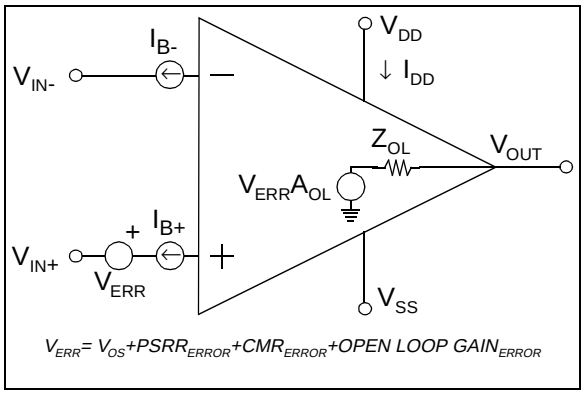

FIGURE 3: *DC parameters for the op amp are modeled in a way to assist definition of specifications and easy error analysis of circuits.*

For the remainder of this application note, these DC specifications will be defined and then evaluated within a sensitive application.

Input Offset Voltage (V_{OS})

Specification Discussion - The input offset voltage specification of an amplifier defines the maximum voltage difference that will occur between the two input terminals in a closed loop circuit while the amplifier is operating in its linear region. The input offset voltage is always specified at room temperature in terms of µV or mV. The over temperature specification can be guaranteed as µV/°C as well as an absolute value of µV or mV. Offset voltage is always modeled as a voltage source at the non-inverting input of the amplifier, as shown in Figure 3.

As with any amplifier specification, offset voltage can vary from part to part and with temperature, as shown in the distribution graphs in the Figure 4. The offset voltage of a particular amplifier does not vary unless the temperature, power supply voltage, common-mode voltage or output voltage changes, as shown in Figure 3 as part of V_{ERR}. The affects of these changes are discussed later.

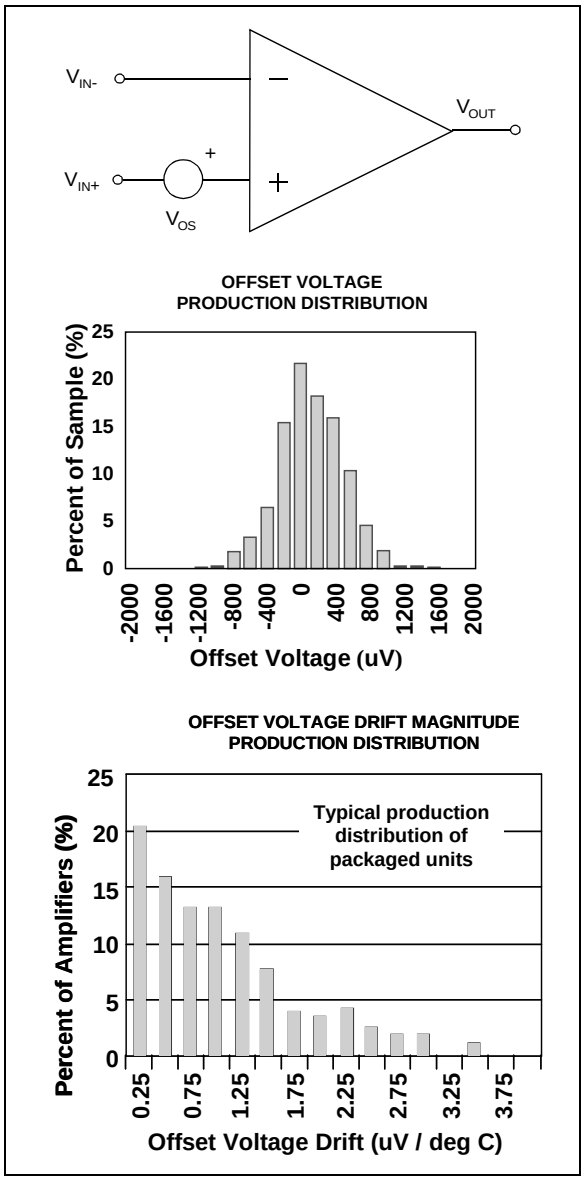

FIGURE 4: *The input offset voltage of an amplifier varies from part to part but always falls within the stated specification voltage range.*

Application Challenge - The offset voltage error of a particular amplifier may or may not be a problem, dependent on the application circuit. For instance, if a device is configured as a buffer (also known as a voltage follower), amplifiers with larger offset voltage errors, in the range of 2mV to 10mV, are usually not significantly different in performance than high precision amplifiers with extremely low offset voltage specifications, in the range of 100µV to 500µV. On the other hand, an amplifier with a high offset voltage that is in a high closed loop gain configuration can dramatically compromise the dynamic range of the circuit.

For example, the circuit in the Figure 5 is designed so that the analog input voltage (V_{IN}) is gained by:

$$V_{OUT} = (1 + R_F / R_{IN}) (V_{IN} + V_{OS})$$

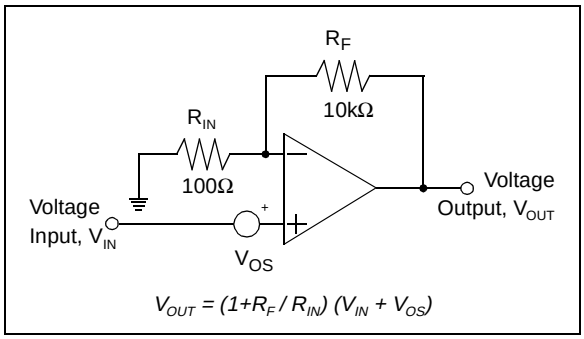

FIGURE 5: *An amplifier with a high input Offset Voltage can cause errors in the system, if the amplifier is configured in a high closed loop gain circuit.*

Unfortunately, the offset voltage of the amplifier is also multiplied by the same gain factor as the input signal. In this example, $(1 + R_F / R_{IN})$ is equal to 101V/V. An amplifier with an offset voltage of 1mV would produce a constant DC error at the output of 101mV. In a 5V system, 101mV lessens the dynamic range by approximately 2%.

Input Bias Current (I_B, I_{B+}, I_{B-}, and I_{OS})

Specification Discussion - All op amps have a leakage current that sources or sinks at both input terminals. Typically, this leakage current is called input bias current. The model for input bias current error is shown in Figure 3. The input offset current (I_{OS}) is equal to the difference between the input bias current at the non-inverting terminal (I_{B+}) minus the input bias current at the inverting (I_{B-}) terminal of the amplifier.

With CMOS and FET input amplifiers, the magnitude of the input bias current ranges from sub-pico amperes to several hundred pico amperes. The leakage at the input terminals of the CMOS amplifier usually does not come from the gate of the CMOS device but rather from the ESD cell. At room temperature, the input bias current of a CMOS amplifier can be less than a few tens of pico amperes. As the temperature increases, the ESD cells start to conduct current. This current appears at the input terminals of the amplifier.

In contrast, amplifiers with Bipolar inputs typically have input bias currents that range in the 10s of nano amps to several hundred nano amps. This current is the base current of the input Bipolar transistors. These amplifiers also have ESD cells, but the leakage from the base of the input transistor is much higher than the leakage from the ESD cells over temperature.

Application Challenge - Circuits that use high value resistors in the feedback loop or at the input of the amplifier are the most sensitive configurations for the op amp's input bias current error. For instance, if a high value resistor, such as 100kΩ is placed in series with the input of a Bipolar input amplifier that has an input bias current of 100nA, the resultant voltage is 100kΩ x 100nA or 10mV. This error at the input to the amplifier is added to any offset voltage error and then gained by the amplifier circuit.

In contrast, the input bias current of a CMOS amplifier could be 100pA. The voltage generated by the combination of this input bias current and a 100kΩ resistor is 10μV. In this scenario it is quite possible that the offset voltage error of the amplifier is greater than the error generated by the input bias current.

An example of a circuit that might use higher value resistors is a filter, such as the low pass filter shown in the Figure 6. In this circuit, the poles are established using the combination of resistors and capacitors. As the cut-off frequency of a low pass filter is decreased, the RC time constants that generate the poles increase. In the situation where a low frequency, low pass filter is required, it is easy enough to find higher value capacitors. However, if board real-estate is an issue, higher value resistors are a more economical alternative.

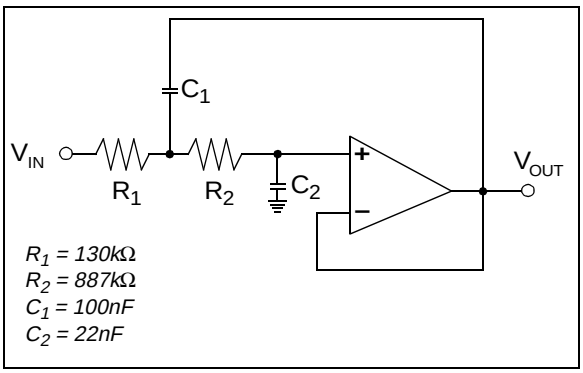

FIGURE 6: *This Sallen-Key, 2nd order, 10Hz, Butterworth, low pass filter circuit has two large resistors in series with the non-inverting input of the op amp. Input bias current errors from a Bipolar op amp will cause a considerable amount of error. In contrast, the input bias current from CMOS or BiFET amplifiers will be low enough not to cause appreciable errors.*

This RC relationship in combination with CMOS op amps can be used to an advantage with filters that have lower cut-off frequencies. Surface mount resistors can be found up to several mega ohms and surface mount film capacitors that are approximately the same size as the surface mount resistors can be found as high as several hundred nano farads. With this combination of passive devices, a compact, second order low pass filter can easily be designed down to 10Hz or lower.

In the example in Figure 6, a Bipolar amplifier with an input bias current of 100nA would generate a DC error through the resistor combination of R_1 and R_2 of 102.7mV. In contrast, a CMOS amplifier with an input bias current of 100pA would generate a DC error of 102.7μV.

Input Voltage Range (V_{IN} or V_{CM})

Specification Discussion - Each of the two input pins of the op amp has voltage swing restrictions. These restrictions are due to the input stage design. In the device product data sheet, the input voltage restrictions are clearly defined in one of two ways. Most commonly, the Input Voltage Range, V_{IN}, is specified as a separate line item in the specification table. This specification is also usually defined as a condition for the CMRR specification, input common-mode voltage range, V_{CM}. The more conservative specification of the two is where the input voltage range is called out as a CMRR test condition because the CMRR test validates the input voltage range with a second specification.

The input voltage range is more a function of the input circuit topology rather than the silicon process. Although the input devices of the amplifier can be CMOS, Bipolar or FET, there are three basic topologies that are used to design the input stage of single supply, voltage feedback amplifiers. These topologies are shown with a CMOS input stage in Figure 7. In Figure 7a, PMOS transistors (Q_1 and Q_2) are used for the first device at the input terminals. With this particular topology, the gate of both transistors can go 0.2 to 0.3V below the negative power supply voltage before these devices leave their active region. However, the input terminal can not go any higher than several hundred millivolts from the positive power supply voltage before the input devices are pulled out of their linear region. An amplifier designed with a PMOS input stage will typically have an input range of V_{SS} -0.2V to V_{DD} - 1.2V.

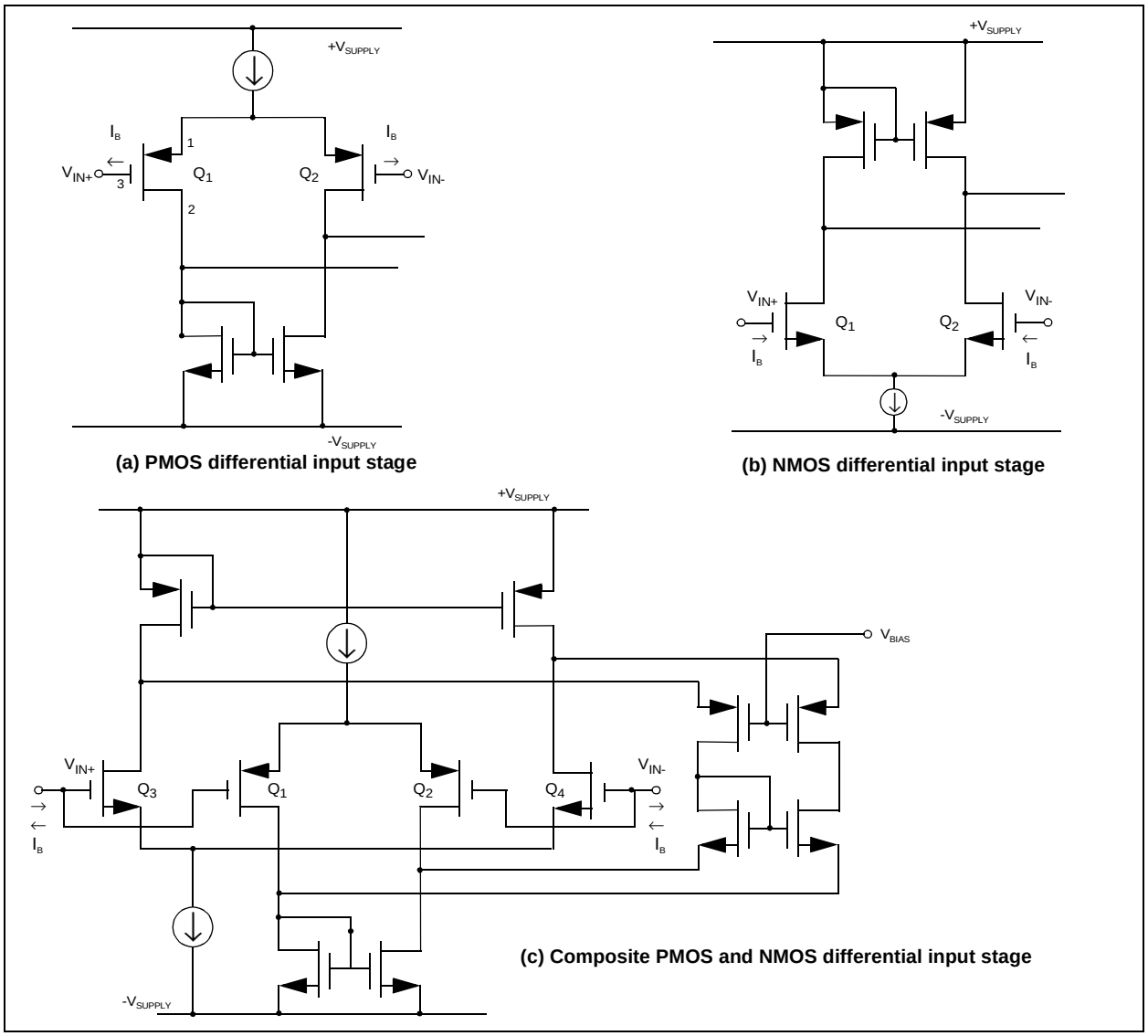

FIGURE 7: *The input voltage range of an op amp is dependant on the topology of the input stage of the amplifier. The input stage can be constructed of PMOS (a) devices allowing for the input to swing below the negative supply or a NMOS differential pair (b) where the inputs can swing above the positive supply. A composite input stage (c) uses PMOS and NMOS differential pairs so the input voltage range can extend from above the positive rail to below the negative rail.*

If the amplifier is designed with NMOS input transistors as shown in Figure 7b, the input range is restricted near the negative power supply voltage. In this case, the input terminals can be taken to a few tenths of a volt above the positive supply rail, but only to 1.2V above the negative supply rail.

If an amplifier input stage uses PMOS and NMOS transistors, it is configured as a composite stage, as shown in Figure 7c. With this topology, the amplifier effectively combines the advantages of the PMOS and NMOS transistors for true rail-to-rail input operation. When the input terminals of the amplifier are driven towards the negative rail, the PMOS transistors are turned completely on and the NMOS transistors are completely off. Conversely, when the input terminals are driven to the positive rail, the NMOS transistors are in use while the PMOS transistors are off.

Although, this style of input stage has rail-to-rail input operation there are trade-offs. This design topology will have wide variations in offset voltage. In the region near ground, the offset error of the PMOS portion of the input stage is dominant. In the region near the positive power supply, the input stage offset error is dominated by the NMOS transistor pair. With this topology, the offset voltage error can change dramatically in magnitude and sign as the common mode voltage of the amplifier inputs extend over their entire range.

The basic topologies shown in Figure 7 can be used with FET input or Bipolar input amplifiers. In the case of the FET input amplifier, the offset errors between the PFET and NFET are consistent with the CMOS errors with the circuit shown in Figure 7c. With Bipolar input stages, input offset voltage variations are still a problem, but input bias current is an additional error that is introduced. The nano ampere base current of an NPN transistor comes out of the device, while the nano ampere base current of a PNP transistor goes into the device.

Application Challenge - The input voltage range restrictions become critical in a subset of op amp circuit applications. For instance, if an op amp is configured as a voltage follower, it will most likely exhibit limitations in linearity due the input stage restrictions. This type of circuit is shown in Figure 8a, along with a current monitor circuit in Figure 8b.

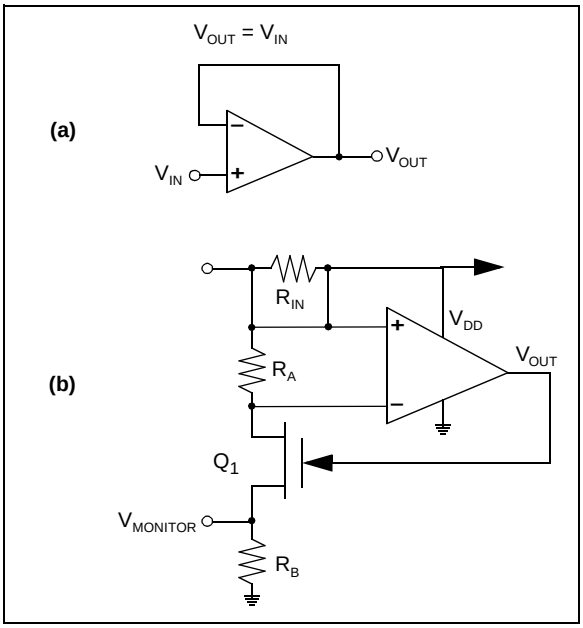

FIGURE 8: *If an amplifier is used as a buffer (a), the input devices of the operation amplifier may limit the input range of the buffer. If an amplifier is used in a high power supply sense circuit (b), the input stage must be able to extend to the positive rail.*

A buffer circuit configuration (Figure 8a.), requires rail-to-rail operation of the amplifier at its inputs as well as its outputs.

The high side current monitor circuit (Figure 8b), uses an op amp that must have an input voltage range up to the positive power supply rail. This circuit design senses the amount of current that is coming from the power supply. When the current exceeds 2A, the non-inverting input of the amplifier falls below the inverting input. As a result, that output goes low which turns off the JFET, Q_1, pulling the drain of the JFET low. This action brings the monitor output low.

These two applications present special requirements on the op amp. Most typically, an op amp is designed with a closed loop gain greater than one. In this instance, the output stage restrictions will limit the linear performance of the amplifier before the input stage will.

Open Loop Gain (A_{OL})

Specification Discussion - The Open Loop Gain of an op amp is the ratio of change in output voltage signal to the change in differential input voltage offset. This parameter is measured with or without a load. Ideally, the open loop gain of an amplifier should be infinite. In reality, the open loop gain, A_{OL}, is less than ideal at DC ranging from 95dB to 110dB. This can be translated into volts per volts with the formula:

$$A_{OL}\ (V/V) = 10^{(A_{OL}(dB)\ /\ 20)}$$

Using this formula, a 10µV differential input signal to an amplifier with an open loop gain of 100dB (10^5 V/V) in an open loop configuration would be gained to the output of the amplifier to 1V.

In production runs, the open loop gain can vary up to 30% from part to part, consequently, a closed loop system is a more desirable configuration when using an amplifier, unless the amplifier is used as a comparator. With a closed loop system, the gain is dependent on the accuracy of the resistors in the circuit.

In a closed loop system, the effects of the open loop gain error is easily determined with:

$$A_{OL}\ (dB) = 20\ log\ (\Delta V_{OUT} / \Delta V_{OS})$$

This formula states that a change in the output voltage of the closed loop system will generate a small change in offset voltage. The offset voltage error is then gained by the closed loop system, generating a gain error. (Refer to Figure 3, where ΔV_{OS} = open loop gain error.)

A load will degrade the open loop gain performance. Some manufacturers recognize this and specify more than one test condition.

Power Supply Rejection (PSRR)

Specification Discussion - The power supply rejection ratio specification quantifies the amplifier's sensitivity to power supply changes. Ideally, the power supply rejection ratio should be infinite. Typical specifications for a power supply rejection ratio of an amplifier range from 60dB to 100dB.

As is with the open loop gain (A_{OL}) characteristics of an amplifier, DC and lower frequency power supply noise is rejected more than at higher frequencies. In a closed loop system, a less than ideal power supply rejection capability of an amplifier manifests itself as an offset voltage error as shown in Figure 3 ($PSRR_{ERROR} = \Delta V_{OS}$). This error is best described with the formula:

$$PSRR(dB) = 20\ log\ (\Delta V_{SUPPLY} / \Delta V_{OS})$$

The formula that describes power supply rejection is:

$$PSR(V/V) = \Delta V_{OS} / \Delta V_{SUPPLY}$$

Where:

$$V_{SUPPLY} = V_{DD} - V_{SS}$$

Application Challenge - An application where power supply rejection is critical is shown in Figure 9. In this circuit, a battery is used to power an amplifier which is configured in a high, closed loop gain of 101V/V. During the life of the battery, the output voltage ranges from 5.75V down to 4.75V. If the power supply rejection of the amplifier is 500µV/V (or 66dB), the error at the output of the amplifier over time would be 50.5mV. In a 12-bit system with a full-scale range of 4.096V, this would equate to a 50.5 counts worth of offset change over the life of the battery.

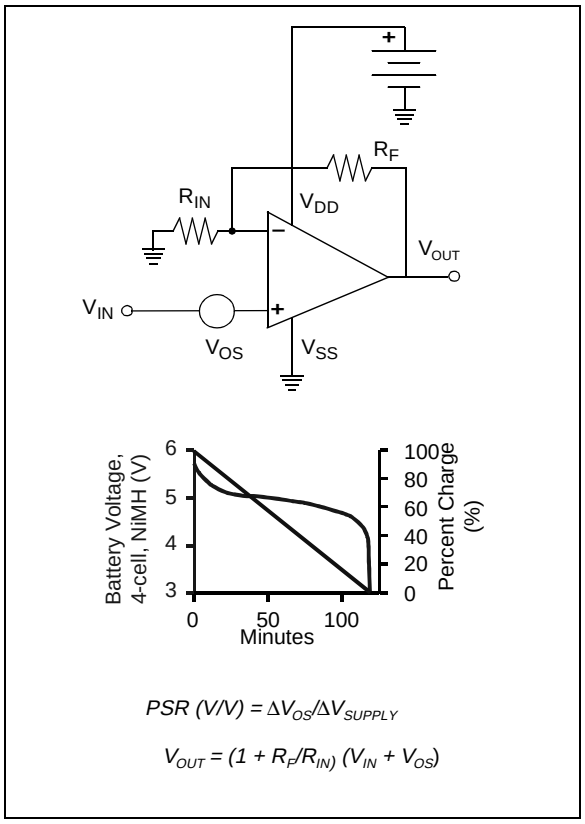

FIGURE 9: *A battery powered application can see a change in power supply voltage of several hundreds of millivolts over the life of the product. If an op amp is configured with a high closed loop gain in these types of applications, it must have good DC power supply rejection.*

Common Mode Rejection Ratio (CMRR)

Specification Discussion - The Common Mode Rejection Ratio of an amplifier describes the amplifier's input sensitivity to equivalent voltage changes of both inputs. This error manifests itself as an offset error ($CMRR_{ERROR}$), as shown in Figure 3.

$$CMRR(dB) = 20\ log\ (\Delta V_{CM} / \Delta V_{OS})$$

Where:

$$\Delta V_{OS} = CMRR_{ERROR}$$

Application Challenge - The specification range for CMRR in single supply amplifiers is from 45dB up to 90dB. Typically, this error becomes an issue when an amplifier is in a circuit where the input common mode voltage changes with input signal. A good example where this is the case, is when the amplifier is in a non-inverting configuration. A common circuit that has this configuration is shown in the Figure 10.

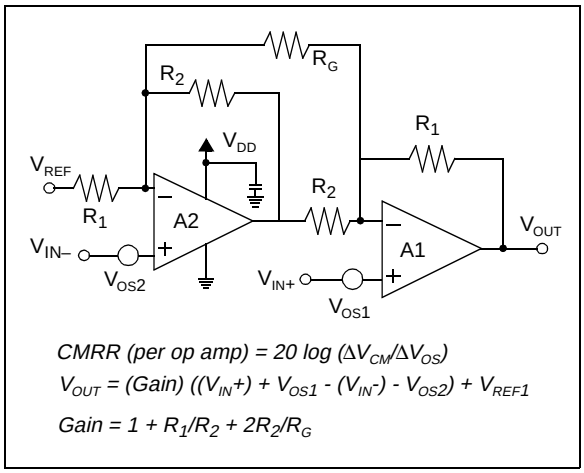

FIGURE 10: *A poor common mode rejection capability with either amplifier will cause an offset error that is gained to the output of the circuit.*

Voltage Output Swing (V_{OUT}, V_{OH}, or V_{OL})

Specification Discussion - The output swing specification of an op amp defines how close the output terminal of the amplifier can be driven to the negative or positive supply rail under defined operating and load conditions. Unlike the input voltage range (V_{IN}) specification, the voltage output swing of an amplifier is not as well defined from manufacturer to manufacturer. The output current as well as the amplifier's open loop gain (A_{OL}) are related to this specification. The output current is a test condition for the voltage output swing specification.

It is also a test condition for the open loop gain test, which validates the voltage output swing test with a second amplifier specification.

The output swing capability of the amplifier is dependent on the output stage design and the amount of current that the output stage is driving under test. With this portion of the specification, care should be taken when comparing amplifiers.

For instance, a single supply amplifier, MCP601, is used to generate the data in Table 1. It should be noted that the defined conditions of this specification have a significant influence on the amplifier's performance capability. All of these conditions, as well as others, can be found in op amp data sheets.

The key to comparing voltage output swing specifications, is to determine the amount of current that the amplifier is sinking or sourcing. The smaller the output current is, the closer the amplifier will swing to the rail.

If the load is specified as a current, this determination is easy. However, if the load is reference to $(V_{DD} – V_{SS})$ /2 + V_{SS}, the output current is determined by dividing the voltage across the load resistor by the load resistor. It is useful to note that when the load is referenced to $(V_{DD} – V_{SS})/2 + V_{SS}$, the output of the amplifier will be sourcing or sinking half the current, as when the load is referenced to V_{DD} or V_{SS}.

The device in Table 1 was tested with the V_{DD} equal to 5V and V_{SS} equal to ground. Since this data was taken with one device, it does not necessarily represent the performance of all devices in the product family.

Output Voltage Swing	Test Conditions	Measured Output Swing from V_{SS} (mV)	Measured Output Swing from V_{DD} (mV)
High, to V_{DD}	w / 10kΩ load referenced to $(V_{DD} – V_{SS}) / 2 + V_{SS}$		11.2
High, to V_{DD}	w / 10kΩ load referenced to V_{SS}		20.4
High, to V_{DD}	w / 10kΩ load referenced to V_{DD}		1.95
High, to V_{DD}	w / amplifier source current equal to 100µA		3.8
Low, to V_{SS}	w / 10kΩ load referenced to $(V_{DD} – V_{SS}) / 2 + V_{SS}$	11.6	
Low, to V_{SS}	w / 10kΩ load referenced to V_{SS}	3.7	
Low, to V_{SS}	w / 10kΩ load referenced to V_{DD}	25.5	
Low, to V_{SS}	w / amplifier sink current equal to 100µA	8.1	

TABLE 1: *This data was taken with one sample of the MCP601 op amp and demonstrates the effects of the output conditions on the output swing performance of that amplifier. This data was taken with no regard to the open loop gain of the amplifier.*

The output voltage swing versus input offset voltage of this amplifier is shown in Figure 11. By using this plot, the open loop gain of the device can be calculated as the slope between two points. For example, the open loop gain of this amplifier using V_{OUT} = 1V to 4V, is 75dB.

With this plot, it is noticeable that the linearity of the amplifier starts to degrade long before the output swing maximums are reached. If the output of an amplifier is operated beyond the linear region of this curve, the input to output relationship of the signal will be non-linear.

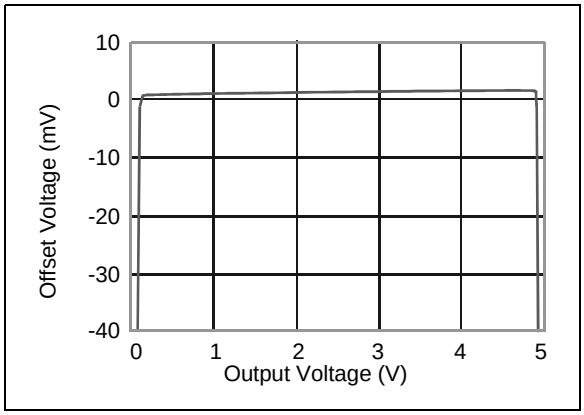

FIGURE 11: *This graph shows the relationship between the output swing of an amplifier and input offset voltage with a 25kΩ load and V_{DD} = 5V. The open loop gain of the amplifier can be calculated by selecting two points on the graph and calculating the slope. As the output swing of the amplifier goes towards the rail, the amplifier function eventually breaks down. This is first manifested with changes in input offset voltage.*

Output Impedance (R_{OUT}, R_{CL}, R_{OL}, Z_{CL}, Z_{OL})

Specification Discussion - The fact that the output impedance of an op amp is low, makes the device useful in terms of "isolating" the impedance of two portions of a circuit. For this reason, low output impedance of an op amp is an important characteristic, but the precise output impedance is usually is not specified.

When the output impedance is specified, it is given in terms of a resistance or impedance of a closed loop configuration (R_{CL} or Z_{CL}) or an open loop configuration (R_{OL} or Z_{OL}). Output impedance is most often specified as resistance.

Closed loop output resistance is the easiest to measure and is equal to:

$$R_{CL} = \Delta V_{OUT} / \Delta I_L$$

where

ΔV_{OUT} = the change in output voltage and

ΔI_L = the change in output current with a change in output voltage

The effective closed loop output impedance is less than the open loop output impedance by a factor equal to the reciprocal of the loop gain. The loop gain is equal to the open loop gain of the amplifier divided by the closed loop gain of the non-inverting circuit. For the circuit shown in Figure 12, the open loop resistance is equal to:

$$R_{CL} = R_{OL} / (A_{OL} / (1 + R_F / R_{IN}))$$

In this formula ($1 + R_F / R_{IN}$), is the non-inverting closed loop gain. This closed loop gain is also known as 1/β.

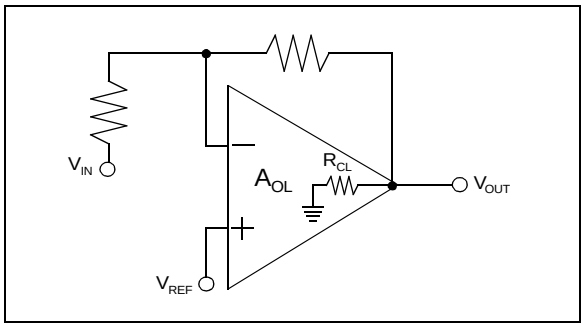

FIGURE 12: *The closed loop output resistance of an amplifier is lessened by the magnitude of the open loop gain of the amplifier.*

Power Supply Requirements (V_{SS}, V_{DD}, I_{DD}, I_Q)

Specification Discussion - Power supply voltage defines the acceptable difference between V_{DD} and V_{SS} which allows linear operation of the amplifier. If this voltage difference is less than specification, the amplifier may not operate reliably. If the power supply voltage is greater than specified, the amplifier most likely will operate as expected, but it is possible that damage may occur due to overvoltage stress on the internal transistors in the amplifier.

The power supply range is usually listed as a separate line item in the specification table in the product data sheet. Occasionally, the specification is called out as a condition under the PSRR specification.

Power supply current (I_{DD} or I_Q) is specified with no load. Typically, if a load is applied to the amplifier, a source current will primarily be pulled from V_{DD}, through the op amp output stage, and then through the load. A sink current will primarily result in an increase of V_{SS}.

Temperature Range

There are three types of temperature ranges that are specified with op amps.

- *Specified Temperature Range* - The range where the amplifier will meet specifications as called out in the specification table.
- *Operating Temperature Range* - The range where the amplifier will operate without damage but performance is not necessarily guaranteed.
- *Storage Temperature Range* - Defines the temperature maximums and minimums where the package will not sustain permanent damage. In this range the amplifier may not operate properly.

CONCLUSION

When searching for the right amplifier for an application, various performance specifications need to be taken into consideration. The first set of specifications to consider are the affects of the DC limitations of the amplifier. In single supply applications, amplifier errors such as input voltage swing, input offset voltage and input bias current could reduce the dynamic range of the amplifier. Conversely, in high gain circuits, the output voltage swing could cause signal clipping problems.

The second set of specifications to consider are the AC specifications. These issues are discussed in detail in the application note from Microchip entitled “Operational Amplifier AC Specifications and Applications”, AN723 (*available December, 1999*.)

REFERENCES

Wait, Huelsman, Korn, Introduction to Operational Amplifier Theory and Applications, *McGraw Hill, 1975*

“Operational Amplifier AC Specifications and Applications”, Baker, Bonnie, *Microchip Technology, Inc. AN723 (available December, 1999)*

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