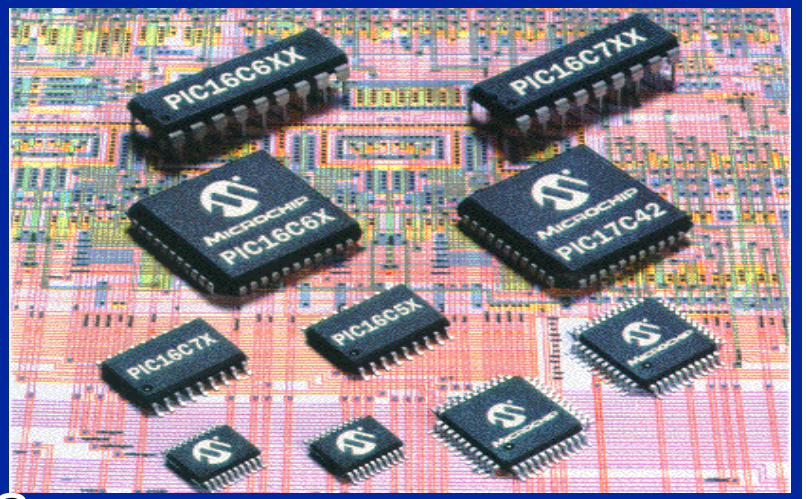
MICROCHIP

Architecture (x14)

MICROCHIP

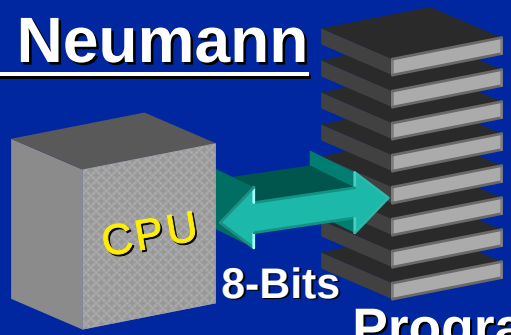
PICmicro® MCU Architecture

- RISC Microcontroller Features
- The high performance of the PICmicro can be attributed to the following:
  - Harvard Architecture
  - Instruction Pipelining
  - Register File Concept
  - Single Cycle Instructions
  - All Single Word Instructions
  - Long Word Instruction
  - Reduced Instruction Set
  - Orthogonal Instruction Set

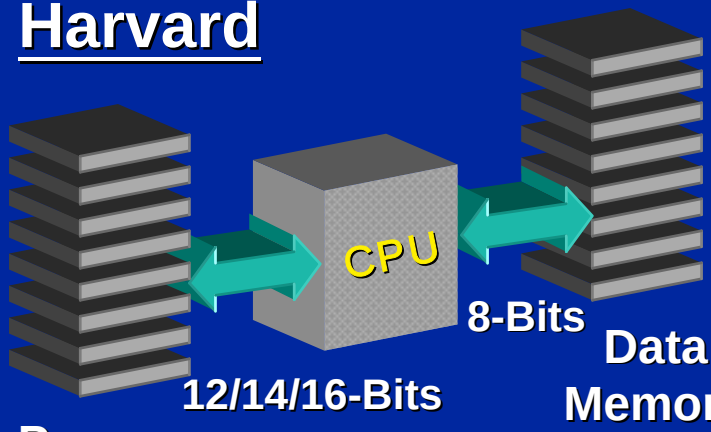


PICmicro MCU Architecture
Harvard Architecture

Von Neumann



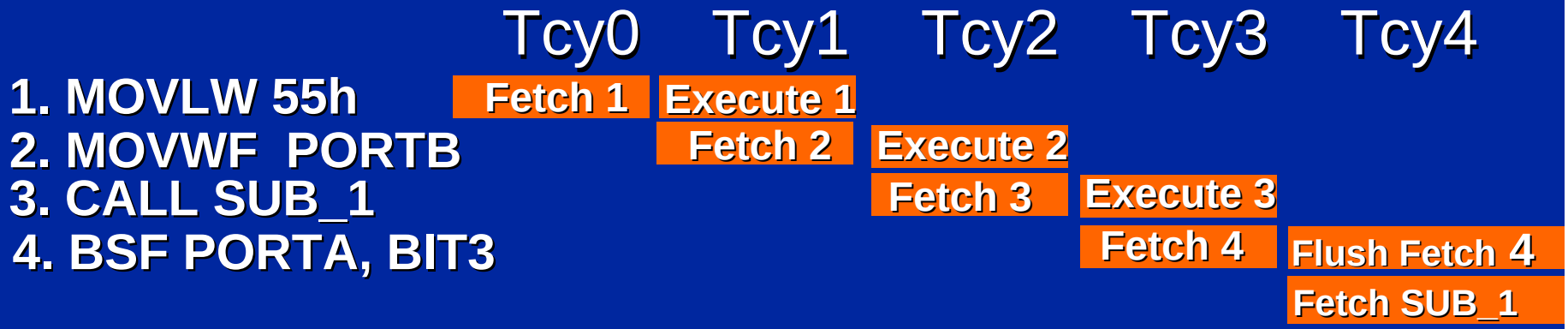
Harvard



- Fetches instructions and data from one memory.
  - Limits Operating Bandwidth
- Two separate memory spaces for instructions and data.
  - Increases throughput
  - Different program and data bus widths are possible

PICmicro MCU Architecture
Pipelining

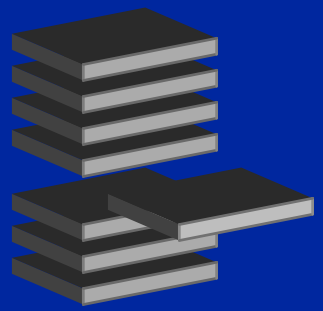
- In most microcontrollers, instructions are fetched and executed sequentially.
- Allows overlap of fetch and execution.
- Makes single cycle execution.
- Program branches (e.g. GOTO, CALL or Write to PC) takes two cycles.



PICmicro MCU Architecture
Long Word Instruction

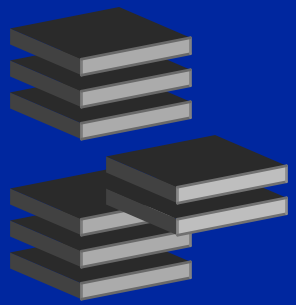
- Separate instruction/data bus allows different bus widths.
- PICmicro word-length 12-, 14- or 16-bits.
- Harvard architecture: single-word/single-cycle instruction.
- 2k x 14 words on a PIC16CXX is approximately equivalent to 4k x 8 words on other 8-bit MCUs.
- Single-cycle access increases execution bandwidth.

PICmicro MCU Architecture
Long Word Instruction (con't)



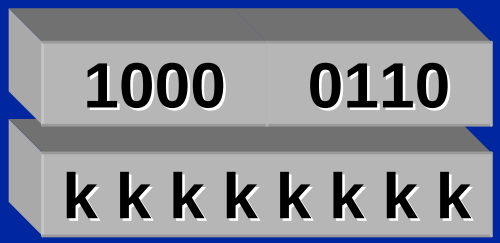
PICmicro

```
movlw     #imm<8>
```

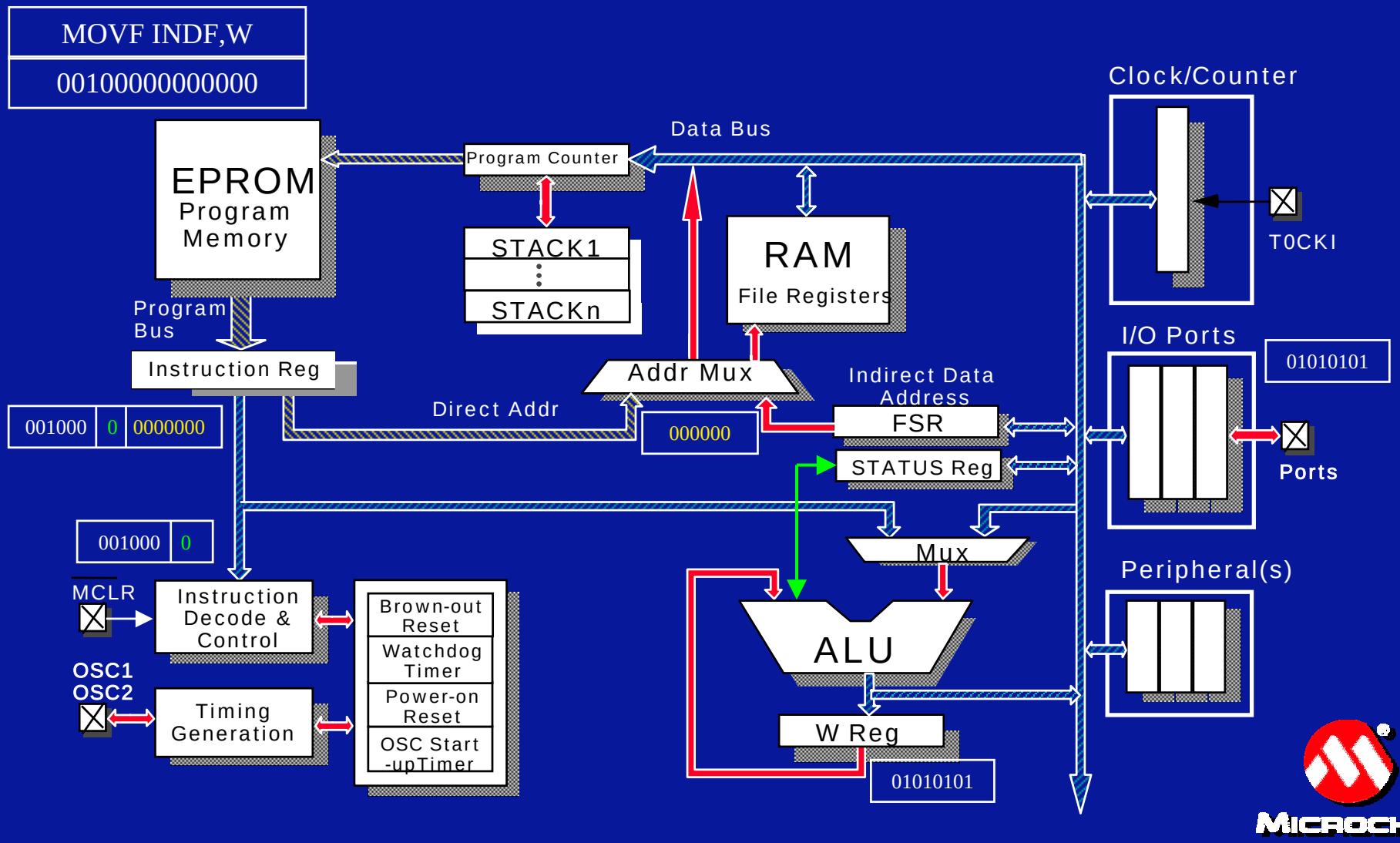


MC68HC05

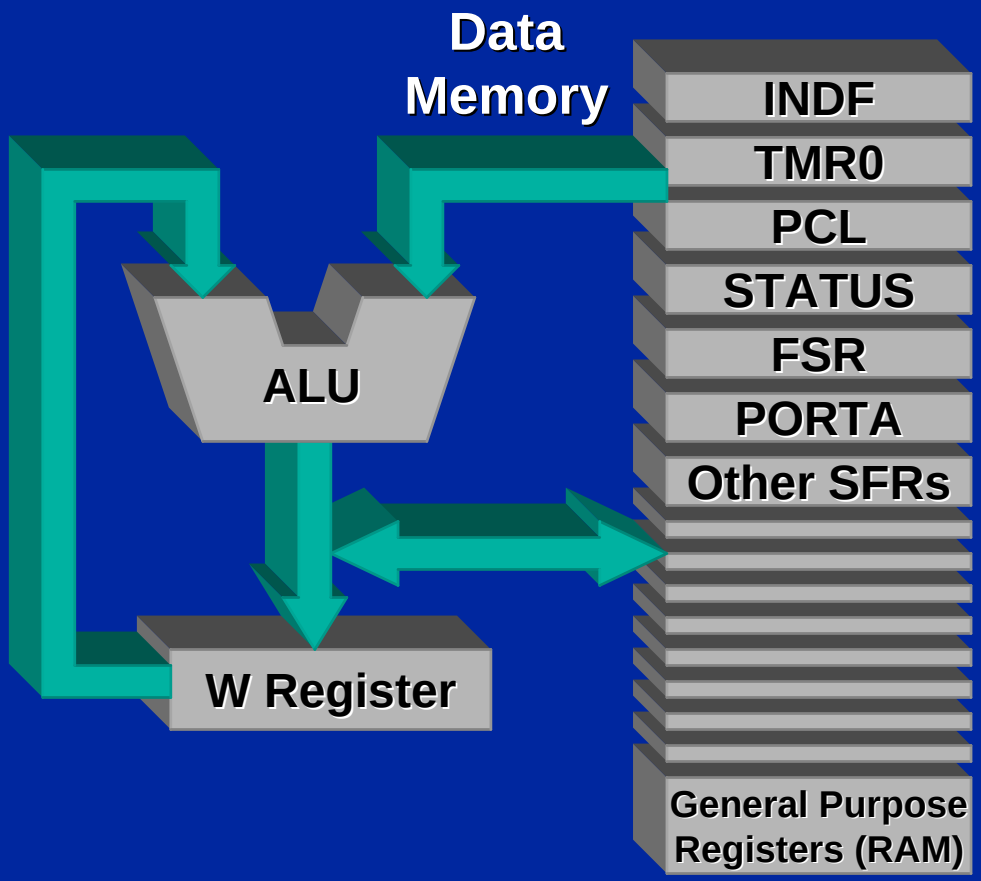
```
ldaa #imm<8>
```



PICmicro MCU Architecture
Block Diagram



PICmicro MCU Architecture
Register File Concept

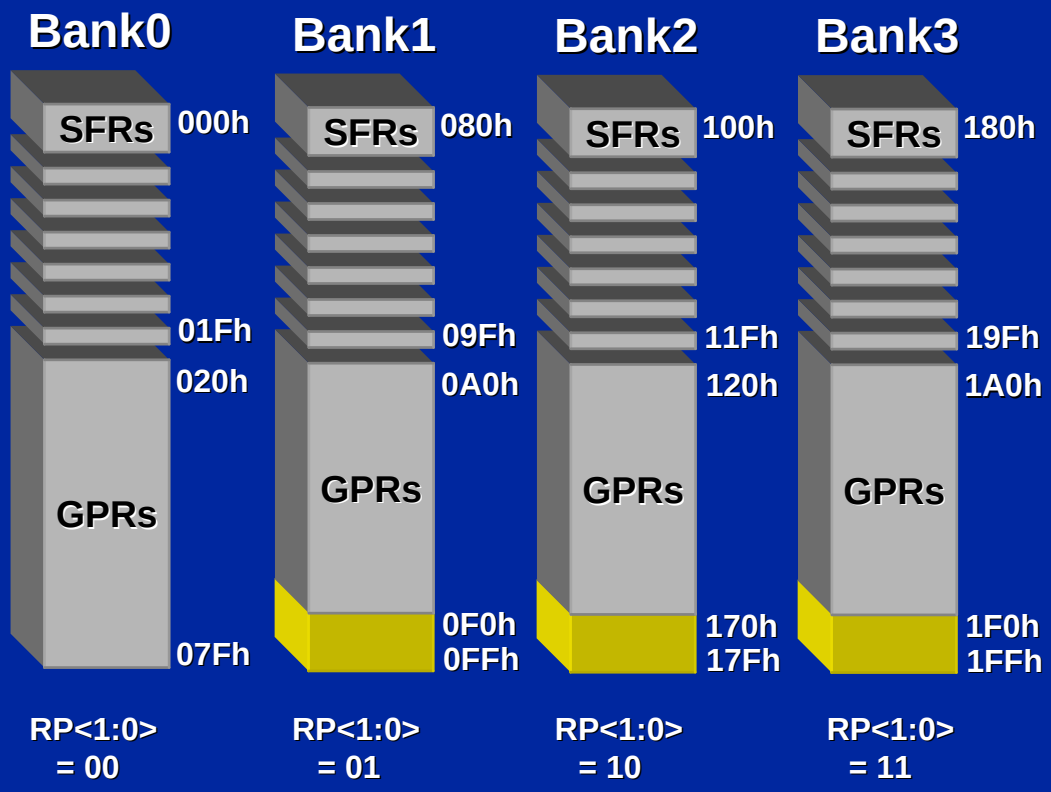


- RAM is a bank of general purpose registers.
- Peripherals (I/O) are registers.
- All instructions operate on any register.
- Long word instruction allows direct addressing of registers.

14-bit Instruction Format Example:

Op code <7>	Direct data addr <7>

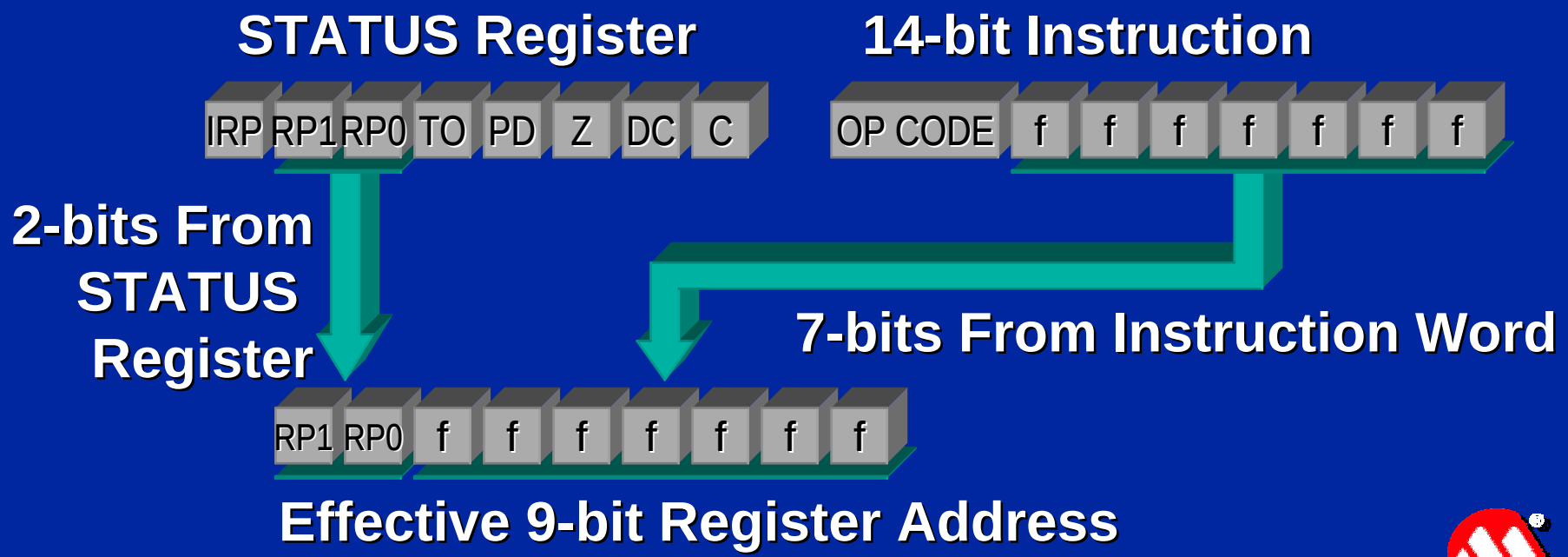
PIC16CXX MCU Architecture
Data Memory



- Four banks each of 128 bytes of Data Memory
- Special Function Registers (SFRs) are mapped in top 32 locations
- Banks selected by RP0,1 and IRP in Status register

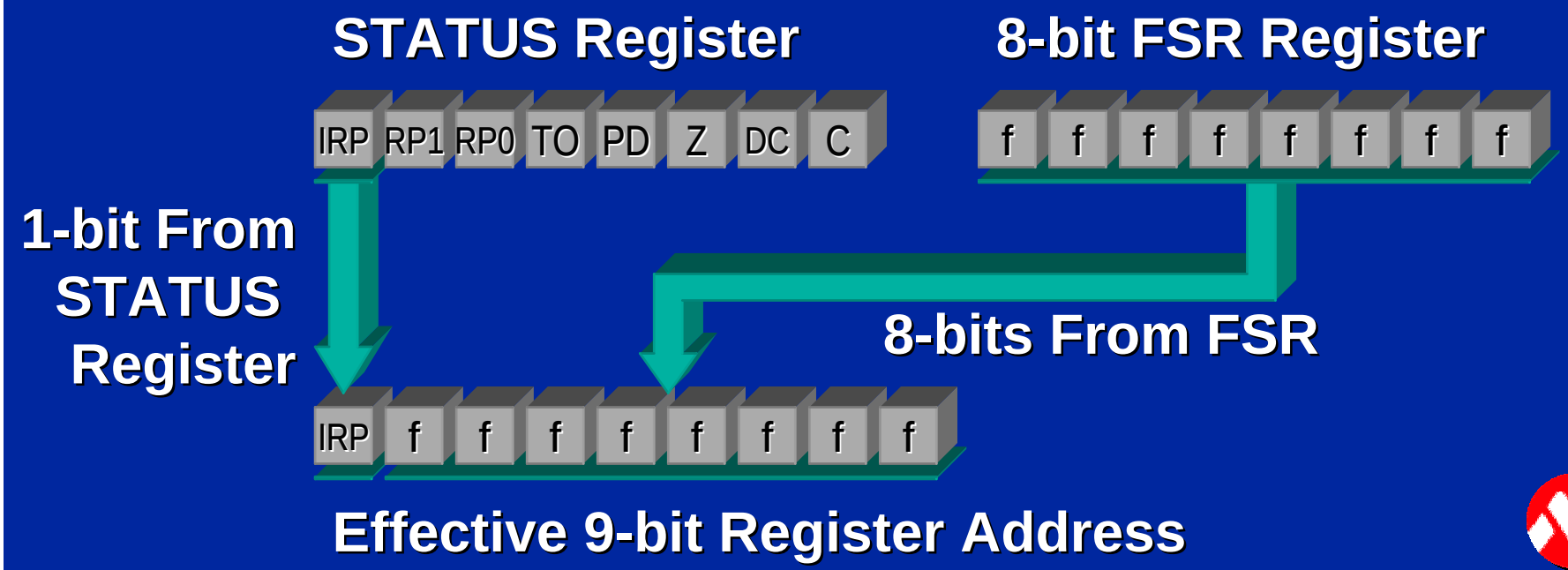
PICmicro MCU Architecture
Data Memory: Direct Addressing

- 7-bit direct address from the instruction
- 2-bits from STATUS register



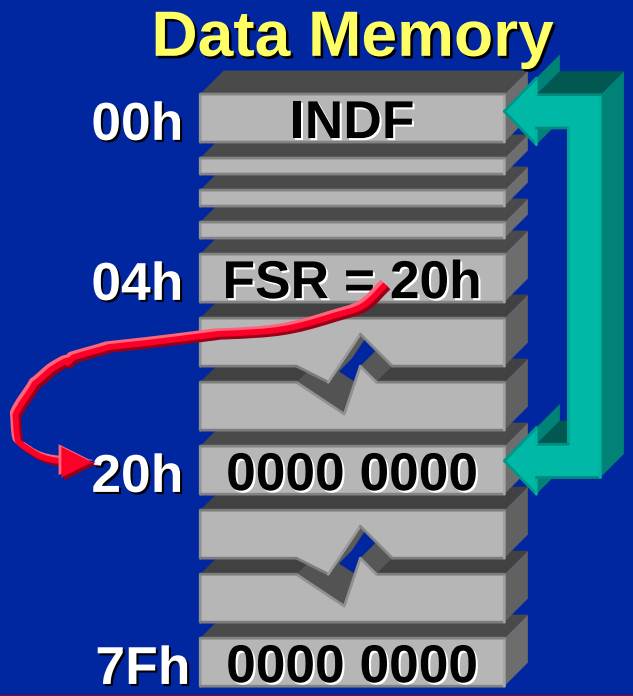
PICmicro MCU Architecture
Data Memory: Indirect Addressing

- 8-bit indirect address from the FSR (File Select Register).
- 1-bit from STATUS register.



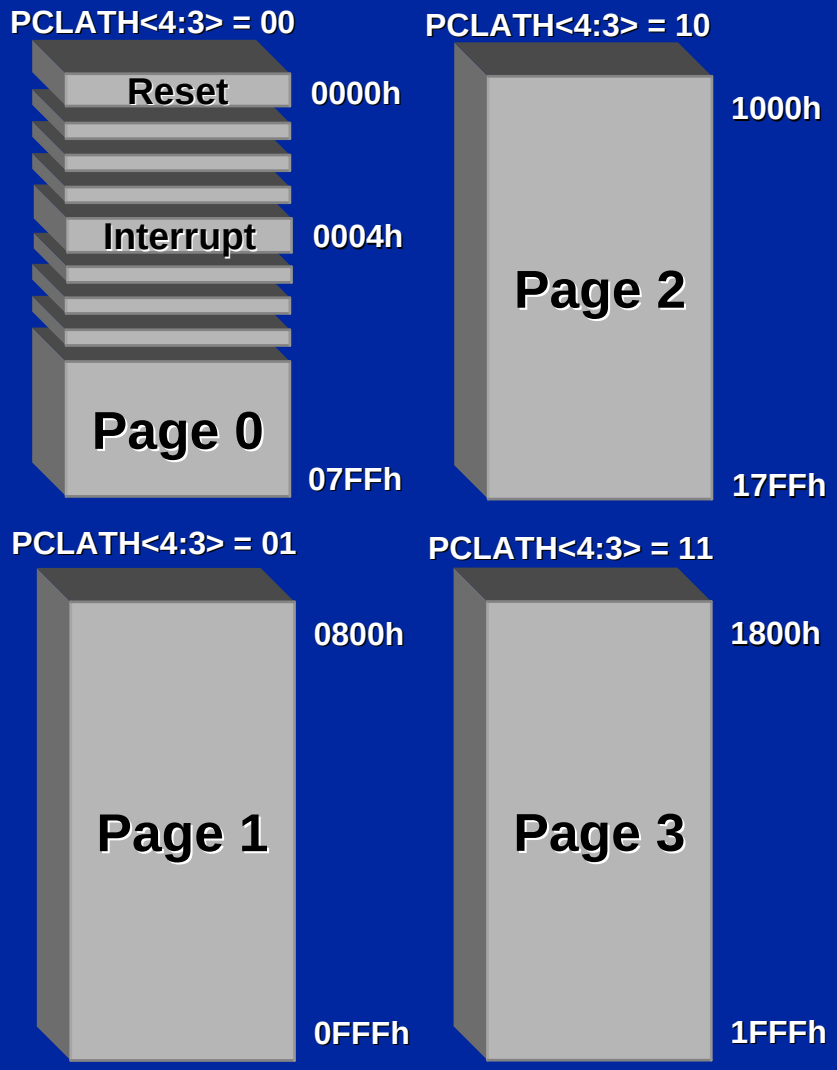
PICmicro MCU Architecture
Data Memory: Indirect Addressing

- Clear all RAM locations from 0x20 to 0x7F.
  - Indirect address is loaded into FSR.
  - Every time INDF is used as operand, register pointed to by FSR is actually used.




```
        movlw   0x20
        movwf   FSR
LOOP    clrf    INDF
        incf    FSR,F
        btfss   FSR,7
        goto    LOOP
        <next instruction>
```

PIC16CXX MCU Architecture
Program Memory

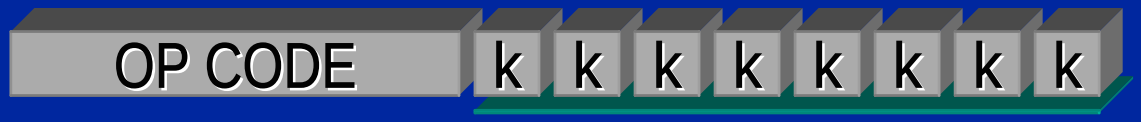


- Maximum 8K words (13 bits) of program memory space
- Four Pages each 2K words (11 bits)
- Page access using PCLATH<4:3>
- Reset Vector at 0000h
- Interrupt Vector at 0004h

PICmicro MCU Architecture
Program Memory: Immediate Operation

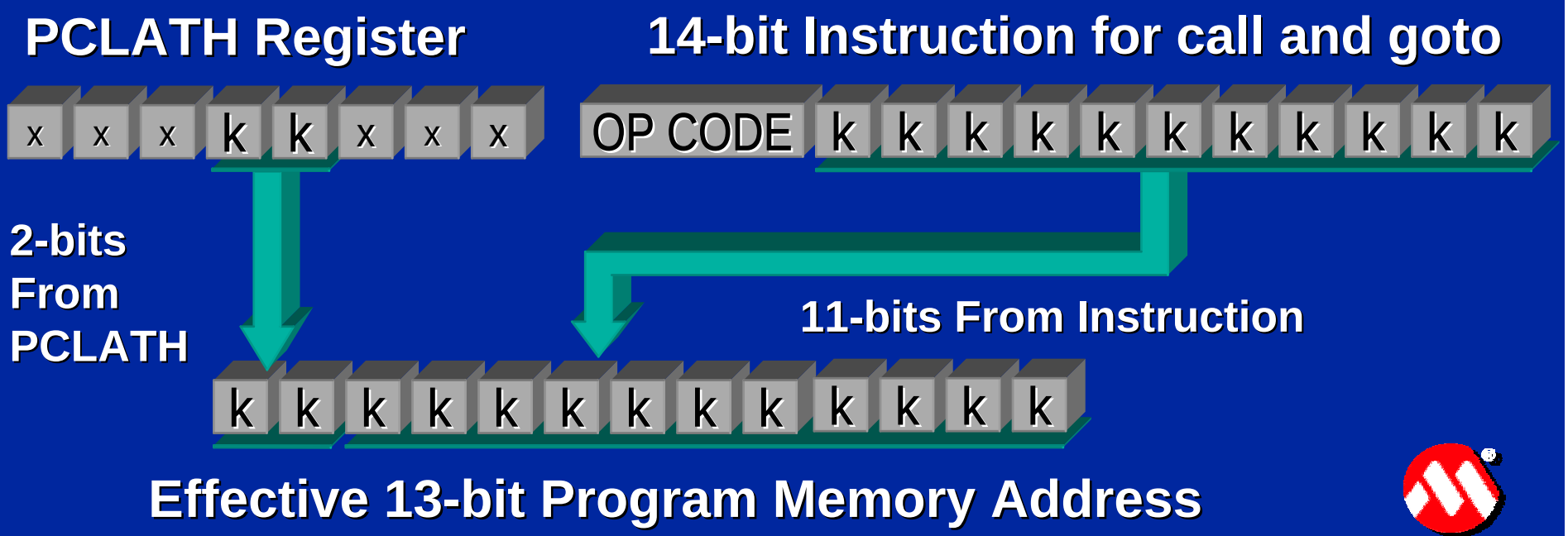
- 8-bit constant (literal) value included in instruction word.
- Used by literal instructions such as movlw, addlw, retlw, etc.

14-bit Instruction for Literal Instructions



PICmicro MCU Architecture
Program Memory: PC Absolute Addressing

- Used by control instructions CALL and GOTO to modify the PC (Program Counter)

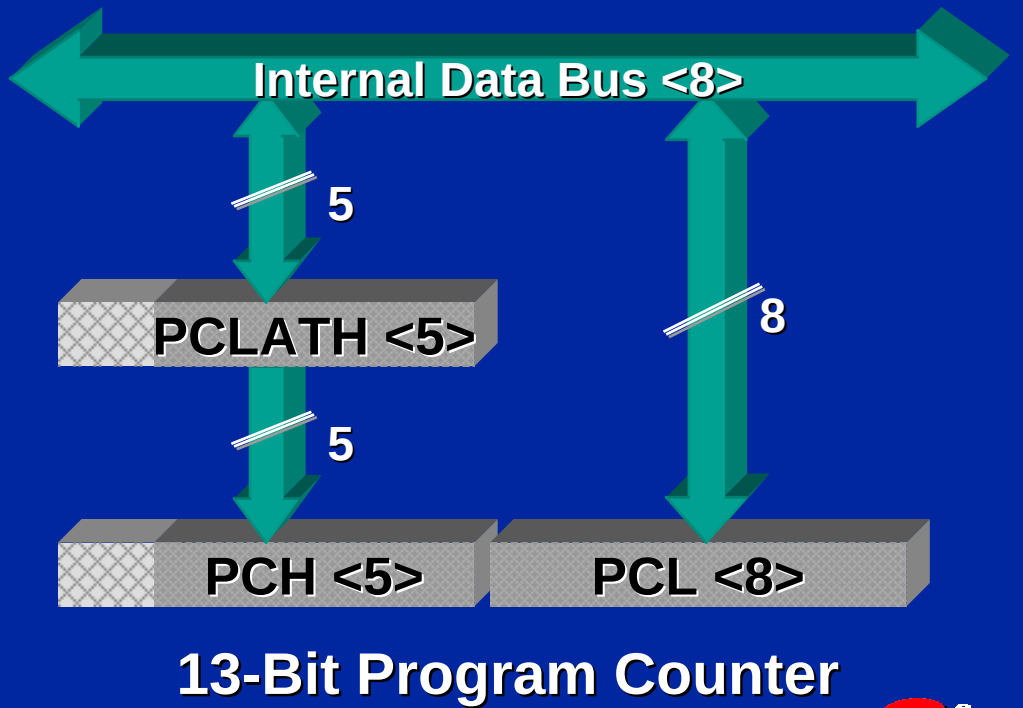


PICmicro MCU Architecture

PC Relative Addressing

- First write high byte to PCLATH.
- Next write low byte to PCL, this loads the entire 13-bit value to PC.

```
movlw    HIGH Delay
movwf    PCLATH
movlw    LOW Delay
movwf    PCL
```

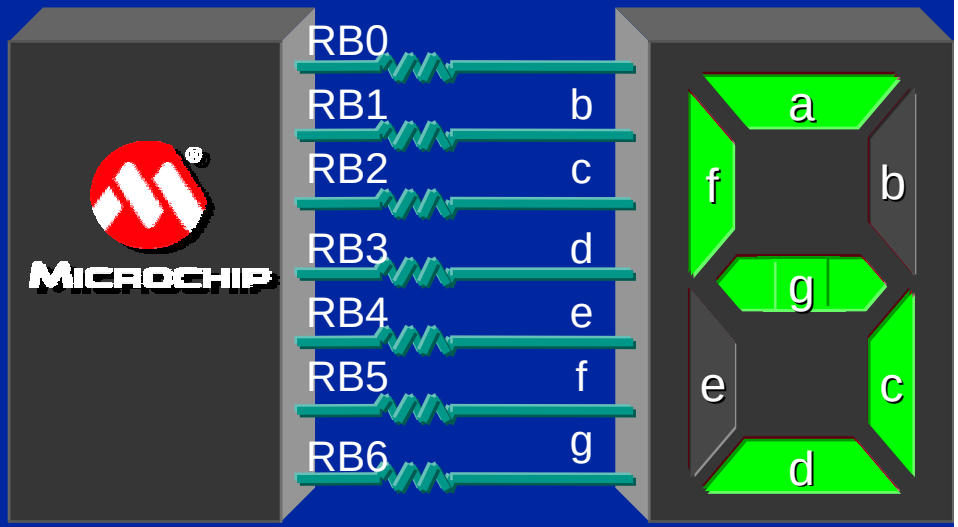


Note: PCH cannot be read

PICmicro MCU Architecture
PC Relative Addressing

```
    movlw  HIGH Decode
    movwf  PCLATH
    movf   DisplayValue,W
    call   Decode
    movwf  PORTB
    goto   Continue
Decode
    addwf  PCL,F
    retlw  B'00111111' ;decode 0
    retlw  B'00000110' ;decode 1
    retlw  B'01011011' ;decode 2
    retlw  B'01001111' ;decode 3
    retlw  B'01100110' ;decode 4
    retlw  B'01101101' ;decode 5
    retlw  B'01111101' ;decode 6
    retlw  B'00000111' ;decode 7
    retlw  B'01111111' ;decode 8
    retlw  B'01101111' ;decode 9
Continue
```

- Look-up Table Example



01101101
W Register

01101101
I/O Port B

PICmicro MCU Architecture
Interrupt Overview

- Multiple internal and external interrupt sources.
- Peripheral interrupt priority set by software.
- Global and individual interrupt enables.
- Each interrupt has an individual interrupt flag.
- Most interrupts wake processor from sleep.
- Fixed interrupt latency is three instruction cycles.

PICmicro MCU Architecture
Interrupt Logic