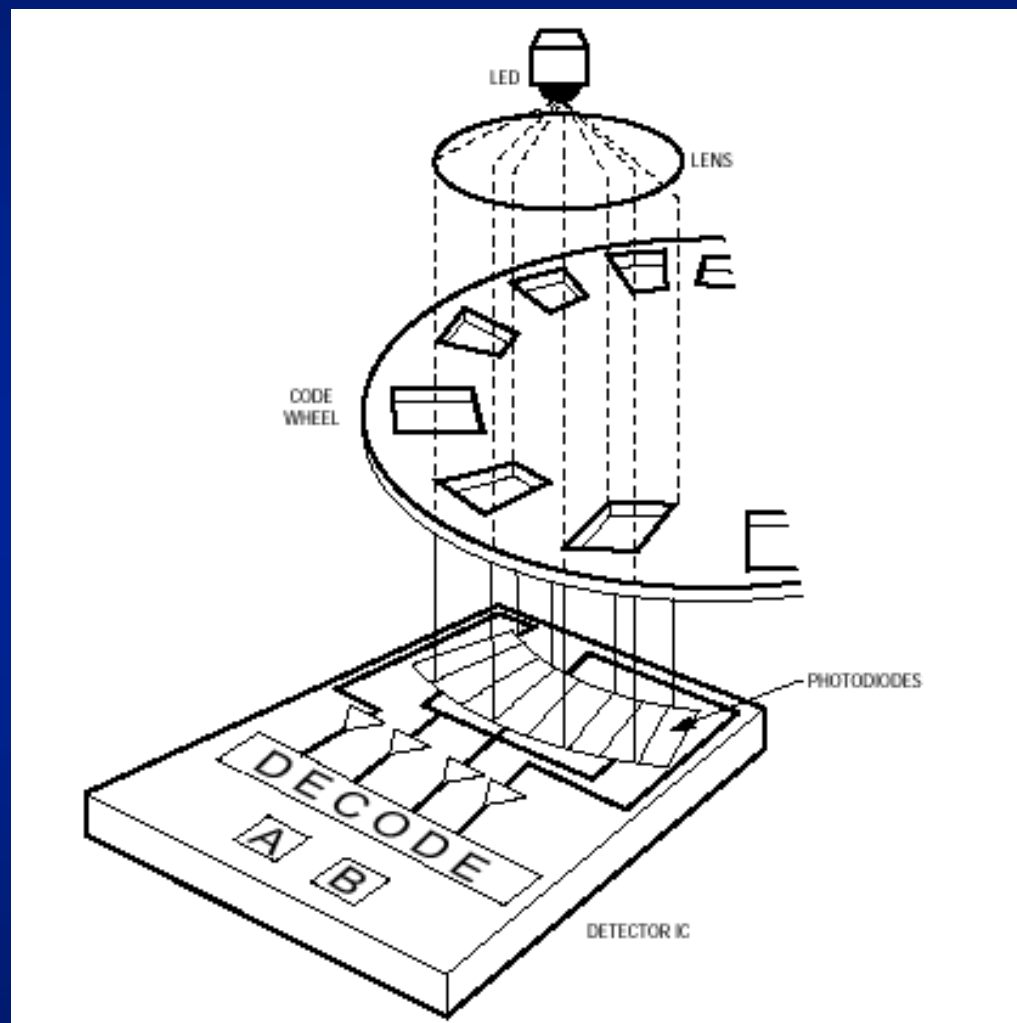# dsPIC30F Peripheral Module

dsPIC30F QEI Module
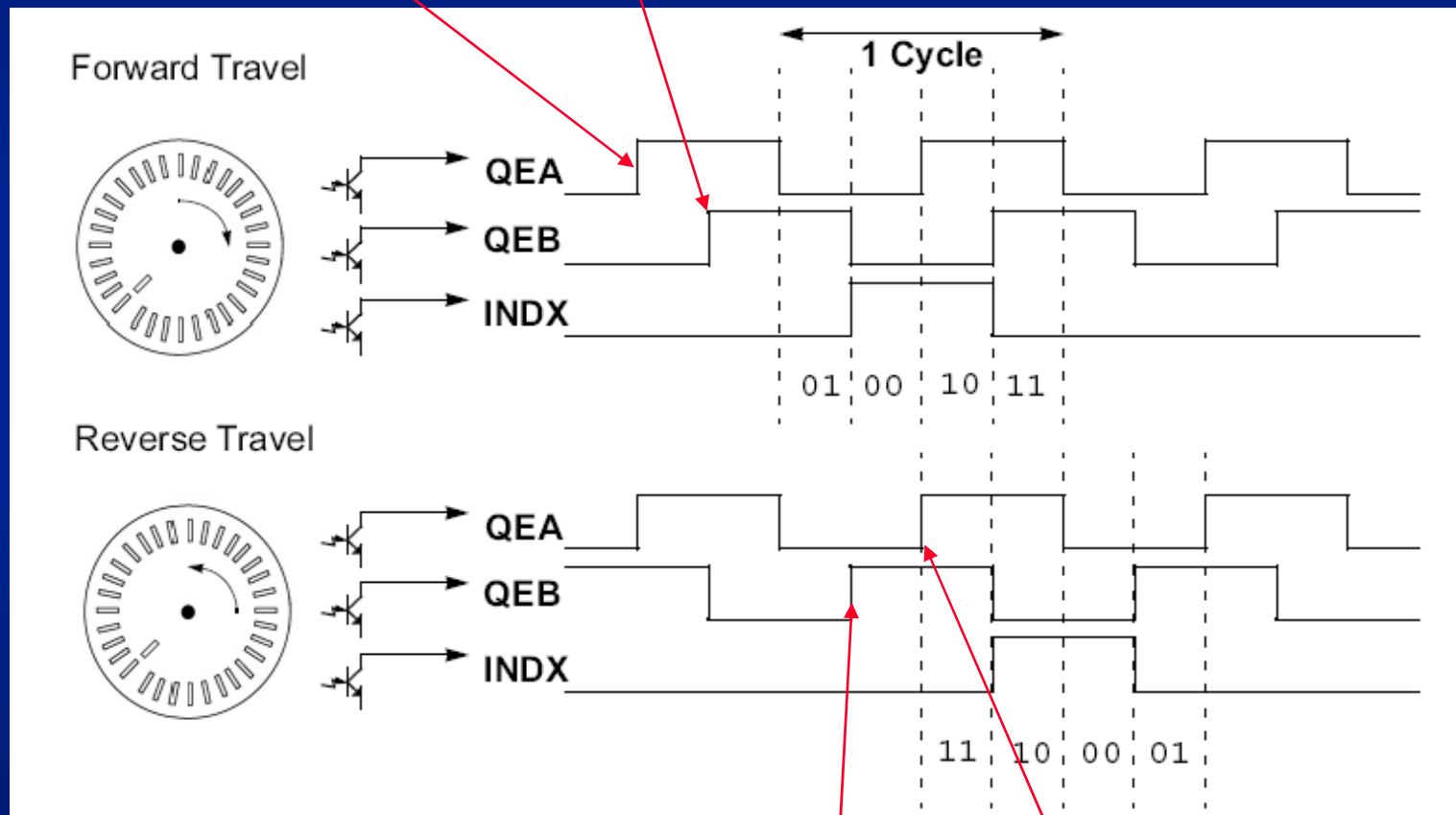### (Motion Control Feedback Peripheral)

Session Agenda

- What is a Quadrature Encoder?
- General Features Overview
- Programmable digital noise filters
- Quadrature Decoder
- The QEI as a Timer/Counter
- Code Example for RPM

Incremental Encoders

What is a Quadrature Encoder?
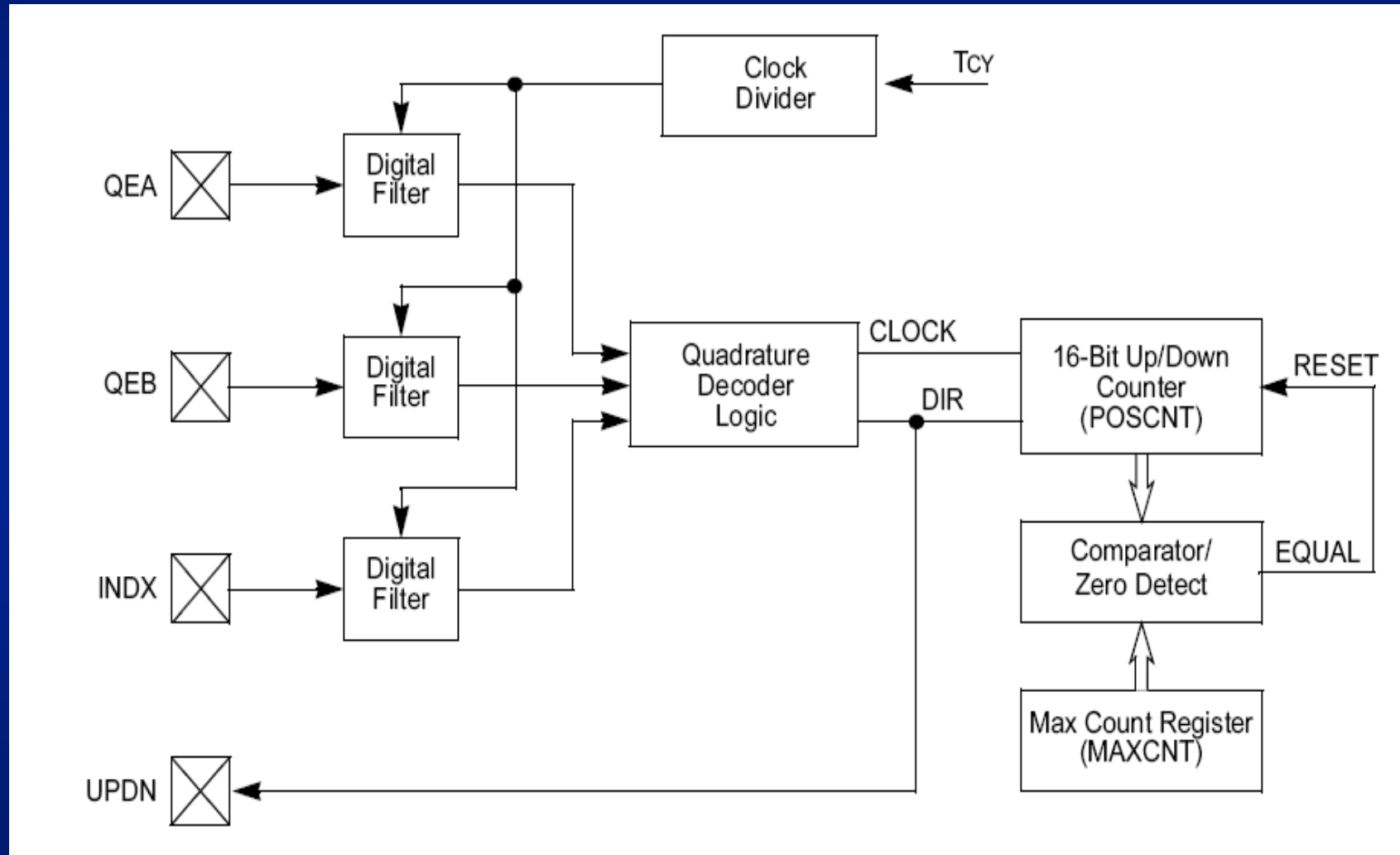

Phase A leads Phase B

Phase B leads Phase A

dsPIC QEI Features

- ## QEI Features

  - ❖ QEI decodes signals and accumulates count
  - ❖ Two inputs for Phase A and Phase B signals
  - ❖ Index pulse input (output from encoder)
  - ❖ Programmable noise filters on inputs
  - ❖ x2 and x4 counting modes
  - ❖ 16-bit Position count register
  - ❖ Reset on index pulse (if enabled)
  - ❖ Reset on rollover/underflow
  - ❖ Count error status bit
  - ❖ Module may function as 16-bit Up/down Timer
  - ❖ Digital noise filter on all inputs

Block Diagram

QEI Registers

- QEICON – Control / Status Register (16 bits)

- DFTCON – Digital Filter Control Register (8 bits)

- POSCNT – Position Count Register (16 bits)

- MAXCNT – Maximum Count Register (16 bits)

QEICON Register

QEICON Register

CNERR	-	QEISIDL	INDEX	UPDN	QEIM<2>	QEIM<1>	QEIM<0>
bit15	14	13	12	11	10	9	bit8

- **CNERR : Count Error Status Flag bit**
- **QEISIDL : Stop in Idle Mode**
- **INDEX : Index Pin Status bit (Read Only)**
- **UPDN : Position Counter Direction Status bit**
- **QEIM<2:0> : QEI Mode Select bit**
  - ❖ 111 : x4 mode with position counter reset by match MAXCNT
  - ❖ 110 : x4 Mode with Index Pulse reset of position counter
  - ❖ 101 : x2 mode with position counter reset by match MAXCNT
  - ❖ 100 : x2 Mode with Index Pulse reset of position counter
  - ❖ 001 : Starts 16-bit Timer
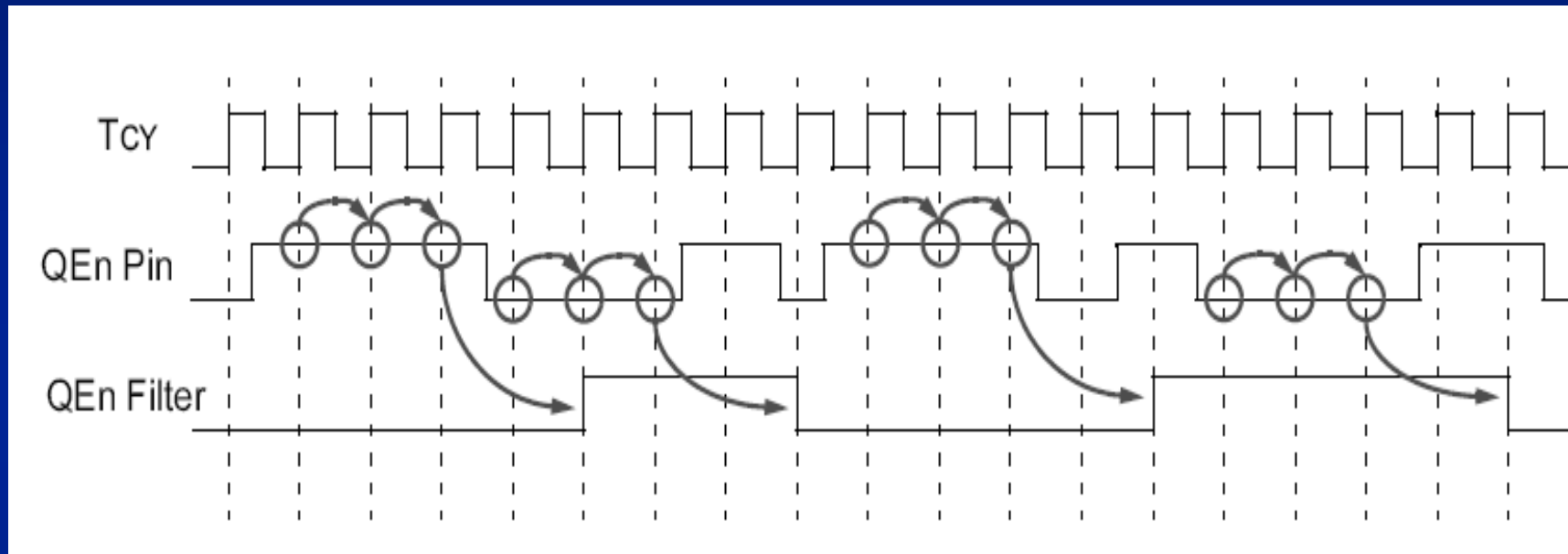
QEICON Register (cont.)

QEICON Register

SWPAB	PCDOUT	TQGATE	TQCKPS<1>	TQCKPS<0>	POSRES	TQCS	UDSRC
bit7	6	5	4	3	2	1	bit0

- SWPAB : Phase A and Phase B input swap bit
- PCDOUT : Position Counter Direction State Output Enable
- TQGATE : Time Gated Time Accumulation Enable
- TQCKPS<1:0> : Timer Input Clock Prescale Select
    - ❖ For 16-bit Timer mode only
- POSRES : Position Counter Reset Enable
    - ❖ Effective on QEIM<2:0> = 100 or 110
- TQCS : Timer Clock Source Select bit
- UDCRC : Position Counter Direction Selection Control bit

Digital Noise Filters

- Multiple clock options to digital filter
  - T_{cy}, $2T_{cy}$, $4T_{cy}$, $8T_{cy}$, $16T_{cy}$, ..., $256T_{cy}$
- Signal must be stable for 3 clock cycles
- Adjust clock divide bits to change noise filtering characteristics
- Use of digital filter generates latency

Digital Noise Filter Timing

Schmitt trigger inputs and three-clock cycle delay filter combine to reject low level noise and large, short duration noise spikes .
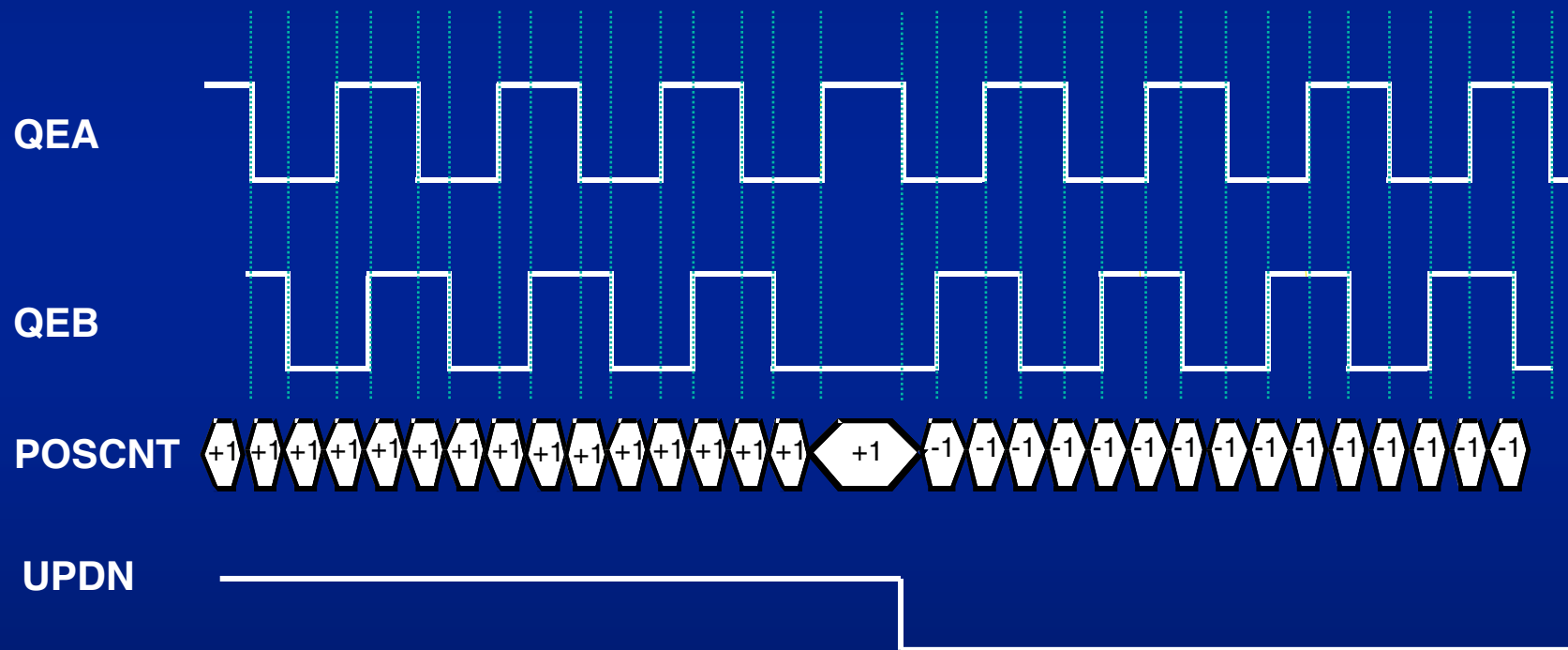
Set the QEOUT bit to enable the noise filter for both QEA & QEB
Set the INDOUT bit to enable the noise filer for Index input

Quadrature Decoder

- Four basic modes
  - ❖ x 2 mode with Index Pulse reset
  - ❖ X 2 mode with reset by match
  - ❖ X 4 mode Index Pulse reset
  - ❖ X 4 mode with reset by match

Encoder Timing Diagram

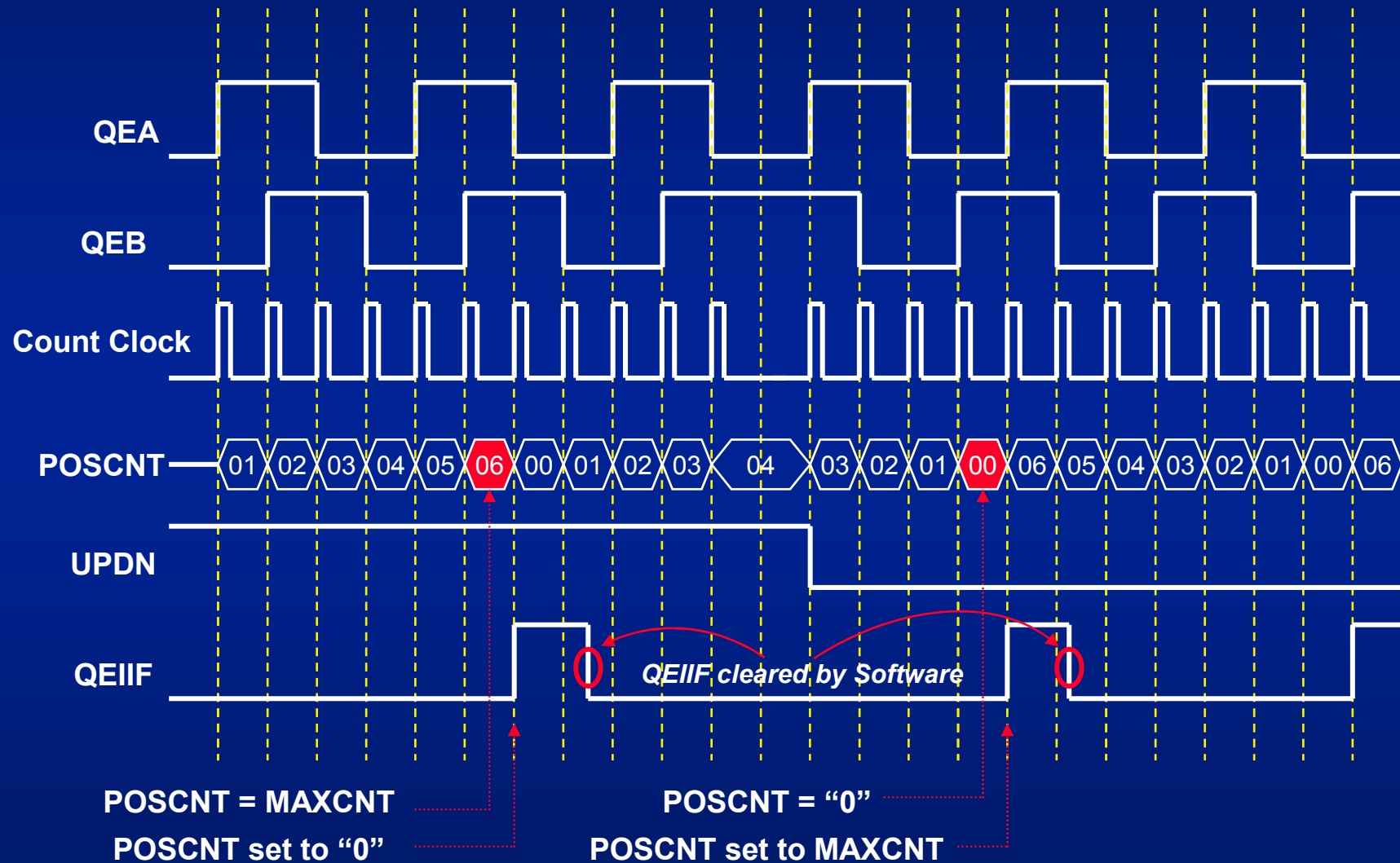- Quarature Decoder Signal Timing in 4x Mode

Position Counter

- Up/down counter

- Counts pulses generated by the decoder

- Count is accumulated in POSCNT register

- POSCNT can be accessed, both for read and write

- Its value can be compared to MAXCNT register

Using MAXCNT Register

- QEIM<2:0> = 111 or 101, Using the MAXCNT

  ❖ If the forward (increase) counter value matches the valve in the MAXCNT register, POSCNT will reset to zero, and an QEI interrupt event is generated on this overflow event

  ❖ If the reverse (decrement) counter value count down to zero, the POSCNT is loaded the new value from MAXCNT, and an QEI interrupt event is generated on this underflow event
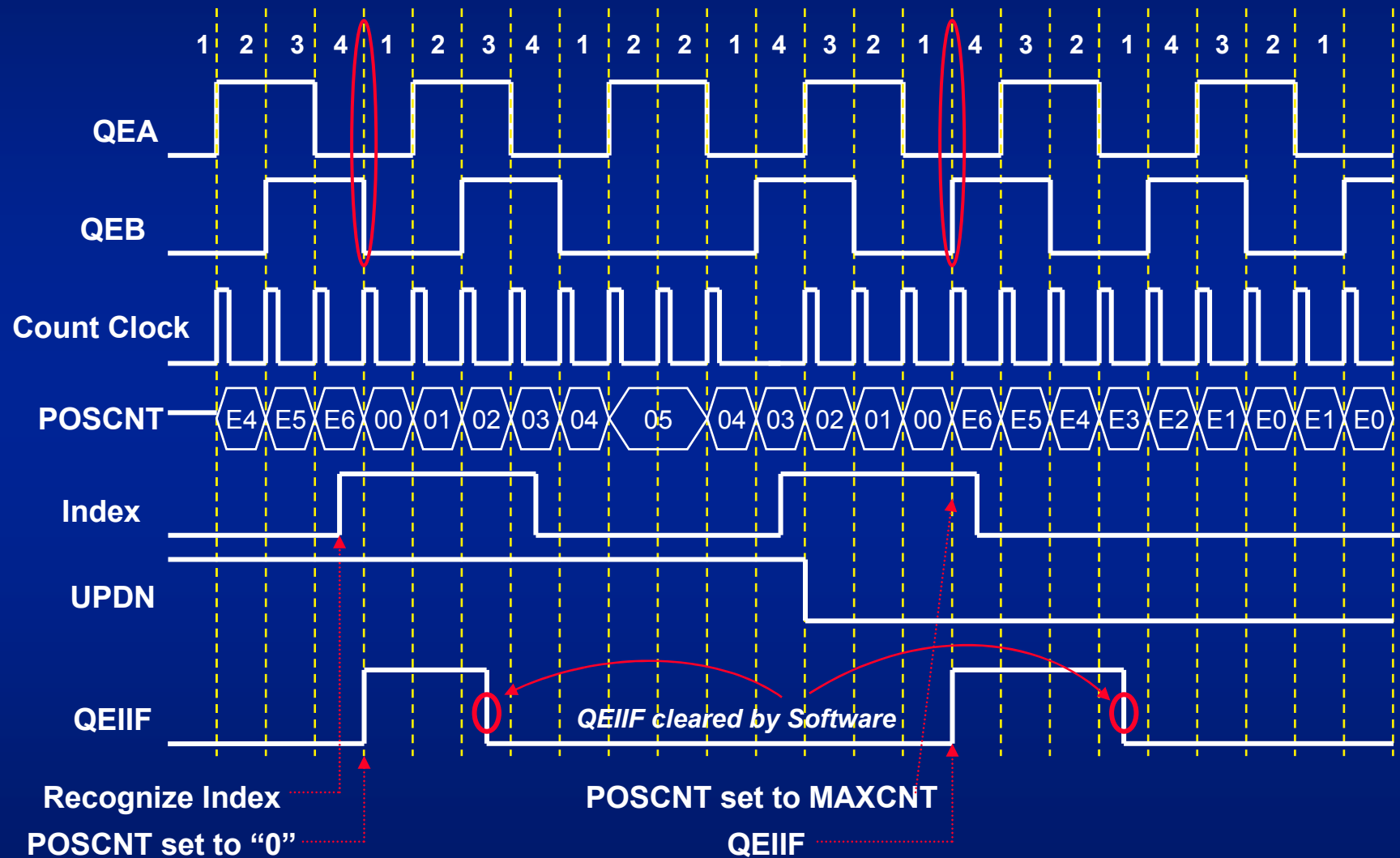
MAXCNT vs. Interrupt

QEA

QEB

Count Clock

POSCNT — 01 02 03 04 05 06 00 01 02 03 04 03 02 01 00 06 05 04 03 02 01 00 06

UPDN

QEIIF

QEIIF cleared by Software

POSCNT = MAXCNT ....

POSCNT set to "0" ....

POSCNT = "0" ....

POSCNT set to MAXCNT ....

Using Index Pulse

- QEIM<2:0> = 110 or 100, the Index Pulse is utilized for reset the POSCNT

  - ❖ The position count is reset each time an index pulse is received on the INDEX pin

  - ❖ If the encoder is travelling in the forward direction, the POSCNT is reset to "0"

  - ❖ If the encoder is travelling in the reverse direction, the MAXCNT register is loaded into POSCNT
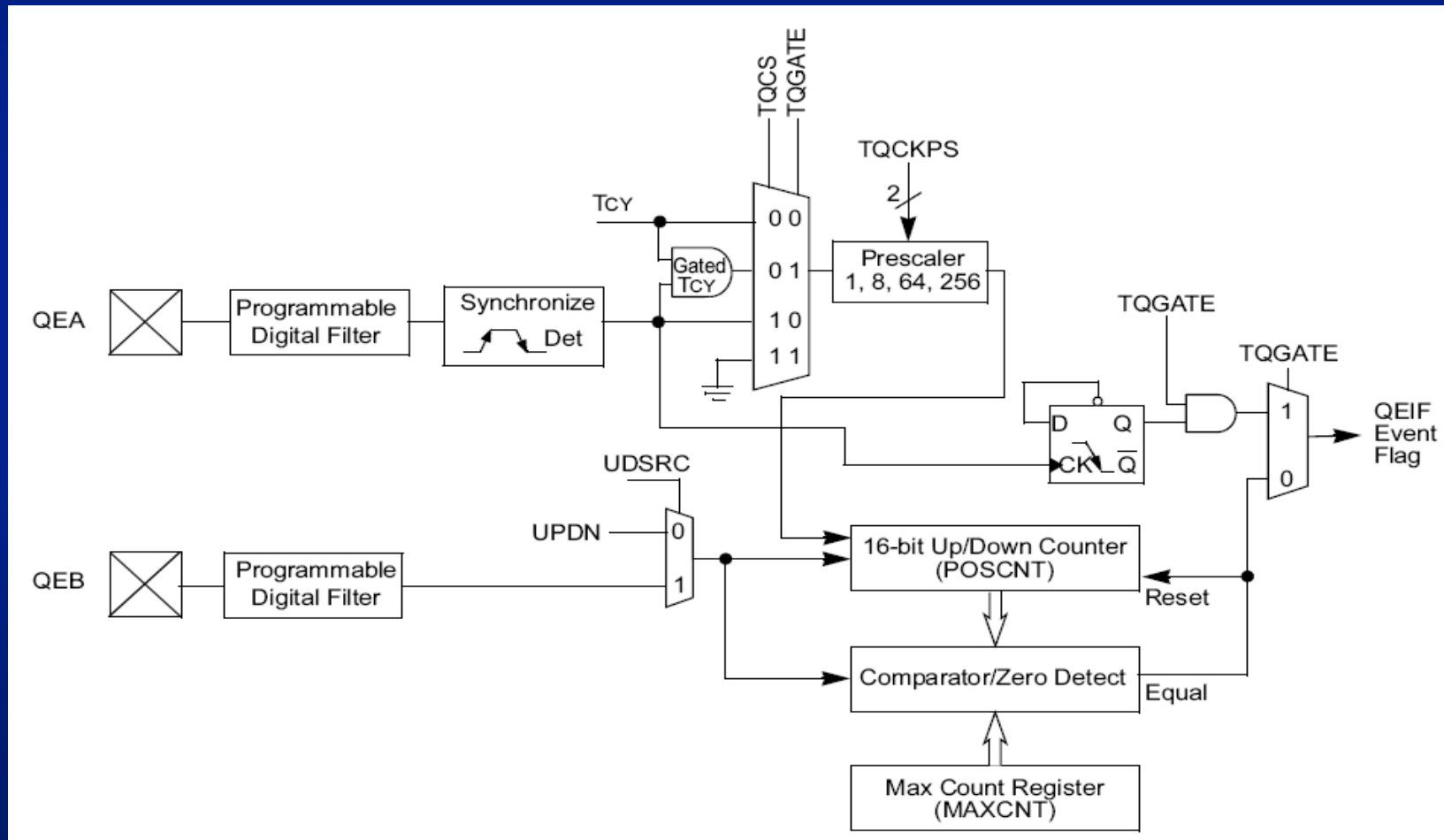
Index Mode-Up/Down

QEI as a 16 bit Timer/Counter

- Set QEIM<2:0> = 001 , QEI as a 16-bit Timer

Calculate the RPM

```
if ( QEICONbits.UPDN )                    // 馬達正轉時的計算
{
    if ( QEI_New >= QEI_Old )        // 計算單位時間內的旋轉數量
        QEI_Diff = QEI_New – QEI_Old ;
    else                                   // 溢位時的處理
        QEI_Diff = QEI_New + ( 65536 – QEI_Old ) ;
}
else                                       // 馬達反轉時的計算
{
    if (QEI_New < QEI_Old )
        QEI_Diff = QEI_Old – QEI_New ;
    else
        QEI_Diff = ( 65536 – QEI_New )+ QEI_Old ; // 借位時的處理
}

    QEI_Old = QEI_New ;                    // 更新的QEI數值

    RPM = ((long)QEI_Diff*600/256); // 轉速的計算 (100mS * 600= 1 Minute,
                                     // Index=64 採4倍精度 = 256)
```

QEI Lab

- The QEI signal can be generated by PIC12F675 which was programmed

- Please make sure close position for sw1 sw2 & sw3 in DSW4

- Calculate the QEI input signal with x4 mode, every 100mS display the RPM on the LCD Module

- Adjust the VR3 to modify the QEI speed