Section 32. High-Level Device Integration

HIGHLIGHTS

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32.1 INTRODUCTION

At their highest level of functionality, PIC24F devices integrate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

- Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options, and changing them if needed during run time.
- Device Identification – Allowing electronic confirmation of a device part number and revision level in the target application.
- On-Chip Voltage Regulator – Allowing the device to be used over a range of application voltage levels.

32.2 DEVICE CONFIGURATION

The basic behavior and operation of PIC24F devices are set by the device Configuration bits. These allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In PIC24F family devices, device Configuration bits are mapped to the device's program memory space, starting at location F80000h. This is beyond the user program memory space and belongs to the configuration memory space (800000h-FFFFFFh). These Configuration bits are implemented as volatile memory; that is, the configuration data must be loaded each time the device is powered up. The actual configuration data is stored in the two or three words at the end of the on-chip program memory space, known as the Flash Configuration Words. These are packed representations of the actual device Configuration bits, the actual locations of which are distributed among several locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during all types of device Resets.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once. After a bit is initially written during a power cycle or any Reset, it cannot be written to again. Any change of a Configuration bit (not a change to a Flash Configuration Word) causes a Configuration Mismatch (CM) Reset, which then forces a reload of the original values.

Table 32-1 provides a list of the available Configuration bit options. Each Configuration bit and its operation is described in the relevant section of the *"PIC24F Family Reference Manual*".

Note:	All the bits that are described here are not available on all the devices.

For more information on the location of device Configuration Words and Configuration bit mapping of a particular device, refer to the specific device data sheet.

32.2.1 Considerations When Using Flash Configuration Words

When creating applications for PIC24F devices, always specifically allocate the location of the Flash Configuration Word for configuration data. This is to ensure that the program code is not stored in this address when the code is compiled.

The upper byte of all the Flash Configuration Words in the program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since the Configuration bits are not implemented in the corresponding locations, writing '1' to these locations has no effect on device operation.

As mentioned before, changes to the actual device Configuration bits during run time would cause a Configuration Mismatch Reset. This does not prevent changes to Flash Configuration Words during normal operation. This also makes it possible for an application to change its hardware configuration by writing new data to these Flash Configuration Words, and then executing a RESET command, which results in reloading the new values.

Table 32-1: PIC24F Device Configuration Bits

Configuration Bit	Function
$\overline{\text{DEBUG}}$	Enables background debugger operation with external device control.
$\overline{\text{DISUVREG}}$	Disables internal USB 3.3V regulator.
FCKSM	Configures device clock switching and Fail-Safe Clock Monitor (2 bits, 3 configuration options).
FNOSC	Selects initial (default) device oscillator (3 bits, up to 8 configuration options).
FWDTEN	Enables Watchdog Timer.
FWPSA	Selects WDT prescaler.
GCP	Enables code protection for the program memory space.
GWRP	Enables write/erase protection for program memory.
I2CxSEL	Selects standard or alternate I/O pin mapping of SCLx and SDAx.
ICS	Selects the ICSP™ port used with ICD (2 bits, up to 4 options).
IESO	Enables Two-Speed Start-up.
IOL1WAY	Selects one-time or unrestricted run-time changes to peripheral mapping.
JTAGEN	Enables dedicated JTAG port and disables corresponding I/O ports on designated pins.
OSCIOFCN	Selects function of OSC2 pin (I/O port or CLKO) in certain external oscillator modes.
POSCMD	Selects primary (external) oscillator configuration (2 bits, 4 configurations).
PL96DIS	Bypasses 96 MHz PLL.
PLLDIV	Selects USB 96 MHz PLL prescaler (3 bits, up to 8 options).
WDTPS	Selects WDT postscaler (4 bits, up to 16 configuration options).
WINDIS	Selects Windowed Operation mode for Watchdog Timer.
WPCFG	Protects or unprotects write and erase of last (upper most) page, regardless of the selection of write-protect segment.
WPFP	The start/end page (16K word) address of write-protect segment. If WPEND = 0, the WPFP<8:0> bits are the start page address and if WPEND = 1, the WPFP<8:0> bits are the end page address (9 bits).
WPEND	Selects the write-protect segment to start from page 0 and end at page WPFP<8:0>, or start from page WPFP<8:0> and end at user program memory upper boundary.
WPDIS	Protects or unprotects the selected write-protect segment and last page if WPCFG is cleared.

32.3 DEVICE IDENTIFICATION

PIC24F devices have two read-only registers that provide device-specific identification information. These are located near the end of the device configuration space, starting at FF0000h. Like the Flash Configuration Words, the Device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using table read instructions.

The DEVID register at FF0000h (Register 32-1) identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register at FF0002h (Register 32-2) identifies the particular silicon revision for that device in terms of major and minor revision levels ("letter and dot revision" format).

For any given family of PIC24F devices, the corresponding device data sheet provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a silicon revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in part-specific literature, such as device silicon errata, or through Microchip's development tools, such as MPLAB® IDE. For assistance with interpreting values of DEVREV, contact Microchip technical support or your local Microchip representative.

Register 32-1: DEVID: Device ID Register

U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
FAMID7	FAMID6	FAMID5	FAMID4	FAMID3	FAMID2	FAMID1	FAMID0
bit 15							bit 8

R	R	R	R	R	R	R	R
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as '0'

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **FAMID<7:0>:** Device Family Identifier bits

bit 7-0 **DEV<7:0>:** Individual Device Identifier bits

Register 32-2: DEVREV: Device Revision Register

U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15							bit 8

U	U	U	U	R	R	R	R
—	—	—	—	DOT3	DOT2	DOT1	DOT0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as '0'

bit 23-4 **Unimplemented:** Read as '0'

bit 3-0 **DOT<3:0>:** Revision Identifier bits

32.4 ON-CHIP VOLTAGE REGULATION

The PIC24FJ family powers its core digital logic at a nominal 2.5V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all PIC24FJ family devices incorporate an on-chip regulator that allows the device to run its core logic from VDD.

PIC24FJ family devices use two different control systems to control the on-chip regulators: in some devices the regulator is enabled by supplying VDD to the control pin; while in some devices, regulator is disabled when the control pin is supplied with VDD. For the devices with the control pin, which enables the regulator when VDD is supplied. The control pin is named as ENVREG, and for the devices with the control pin, which disables the regulator when VDD is supplied, the control pin is named as DISVREG.

When enabled, the regulator draws power from the VDD pins to provide power to the digital logic. When disabled, power for the core logic must be supplied to the device on the VDDCORE/VCAP pin. This can be done by supplying separate VDD and VDDCORE voltage to allow the I/O pins to run at higher voltage levels (nominal 2.5V and 3.3V for VDDCORE and VDD, respectively). If the higher voltage is not required, the VDDCORE/VCAP and VDD pins can be tied together to operate at a lower nominal voltage. Refer to the device data sheet for device-specific voltage limitations.

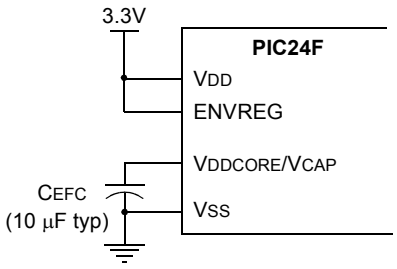
If regulator is enabled, a capacitor with a low effective series resistance (made of tantalum or ceramic) must be connected to the VDDCORE/VCAP pin. This helps maintain the stability of the regulator. The recommended value for the filter capacitor and its ESR (Equivalent Series Resistance) are provided in the Electrical Characteristics section of the specific device data sheet.

Possible configurations for both positive enable and positive disable regulators are provided in Figure 32-1.

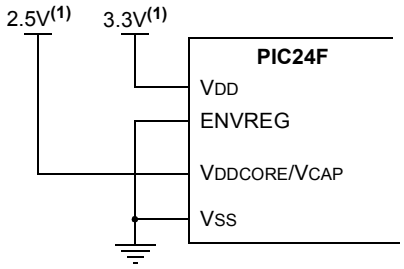
Figure 32-1: Connections for On-Chip Regulator (Positive Enable and Positive Disable)

Positive Enable (ENVREG) Devices

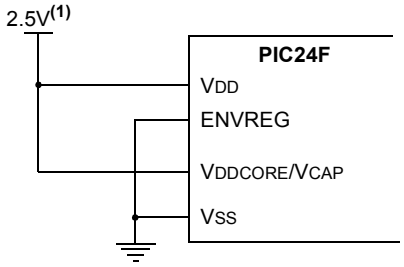
Regulator Enabled (ENVREG tied to VDD):



Regulator Disabled (ENVREG tied to ground):

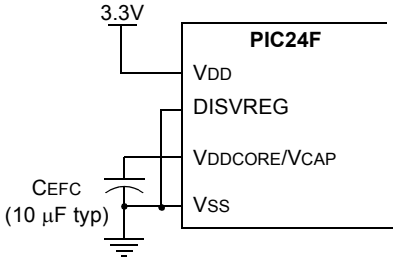


Regulator Disabled (VDD tied to VDDCORE):

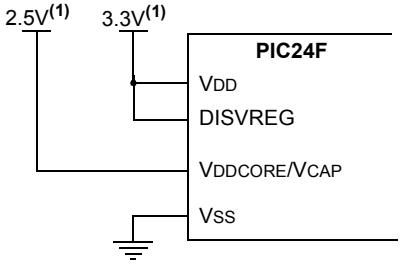


Positive Disable (DISVREG) Devices

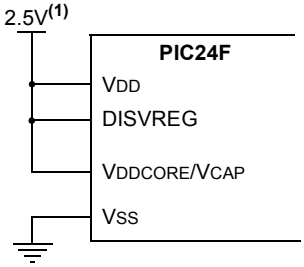
Regulator Enabled (DISVREG tied to VSS):



Regulator Disabled (DISVREG tied to VDD):



Regulator Disabled (VDD tied to VDDCORE):



Note 1: These are typical operating voltages. Refer to the Electrical Characteristics in the specific device data sheet for the full operating ranges of VDD and VDDCORE.

32.4.1 On-Chip Regulator and Power-on Reset (POR)

When the voltage regulator is enabled, it takes approximately 20 μs for it to generate output from the point where VDD attains the stability. During this time, designated as TSTARTUP, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any Power-Down modes and Sleep mode.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed delay of 64 ms nominal delay at device start-up.

32.4.2 On-Chip Regulator and Brown-out Reset (BOR)

When the on-chip regulator is enabled, the PIC24F family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain device operation, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are listed in the specific device data sheet.

32.4.3 Voltage Regulator Tracking Mode

When the on-chip regulator is enabled, the regulator provides a constant voltage of 2.5V nominal to the digital core logic. The regulator can provide this level from a VDD of about 2.7V all the way up to the device's VDDMAX. It does not have the capability to rise the regulator output voltage to 2.5V when the VDD drops below 2.5V. In order to prevent "brown-out" conditions when the voltage drops too low for the regulator, devices with the Low-Voltage Detect (LVD) feature enter a Tracking mode. In Tracking mode, the regulator output follows VDD, with a typical voltage drop of 100 mV.

When the device enters Tracking mode, it is no longer possible to operate at full speed. To provide information on when the device enters Tracking mode, the on-chip regulator includes a simple, Low-Voltage Detect circuit. When VDD drops below full-speed operating voltage, the circuit sets the Low-Voltage Detect Interrupt Flag, LVDIF. This can be used to generate an interrupt and put the application into a low-power operational mode or trigger an orderly shutdown. Low-Voltage Detection is only available when the regulator is enabled. If VDD drops below minimum Tracking mode voltage, a Brown-out Reset will be generated. Refer to the Electrical Characteristics section of the specific device data sheet to find the LVD trip point and the BOR trip point.

32.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Level Device Integration are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

32.6 REVISION HISTORY

Revision A (January 2007)

This is the initial released revision of this document.

Revision B (March 2008)

Minor edits to text throughout document.

NOTES: