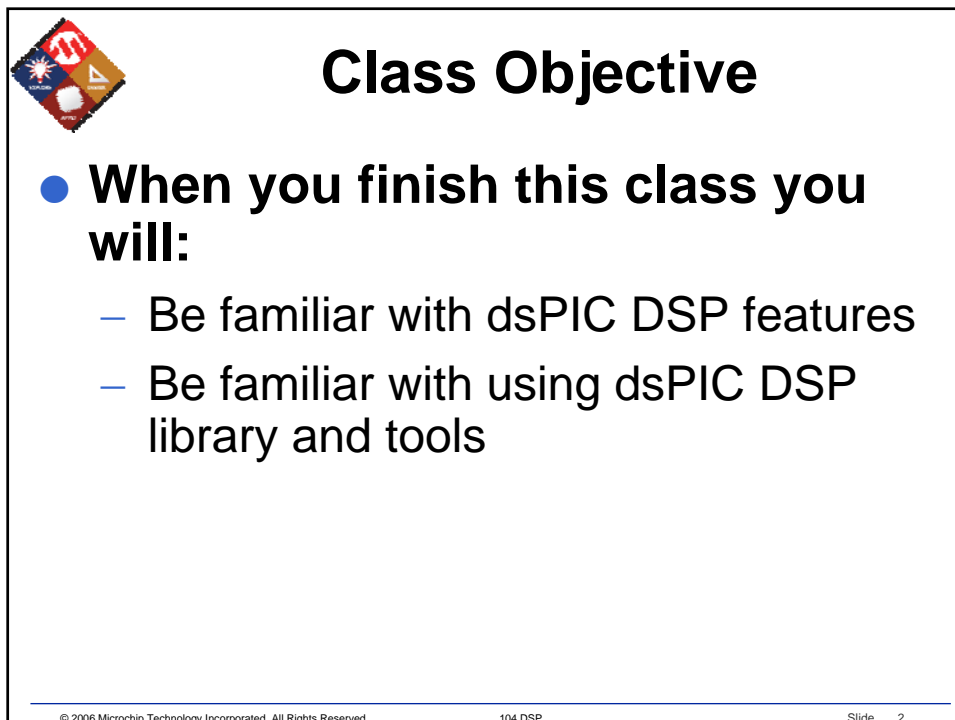
A slide titled "HANDS-ON Training" featuring a background image of a person presenting to a group in a classroom. Overlaid on this is a semi-transparent box containing the text "104 DSP 16-bit DSP Engine and DSP Libraries". In the bottom left corner is the Microchip Technology logo with the words "EXPLORE" and "DESIGN" below it. In the bottom right corner is a small graph showing a signal waveform. At the very bottom, there is a copyright notice and a slide number.

HANDS-ON Training

104 DSP
16-bit
DSP Engine and DSP Libraries

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A slide titled "Class Objective" with a Microchip Technology logo in the top left corner. The main content is a bulleted list of objectives. At the bottom, there is a copyright notice, the text "104 DSP", and a slide number.

Class Objective

- **When you finish this class you will:**
 - Be familiar with dsPIC DSP features
 - Be familiar with using dsPIC DSP library and tools

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Agenda

- **Why DSP**
- **dsPIC Support for DSP**
 - dsPIC DSP architecture
 - dsPIC DSP Tools and Libraries

HANDS-ON Training

Why DSP

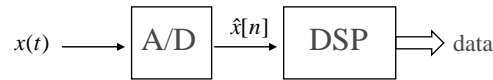
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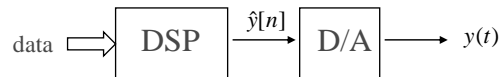
Slide 4



DSP Systems



Analysis (Receiver / Encoder)



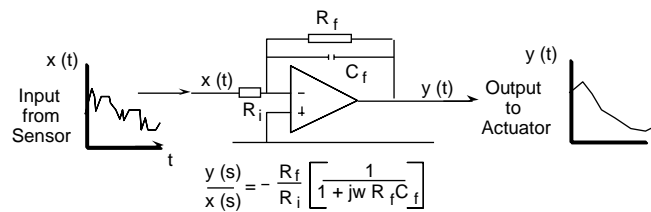
Synthesis (Transmitter / Decoder)



Signal Conditioning/Control



Analog Control Systems



- Drawbacks:

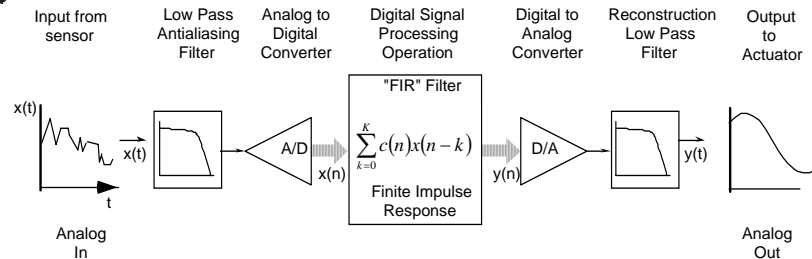
- Low noise immunity
- Little flexibility
- Requires adjustments
- Critical component specification, especially for high order filters

- Filter characteristics change with

- Temperature
- Component aging
- Power supply variation



Digital Control Systems



- Some key advantages of digital filtering:
 - Less affected by noise
 - Lower power consumption
 - Programmable systems
 - Minimal effect of drift in characteristics with age

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Slide 7



FIR Filters: Definition

- The input-output relation of a FIR filter is given by

$$y[n] = \sum_{k=0}^{T-1} b_k x[n-k]$$

where:

T = filter length (# of taps)

b_k = the k^{th} coefficient of the filter

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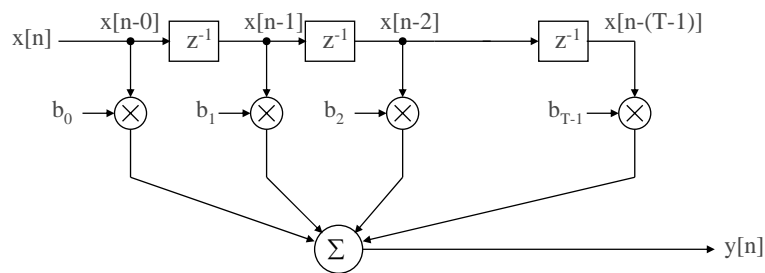
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Slide 8



FIR Filters: Structure

- **FIR filter tapped delay line form**
 - z^{-1} refers to a unit sample delay



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HANDS-ON Training

DSP Architecture

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dsPIC support for Filters

- DSP Library Support
- Dual Harvard Architecture
- MAC instructions with data prefetch
- Modulo Addressing
- Loop control - DO and REPEAT instructions



C-callable fixed point FIR from MPLAB

Description: FIR applies an FIR filter to the sequence of source samples, places the results in the sequence of destination samples, and updates the delay values.

Include: `dsp.h`

Prototype:

```
extern fractional* FIR (  
    int numSamps,  
    fractional* dstSamps,  
    fractional* srcSamps,  
    FIRStruct* filter  
);
```

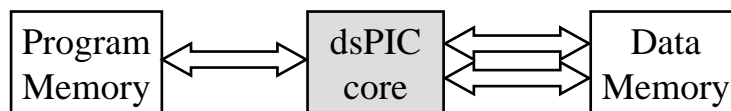
Arguments:

<i>numSamps</i>	number of input samples to filter (also N)
<i>dstSamps</i>	pointer to destination samples (also y)
<i>srcSamps</i>	pointer to source samples (also x)
<i>filter</i>	pointer to FIRStruct filter structure

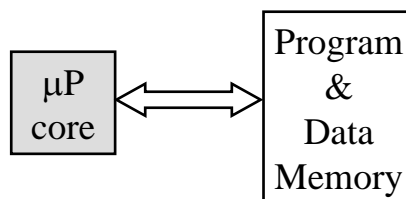
Return Value: Pointer to base address of destination samples.



dsPIC vs. Microprocessor Architectures



Dual Harvard Architecture



Von Neumann Architecture



MAC and dual parallel reads

MAC

Multiply and Accumulate

Syntax: {label;} MAC Wm*Wn, Acc {[Wx], Wxd} {[Wy], Wyd} {,AWB}

Operation: $(Acc(A \text{ or } B)) + (Wm * Wn) \rightarrow Acc(A \text{ or } B)$
 $([Wx]) \rightarrow Wxd; (Wx) + kx \rightarrow Wx$
 $([Wy]) \rightarrow Wyd; (Wy) + ky \rightarrow Wy$
 $(Acc(B \text{ or } A)) \text{ rounded} \rightarrow AWB$

Description: Multiply the contents of two working registers, optionally prefetch operands in preparation for another MAC type instruction and optionally store the unspecified accumulator results. The 32-bit result of the signed multiply is sign-extended to 40 bits and added to the specified accumulator.

Words:

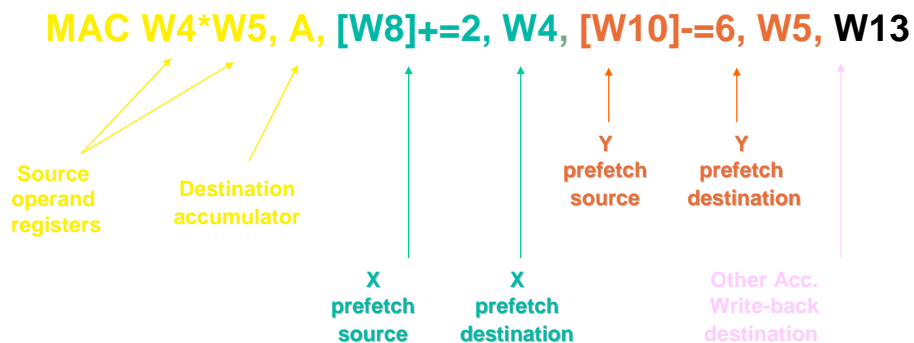
Cycles:

1
1 **One clock cycle, One program word!**

Example 1: MAC W4*W5, A, [W8]+=6, W4, [W10]+=2, W5



MAC and dual parallel reads



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Modulo or “Circular” Addressing

- Eliminates the software overhead associated with effective address (EA) correction
- Data address boundary checks are performed in hardware
- May be used with any instruction that utilizes indirect addressing

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Modulo: FIR Filter Example

- Single Sample FIR Filter Operation (4 taps)
- Vector Dot Product of...
 - Input Delay Line
 - Coefficient Array

$$\begin{array}{|c|c|c|c|} \hline x[n] & x[n-1] & x[n-2] & x[n-3] \\ \hline \end{array} \times \begin{array}{|c|} \hline b_0 \\ \hline b_1 \\ \hline b_2 \\ \hline b_3 \\ \hline \end{array} = \boxed{y[n]}$$

Delay line

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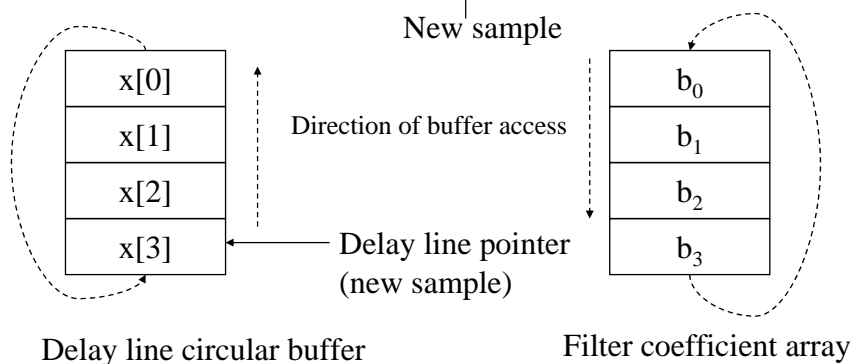
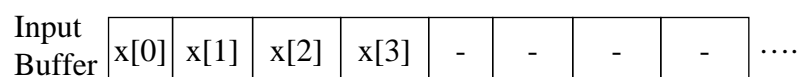
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Modulo: FIR Filter Example

Buffer at $n = 3$ (before computation):



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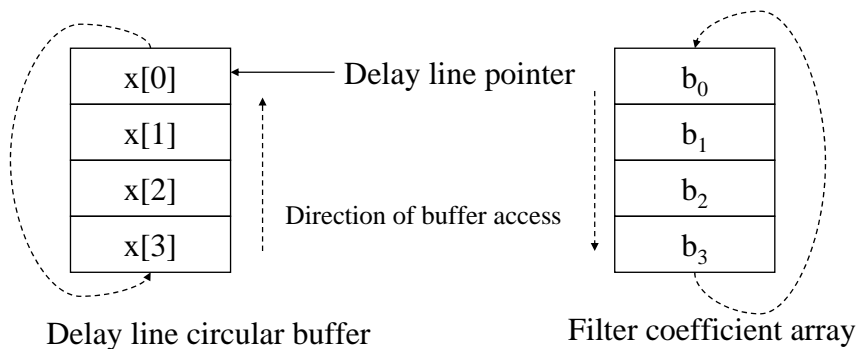
Slide 18



Modulo: FIR Filter Example

FIR output for $n = 3$:

$$y[3] = x[3]*b_0 + x[2]*b_1 + x[1]*b_2 + x[0]*b_3$$



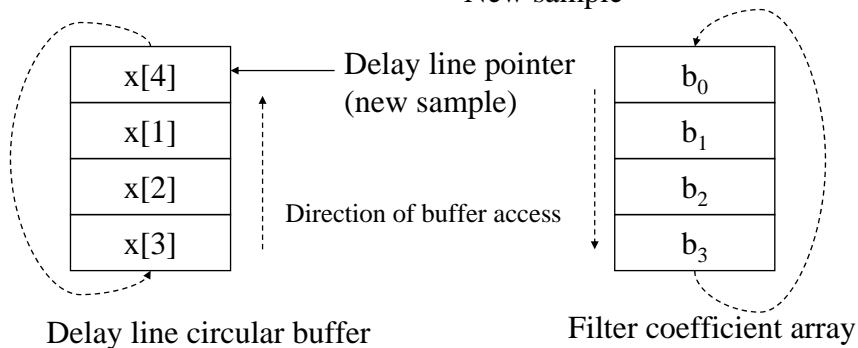
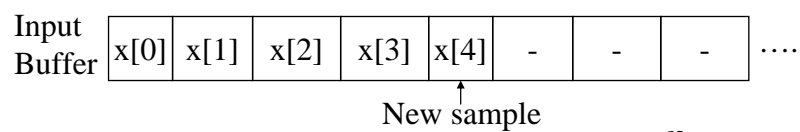
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Modulo: FIR Filter Example



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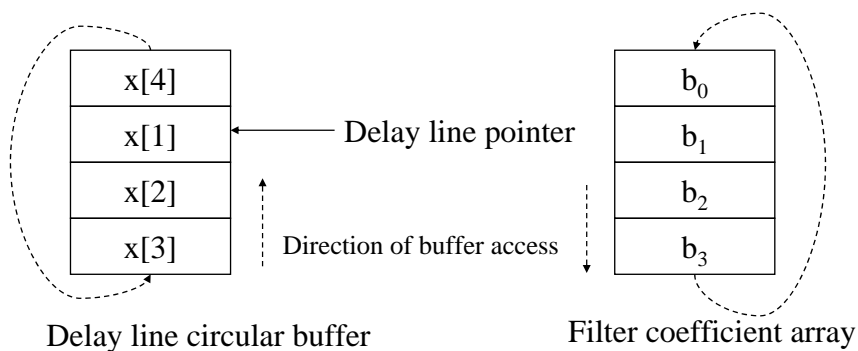
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Modulo: FIR Filter Example

FIR output for $n = 4$:

$$y[4] = x[4]*b_0 + x[3]*b_1 + x[2]*b_2 + x[1]*b_3$$



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Zero Overhead Looping

- Two Instructions
 - **REPEAT** for single instruction loops
 - **DO** for multiple instruction loops
- Interruptable
- STATUS register indicates when looping is active

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REPEAT Examples

- **REPEAT #200**
MOV [W0--], [W1]++
- **REPEAT W8**
CLR [W5]++
- **REPEAT #0x20**
ADD A, [W3++]



Nested DO Example

```
DO      LOOP1, #0x100
MOV     [W0], W1
AND     #0x3FF, W1
DO      LOOP2, #0x8
BTG     W1, #0x9
LOOP2:  IOR     W1, [W2]++, [W3]++
LOOP1:  MOV     W1, [W0]++
```



4 Lines (dsPIC) vs. 31 Lines (16-bit MCU)

```
repeat    w4
mac       w5*w6,a,[w8]+=2,w5,[w10]+=2,w6
mac       w5*w6,a,[w8]+=2,w5,[w10],w6
mac       w5*w6,a
```

16-bit MCU

```
do_again1:
    mov R6,R5      ;Get next x(n-l)
    mov R7,[R12+]  ;Get next FIR filter coeff-a(i)
    mul R6,R7      ;Form product a(i)*x(n-l)
    jmpr cc_NV,copy1 ;Test for only 16 bit result
    mov R9,MDH     ;Move high portion of MD

copy1:
    mov R6,MDL     ;Move low portion of MD
    add R11,R6     ;acc. Product terms in R10 and R11
    addc R10,R9
    sub R5,#2      ;Point to a next item in x(n-l)
    cmp R5,R13     ;Chk if ptr falls out of circ buffer table
    jmp cc_NN,leap1 ;If still in table keep going otherwise
                                ;adj. Ptr. To top of table

    mov R4,R2
    shl R4,#1
    add R5,R4      ;adj. Ptr to top of table

leap1:
    add R1,#1h     ;Determine if all taps computed
    cmp R1,R2
    jmp cc_NZ,do_again1
    mov R4,#curr_ptr
    mov R5,[R4]
    add R5,#2h     ;Inc. ptr. Into circ. Buffer
    mov R3,R2
    shl R3,#1
    sub R3,#2
    mov R6,R13
    add R6,R3
    cmp R5,R6      ;Does curr_ptr exceed top of table?
    jmpr cc_NZ,leap3
    mov R5,R13     ;Back to beginning of table

leap3:
    cmp R10,#0h
    jmpr cc_Z,leap2
```

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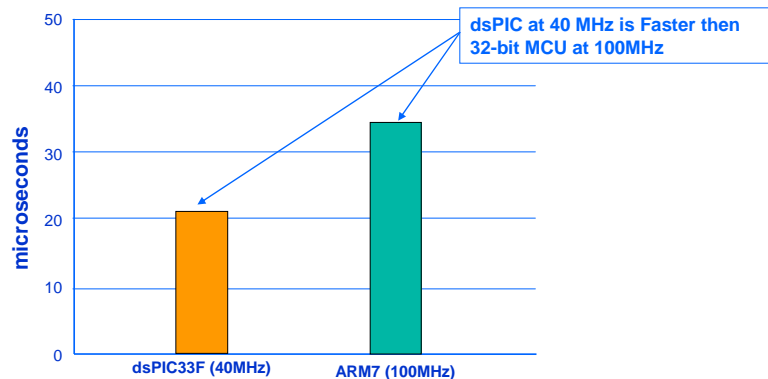
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DSP Benchmark

● BDTI's Real Block FIR Filter Benchmark

- Execution time (lower is better)




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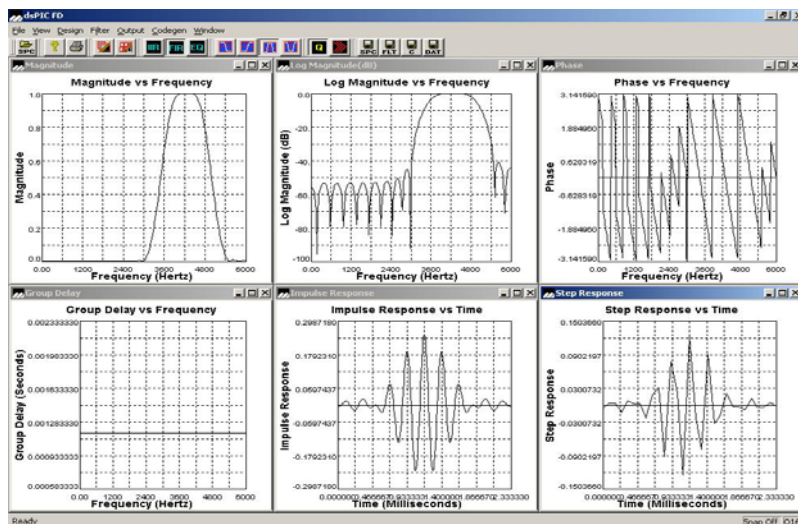
dsPIC® Digital Filter Design

- **Graphically design all types of digital filters**
 - Low-pass, high-pass
 - Band-pass, band-stop
- **Digital filter algorithm kernels are provided for:**
 - FIR—Finite Impulse Response
 - IIR—Infinite Impulse Response
- **Designing coefficients to control the filter response is the tricky part**
 - You can do the math or use this tool!!
- **Quickly observe filters response**
- **Generated code and coefficients fully compatible with MPLAB® C30 C Compiler language tools**

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dsPIC® Digital Filter Design



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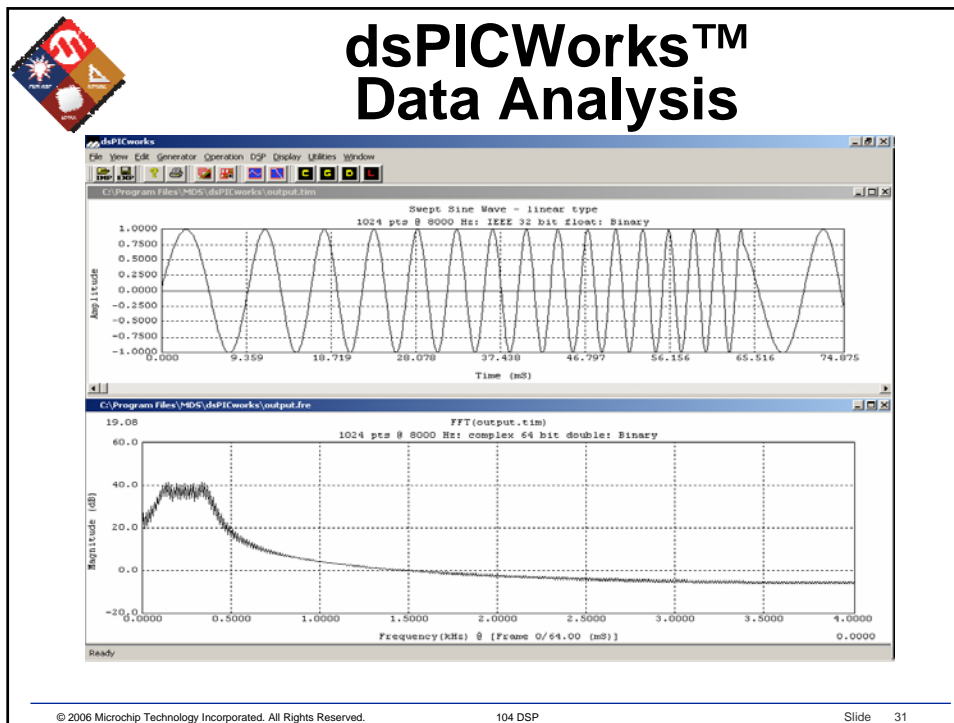
dsPICWorks™ Data Analysis and DSP Software

- **Graphical signal analysis and generation tool**
 - Create waveforms and process them
 - Signal generation
 - SIN, square, swept SIN, triangular, etc...
 - Signal operations
 - Add, Flip and Shift, Multiply, etc...
 - DSP operations
 - Filtering, correlation, FFT, LPC analysis, etc...
- **Designed especially for the dsPIC30F**
 - Import/export data with MPLAB® compatible files
 - Processes filter files saved from dsPIC® Digital Filter Design

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HANDS-ON Training

Lab 1
Using DSP Tools and Libraries

The background image shows a group of people in a classroom setting, attending a hands-on training session. A large screen in the background displays a graph of Magnitude (dB) versus Frequency (kHz). The foreground shows a person working on a laptop. The Microchip Technology logo is visible in the bottom left corner.

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Lab 1 – Using DSP

- **Goals**

- Learn DSP tools and Libraries

- **Lab**

- Implement signal filtering using FIR filter

HANDS-ON Training

DSP Related Libraries

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Math Library

- **Supports all of <MATH.H> from ANSI “C”**
 - Trigonometric Functions
 - Exponent and Log Functions
 - Power, Square Root, Floor, Ceiling, etc.
- **IEEE-754 Compliant**
- **Optimized for code size, developed in Assembly**
- **Supports 2 data types**
 - 32-bit floating point
 - 64-bit double
- **Benefits any application which uses floats/doubles**
- **C and assembly callable**



DSP Library

- **Libraries for your DSP requirements**
- **Collection of 49 of the most common DSP functions**
 - Vector and Matrix Functions
 - **Add, Subtract, Multiply, Max, Min**
 - **Convolution, Correlation, Power, etc...**
 - Filter Functions—block and single sample processing
 - **FIR, IIR, Adaptive LMS, Lattice and more**
 - Transform Functions
 - **FFT, Inverse FFT, Discrete Cosine Transform**
 - Window Functions
 - **Bartlett, Blackman, Hamming, Hanning, Kaiser**
- **Most functions are hand coded in assembly language**
 - Fast execution time, C and assembly callable



Embedded Modem Library

- **Software Modem (soft-modem) Support**
 - Replacing external modem chip with software!
- **Benefits**
 - Single-chip integrated solution (up to 14.4 kbps)
 - Quick dialup and connection times
 - **Perfect for small transactions on analog phone line**
- **Application Examples**
 - Home automation, remote access, security systems
 - POS applications, web-enabled devices
 - Tele-metering, remote upgrades
- **Library supplied with full DTMF Generation/Detection modules**

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Soft-Modem Resource Summary

- **dsPIC30F implementation leaves room for other tasks...**

ITU-T Specification	Bit Rate (bps)	RAM (Bytes)	Program Memory (Kbytes)	MIPS
V.32bis	14400	3600	36	15
V.32	9600	3200	31	12
V.22bis	2400	1700	22	7
V.23	600/1200	1000	15	4.5
V.21	300	1000	13	4.5
V.42 (Error Corr.)	na	2000	14	1.5



Includes DTMF Library

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Speech Coding Library

- **Performs speech compression / decompression**
- **Encoder - 16:1 compression ratio**
 - Speech input: 8 KHz, 16-bit mono
 - Encoded output: 8kbps data stream
- **Decoder**
 - Decoder input: 8 kbps data stream
 - Speech output: 8 KHz, 16-bit mono
- **Based on Speex**
 - Open source technology
 - Numerous PC plug-ins / apps readily available
 - www.speex.org
- **Includes PC Utility for making “playback” files**



Speech Coding Library How may it be used?

- **By any application with voice communication**
- **Benefits**
 - Reduces communication bandwidth
 - Reduces storage requirements
- **Sample Applications**
 - Digital radios / walkie-talkies
 - Answering machines / voice recorders
 - Playback-only systems
 - **Security Systems (building evacuation)**
 - **Museum Guides**
 - **Application Voice Prompts**



Speech Coding Library Resource Requirements

- Small Decoder footprint / Encoder is RAM intensive

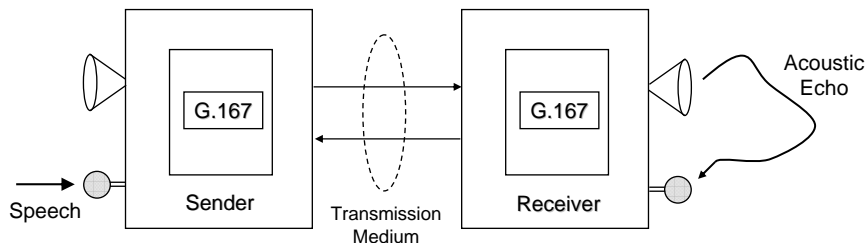
	Encoder	Decoder
MIPs	19	3
RAM	5.4 KB	3.2 KB
Flash	33 KB	15 KB

- 2 analog interfaces supported
 - Silicon Labs Si-3000 Codec
 - Alternate interface for cost-sensitive applications
 - ADC for microphone input
 - Output compare for speaker output
 - Sample circuits provided in User's Guide



Acoustic Echo Cancellation Library

- Provides 'far-end' echo cancellation
 - Speaker output is picked up by the local microphone and transmitted back to the sender
- Features
 - G.167-compliant algorithm (up to 64 msec)
 - Supports full-duplex operation





Acoustic Echo Cancellation Library

- **G.167 CPU Resources**

Echo Delay	RAM (KB)	Program Memory (KB)	MIPS
16 msec	4.6*	6	7.5
32 msec	5.4*	6	10.5
64 msec	7.7*	6	16.5

* Includes up to 2KB for CODEC and UART buffers and A/U-law compression

- **Target Applications**

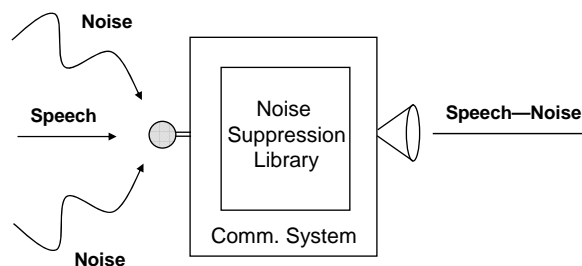
- Speakerphone
- Hands-free car phone
- Intercom
- Emergency alarm units



Noise Suppression Library

- **Removes extraneous noise picked up by microphone**

- Voice activity detector differentiates noise and speech
- Noise reduction filters adjust every 10 ms during periods of speech inactivity (uses FFT analysis)
- Speech is continuously filtered, reducing noise





Noise Suppression Library

- **Noise Suppression CPU Resources**
 - 3.3 MIPS
 - 5 Kbytes Flash memory
 - 2 Kbytes RAM
 - Includes up to 1 Kbyte for buffering Codec data
- **Target Applications**
 - Front end for any voice based system
 - Headsets
 - Hands-free telephone
 - Intercom
 - Speech recognition
 - Speech coding



Embedded Encryption Libraries

- **dsPIC30F Symmetric Key Library**
 - Message Digests: SHA-1, MD5
 - Symmetric Key Encryption: T-DES, AES
 - Deterministic Random Bit Generator: ANSI X9.82
- **dsPIC30F Asymmetric Key Library**
 - Signing and Verification: RSA, DSA
 - Public Key Encryption: RSA
 - Key Agreement Protocol: Diffie-Hellman
 - Big Integer Arithmetic Package



Embedded Encryption Applications

- **Secure Web Transactions**
 - Secure web access (SSL/TLS)
 - E-mail (S/MIME), secure XML transactions, and Virtual Private Networks (IPsec)
- **Smart Card Readers**
- **PDA's and other mobile devices**
- **Secure communications between a dsPIC® DSC application and personal computers**
 - Trusted Computing Group (TCG)
 - Microsoft® Next Generation Secure Computing Base (NGSCB)



Summary

- We learned advantages of dsPIC DSP architecture
- We learned DSP tools and libraries available for dsPIC



References

- dsPIC30 & dsPIC33 Datasheet
- dsPICDEM1.1 User's Guide
- MPLAB® IDE
- C30 Compiler
- ICD2 In Circuit Debugger

HANDS-ON Training

All Done!
Thank you all for attending
Please remember the evaluation sheets

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