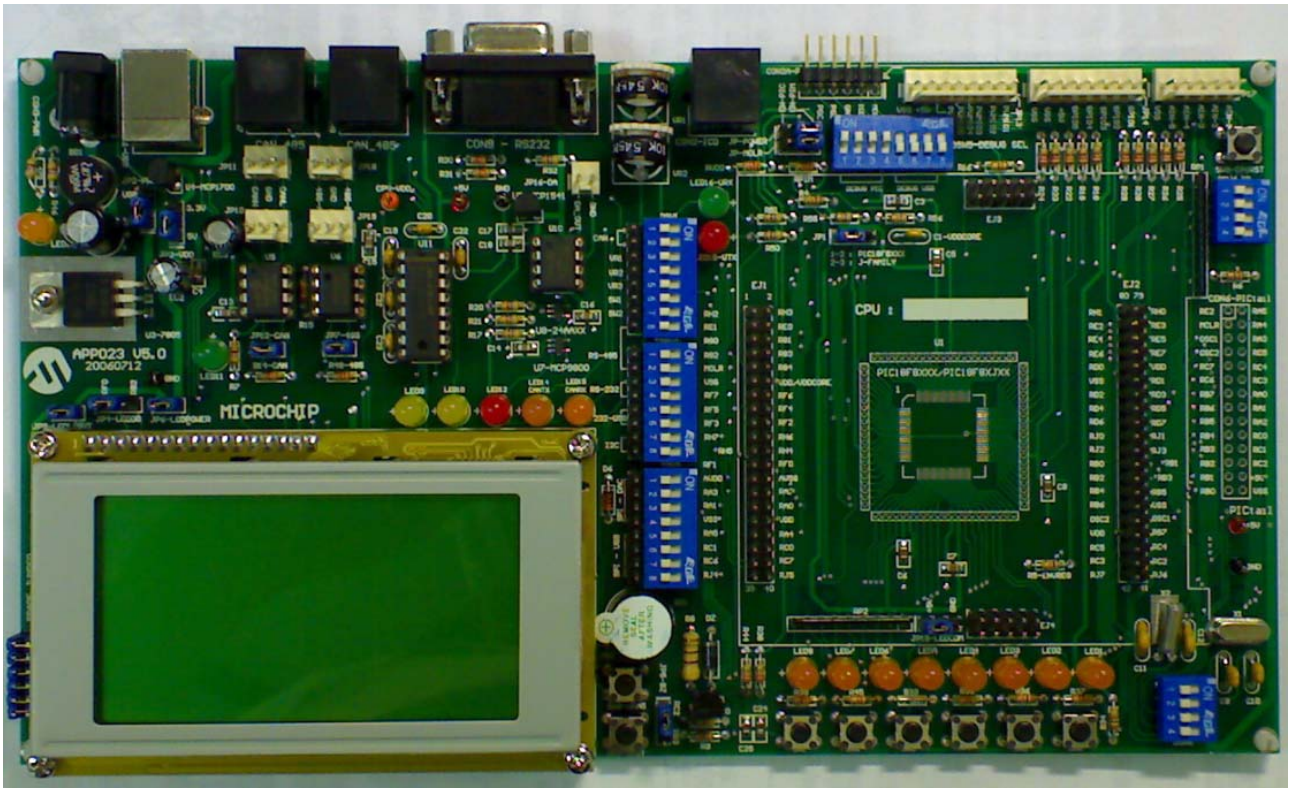
MICROCHIP EVM Board : APP023 使用手冊



1-1. APP023 多工能實驗板介紹：

Microchip 在推出 PIC18 系列的 MCU 之後，更推出了一系列功能更多的微處理器，包括內含 CAN、USB、ETHERNET、LCD 等的微處理器。還有使用較先進製程而達到更高功能/價格比的 PIC18FJ 系列以及執行效能數倍於 PIC18F 系列的 16-Bit MCU - PIC24F/PIC24H 以及 dsPIC30F/dsPIC33F。 爲了讓有心學習這些新型微處理器的使用者能有一個標準化的共同平台。於是 Microchip Taiwan office 推出 **APP023** 實習板，來滿足此類的需求.。

APP023 的 CPU 可以是安裝於主機板上的 80 PIN PIC18FXXXX or pic18FXXJXX. 或者利用 EJ1 – EJ4 這 4 個連接器，接上另外設計的 PIM 模組並且調整 JP-POWER & JP-MCLR 就可以 DISABLE 主機板的 CPU , 就可以外接其他的 CPU . 目前已經完成的 PIM 如下：

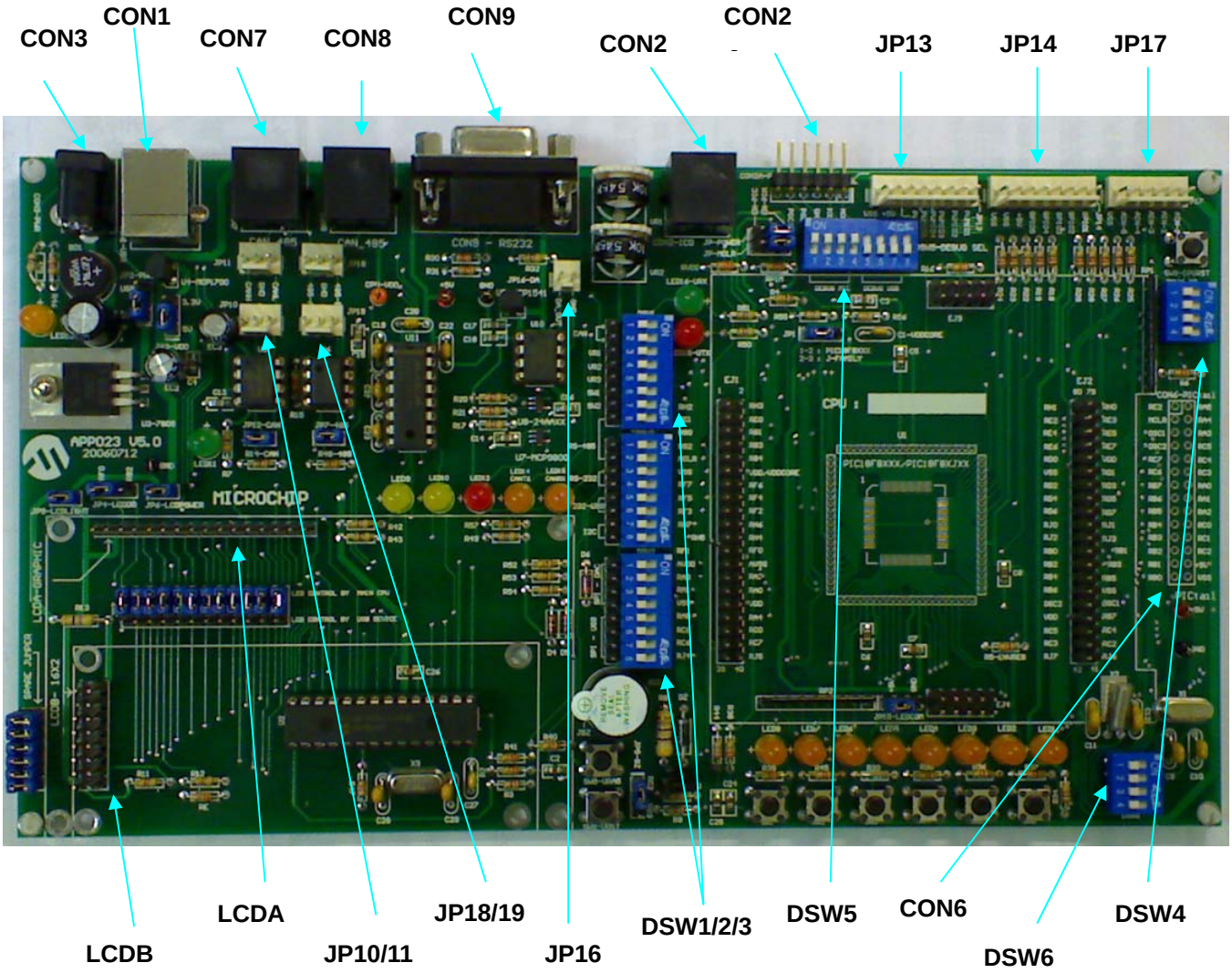
APP023-1 : 用於 80-PIN 的 PIC18F 系列

APP023-2 : 用於 dsPIC33FJ128MC708 或相對應的 CPU

APP023-3 : 用於 dsPIC30F6010A 或相對應的 CPU

1-2. APP023 主要的 CONNECTOR 及其功能

以下爲 APP023 主要 CONNECTOR 的位置標示



CON1　USB 連接器 **
（ APP023 可由 USB Bus 供電 ， 但需注意 USB 的供電是否足夠且須調整 JP2 ）
CON2　ICD2 除錯及燒錄用連接器 **
CON2A　與 PICKit2 相容的 ICD/ICSP 連接器 **
CON3　2.1mm 9V DC 電源輸入
CON6　與 PICTail 信號相容的界面 ， 可接 Microchip 標準的 pictAIL 子卡
CON7　CAN 與 RS-485 共用的連接器 ， 與 CON8 是並連的
CON8　CAN 與 RS-485 共用的連接器 ， 與 CON7 是並連的
CON9　DB-9 ， 用於 RS-232 通信的 9-PIN D-Type Connector
LCDA　使用於連接 Graphic LCD 模組的連接器
LCDB　使用於連接 文字型 LCD 模組的連接器

DSW5　切換 CON2 及 CON2A 的 ICD/ICSP 信號連接至主 CPU 或 U2(PIC18F2550)

DSW6　CPU 的主要外接振盪器與 TIMER1 振盪器的致能開關

CPU XTAL 致能 -> DSW6 的 1 & 2

TIMER1 XTAL 致能-> DSW6 的 3 & 4

DSW4　保留來做為 ID 選擇的開關，有 RP1 排阻為提昇電阻並連接至 CPU 的下列信號

DSW4-PIN1 - 連接到 P-GPIO1/RH0

DSW4-PIN2 - 連接到 P-GPIO2/RH1

DSW4-PIN3 - 連接到 P-GPIO3/RH2

DSW4-PIN4 - 連接到 P-GPIO4/RH3

DSW1~3　DSW1, DSW2 , DSW3 用來切換 CPU 信號與機板上的周邊是否連線

DSW1-PIN1/2　CAN 收發器 (U5 , MCP2551)

DSW1-PIN3　VR1

DSW1-PIN4　VR2

DSW1-PIN5　VR3 (用來讀取 SW3 ~ SW6 的按鍵值

DSW1-PIN6　SW1 (連接到 按鍵 1)

DSW1-PIN7　SW2 (連接到 按鍵 2)

DSW1-PIN8　RS-485 DE (連接到 P-RS485DE/RB4)

DSW2-PIN1/2　RS485 的 TX & RX , 接到 P-UTX/RC6 & P-URX/RC7

DSW2-PIN3/4　RS-232 的 TX & RX , 接到 P-UTX/RC6 & P-URX/RC7

DSW2-PIN5/6　利用 RS-232 與 USB (PIC18F2550) 的 RS-232 連接

UTX-USB/URX-USB 與主 CPU 的 P-UTX/RC6 , P-URX/RC7

DSW2-PIN7/8　利用 I2C 連接機板上的溫度感測器與 EEPROM

DSW3-PIN1/4　利用 SPI 連接機板上的 DAC (MCP4921)

P-GPIO5/RB1 - LOAD-DA

P-SPIDO/RC5 - SPIDO-DA

P-SPISCK/RC3 - SPISCK-DA

P-SPISS/RB5 - SPISS-DA

DSW3-PIN5/8　利用主 CPU 的 SPI 與 USB (PIC18F2550)的 SPI 相連

P-SPIDI/RC4 - SPIDI/USB

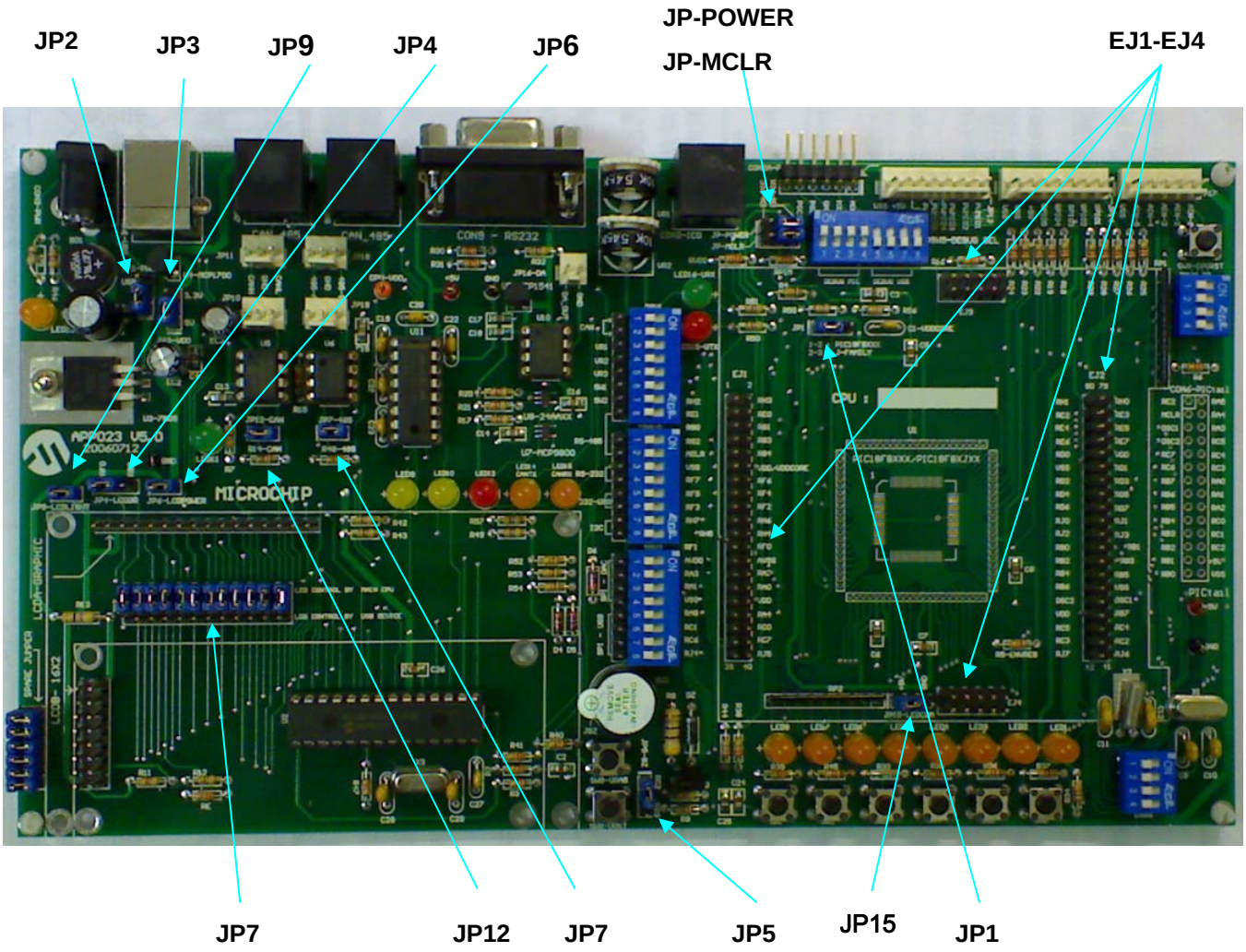
P-SPIDO/RC5 - SPIDO/USB

P-SPISCK/RC3 - SPISCK/USB

P-SPISS/RB5 - SPISS/USB

1-3. APP023 主要的 JUMPER 及其功能

以下爲 APP023 主要 JUMPER 的位置標示

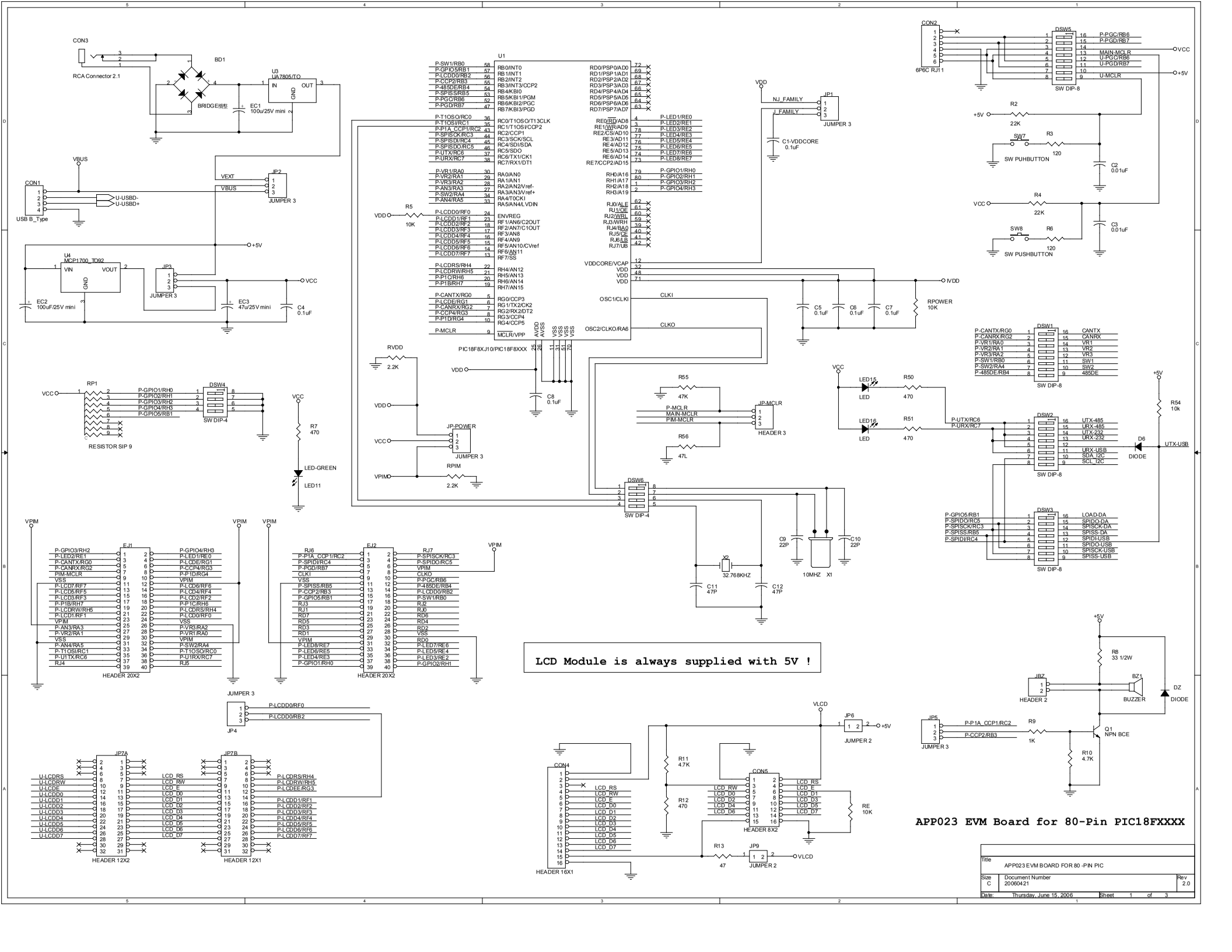


JP2	5V VCC 來源選擇 , 1&2 ON 選外部的 9V DC , 2&3 ON 選 USB
JP3	主 CPU VDD 的電壓選擇 , 1&2 ON 選 5V , 2&3 ON 選 3.3V
JP-POWER	JP-POWER & JP-MCLR 控制 CPU 的 VDD 與 MCLR 要供應至主機板的 CPU 或 PIM
JP-MCLR	>> JP-POWER & JP-MCLR 的 1&2 ON 時 , VDD 與 MCLR 供應至主機板的 CPU
	>> JP-POWER & JP-MCLR 的 2&3 ON 時 , VDD 與 MCLR 供應至 PIM
	** 利用 JP-POWER & JP-MCLR 的控制 , 可以讓使用者在 PIM 不拔除的狀態下自行選擇要讓主機板的 CPU 或 PIM 上的 CPU 工作
	** PIM 是 Plug-In-Module 的縮寫 , 指的是 CPU 的擴充板
JP1	用來選擇主機板上的 CPU 種類
	>> 1&2 ON 選擇 PIC18F8XXX 等可工作至 5V DC 的 CPU
	>> 2&3 ON 選擇工作電壓為 3.3 V 的 PIC18FXXJXX , J 系列產品
EJ1-EJ4	這 4 個 Connector 用來連接 PIM 或者是使用者自行設計的轉接板

JP15　　控制 LED1 到 LED8 限流電阻要共地或者是 VDD
　　APP023 在出貨時的接法為共 VDD 的方式
JP5　　選擇蜂鳴器由 RC2 or RB3 推動
JP7　　RS-485 終端電阻 (R48)的致能用
JP12　　CAN 終端電阻 (R14) 的致能用
JP7　　12*3 的 Jumper , 用來選擇 LCD 的驅動信號來自主 CPU 或是 USB 控制器(U2)
　　APP023 的預設值為 2&3 ON , 也就是由主 CPU 來控制 LCD
JP9　　控制 LCD 的背光電源 , CLOSE = ON
JP4　　選擇 LCD 模組的 Data 0 來源 , 1&2 ON = RF0 , 2&3 ON = RB2
JP6　　LCD 模組的電源開關

1-4 電路圖

以下為 APP023 之線路圖


CON3
RCA Connector 2.1
BD1
BRIDGE桥整
U3
UA7805/TO
IN
OUT
GND
EC1
100u/25V mini
VBUS
CON1
USB B_Type
U-USBD-
U-USBD+
VEXT
VBUS
JP2
JUMPER 3
+5V
U4
MCP1700_TO92
VIN
VOUT
GND
JP3
JUMPER 3
VCC
EC2
100uF/25V mini
EC3
47u/25V mini
C4
0.1uF
U1
P-SW1/RB0
P-GPIO5/RB1
P-LCDD0/RB2
P-CCP2/RB3
P-485DE/RB4
P-SPISS/RB5
P-PGC/RB6
P-PGD/RB7
P-T1OSO/RC0
P-T1OSI/RC1
P-P1A_CCP1/RC2
P-SPISCK/RC3
P-SPISDI/RC4
P-SPISDO/RC5
P-UTX/RC6
P-URX/RC7
P-VR1/RA0
P-VR2/RA1
P-VR3/RA2
P-SW2/RA4
P-AN4/RA5
P-LCDD0/RF0
P-LCDD1/RF1
P-LCDD2/RF2
P-LCDD3/RF3
P-LCDD4/RF4
P-LCDD5/RF5
P-LCDD6/RF6
P-LCDD7/RF7
P-LCDRS/RH4
P-LCDRW/RH5
P-P1B/RH6
P-P1C/RH7
P-CANTX/RG0
P-CANRX/RG2
P-CCP4/RG3
P-P1D/RG4
P-MCLR
RD0/PSP0/AD0
RD1/PSP1/AD1
RD2/PSP2/AD2
RD3/PSP3/AD3
RD4/PSP4/AD4
RD5/PSP5/AD5
RD6/PSP6/AD6
RD7/PSP7/AD7
RE0/RD/AD8
RE1/WR/AD9
RE2/CS/AD10
RE3/AD11
RE4/AD12
RE5/AD13
RE6/AD14
RE7/CCP2/AD15
RH0/A16
RH1/A17
RH2/A18
RH3/A19
RJ0/ALE
RJ1/OE
RJ2/WRL
RJ3/WRH
RJ4/BA0
RJ5/CE
RJ6/LB
RJ7/UB
VDDCORE/VCAP
VDD
VDD
VDD
OSC1/CLKI
OSC2/CLKO/RA6
MCLR/VPP
AVDD
AVSS
VSS
VSS
VSS
VSS
PIC18F8XJ10/PIC18F8XXX
RC0/T1OSO/T13CLK
RC1/T1OSI/CCP2
RC2/CCP1
RC3/SCK/SCL
RC4/SDI/SDA
RC5/SDO
RC6/TX1/CK1
RC7/RX1/DT1
RA0/AN0
RA1/AN1
RA2/AN2/Vref-
RA3/AN3/Vref+
RA4/T0CKI
RA5/AN4/LVDIN
ENVREG
RF1/AN6/C2OUT
RF2/AN7/C1OUT
RF3/AN8
RF4/AN9
RF5/AN10/CVref
RF6/AN11
RF7/SS
RH4/AN12
RH5/AN13
RH6/AN14
RH7/AN15
RG0/CCP3
RG1/TX2/CK2
RG2/RX2/DT2
RG3/CCP4
RG4/CCP5
NJ_FAMILY
J_FAMILY
JP1
JUMPER 3
C1-VDDCORE
0.1uF
R5
10K
RVDD
2.2K
C8
0.1uF
JP-POWER
JUMPER 3
RPIM
2.2K
R55
47K
P-MCLR
MAIN-MCLR
PIM-MCLR
JP-MCLR
HEADER 3
R56
47L
C5
0.1uF
C6
0.1uF
C7
0.1uF
RPOWER
10K
IVDD
CLKI
CLKO
RP1
RESISTOR SIP 9
P-GPIO1/RH0
P-GPIO2/RH1
P-GPIO3/RH2
P-GPIO4/RH3
P-GPIO5/RB1
DSW4
SW DIP-4
R7
470
LED-GREEN
LED11
DSW6
SW DIP-4
CON2
6P6C RJ11
DSW5
SW DIP-8
P-PGC/RB6
P-PGD/RB7
MAIN-MCLR
P-PGD/RB7
U-MCLR
R2
22K
SW7
SW PUHBUTTON
R3
120
C2
0.01uF
R4
22K
SW8
SW PUSHBUTTON
R6
120
C3
0.01uF
DSW1
SW DIP-8
P-CANTX/RG0
P-CANRX/RG2
P-VR1/RA0
P-VR2/RA1
P-VR3/RA2
P-SW1/RB0
P-SW2/RA4
P-485DE/RB4
CANTX
CANRX
VR1
VR2
VR3
SW1
SW2
485DE
LED15
LED
R50
470
LED16
LED
R51
470
DSW2
SW DIP-8
P-UTX/RC6
P-URX/RC7
UTX-485
URX-485
UTX-232
URX-232
URX-USB
SDA_I2C
SCL_I2C
D6
DIODE
UTX-USB
R54
10k
DSW3
SW DIP-8
P-GPIO5/RB1
P-SPIDO/RC5
P-SPISCK/RC3
P-SPISS/RB5
P-SPIDI/RC4
LOAD-DA
SPIDO-DA
SPISCK-DA
SPISS-DA
SPIDI-USB
SPIDO-USB
SPISCK-USB
SPISS-USB
C9
22P
C10
22P
X2
32.768KHZ
10MHZ
X1
C11
47P
C12
47P
EJ1
HEADER 20X2
P-GPIO3/RH2
P-LED2/RE1
P-CANTX/RG0
P-CANRX/RG2
PIM-MCLR
VSS
P-LCD7/RF7
P-LCD5/RF5
P-LCD3/RF3
P-P1B/RH7
P-LCDRW/RH5
P-LCD1/RF1
VPIM
P-AN3/RA3
P-VR2/RA1
VSS
P-AN4/RA5
P-T1OSI/RC1
P-U1TX/RC6
RJ4
P-GPIO4/RH3
P-LED1/RE0
P-LCDE/RG1
P-CCP4/RG3
P-P1D/RG4
VPIM
P-LCD6/RF6
P-LCD4/RF4
P-LCD2/RF2
P-P1C/RH6
P-LCDRS/RH4
P-LCD0/RF0
VSS
P-VR3/RA2
P-VR1/RA0
VPIM
P-SW2/RA4
P-T1OSO/RC0
P-U1RX/RC7
RJ5
EJ2
HEADER 20X2
RJ6
P-P1A_CCP1/RC2
P-SPIDI/RC4
P-PGD/RB7
CLKI
VSS
P-SPISS/RB5
P-CCP2/RB3
P-GPIO5/RB1
RJ3
RJ1
RD7
RD5
RD3
RD1
VPIM
P-LED3/RE7
P-LED6/RE5
P-LED4/RE3
P-GPIO1/RH0
RJ7
P-SPISCK/RC3
P-SPIDO/RC5
VPIM
CLKO
P-PGC/RB6
P-485DE/RB4
P-LCDD0/RB2
P-SW1/RB0
RJ2
RJ0
RD6
RD4
RD2
VSS
RD0
P-LED7/RE6
P-LED5/RE4
P-LED3/RE2
P-GPIO2/RH1
JUMPER 3
JP4
P-LCDD0/RF0
P-LCDD0/RB2
JP7A
JP7B
HEADER 12X2
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U-LCDRS
U-LCDRW
U-LCDE
U-LCDD0
U-LCDD1
U-LCDD2
U-LCDD3
U-LCDD4
U-LCDD5
U-LCDD6
U-LCDD7
LCD_RS
LCD_RW
LCD_E
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LCD_D1
LCD_D2
LCD_D3
LCD_D4
LCD_D5
LCD_D6
LCD_D7
P-LCDRS/RH4
P-LCDRW/RH5
P-LCDEE/RG3
P-LCDD1/RF1
P-LCDD2/RF2
P-LCDD3/RF3
P-LCDD4/RF4
P-LCDD5/RF5
P-LCDD6/RF6
P-LCDD7/RF7
LCD Module is always supplied with 5V !
VLCD
JP6
JUMPER 2
CON4
HEADER 16X1
CON5
HEADER 8X2
R11
4.7K
R12
470
RE
10K
R13
47
JP9
JUMPER 2
JBZ
HEADER 2
BZ1
BUZZER
DZ
DIODE
R8
33 1/2W
JP5
JUMPER 3
P-P1A_CCP1/RC2
P-CCP2/RB3
R9
1K
Q1
NPN BCE
R10
4.7K
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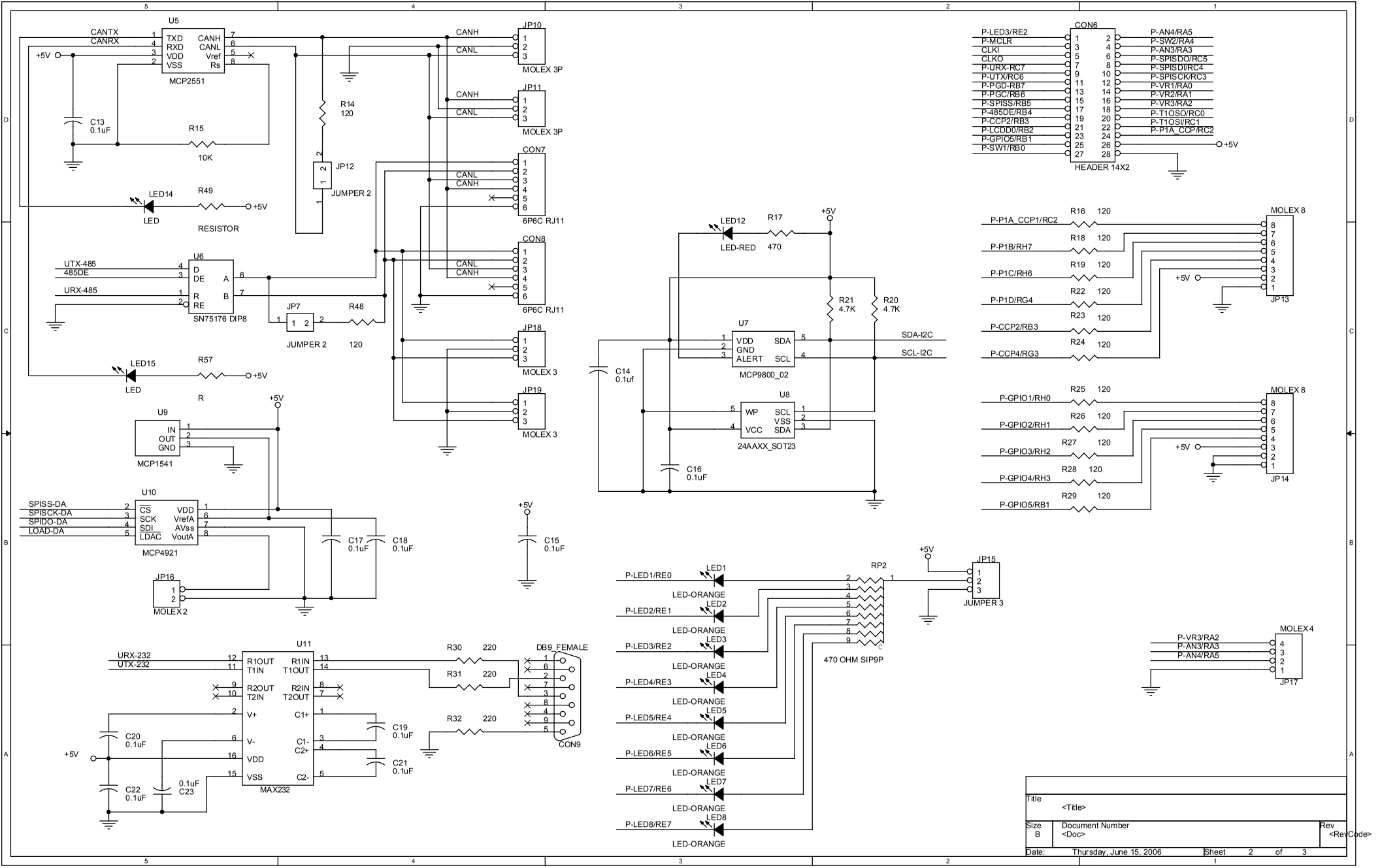
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RXD
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VSS
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CANL
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10K
R14
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JP12
JUMPER 2
LED14
R49
LED
RESISTOR
JP10
JP11
MOLEX 3P
CON7
6P6C RJ11
U6
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485DE
URX-485
D
DE
R
RE
A
B
SN75176 DIP8
JP7
JUMPER 2
R48
120
CON8
JP18
JP19
MOLEX 3
LED15
R57
R
U9
IN
OUT
GND
MCP1541
U10
SPISS-DA
SPISCK-DA
SPIDO-DA
LOAD-DA
CS
SCK
SDI
LDAC
VDD
VrefA
AVss
VoutA
MCP4921
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C18
0.1uF
C15
0.1uF
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MOLEX 2
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URX-232
UTX-232
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T1IN
R1IN
T1OUT
R2OUT
T2IN
R2IN
T2OUT
V+
V-
VDD
VSS
C1+
C1-
C2+
C2-
MAX232
C19
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C20
0.1uF
C21
0.1uF
C22
0.1uF
0.1uF
C23
R30
220
R31
220
R32
220
DB9_FEMALE
CON9
LED12
R17
LED-RED
470
R21
4.7K
R20
4.7K
U7
VDD
GND
ALERT
SDA
SCL
MCP9800_02
SDA-I2C
SCL-I2C
C14
0.1uf
U8
WP
VCC
24AAXX_SOT23
C16
0.1uF
CON6
P-LED3/RE2
P-MCLR
CLKI
CLKO
P-URX-RC7
P-UTX/RC6
P-PGD-RB7
P-PGC/RB6
P-SPISS/RB5
P-485DE/RB4
P-CCP2/RB3
P-LCDD0/RB2
P-GPIO5/RB1
P-SW1/RB0
P-AN4/RA5
P-SW2/RA4
P-AN3/RA3
P-SPISDO/RC5
P-SPISDI/RC4
P-SPISCK/RC3
P-VR1/RA0
P-VR2/RA1
P-VR3/RA2
P-T1OSO/RC0
P-T1OSI/RC1
P-P1A_CCP/RC2
HEADER 14X2
P-P1A_CCP1/RC2
P-P1B/RH7
P-P1C/RH6
P-P1D/RG4
P-CCP2/RB3
P-CCP4/RG3
R16
R18
R19
R22
R23
R24
120
MOLEX 8
JP13
P-GPIO1/RH0
P-GPIO2/RH1
P-GPIO3/RH2
P-GPIO4/RH3
P-GPIO5/RB1
R25
R26
R27
R28
R29
JP14
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
P-LED1/RE0
P-LED2/RE1
P-LED3/RE2
P-LED4/RE3
P-LED5/RE4
P-LED6/RE5
P-LED7/RE6
P-LED8/RE7
LED-ORANGE
RP2
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JP15
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of
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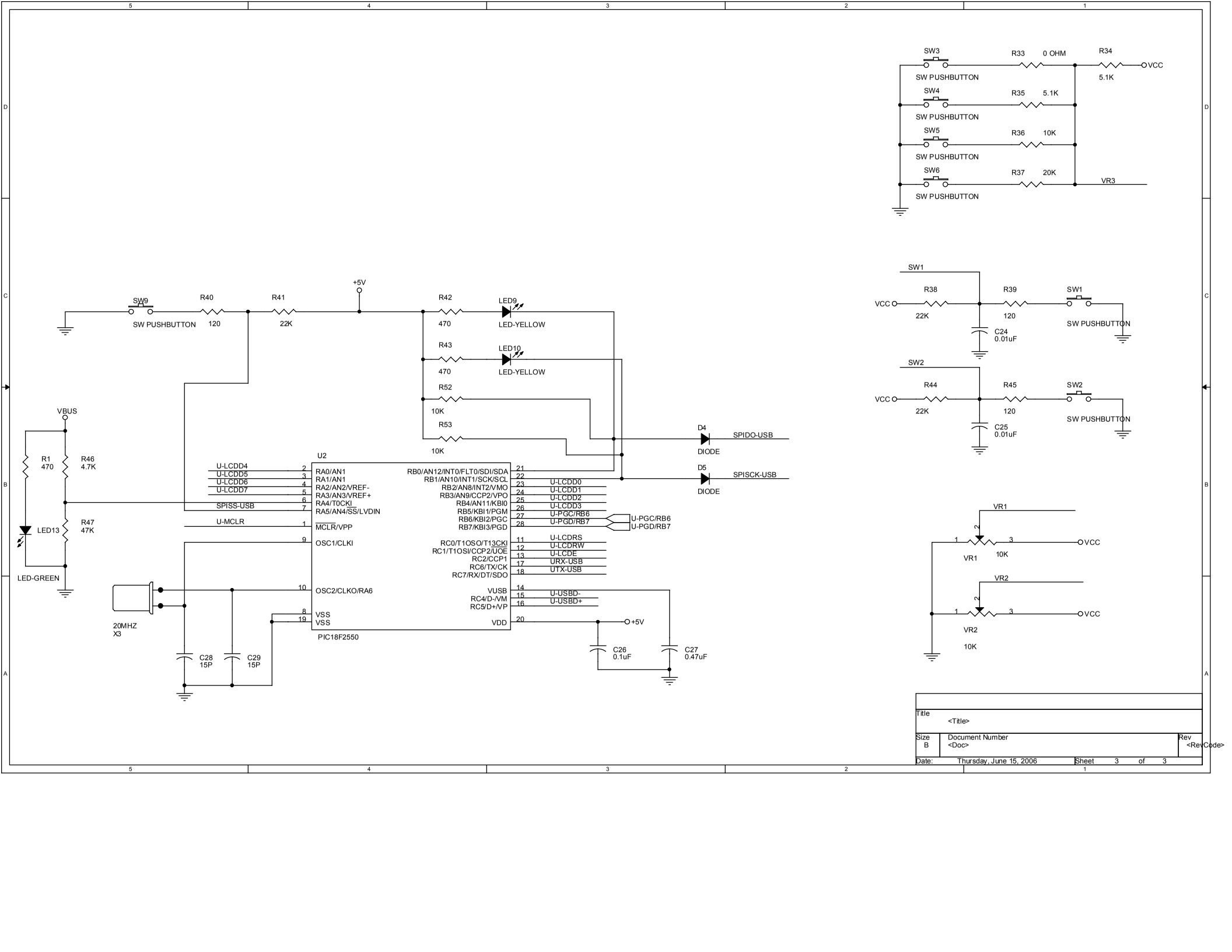

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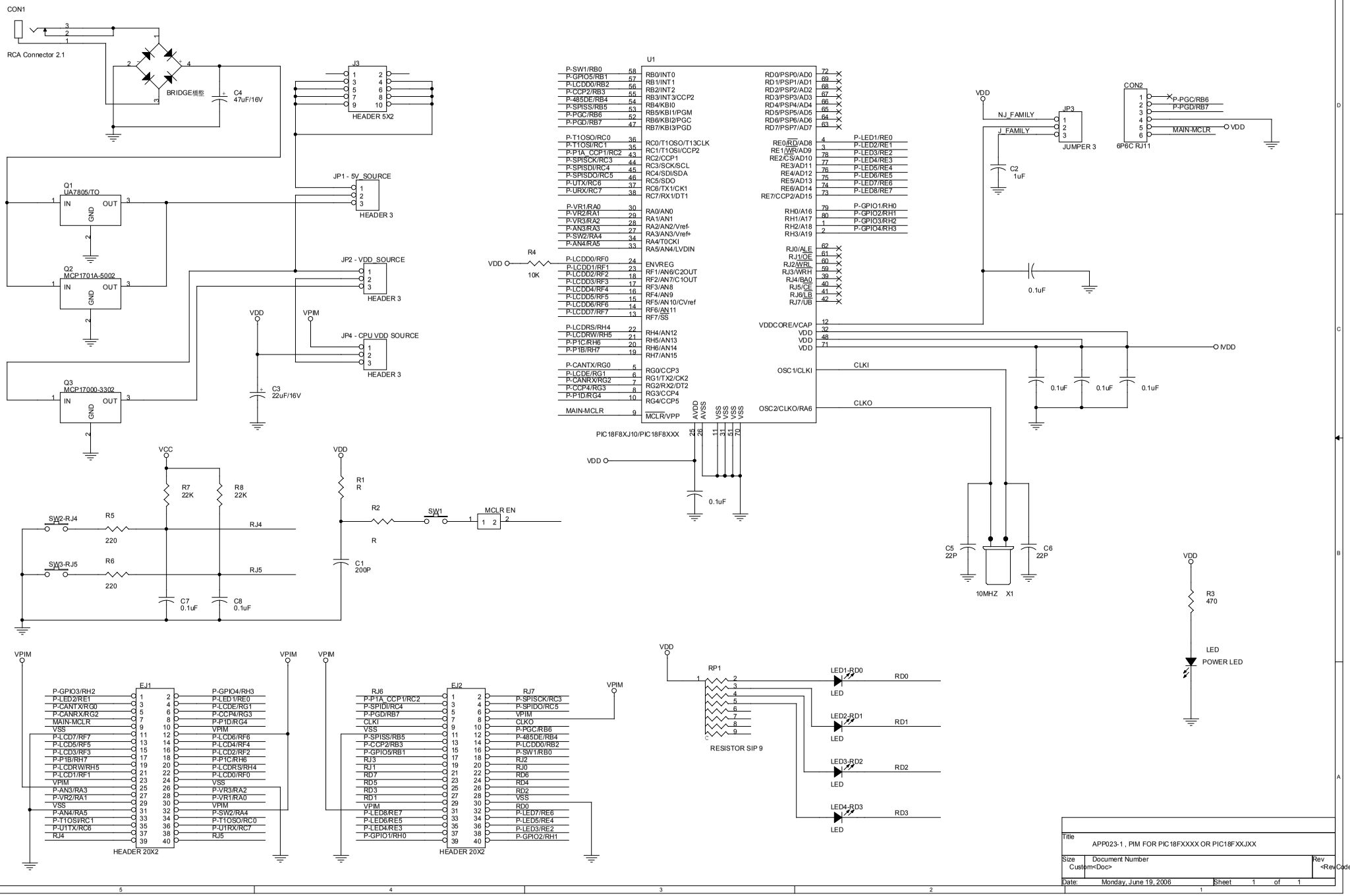

CON1
RCA Connector 2.1
BRIDGE橋整
C4
47uF/16V
J3
HEADER 5X2
Q1
UA7805/TO
IN
OUT
GND
Q2
MCP1701A-5002
Q3
MCP17000-3302
JP1 - 5V_SOURCE
JP2 - VDD_SOURCE
JP4 - CPU VDD SOURCE
HEADER 3
C3
22uF/16V
VDD
VPIM
VCC
R7
22K
R8
22K
SW2-RJ4
SW3-RJ5
R5
R6
220
RJ4
RJ5
C7
0.1uF
C8
0.1uF
R1
R
R2
SW1
MCLR EN
C1
200P
U1
P-SW1/RB0
P-GPIO5/RB1
P-LCDD0/RB2
P-CCP2/RB3
P-485DE/RB4
P-SPISS/RB5
P-PGC/RB6
P-PGD/RB7
P-T1OSO/RC0
P-T1OSI/RC1
P-P1A_CCP1/RC2
P-SPISCK/RC3
P-SPISDI/RC4
P-SPISDO/RC5
P-UTX/RC6
P-URX/RC7
P-VR1/RA0
P-VR2/RA1
P-VR3/RA2
P-AN3/RA3
P-SW2/RA4
P-AN4/RA5
P-LCDD0/RF0
P-LCDD1/RF1
P-LCDD2/RF2
P-LCDD3/RF3
P-LCDD4/RF4
P-LCDD5/RF5
P-LCDD6/RF6
P-LCDD7/RF7
P-LCDRS/RH4
P-LCDRW/RH5
P-P1C/RH6
P-P1B/RH7
P-CANTX/RG0
P-LCDE/RG1
P-CANRX/RG2
P-CCP4/RG3
P-P1D/RG4
MAIN-MCLR
RD0/PSP0/AD0
RD1/PSP1/AD1
RD2/PSP2/AD2
RD3/PSP3/AD3
RD4/PSP4/AD4
RD5/PSP5/AD5
RD6/PSP6/AD6
RD7/PSP7/AD7
RE0/RD/AD8
RE1/WR/AD9
RE2/CS/AD10
RE3/AD11
RE4/AD12
RE5/AD13
RE6/AD14
RE7/CCP2/AD15
P-LED1/RE0
P-LED2/RE1
P-LED3/RE2
P-LED4/RE3
P-LED5/RE4
P-LED6/RE5
P-LED7/RE6
P-LED8/RE7
RH0/A16
RH1/A17
RH2/A18
RH3/A19
P-GPIO1/RH0
P-GPIO2/RH1
P-GPIO3/RH2
P-GPIO4/RH3
RJ0/ALE
RJ1/OE
RJ2/WRL
RJ3/WRH
RJ4/BA0
RJ5/CE
RJ6/LB
RJ7/UB
VDDCORE/VCAP
OSC1/CLKI
OSC2/CLKO/RA6
PIC18F8XJ10/PIC18F8XXX
R4
10K
NJ_FAMILY
J_FAMILY
JP3
JUMPER 3
C2
1uF
0.1uF
CON2
6P6C RJ11
P-PGC/RB6
P-PGD/RB7
MAIN-MCLR
IVDD
CLKI
CLKO
C5
22P
C6
22P
10MHZ
X1
R3
470
LED
POWER LED
RP1
RESISTOR SIP 9
LED1-RD0
LED2-RD1
LED3-RD2
LED4-RD3
RD0
RD1
RD2
RD3
EJ1
HEADER 20X2
EJ2
HEADER 20X2
RJ6
RJ7
Title
APP023-1 , PIM FOR PIC18FXXXX OR PIC18FXXJXX
Size
Custom<Doc>
Document Number
Rev
<RevCode>
Date:
Monday, June 19, 2006
Sheet
1
of
1

DOT MATRIX
LIQUID CRYSTAL DISPLAY
MODULE

LMG-SSC12K64 Serial

USER‘ MANUAL

	LMG-SSC12K64DRG		**LMG-SSC12K64DRY**
	LMG-SSC12K64DLGY		**LMG-SSC12K64DLYY**
	LMG-SSC12K64DLGY-E		**LMG-SSC12K64DLYY-E**

PROPOSED BY		**APPROVED**
Design	Approved	

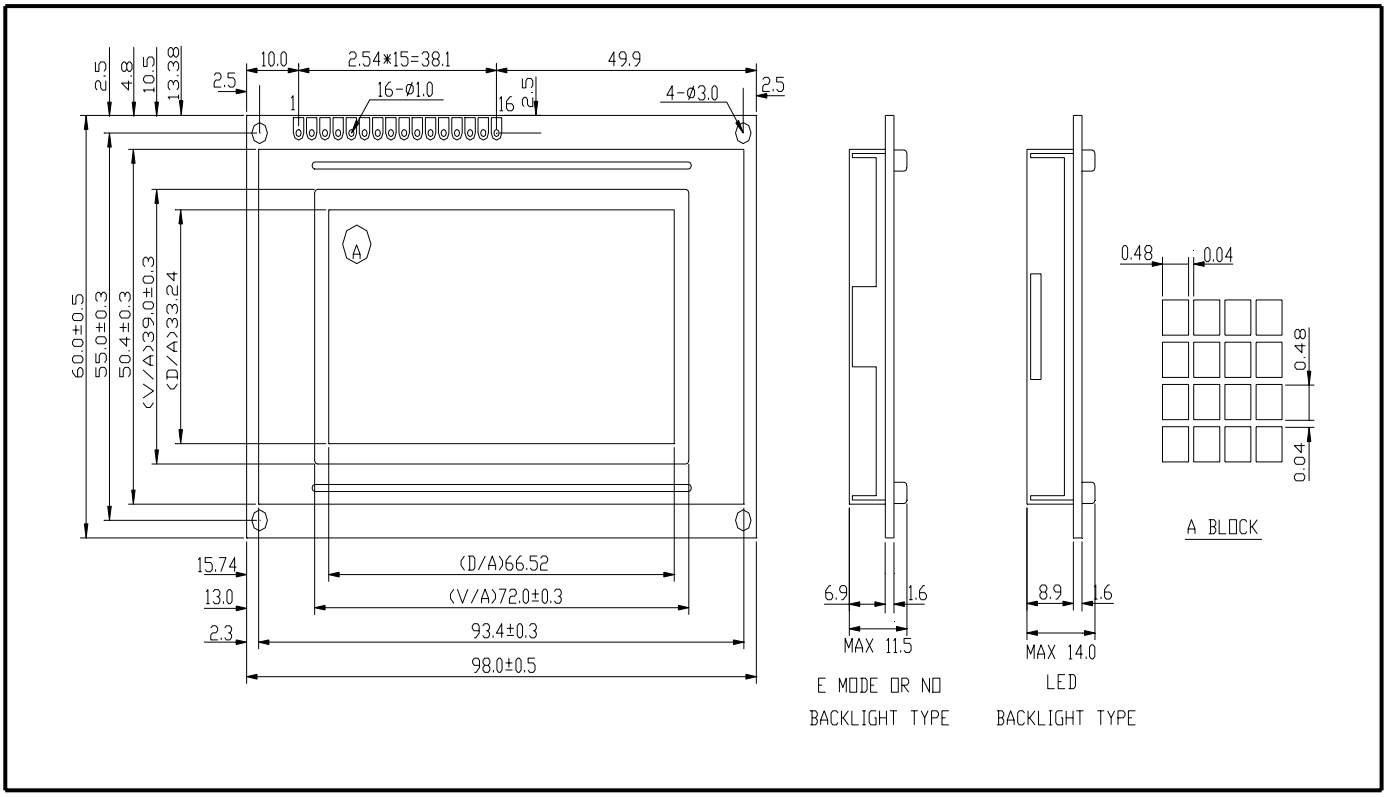
SDEC TECHNOLOGY CORP.

CONTENTS

1. Mechanical Specification

ITEM	STANDARD VALUE			UNIT
NUMBER OF CHARACTERS	8 CHARACTERS X 4 LINES (16*16 中文字)			--
CHARACTER FORMAT	16 X 16 DOTS			--
MODULE DIMENSION	98.0 (W) X 60.0 (H) X 11.5 (T)	98.0 (W) X 60.0 (H) X 14.0 (T)		mm
VIEWING DISPLAY AREA	72.0 (W) X 39.0 (H)			mm
ACTIVE DISPLAY AREA	66.52 (W) X 33.24 (H)			mm
DOT SIZE	0.48 (W) X 0.48 (H)			mm
DOT PITCH	0.52 (W) X 0.52 (H)			mm
LMG-SSC12K64DRG	STN , Gray , 1/32 Duty , 6 O'clock			
LMG-SSC12K64DRY	STN , Yellow Green , 1/32 Duty , 6 O'clock			
LMG-SSC12K64DLGY	STN , Gray , 1/32 Duty , 6 O'clock , LED Backlight			
LMG-SSC12K64DLYY	STN , Yellow Green , 1/32 Duty , 6 O'clock , LED Backlight			
LMG-SSC12K64DLGY-E	STN , Gray , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
LMG-SSC12K64DLYY-E	STN , Yellow Green , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
LED Backlight Color	Yellow Green			
LED Backlight Input	DC +5V	V	150	mA
Backlight Half-Lift Time	50,000			HR.
E Mode LED Backlight Color	Yellow Green			
E Mode LED Backlight Input	DC +5V	V	100	mA
E mode Backlight Half-Lift Time	30,000			HR.

2. Mechanical Diagram



3. Interface Pin Connections

NO	SYMBOL	LEVEL	FUNCTION	NO	SYMBOL	LEVEL	FUNCTION
1	VSS	--	GND (0V)	9	DB2	H/L	Data Bit 2
2	VDD	H/L	DC +5V	10	DB3	H/L	Data Bit 3
3	N.C	--	N.C	11	DB4	H/L	Data Bit 4
4	RS	H/L	Register select	12	DB5	H/L	Data Bit 5
5	R/W	H/L	Read/Write	13	DB6	H/L	Data Bit 6
6	E	H,H→L	Enable signal	14	DB7	H/L	Data Bit 7
7	DB0	H/L	Data Bit 0	15	A(+)	DC +5V	LED Backlight +
8	DB1	H/L	Data Bit 1	16	K(-)	0V	LED Backlight -

4. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYPE	MAX.	UNIT
OPERATING TEMPERATURE	TOP	0	--	+50	℃
STORAGE TEMPERATURE	TST	-10	--	+60	℃
INPUT VOLAGE	VI	VSS	--	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	5.0	6.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	--	--	6.5	V
STATIC ELECTRICITY	Be sure that you are grounded when handing LCM.				

5. Electrical Characteristics

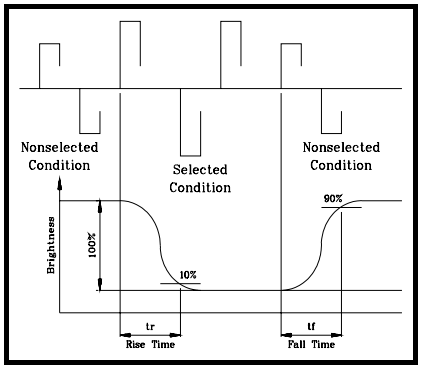
ITEM	SYN	CONDITION	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	4.5	5.0	5.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	Ta= 0 ℃	--	6.1	--	V
		Ta= +25 ℃	--	5.8	--	V
		Ta= +50 ℃	--	5.5	--	V
INPUT HIGH VOLTAGE	VIH	--	2.2	--	VDD	V
INPUT LOW VOLTAGE	VIL	--	0	--	0.6	V
OUTPUT HIGH VOLTAGE	VOH	--	2.4	--	--	V
OUTPUT LOW VOLTAGE	VOL	--	--	--	0.4	V
SUPPLY CURRENT	IDD	VDD=+5V	--	4.5	6.0	mA

6. Optical Characteristics

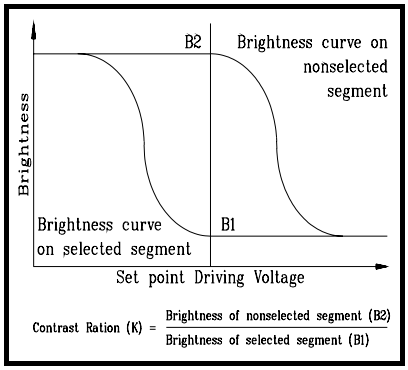
ITEM	SYM	CONDITION	MIN.	TYPE	MAX.	UNIT
VIEW ANGLE (V)	θ	CR≧2	-10	--	40	deg.
VIEW ANGLE (H)	φ	CR≧2	-30	--	30	deg.
CONTRAST RATIO	CR	--	--	5	--	--
RESPONSE TIME	TON	--	--	180	230	mS
RESPONSE TIME	TOFF	--	--	100	150	mS

7. Optical Definitions

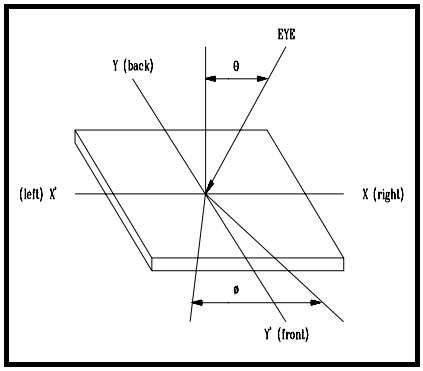
Response Time



Contrast Ration



View Angle



8. Display Address

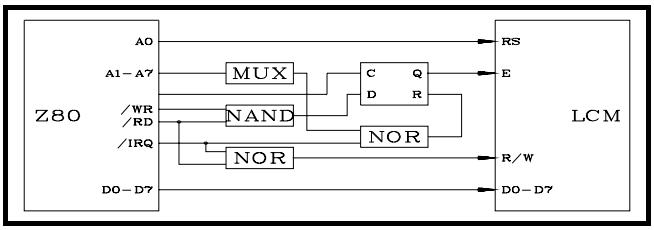
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80H		81H		82H		83H		84H		85H		86H		87H	
Line 2	90H		91H		92H		93H		94H		95H		96H		97H	
Line 3	88H		89H		8AH		8BH		8CH		8DH		8EH		8FH	
Line 4	98H		99H		9AH		9BH		9CH		9DH		9EH		9FH	

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Line 1																
Line 2																
Line 3																
Line 4																

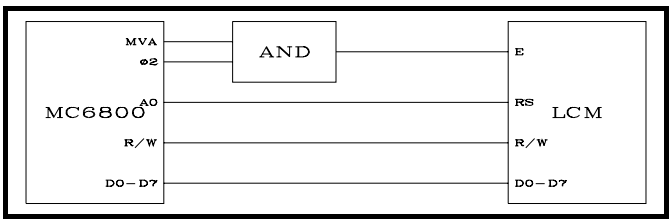
*A Ram Bank is 16 bits (2 bytes)

9. Interface to MPU

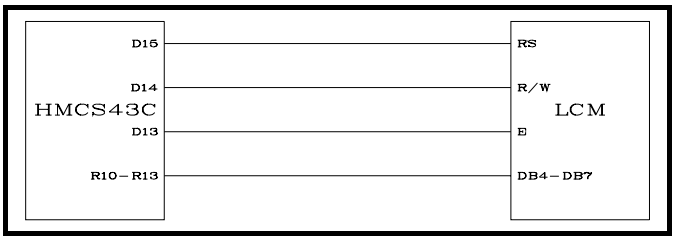
9.1 Interface to Z-80 CPU



9.2 Interface to MC6800 CPU



9.3 Interface to 4-bit CPU (HMCS43C)

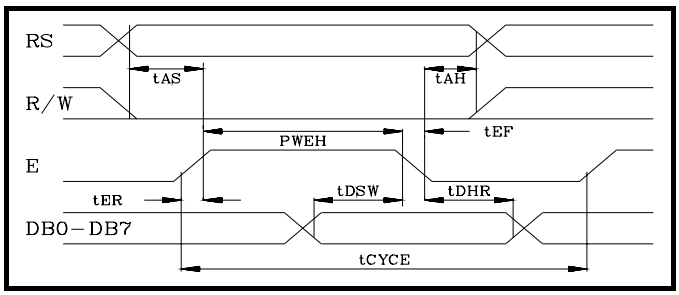


9.4 Interface to HD6805 MP

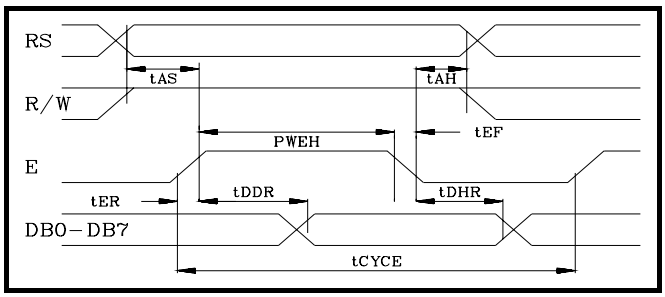
10. Timing Control

10.1 Write and Read Operation

Write Operation

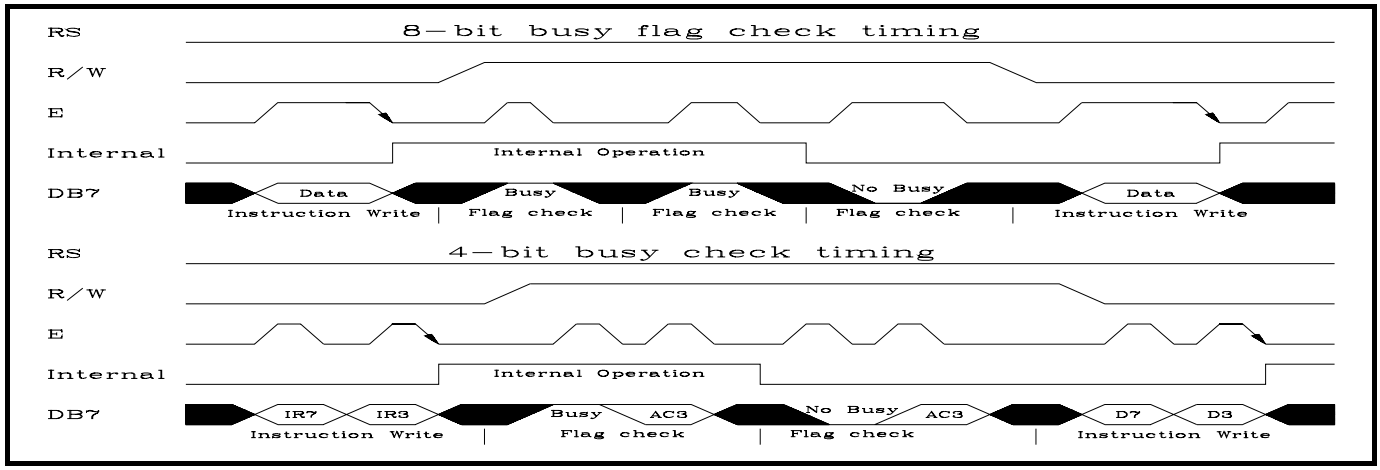


Read Operation



Item	Symbol	Limit (Min.)	Limit (Max.)	Unit
Enable Cycle Time	tCYCE	1200	--	ns
Enable Pules Width (High level)	PWEH	140	--	ns
Enable Rise/Fall Time	tER,tEF	--	25	ns
Address Set-Up Time (RS,R/W,E)	tAS	10	--	ns
Address Hole Time	tAH	20	--	ns
Data Set-Up Time	tDSW	40	--	ns
Data Delay Time	tDDR	--	100	ns
Data Hold Time	tDHR	20	--	ns

10.2 Busy flag check timing

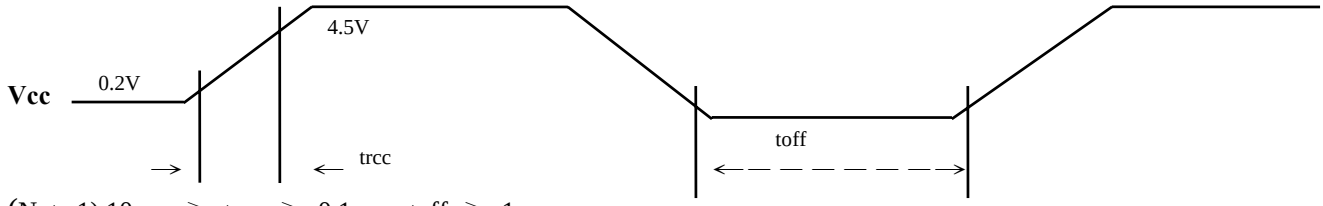


Note : IR7, IR3 : Instruction 7th bit , 3rd bit ; AC3 : Address Counter 3rd bit.

11. Initialization of LCM

The LCM automatically initializes (reset) when power is turned on using the internal reset circuit. If the power supply conditions for correctly operating of the internal reset circuit are not met, initialization by instruction is required. Use the procedure is next page for initialization.

Internal Power Supply reset



(Note 1) 10 ms ≧ trcc ≧ 0.1 ms , toff ≧ 1 ms.
(Note 2) toff stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

Item	Symbol	Test condition	Limit (Min.)	Limit (Max.)	Unit
Power supply rise time	trcc	--	0.1	10	ms
Power supply off time	toff	--	1	--	ms

8 bit Interface

Power On

Wait time > 40 ms

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	0	X	X

Wait time > 100 μ s

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	0	X	X

Wait time > 37 μ s

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Wait time > 100 μ s

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Wait time > 10ms

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Initialization End

4 bit Interface

Power On

Wait time > 40 ms

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

Wait time > 100 μ s

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	X	0	X	X	X	X	X	X

Wait time > 100 μ s

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

Wait time > 100 μ s

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

Wait time > 10ms

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	S	X	X	X	X

Initialization End

12. Instruction Set

Instruction Table: (RE=0: Enable basic instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and return the cursor to home position (address 0).	4.6ms
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to the home position. Also returns the display being shifted to the original position. DDRAM contents remain unchanged.	4.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operation are performed during data rite/read. For normal operation. I/D=1 : increment ; 0 :decrement ; S=1 : accompanies display shift when data is written, for normal operation, set to zero.	72 μ s
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	D=1: ON display ; 0:OFF display. C=1: ON cursor ; 0: OFF cursor. B=1: ON blink cursor ; 0: OFF blink cursor.	72 μ s
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C=1: Display shift; 0:Cursor move. R/L=1: shift to right; 0: shift to left.	72 μ s
Function Set (Modify)	0	0	0	0	1	DL	X	0 RE	X	X	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=0: Normal instruction .1: Extended instruction.	72 μ s
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	72 μ s
Set DDRAM address	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	72 μ s
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μ s
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μ s
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μ s

Instruction Table (RE=1: Enable extension instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby Mode	0	0	0	0	0	0	0	0	0	1	Enter standby mode, only Icon areas display Standby mode can be released by any other instructions.	72 μ s
Start Row Enable	0	0	0	0	0	0	0	0	1	SR	SR=1: Allow change start display Row. SR=0: Disable start display Row change.	72 μ s
Reverse Line select	0	0	0	0	0	0	0	1	R1	R0	Choice one of 4 line which data is reverse display.	72 μ s
Sleep mode and set GRAM page	0	0	0	0	0	0	1	SL	X	X	SL=0:Enter sleep mode. 1:Wake-up from sleep mode	72 μ s
Function Set (Modify)	0	0	0	0	1	DL	X	1 RE	G	0	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=1: Extended instruction.0: Normal instruction. G=1: Graphic display ON. 0: Graphic display OFF	72 μ s
Set Iram/Start Row address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5 – AC0 is start Row. SR=0: AC3 – AC0 is ICON RAM address.	72 μ s
Set Graphic RAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set GDRAM address in address counter. Execute once set the address of display row (AC6-AC0). Execute again set the address of display column (AC3-AC0).	72 μ s
				0	0	0	AC3	AC2	AC1	AC0		

13. User Font Patterns (CG RAM Character)

Character Code (DDRAM data)					CGRAM Address						CGRAM data (High byte)								CGRAM data (Low byte)							
B15 – B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00		X	00		0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0
							0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0
							0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
							0	0	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0
							0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0
							0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0
							0	1	1	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	0
							0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	0	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0
							1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	1	1	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0
							1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
							1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
							1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01		X	01		0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0
							0	0	1	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	0	0
							0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0
							0	1	0	0	1	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
							0	1	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
							0	1	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
							1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0
							1	0	0	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0
							1	0	1	1	1	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
							1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
							1	1	0	1	0	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
							1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14. Icon RAM Data

Icon RAM Address				Icon RAM Data															
				High Byte								Low Byte							
AC3	AC2	AC1	AC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Seg0	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	Seg8	Seg9	Seg10	Seg11	Seg12	Seg13	Seg14	Seg15
0	0	0	1	Seg16	Seg17	Seg18	Seg19	Seg20	Seg21	Seg22	Seg23	Seg24	Seg25	Seg26	Seg27	Seg28	Seg29	Seg30	Seg31
0	0	1	0	Seg32	Seg33	Seg34	Seg35	Seg36	Seg37	Seg38	Seg39	Seg40	Seg41	Seg42	Seg43	Seg44	Seg45	Seg46	Seg47
0	0	1	1	Seg48	Seg49	Seg50	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63
0	1	0	0	Seg64	Seg65	Seg66	Seg67	Seg68	Seg69	Seg70	Seg71	Seg72	Seg73	Seg74	Seg75	Seg76	Seg77	Seg78	Seg79
0	1	0	1	Seg80	Seg81	Seg82	Seg83	Seg84	Seg85	Seg86	Seg87	Seg88	Seg89	Seg90	Seg91	Seg92	Seg93	Seg94	Seg95
0	1	1	0	Seg96	Seg97	Seg98	Seg99	Seg100	Seg101	Seg102	Seg103	Seg104	Seg105	Seg106	Seg107	Seg108	Seg109	Seg110	Seg111
0	1	1	1	Seg112	Seg113	Seg114	Seg115	Seg116	Seg117	Seg118	Seg119	Seg120	Seg121	Seg122	Seg123	Seg124	Seg125	Seg126	Seg127
1	0	0	0	Seg128	Seg129	Seg130	Seg131	Seg132	Seg133	Seg134	Seg135	Seg136	Seg137	Seg138	Seg139	Seg140	Seg141	Seg142	Seg143
1	0	0	1	Seg144	Seg145	Seg146	Seg147	Seg148	Seg149	Seg150	Seg151	Seg152	Seg153	Seg154	Seg155	Seg156	Seg157	Seg158	Seg159
1	0	1	0	Seg160	Seg161	Seg162	Seg163	Seg164	Seg165	Seg166	Seg167	Seg168	Seg169	Seg170	Seg171	Seg172	Seg173	Seg174	Seg175
1	0	1	1	Seg176	Seg177	Seg178	Seg179	Seg180	Seg181	Seg182	Seg183	Seg184	Seg185	Seg186	Seg187	Seg188	Seg189	Seg190	Seg191
1	1	0	0	Seg192	Seg193	Seg194	Seg195	Seg196	Seg197	Seg198	Seg199	Seg200	Seg201	Seg202	Seg203	Seg204	Seg205	Seg206	Seg207
1	1	0	1	Seg208	Seg209	Seg210	Seg211	Seg212	Seg213	Seg214	Seg215	Seg216	Seg217	Seg218	Seg219	Seg220	Seg221	Seg222	Seg223
1	1	1	0	Seg224	Seg225	Seg226	Seg227	Seg228	Seg229	Seg230	Seg231	Seg232	Seg233	Seg234	Seg235	Seg236	Seg237	Seg238	Seg239
1	1	1	1	Seg240	Seg241	Seg242	Seg243	Seg244	Seg245	Seg246	Seg247	Seg248	Seg249	Seg250	Seg251	Seg252	Seg253	Seg254	Seg255

15. Graph Display RAM Address

GDRAM Column Address	GDRAM Row Address			
	0	1	-----	15
0	D15 → D0	D15 → D0	D15 → D0	D15 → D0
1	D15 → D0	D15 → D0	D15 → D0	D15 → D0
2	D15 → D0	D15 → D0	D15 → D0	D15 → D0
:	:	:	:	:
61	D15 → D0	D15 → D0	D15 → D0	D15 → D0
62	D15 → D0	D15 → D0	D15 → D0	D15 → D0
63	D15 → D0	D15 → D0	D15 → D0	D15 → D0

16. Software Example

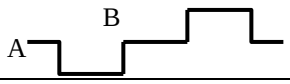
16.1 8-bit operation (8 bits 2 lines)

Function	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0	Display	Description
Power on delay												Initialization. No display appears.
Function set	0	0	0	0	1	1	0	0	0	0		Sets to 8-bit operation and selects 2-line display character font. (Note: number of display lines and character fonts cannot be change after this.)
Display OFF	0	0	0	0	0	0	1	0	0	0		Turn off display.
Display ON	0	0	0	0	0	0	1	1	1	0	_	Turn on display and cursor
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	_	Set mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM Display is not shifted.
Write data to CG/DD RAM	1 1	0 0	1 1	0 0	1 1	1 0	0 1	1 1	1 1	0 1	雄_	Write “雄”. Cursor incremented by one and shift to right.
Write data to CG/DD RAM	1 1	0 0	1 0	1 1	0 0	0 0	0 1	1 1	0 0	1 1	雄鐸	Write “鐸” .
Set DD RAM	0	0	1	0	0	1	0	0	0	0	雄鐸 _	Set RAM address so that the cursor is propositioned at the head of the second line.
Write data to CG/DD RAM	*	*									雄鐸 CR_	Write “C” , and “R”.
Cursor or display shift	0	0	0	0	0	1	0	0	x	x	雄鐸 CR	Shift only the cursor position to the left.
Write data to CG/DD RAM	*	*									雄鐸 CO., LTD._	Write “O., LTD.” .
Entry Mode Set	0	0	0	0	0	0	0	1	1	1	雄鐸 CO., LTD._	Set display mode shift at the time during writing operation.
Write data to CG/DD RAM	1	0	0	1	1	1	1	0	0	0	鐸 ., LTD. x_	Write “ x”. Cursor incremented by one and shift to right. (The display move to left.)
Write data to CG/DD RAM	*	*										Write other characters.
Return Home	0	0	0	0	0	0	0	0	1	0	雄鐸 CO., LTD.	Return both display and cursor to the original position (Set address to zero).

16.2 4-bit operation (4-bit, 1 line)

Function	RS	R/W	D7	D6	D5	D4	Display	Description
power on delay								initialization. No display appears.
Function set	0	0	0	0	1	0		Sets to 4-bit operation. In this case, operation is handled as 8-bits by initialization, and only this instruction completes with one write.
Function set	0 0	0 0	0 0	0 0	1 0	0 0		Sets 4-bit operation and selects 1-line display character font on and resetting is needed. (number of display lines and character fonts cannot be changed hence after).
Display ON/OFF Control	0 0	0 0	0 1	0 1	0 1	0 0	_	Turn on display and cursor.
Entry Mode Set	0 0	0 0	0 0	0 1	0 1	0 0	_	Set mode to incremented the address by one and to shift the cursor to the right, at the time of write. to the DD/CG RAM display is not shifted.
Write data to CG/DD RAM	1 1 1 1	0 0 0 0	1 0 1 1	0 1 0 1	1 1 1 1	1 0 0 1	雄_	Write “雄”. Cursor incremented by one and shift to right.
same as 8-bit operation								

17. Reliability Condition

			TN Type		STN Type	
			Normal Temp.	Wide Temp.	Normal Temp.	Wide Temp.
Viewing Angle	Horizontal Φ		±30°	±30°	±30°	±30°
	Vertical Θ(㎜)		-10° to 30°	-10° to 30°	-10° to 40°	-10° to 40°
Operating Temperature			-10 to 70℃	-25 to 80℃	0 to 50℃	*-20 to 70℃
Storage Temperature			-20 to 80℃	-35 to 90℃	-20 to 70℃	*-30 to 80℃
High Temperature (Power Off)			240 Hours @70℃	240 Hours @90℃	240 Hours @65℃	240 Hours @75℃
Low Temperature (Power Off)			240 Hours @-20℃	240 Hours @-35℃	240 Hours @-15℃	240 Hours @-25℃
High Temperature (Power On)			240 Hours @70℃	240 Hours @80℃	240 Hours @60℃	240 Hours @70℃
Low Temperature (Power On)			240 Hours @-10℃	240 Hours @-25℃	240 Hours @-10℃	240 Hours @-20℃
High Temperature & High Humidity			55℃/90%RH 240 Hours	75℃/90%RH 240 Hours	45℃/90%RH 240 Hours	65℃/90%RH 240 Hours
Thermal Shock 5 Cycle 		A	60min@-20℃	60min@-35℃	60min@-20℃	60min@-30℃
		B	5min@25℃	5min@25℃	5min@25℃	5min@25℃
		C	60min@70℃	60min@90℃	60min@70℃	60min@80℃
Expected Lift			50,000 Hours	50,000 Hours	50,000 Hours	50,000 Hours

*Wide temp. version may not available for some products, Please consult our sales engineer or respresentative.

18. Functional Test & Inspection Criteria

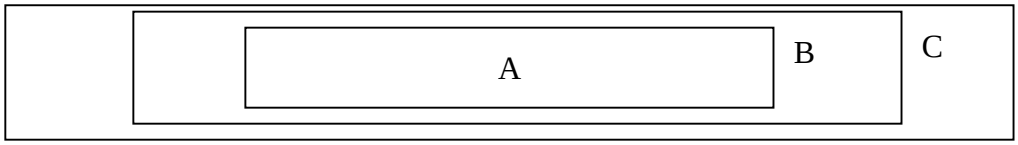
18.1 Sample plan

Sample plan according to MIL-STD-105D level 2, and acceptance/rejection criteria is.
Base on : Major defect : AQL 0.65 Minor defect : AQL 2.5

18.2 Inspection condition

Viewing distance for cosmetic inspection is 30cm with bare eyes, and under an environment of 800 lus (20W) light intensity. All direction for inspecting the sample should be within 45° against perpendicular line.

18.3 Definition of Inspection Zone in LCD



Zone A : Character / Digit area
Zone B : Viewing area except Zone A (Zone A + Zone B = minimum Viewing area)
Zone C : Outside viewing area (invisible area after assembly in customer's product)
Note : As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

18.4 Major Defect

All functional defects such as open (or missing segment), short, contrast differential, excess power consumption, smearing, leakage, etc. and overall outline dimension beyond the drawing. Are classified as major defects.

18.5Minor Defect

Except the Major defects above, all cosmetic defects are classified as minor defects.

Item No.	Item to be Inspected	Inspection Standard				Classification of defects
1.	Spot defect (Defects in spot from)	Zone size (mm)	Acceptable Qty			Minor
			A	B	C	
		Φ ≦0.15	Acceptable (clutering of spot not allowed)		Accepta-ble	
		0.15≦ Φ ≦0.20	1	2		
		0.20≦ Φ ≦0.25	0	1		
		Φ>0.25	0	0		
		Remarks : for dark/white spot, size Φ is defined as Φ=1/2(X+Y)				
2.	Line defect (Defects in line form)	Size (mm)		Acceptable Qty		Minor
		L Length	W Width	Zone		
				A B	C	
		Accep-table	W≦0.02	Accep-table	Accep-table	
		L≦3.0	W≦0.03	2		
		L>2.5	W≦0.03	0		
		L≦3.0	0.03<W≦0.05	2		
		L>2.5	0.03<W≦0.05	0		
			W>0.05	Counted as spot defect (Follows item 18.5.1)		
		Remarks: The total of spot defect and line defect shall not exceed four.				
3.	Orientation defect (such as misalignment of L/C)	Not allowed inside viewing area (Zone A or Zone B)				Minor
4.	Polarizing	18.5.4.1 Polarizer Position 1. Shifting in Position Should not exceed the glass outline dimension. 2. Incomplete covering of the viewing area due to Shifting is not allowed.				Minor
		18.5.4.2 Seratches, bubble or dent on Glass/ Polarizer/Reflector, Bubble between Polarizer & Reflector/Glass:				
		Size (mm)	Acceptable Qty			
			Zone			
			A	B	C	
		Φ ≦0.20	Acceptable		Accep-table	
		0.20<Φ ≦0.50	3			
		0.50<Φ ≦1.00	2			
		Φ>1.00	0			

19. Character Generator ROM Map

	Low 4-bit															
High 4-bit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			☻	♥	♦	♣	♠	•	◘	○	◙	♂	♀	♪	♫	☼
1	►	◄	↕	‼	¶	§	▬	↨	↑	↓	→	←	∟	↔	▲	▼
2		!	"	#	$	%	&	'	(	)	*	+	,	−	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	△

字型碼，前 127 碼為標準 ASCII 碼，在中文為半形，中文碼由 A140 開始，共 8192 字，編碼方式為 BIG-5 碼.