Forum: 32-bit PIC
Topic: PIC32 初始化DDR不成
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作者: 廖文皓
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我使用PIC32MZ2025DAG176, 想要使用內部的SDRAM, 在初始化時脈時, 程式會卡在檢查DDR時脈是否穩定, 這類問題我該如何解決?

```
void SYS_CLK_Initialize( const SYS_CLK_INIT const * clkInit )
{
    SYS_DEVCON_SystemUnlock ( );

    PLIB_OSC_FRCDivisorSelect( OSC_ID_0, OSC_FRC_DIV_1);

    /* Memory PLL */
  PLIB_DEVCON_MPLLVregEnable( DEVCON_ID_0 );
  while (!PLIB_DEVCON_MPLLVregIsReady(DEVCON_ID_0));

  PLIB_DEVCON_MPLLVrefSet(DEVCON_ID_0, DEVCON_MPLL_VREF_EXT);
    PLIB_DEVCON_MPLLInputDivSet( DEVCON_ID_0, 1 );
    PLIB_DEVCON_MPLLMultiplierSet ( DEVCON_ID_0, 50 );
    PLIB_DEVCON_MPLLODiv1Set( DEVCON_ID_0, DEVCON_MPLL_ODIV_3 );
    PLIB_DEVCON_MPLLODiv2Set( DEVCON_ID_0, DEVCON_MPLL_ODIV_1 );
    PLIB_DEVCON_MPLLEnable( DEVCON_ID_0 );

while(!PLIB_DEVCON_MPLLIsReady( DEVCON_ID_0 ))
    {
        PLIB_DEVCON_SystemUnlock(DEVCON_ID_0);
        PLIB_DEVCON_SystemLock(DEVCON_ID_0);
    }
    /* Enable Peripheral Bus 1 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 0, 2 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 0 );

    /* Enable Peripheral Bus 2 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 1, 2 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 1 );
    /* Enable Peripheral Bus 3 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 2, 2 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 2 );
    /* Enable Peripheral Bus 4 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 3, 2 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 3 );
    /* Enable Peripheral Bus 5 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 4, 2 );
```

```
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 4 );
    /* Enable Peripheral Bus 6 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 5, 2 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 5 );
    /* Enable Peripheral Bus 7 */
    PLIB_OSC_PBClockDivisorSet (OSC_ID_0, 6, 1 );
    PLIB_OSC_PBOutputClockEnable (OSC_ID_0, 6 );



    /* Disable REFCLKO1*/
    PLIB_OSC_ReferenceOscDisable ( OSC_ID_0, OSC_REFERENCE_1 );
    /* Disable REFCLK1_OE*/
    PLIB_OSC_ReferenceOutputDisable ( OSC_ID_0, OSC_REFERENCE_1 );
    /* Disable REFCLKO2*/
    PLIB_OSC_ReferenceOscDisable ( OSC_ID_0, OSC_REFERENCE_2 );
    /* Disable REFCLK2_OE*/
    PLIB_OSC_ReferenceOutputDisable ( OSC_ID_0, OSC_REFERENCE_2 );
    /* Disable REFCLKO3*/
    PLIB_OSC_ReferenceOscDisable ( OSC_ID_0, OSC_REFERENCE_3 );
    /* Disable REFCLK3_OE*/
    PLIB_OSC_ReferenceOutputDisable ( OSC_ID_0, OSC_REFERENCE_3 );
    /* Disable REFCLKO4*/
    PLIB_OSC_ReferenceOscDisable ( OSC_ID_0, OSC_REFERENCE_4 );
    /* Disable REFCLK4_OE*/
    PLIB_OSC_ReferenceOutputDisable ( OSC_ID_0, OSC_REFERENCE_4 );
    /* Disable REFCLKO5*/
    PLIB_OSC_ReferenceOscDisable ( OSC_ID_0, OSC_REFERENCE_5 );
    /* Disable REFCLK5_OE*/
    PLIB_OSC_ReferenceOutputDisable ( OSC_ID_0, OSC_REFERENCE_5 );

    SYS_DEVCON_SystemLock ( );
}
```