MICROCHIP

POW002

Advanced 8-Bit PIC Power & Power Supply Examples

Denny Chen

Class Objectives

When you walk out of this class you will…

- **know the available peripherals on 8 bit MCUs for SMPS applications**
- **be able to implement a variety of SMPS topologies using Core Independent Peripherals.**
- **be able to protect you power using Core Independent Peripherals.**

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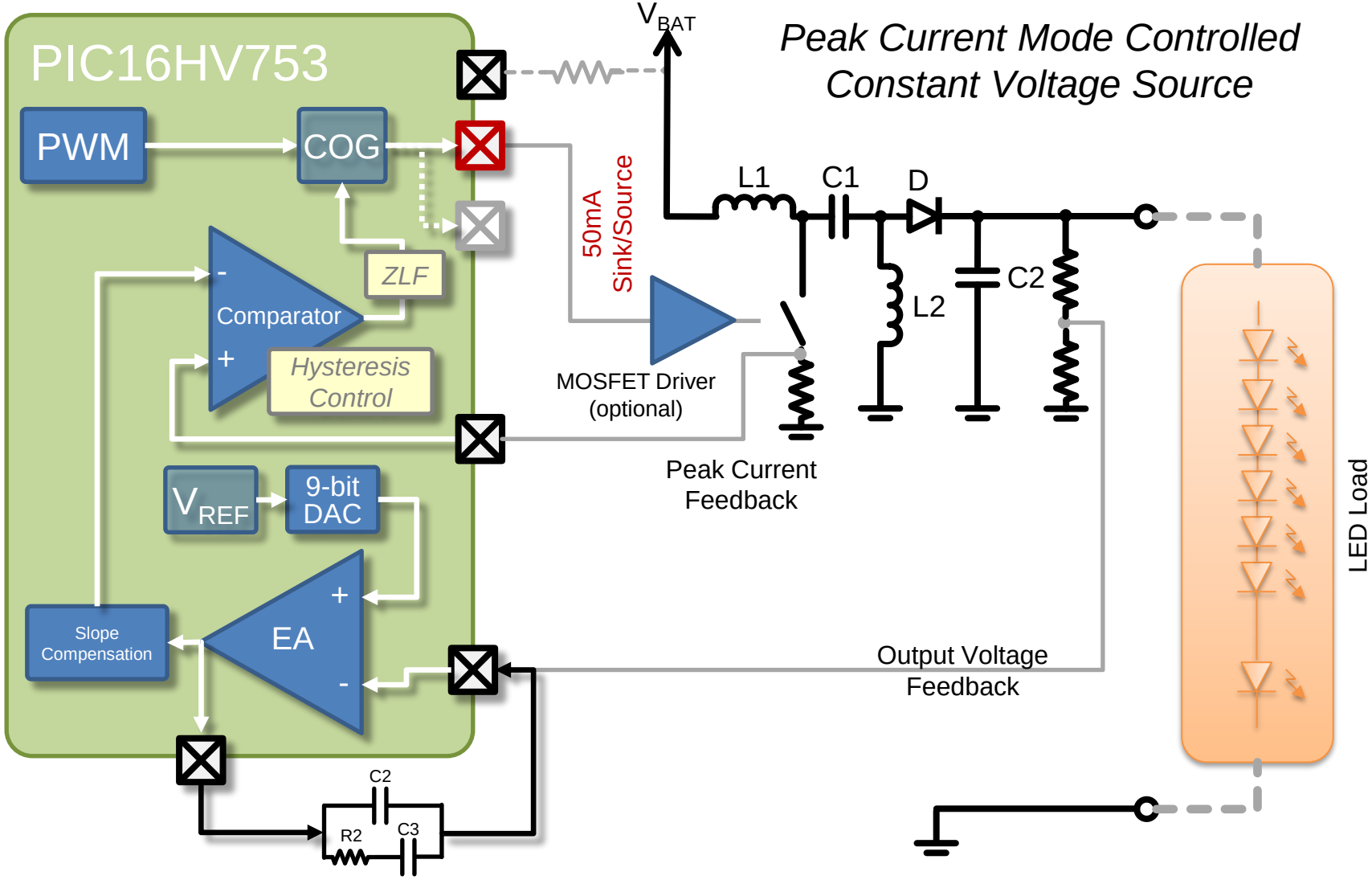
Class Objectives (Design Example)



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Agenda

- Analog Design Review
  - Plant Transfer Function
  - Analyze stability & Design Compensator
- Analog control vs. full digital control
- Different topologies and control strategies using the core independent peripherals
- Protection functions examples
- Summary

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Agenda

- **Analog Design Review**
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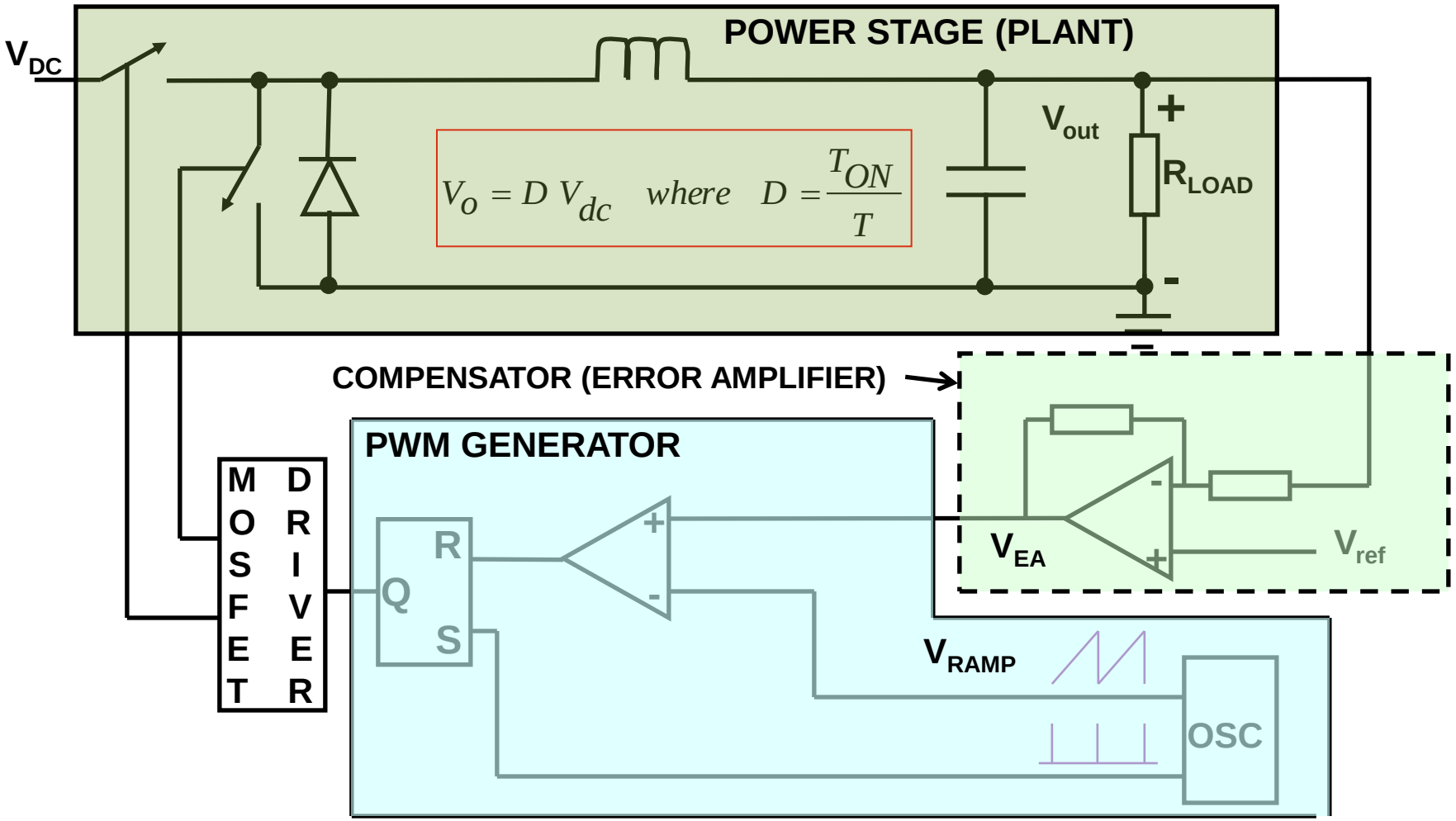
Analog Design Review

Analog World: Buck Converter - Voltage Mode



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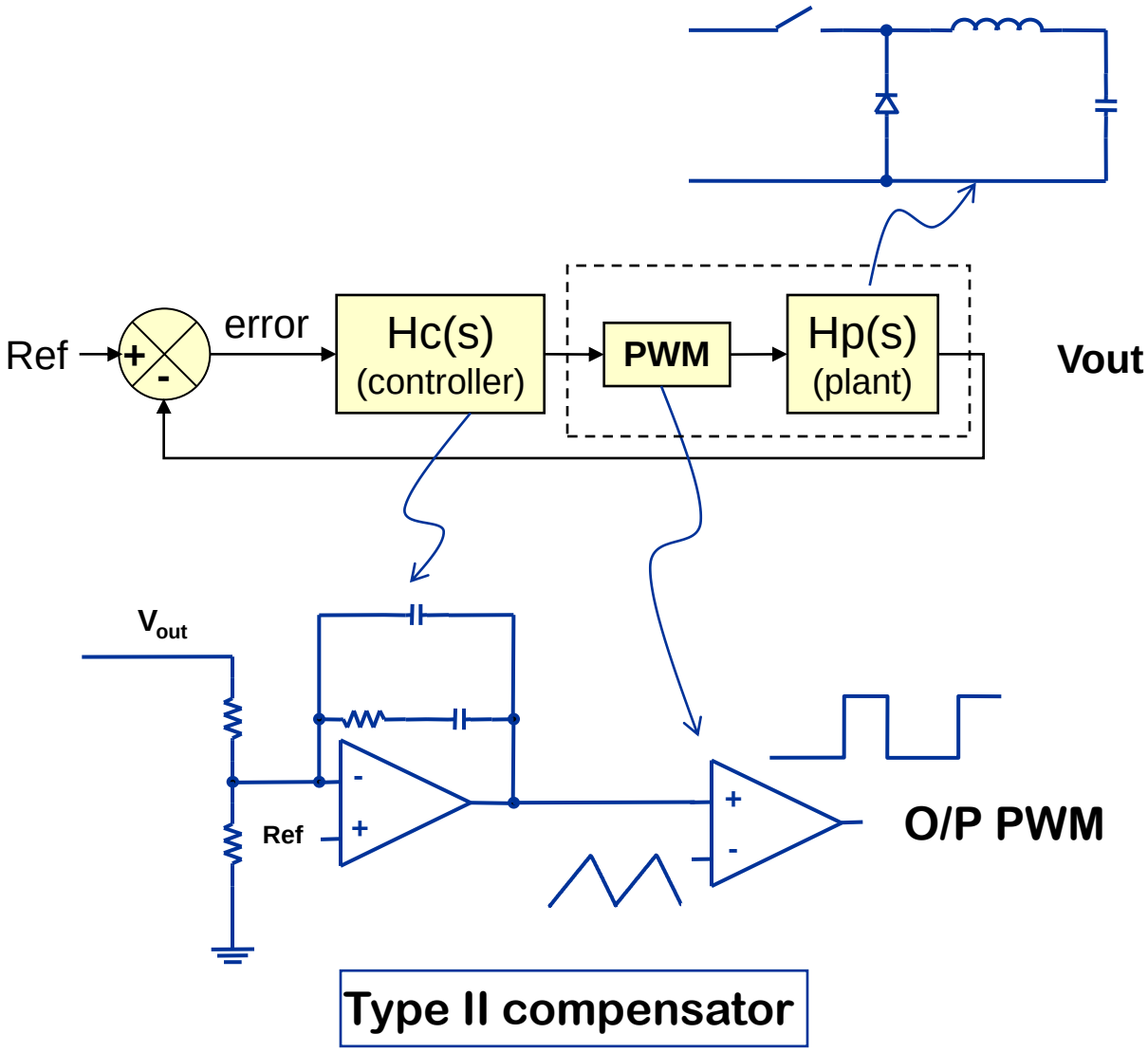
Typical Voltage Mode Analog PSU

- **Typically we tune the compensator by selecting the position of poles and zeros so as to achieve the desirable gain and phase margins**
- **To do this we need the Transfer Functions Hc(s) & Hp(s)**
- **Plant in fact includes PWM but for simplicity we have separated them**



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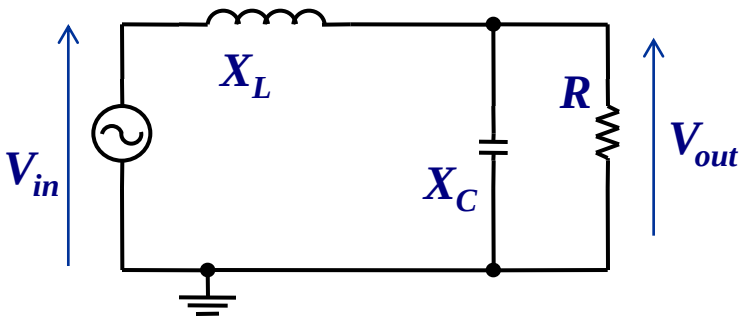
H(s) of a 2nd Order System

- **Our generic Buck converter @ full load:**
  - **L = 22μH C = 440μF & R = 1.8Ω**
  - **ESR is assumed to be 0 for now!**
    - **Cap's equivalent Series Resistance**
  - **Transfer Function Hp(s):**



$$H_p(s) = \frac{1}{\left(s^2LC + s\left(\frac{L}{R}\right) + 1\right)}$$

  - **The denominator of Hp(s) is a 2nd order polynomial**
    - **It has 2 poles* @****

$$\frac{1}{2\pi\sqrt{LC}}$$

    - **This is the resonance frequency F_r of our system**
    - **At resonance we "may" see a bump on our gain plot. The size of the bump is dependent on the load resistor (as well as other things)**
    - **We have two poles so we call this a 2nd order system**

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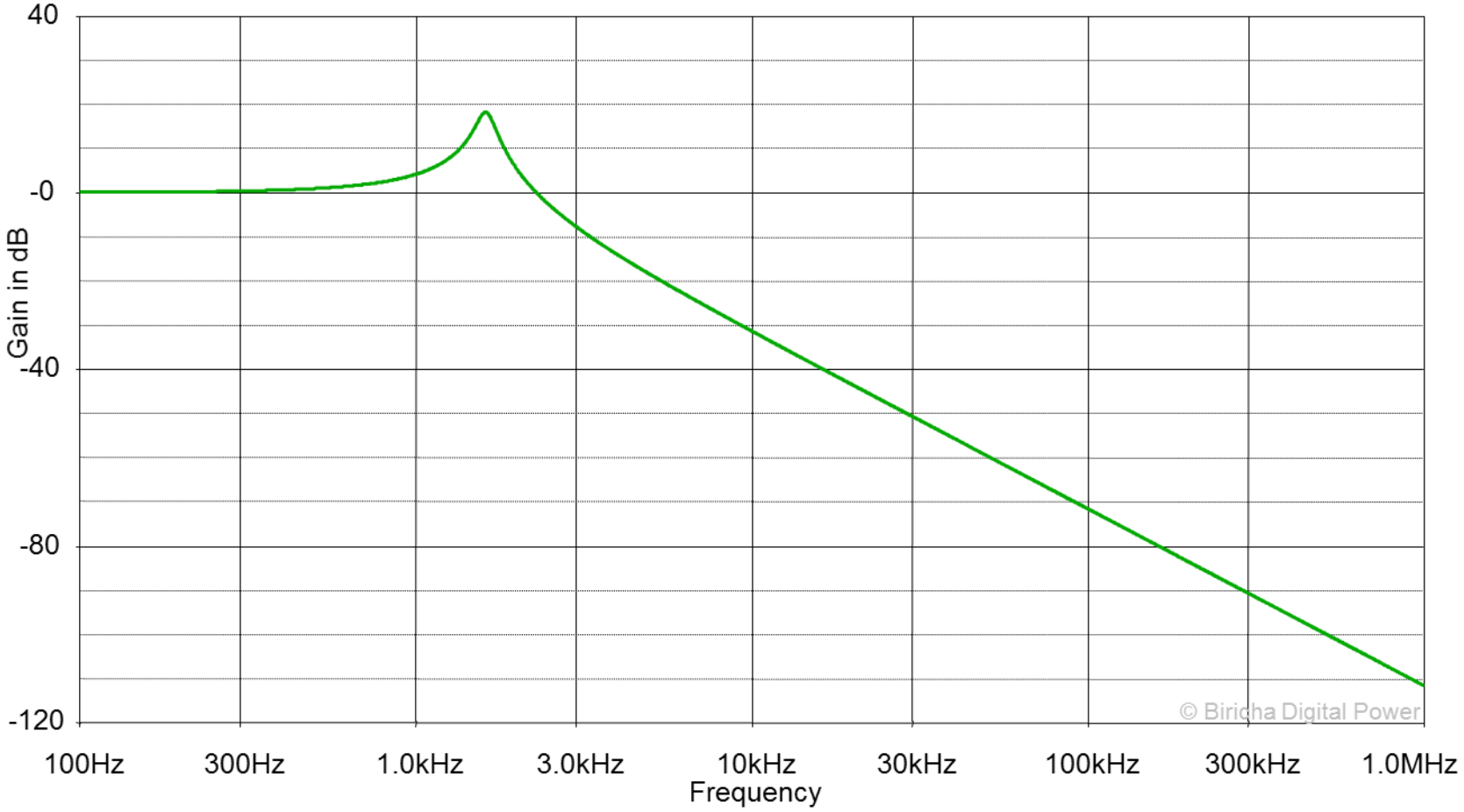
Gain Plot of the 2nd Order LC Circuit

- **Exercise:** Calculate F_r + estimate "roll-off" in dB/decade after F_r
- What is the maximum phase? Is it leading or lagging?



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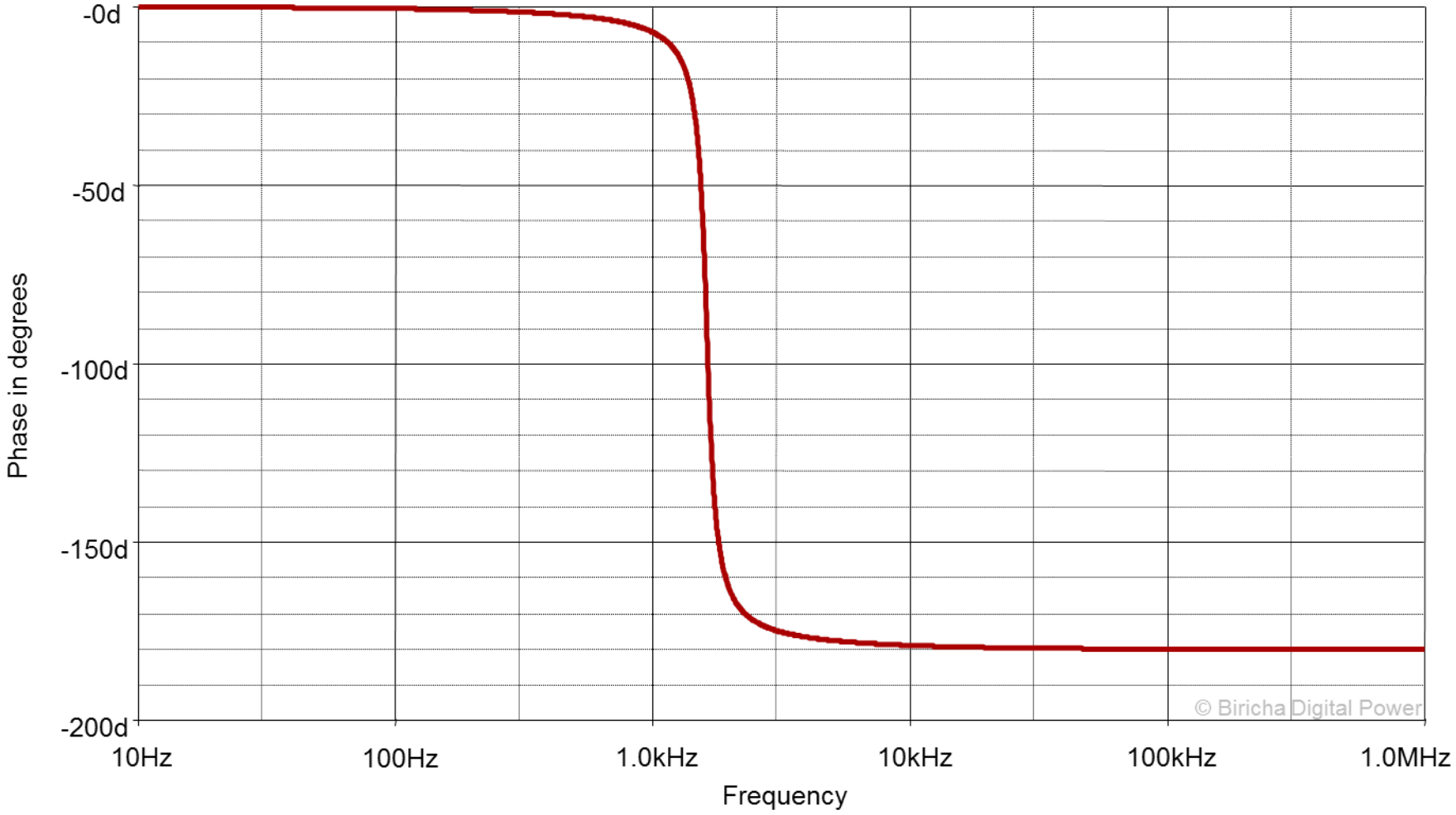
Phase Plot of the 2nd Order LC Circuit



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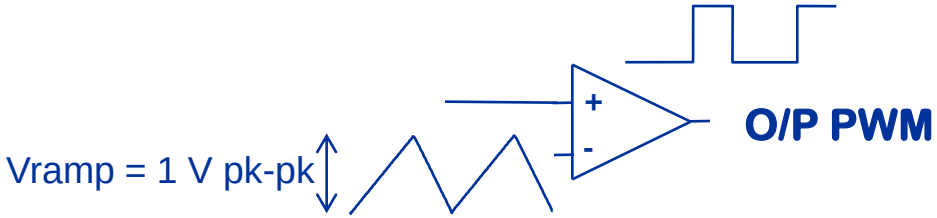
PWM Gain of Our Analog PSU

- **Consider our generic Buck converter with Vin = 12V**
  - **In analog PWM, we typically compare our reference with a ramp; for simplicity let's assume that the height of this ramp is 1V**



    - **When input to the PWM (i.e. our reference) = 0, then PWM duty = 0% & Vout = 0V**
    - **When input to the PWM = 1V, PWM duty = 100% & Vout = 12V which is = it's maximum value i.e. = Vin**
  - **Gain = Output/Input, so in our case**

$$Gain_{PWM} = \frac{V_{out(\max)}}{V_{RAMP}} = \frac{V_{in}}{V_{RAMP}} \Rightarrow \frac{12}{1}$$

  - **IMPORTANT: In decibels a gain of 12 equates to 21.58dB; this means that our bode plot is shifted up from 0dB to 21.58dB → We have now accounted for the effects of our PWM**

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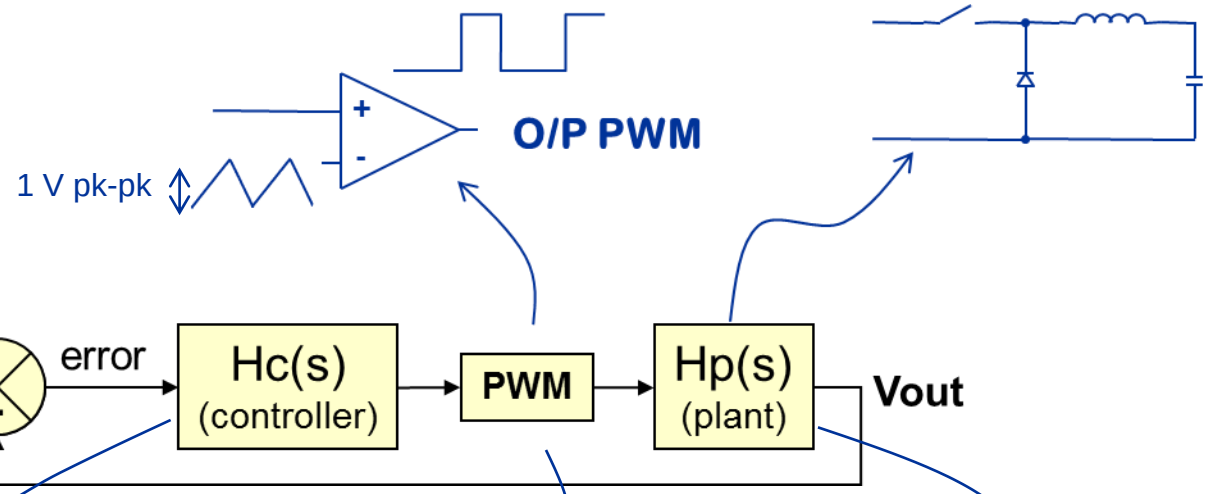
PWM Gain of Our Analog PSU

- **Consider a generic Buck converter → Vin = 12V**



Inverting Op-Amp
H(s)→ -Z2/Z1
For now let's assume that our controller's gain is 1 (0 dB); i.e. there is no compensator

When duty = 0 → Vout = 0V
When duty = 1 → Vout = Vin = 12V
$Gain_{PWM}$ = (Vin / Vramp)

∴ $Gain_{PWM}$ = (12/1) = 20 log(12) = 21.58 dB

Standard LC filter as per previous slides ∴ $Gain_{LC}$ @ low frequencies = 0dB

Total dc Gain = |H(s)| = 0 dB + 21.58 dB + 0 dB = 21.58 dB

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Putting It All into Practice

- The previous equations are from a real life power supply with the following specification:
  - L = 22μH, C = 440μF & R = 1.8Ω
  - Vin = 12V, Vout = 3.3V & Iout = 2.0A
  - For now we are ignoring the ESR (equivalent series resistance of the capacitor
- Let us consider what the Bode plot will look like for the plant of this power supply
- It will have:
  - A dc gain
  - A double pole (complex conjugate pair of poles)

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Open Loop Bode Plot of Buck without a Compensator

Vin = 12V; L = 22 µH

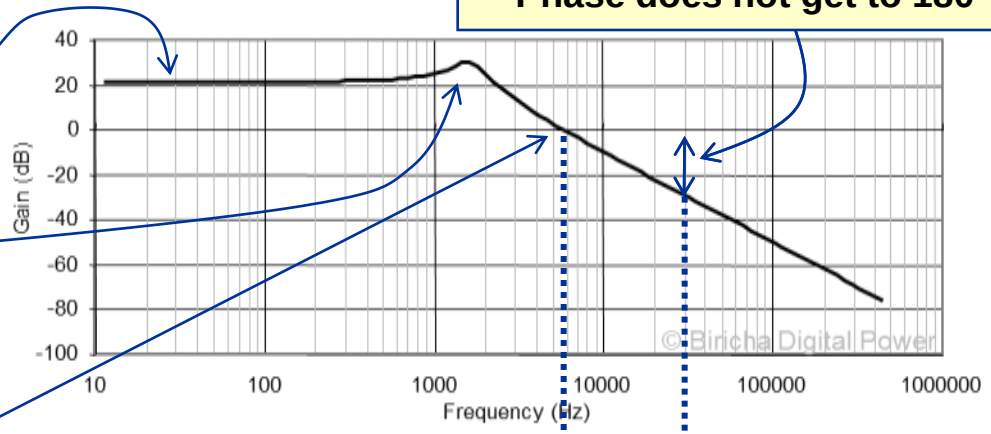
C= 440µF; Cap_{ESR} = assumed 0Ω now!

Gain Margin (G_M) = How much the gain is below 0 dB when Phase = 180º

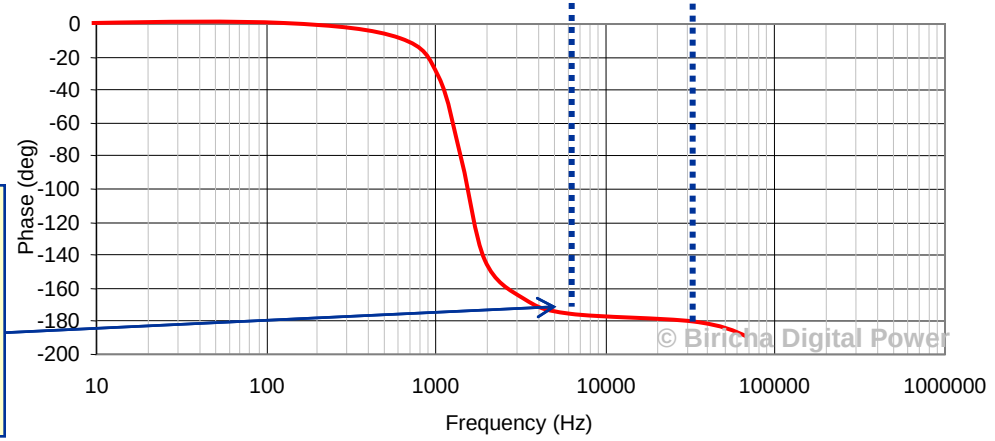
In this theoretical example Phase does not get to 180º

DC Gain = 21.58dB

$$f_r = \frac{1}{2\pi\sqrt{LC}} = 1617.64\ Hz$$



Cross over frequency Fx
i.e. frequency at which gain crosses 0 dB ≅ 6kHz
<u>Important:</u>
Slope @ Fx = -40 dB/decade



Phase Margin (ϕ_M)

i.e. Phase left before reaching -180º when the gain = 0 dB
In this case ≅ 10º

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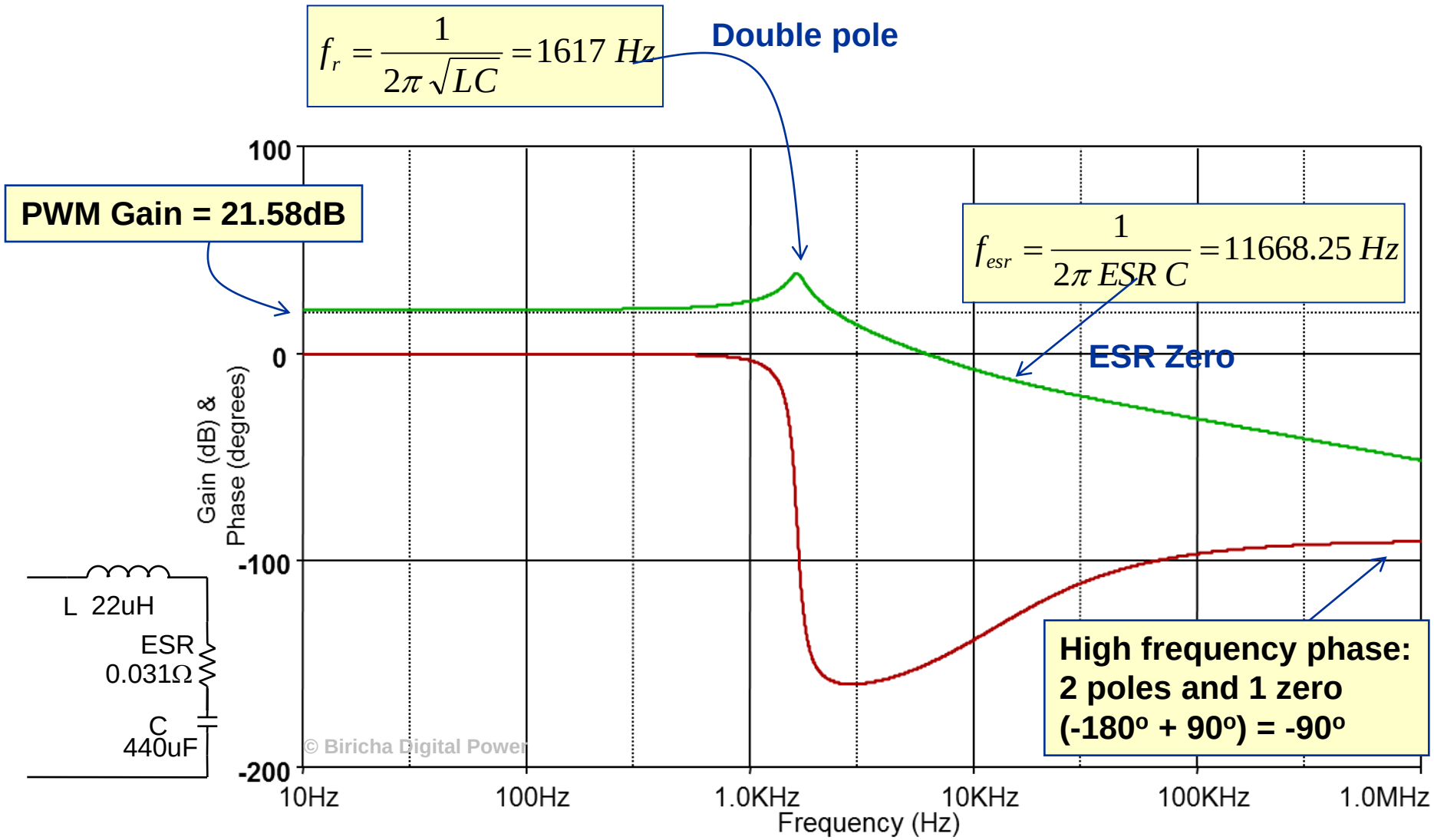
Effects of Cap ESR



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Modeling - Boost

- **Derive small signal model**
  - Calculate input to output relationship for each mode of operation
  - At equilibrium the volt-second balance for the inductor has to be equal
  - Remove DC components and 2nd order effects
  - Convert to s-domain taking Laplace transform

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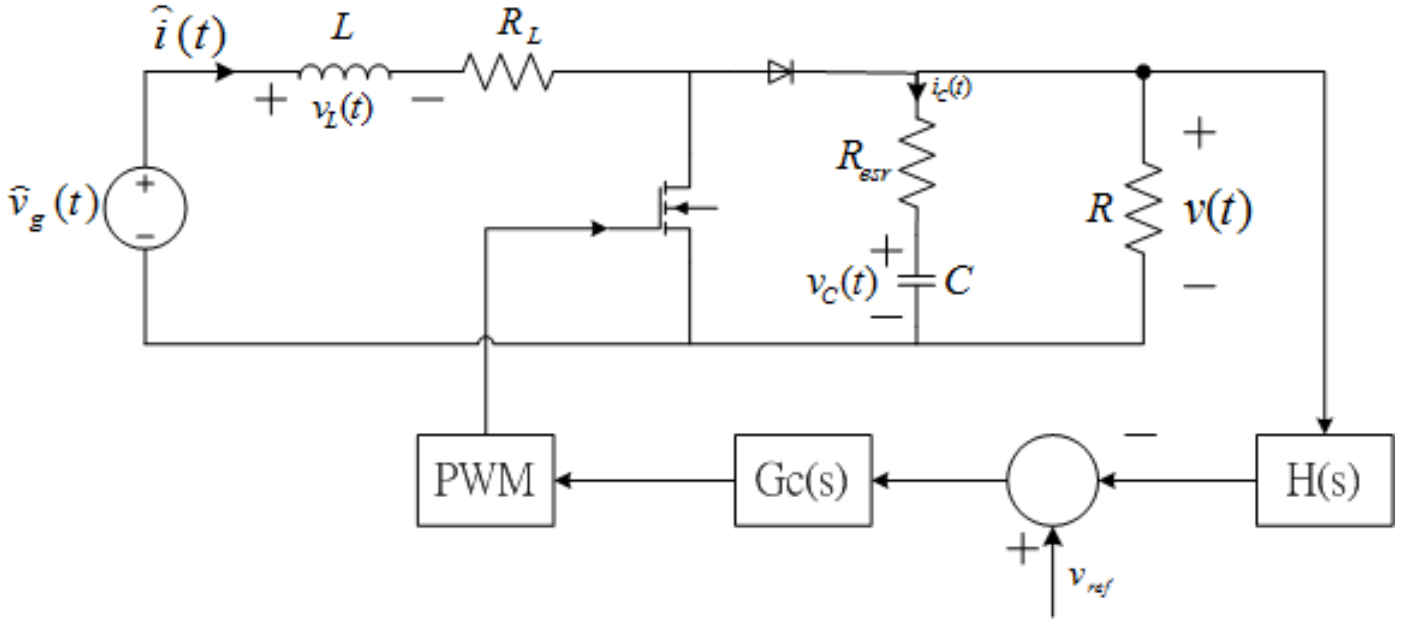
Modeling - Boost



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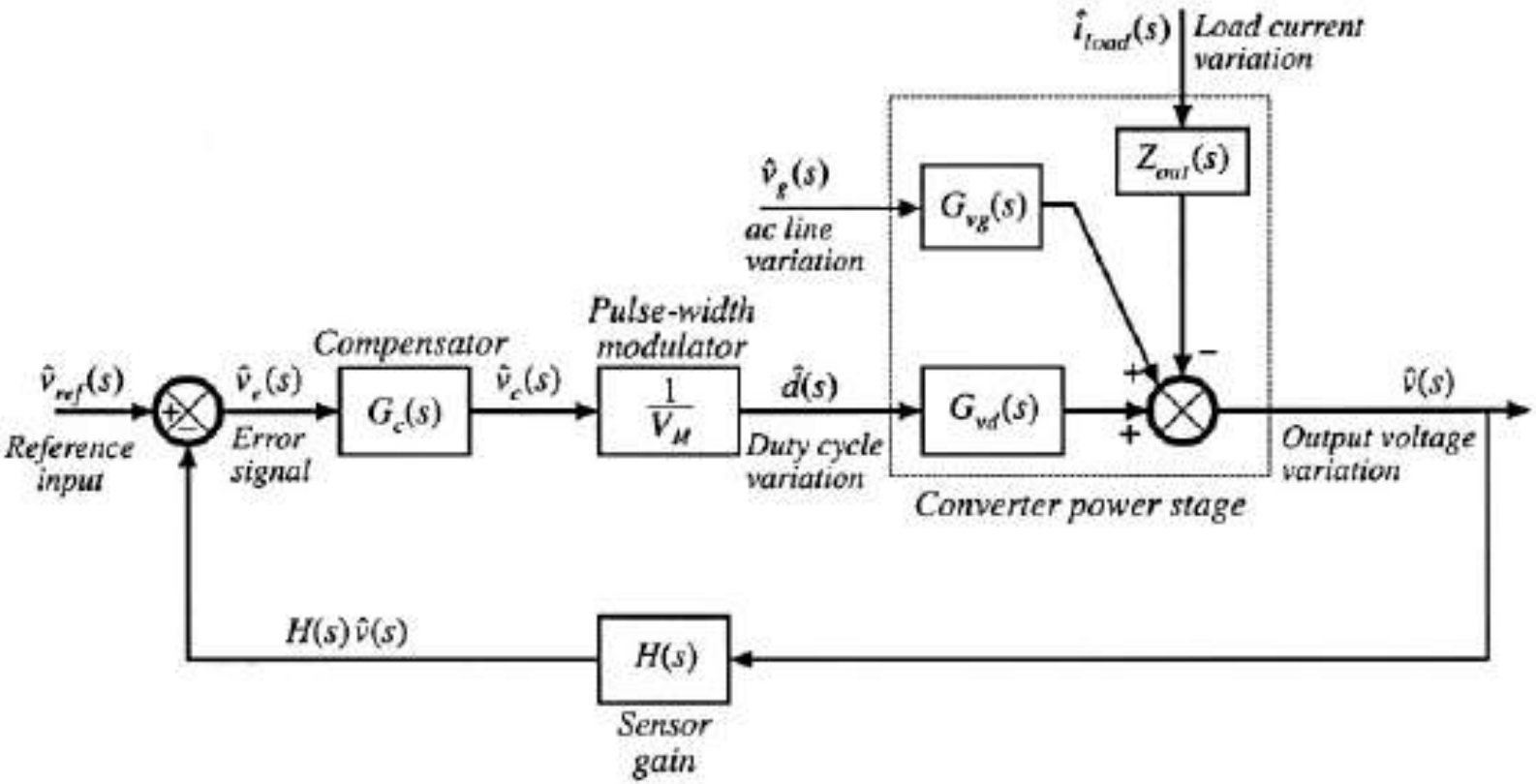
Modeling - Boost



$$\hat{v}(s) = G_{vd}(s) \times \hat{d}(s) + G_{vg}(s) \times \hat{v}_g(s) - Z_{out} \times \hat{i}_{load}(s)$$

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Modeling - Boost

Voltage of Inductor:

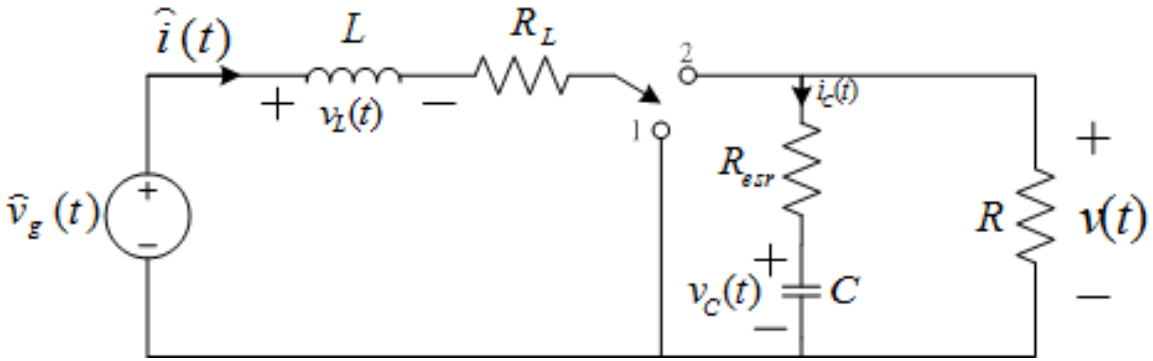
$$L\frac{d<i_L(t)>_{Ts}}{dt}=<v_L(t)>_{Ts}$$

Current of Capacitor:

$$C\frac{d<v_C(t)>_{Ts}}{dt}=<i_C(t)>_{Ts}$$

Average of x(t):

$$<X_L(t)>_{Ts}=\frac{1}{T_s}\int_t^{t+Ts}X(t)dt$$



$$v_g(t)=V_g+\hat{v}_g(t) \qquad <i(t)>_{Ts}=I+\hat{i}(t)$$

$$d(t)=D+\hat{d}(t) \qquad <v(t)>_{Ts}=V+\hat{v}(t)$$

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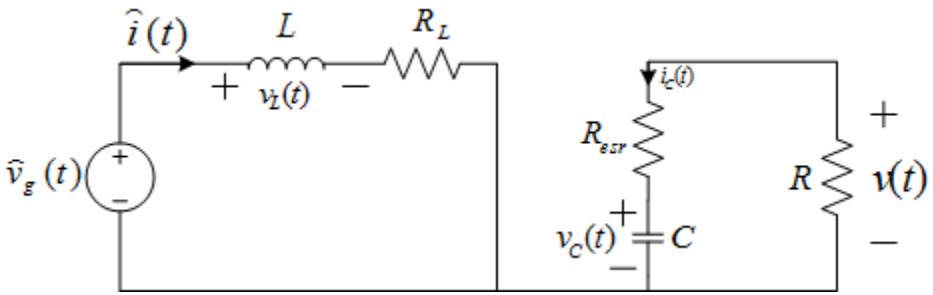
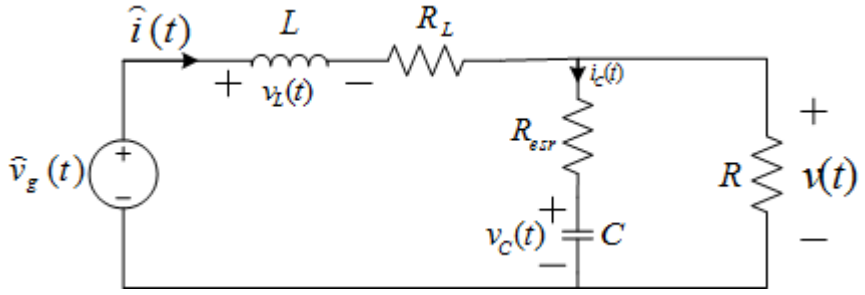
Modeling - Boost





$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) - i(t) \times R_L$$

$$i_C(t) = C\frac{dv_C(t)}{dt} = -\frac{v(t)}{R}$$

$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) - i(t) \times R_L - v(t)$$

$$i_C(t) = C\frac{dv_C(t)}{dt} = i(t) - \frac{v(t)}{R}$$

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Modeling - Boost

$$\begin{cases} L\dfrac{d<i(t)>_{Ts}}{dt} = d(t)\times[<v_g(t)>_{Ts} - <i(t)>_{Ts}\times R_L] + d'(t)\times[<v_g(t)>_{Ts} - <i(t)>_{Ts}\times R_L - <v(t)>_{Ts}] \\ C\dfrac{d<v_C(t)>_{Ts}}{dt} = d(t)\times[-\dfrac{<v(t)>_{Ts}}{R}] + d'(t)\times[<i(t)>_{Ts} - \dfrac{<v(t)>_{Ts}}{R}] \end{cases}$$

$$\Rightarrow \begin{cases} L\dfrac{d<i(t)>_{Ts}}{dt} = <v_g(t)>_{Ts} - <i(t)>_{Ts}\times R_L - d'(t)\times <v(t)>_{Ts} \\ C\dfrac{d<v_C(t)>_{Ts}}{dt} = -\dfrac{<v(t)>_{Ts}}{R} + d'(t)\times <i(t)>_{Ts} \end{cases}$$

$$\Rightarrow \begin{cases} L\dfrac{d(I+\hat{i}(t))}{dt} = V_g + \hat{v}_g(t) - (I+\hat{i}(t))\times R_L - [(D'-\hat{d}(t))\times(V+\hat{v}(t))] \\ C\dfrac{d(V_C+\hat{v}_C(t))}{dt} = -\dfrac{V+\hat{v}(t)}{R} + [(D'-\hat{d}(t))\times(I+\hat{i}(t))] \end{cases}$$

$$\text{Note: } d'(t) = 1-d(t) = 1-(D+\hat{d}(t)) = D'-\hat{d}'(t)$$

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Modeling - Boost

Voltage of Inductor:

$$L\frac{d(I+\hat{i}(t))}{dt}=V_g+\hat{v}_g(t)-(I+\hat{i}(t))\times R_L-[(D'-\hat{d}(t))\times(V+\hat{v}(t))]$$

$$\Rightarrow L\frac{dI}{dt}+L\frac{d\hat{i}(t)}{dt}=[V_g-I\times R_L-D'V]+[\hat{v}_g(t)-\hat{i}(t)\times R_L-D'\times\hat{v}(t)+\hat{d}(t)\times V]+[\hat{d}(t)\times\hat{v}(t)]$$

Current of Capacitor:

$$C\frac{d(V_C+\hat{v}_C(t))}{dt}=-\frac{V+\hat{v}(t)}{R}+[(D'-\hat{d}(t))\times(I+\hat{i}(t))]$$

$$\Rightarrow C\frac{dV_C}{dt}+C\frac{d\hat{v}_C(t)}{dt}=[-\frac{V}{R}+D'\times I]+[D'\times\hat{i}(t)-\hat{d}(t)\times I-\frac{\hat{v}(t)}{R}]-[\hat{d}(t)\times\hat{v}(t)]$$

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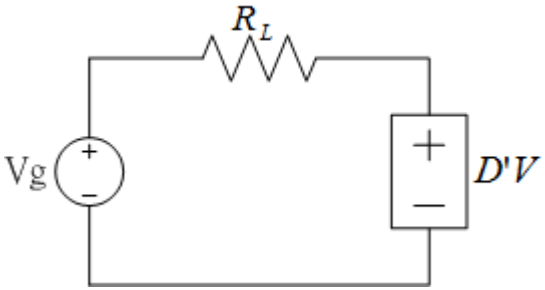
Modeling - Boost

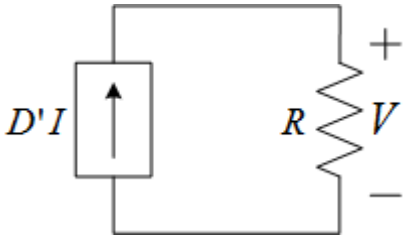
$$L\frac{dI}{dt} = V_g - I \times R_L - D'V$$

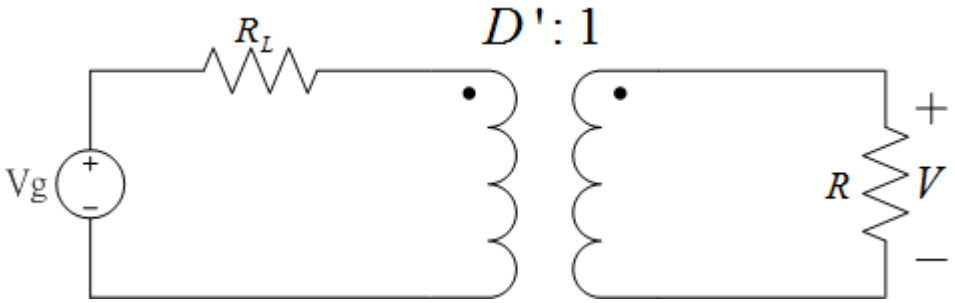
0

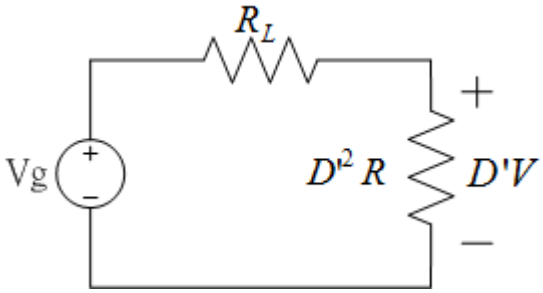


$$C\frac{dV_C}{dt} = -\frac{V}{R} + D' \times I$$

0







Transfer Function :

$$M(D) \equiv \frac{V}{V_g} = \frac{1}{1-D} \times \frac{1}{(1+\frac{R_L}{D'^2 \times R})}$$

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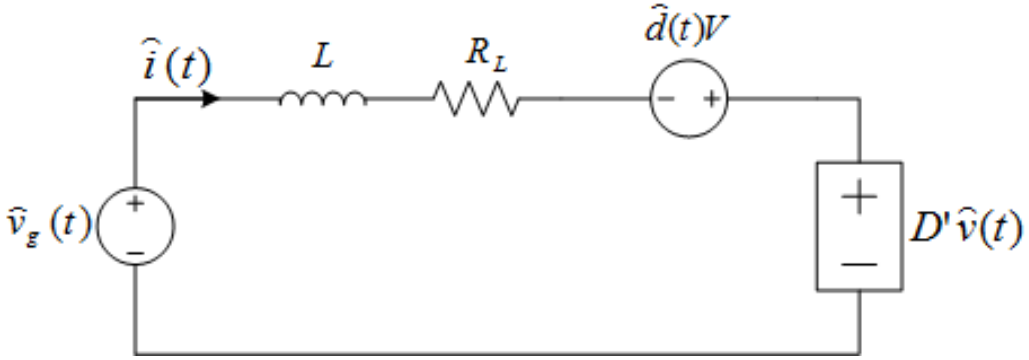
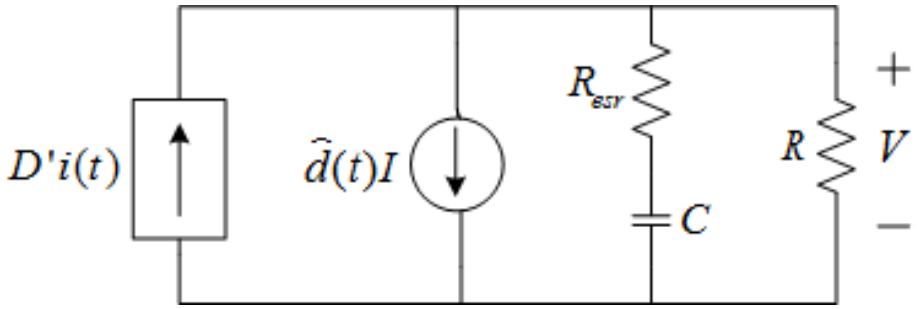
Modeling - Boost

$$L\frac{d\hat{i}(t)}{dt} = \hat{v}_g(t) - \hat{i}(t)\times R_L - D'\times\hat{v}(t) + \hat{d}(t)\times V$$



$$C\frac{d\hat{v}_C(t)}{dt} = D'\times\hat{i}(t) - \hat{d}(t)\times I - \frac{\hat{v}(t)}{R}$$



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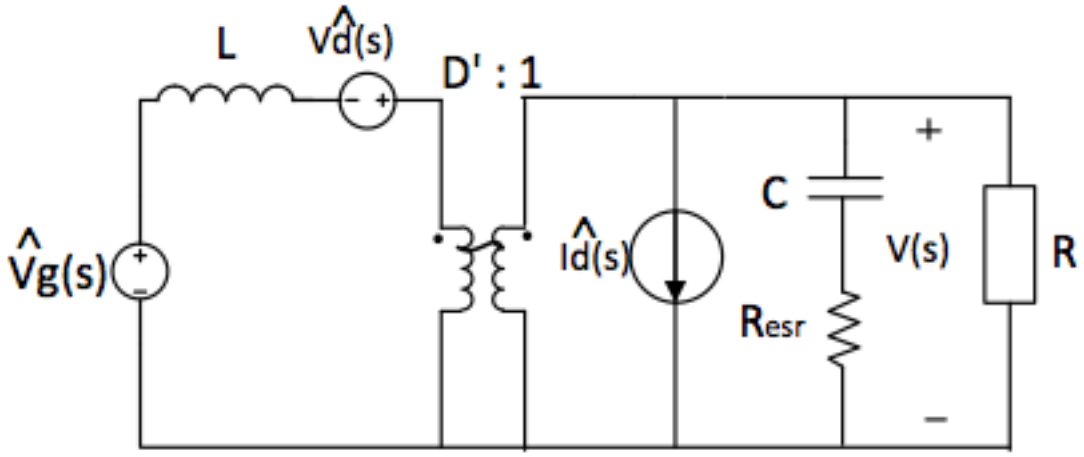
Modeling - Boost



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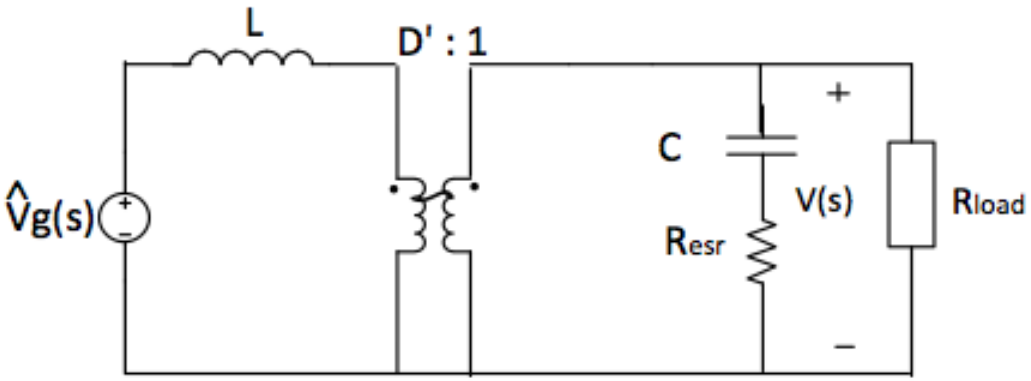
Modeling - Boost

(a)



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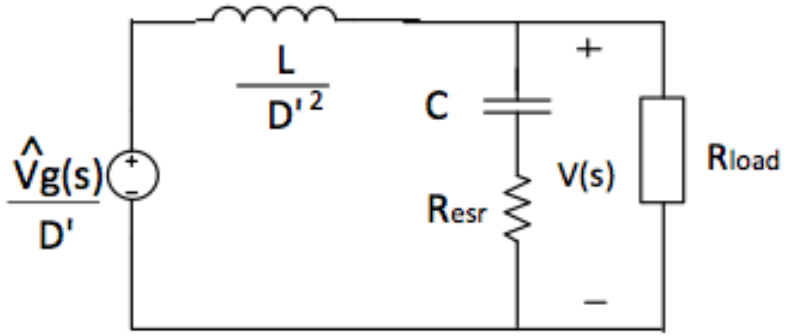

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Modeling - Boost

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = \frac{R_{load} \| (\frac{1}{sC} + R_{esr})}{D' \left[\frac{sL}{D'^2} + R_{load} \| \left(\frac{1}{sC} + R_{esr}\right)\right]}$$

$$G_{vg}(s) = \frac{\frac{R_{load}(\frac{1}{sC} + R_{esr})}{R_{load} + (\frac{1}{sC} + R_{esr})}}{D' \left[\frac{sL}{D'^2} + \frac{R_{load}(\frac{1}{sC} + R_{esr})}{R_{load} + (\frac{1}{sC} + R_{esr})}\right]}$$

$$G_{vg}(s) = \frac{(1 + sR_{esr}C)}{D' \left[1 + s(\frac{L}{D'^2 R_{load}} + R_{esr}C) + s^2 \frac{LC(R_{load} + R_{esr})}{D'^2 R_{load}}\right]}$$

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Modeling

Buck Converter Transfer Function

Control to Output	Line to Output	Output Impedance
$\frac{\hat{v}_O(s)}{\hat{d}(s)} = V_i \frac{1+r_C Cs}{\Delta s / \omega_0^2}$	$\frac{\hat{v}_O(s)}{\hat{v}_i(s)} = D \frac{1+r_C Cs}{\Delta s / \omega_0^2}$	$\frac{\hat{v}_O(s)}{\hat{i}_d(s)} = R_{eq} \frac{1+\frac{s}{\omega_1 Q_1}+\left(\frac{s}{\omega_1}\right)^2}{\Delta s / \omega_0^2}$

$$\Delta s = s^2 + \frac{\omega_0}{Q} s + \omega_0^2$$

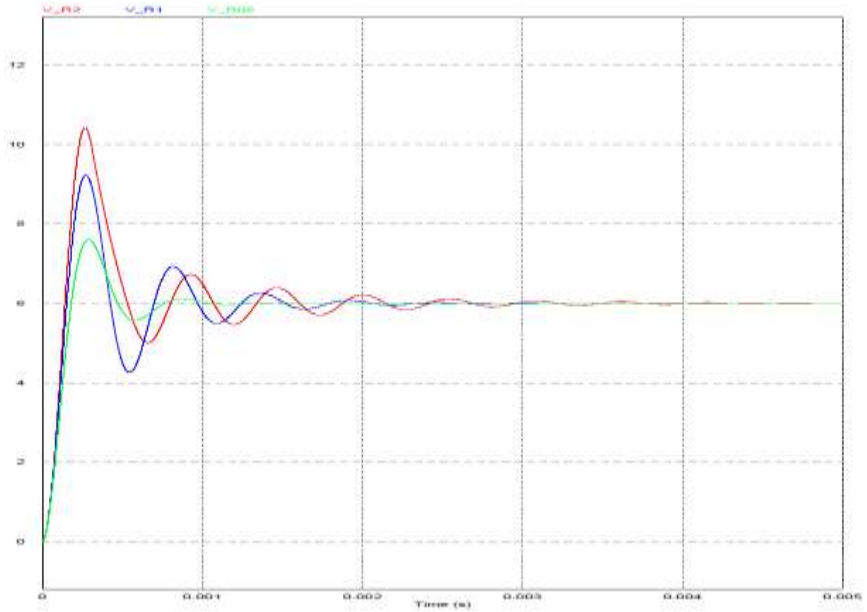
$$R_{eq} = r_L$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{1}{\omega_0} \frac{1}{\frac{L}{R} + (r_L + r_C)C}$$

$$\omega_1 = \frac{1}{\sqrt{LC}} \sqrt{\frac{r_L}{r_C}}$$

$$Q_1 = \frac{1}{\omega_1} \frac{1}{\frac{L}{r_C} + r_L C}$$



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Modeling

Boost Converter Transfer Function

Control to Output	Line to Output	Output Impedance
$\frac{\hat{v}_O(s)}{\hat{d}(s)} = \frac{V_i}{(D')^2} \frac{(1+\frac{s}{\omega_z})(1-\frac{s}{\omega_a})}{\Delta s/\omega_0^2}$	$\frac{\hat{v}_O(s)}{\hat{v}_i(s)} = \frac{V_i}{D'} \frac{1}{\Delta s/\omega_0^2}$	$\frac{\hat{v}_O(s)}{\hat{i}_d(s)} = R_{eq} \frac{1+\frac{s}{\omega_1 Q_1}+\left(\frac{s}{\omega_1}\right)^2}{\Delta s/\omega_0^2}$

$$\Delta s = s^2 + \frac{\omega_0}{Q} s + \omega_0^2$$

$$R_{eq} = \frac{r_L}{(D')^2} \frac{D}{D'} r_C$$

$$Q = \frac{D'}{\omega_0} \frac{1}{\frac{L}{D'R} + \frac{r_L C}{D'} + D' r_C C}$$

$$Q_1 = \frac{1}{\omega_1} \frac{1}{(\frac{L}{(D')^2 R_{eq}} + r_C C)}$$

$$\omega_0 = \frac{D'}{\sqrt{LC}} \qquad \omega_1 = \frac{D'}{\sqrt{LC}} \sqrt{\frac{R_{eq}}{r_C}}$$

$$\omega_z = \frac{1}{r_C C} \qquad \omega_a = \frac{(D')^2 R}{L}$$

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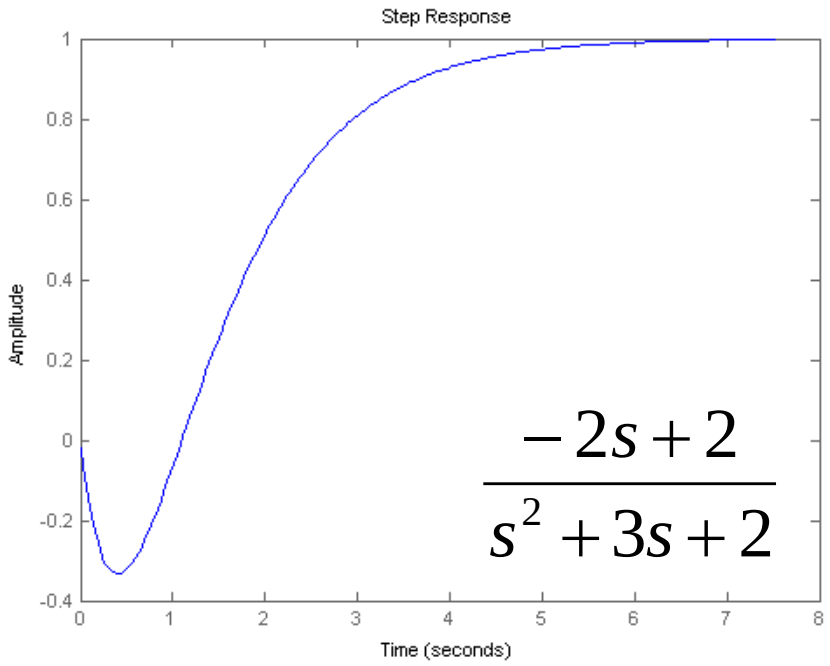
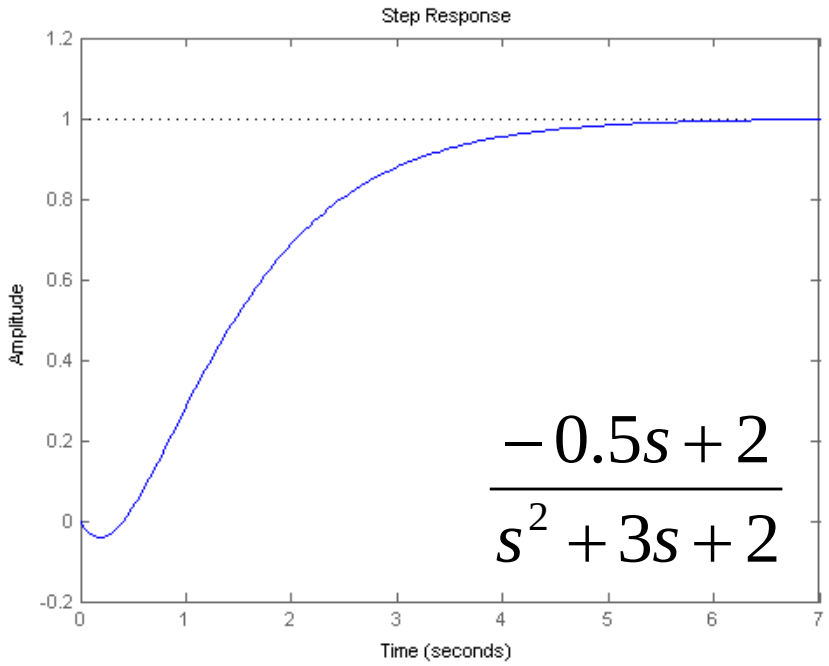
Modeling

- **Right-Half Plane Zero**
  - **Output voltage drop deeply when load increase.**
  - **Can not counteract via pole**
  - **Feedback Bandwidth will be limited**





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Agenda

- **Analog Design Review**
  - Plant Transfer Function
  - **Analyze stability & Design Compensator**
- Analog control vs. full digital control
- Different topologies and control strategies using the core independent peripherals
- Protection functions examples
- Summary

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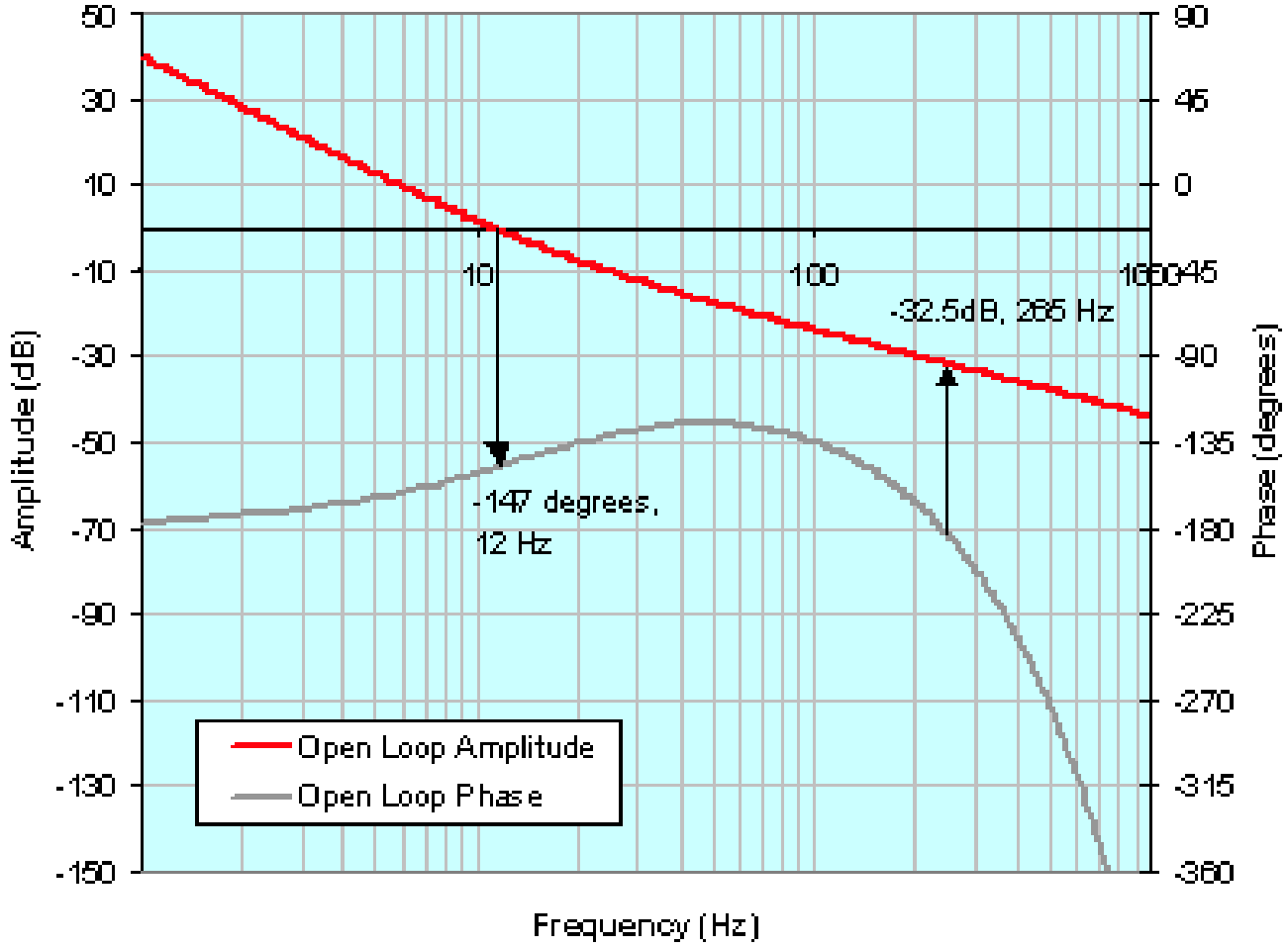
Phase and Gain margin



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Stability

- **Phase Margin**
  - **How much can the phase change before the system becomes unstable?**
  - **<45^{o} of phase margin exhibits ringing (under damped)**
- **Gain Margin**
  - **How much can the gain change before A_{FB} > 1 and the system becomes unstable.**

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Stability

- **Phase Margin**
  - **Design for at least 45º of phase margin.**
- **Gain Margin**
  - **Design for a gain margin of at least 3dB (gain of 2x)**

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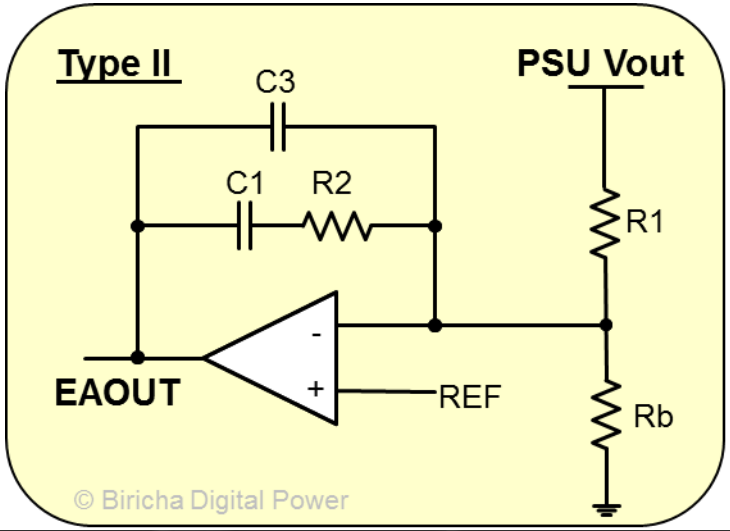
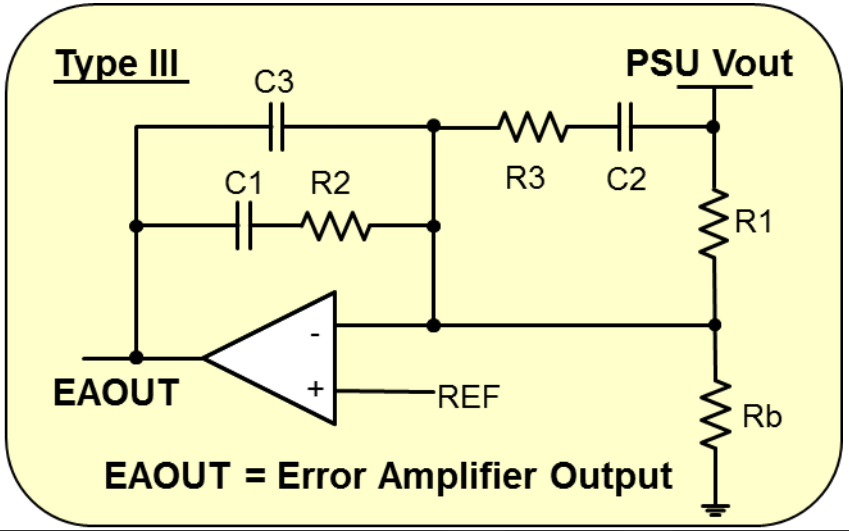
Compensators for Analog PSUs

- In order to meet the stability criteria, analog PSU designers add a controller/compensator circuit to the system
- For Analog PSUs we typically only use two different types of compensators: Type II & Type III
  - The transfer function for these is represented as Hc(s) in the block diagram of the overall system
- The component values set the poles and zeros of Hc(s)
  - Analog designers select these values such that they meet the criteria in the previous slide





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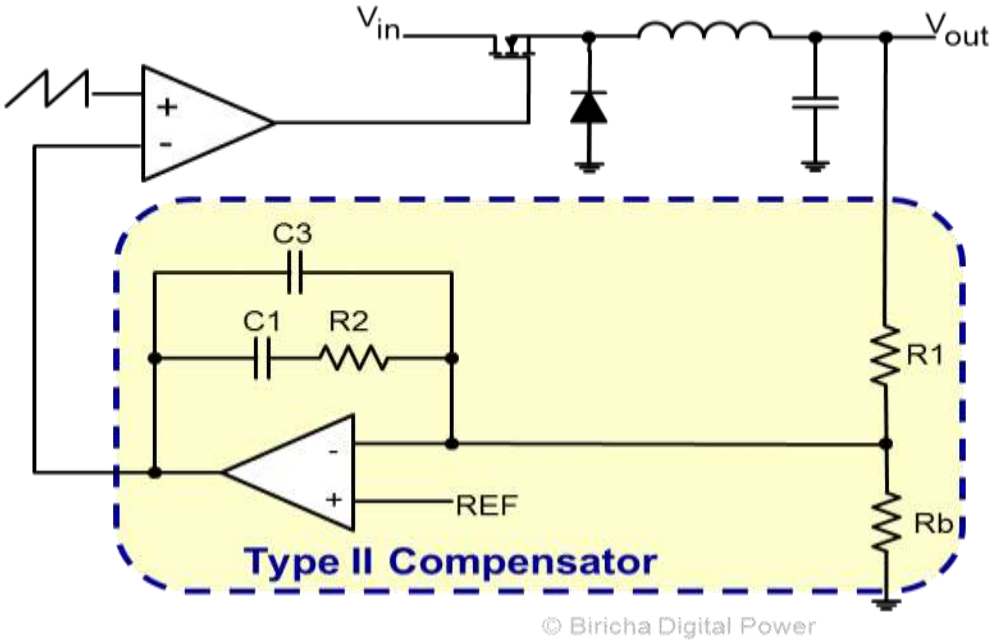
Type II Compensator

- **Type II:**
  - **2 poles & 1 zero**
  - **Most commonly used for current mode control**
  - **Not suitable for voltage mode Buck converters (need type III)**
  - **Transfer function:**



$$H_c(s) = \left(\frac{\omega_{p0}}{s}\right) \times \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right)}$$

© Biricha Digital Power

  - **Where:**

$$\omega_{z1} = \frac{1}{R_2\ C_1}\ ;\ \omega_{p0} = \frac{1}{R_1\ (C_1 + C_3)}\ ;\ \omega_{p2} = \frac{C_1 + C_3}{R_2\ C_1\ C_3}$$

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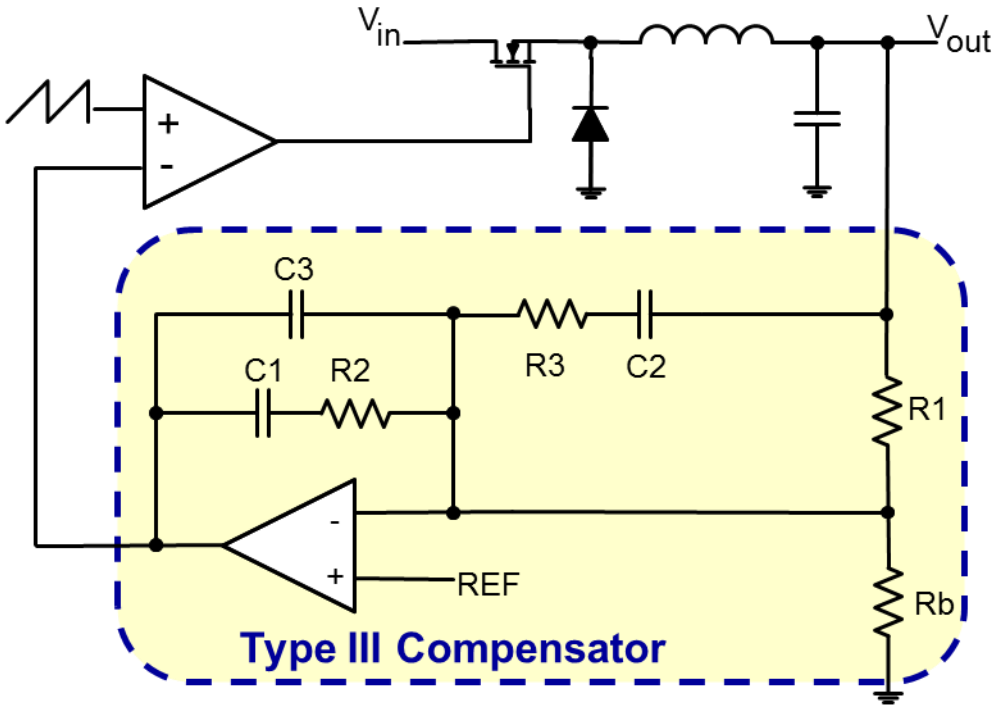
Type III Compensator

- **Type III:**
  - 3 poles & 2 zeros
  - Used for voltage mode Buck
  - Transfer function:



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$$H_c(s) = \frac{\omega_{p0}}{s} \frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{\left(\frac{s}{\omega_{p2}}+1\right)\left(\frac{s}{\omega_{p3}}+1\right)}$$

- Where:

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$$\omega_{z1} = \frac{1}{R_2 C_1};\ \omega_{z2} = \frac{1}{C_2 (R_1 + R_3)};\ \omega_{p0} = \frac{1}{R_1 (C_1 + C_3)};\ \omega_{p2} = \frac{C_1 + C_3}{R_2 C_1 C_3};\ \omega_{p3} = \frac{1}{R_3 C_2}$$

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Compensator Summary

- Analog Type II / Digital 2P2Z
  - Required Phase boost up to 90º
  - System-Plant dominant pole is of first order (Example: Rload x Cout)
  - Current-mode converters
- Analog Type III / Digital 3P3Z
  - Required Phase boost greater than 90º
  - System-Plant dominant pole is of second order (Example: Lout * Cout)
  - Voltage-mode buck or boost-derived converters
- Proportional Integral Derivative (PID)
  - Most common compensator type in industrial control applications, although not ideal for SMPS applications
  - Only uses three coefficients and is possible to boost phase > 90º

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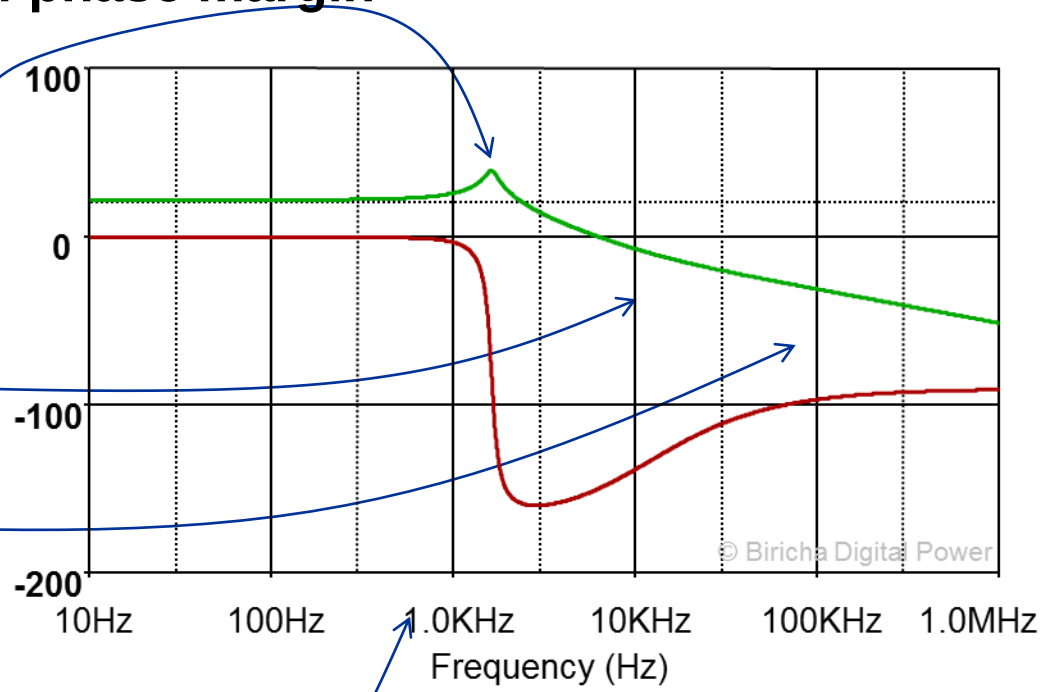
Analog Compensator Design Example

- **Type III controller: quick and simple but not exact**
  - **You typically get ~70º of phase margin**



- **Place two zeros at**
  - ***Fr i.e. @ 1617Hz***
- **Place one pole at F_{esr}**
  - ***i.e. 11668.25 Hz***
- **Place second pole at $F_s/2$**
  - ***i.e. 100 kHz***
- **Place pole at origin at:**

$$f_{p0} = \frac{V_{ramp} \times F_x}{V_{in}}$$

- **i.e. for a V_{ramp} of 1V, V_{in} = 12 and F_x of 10kHz → f_{p0} = 833Hz**

Important: If you need more phase margin, say ~75º (e.g. a digital PSU) then reduce one of the zeros and the pole@ origin by 25%; i.e. one of the zero @ 1617x0.75 = 1.2kHz, & pole @ origin = 833x0.75 = 625Hz

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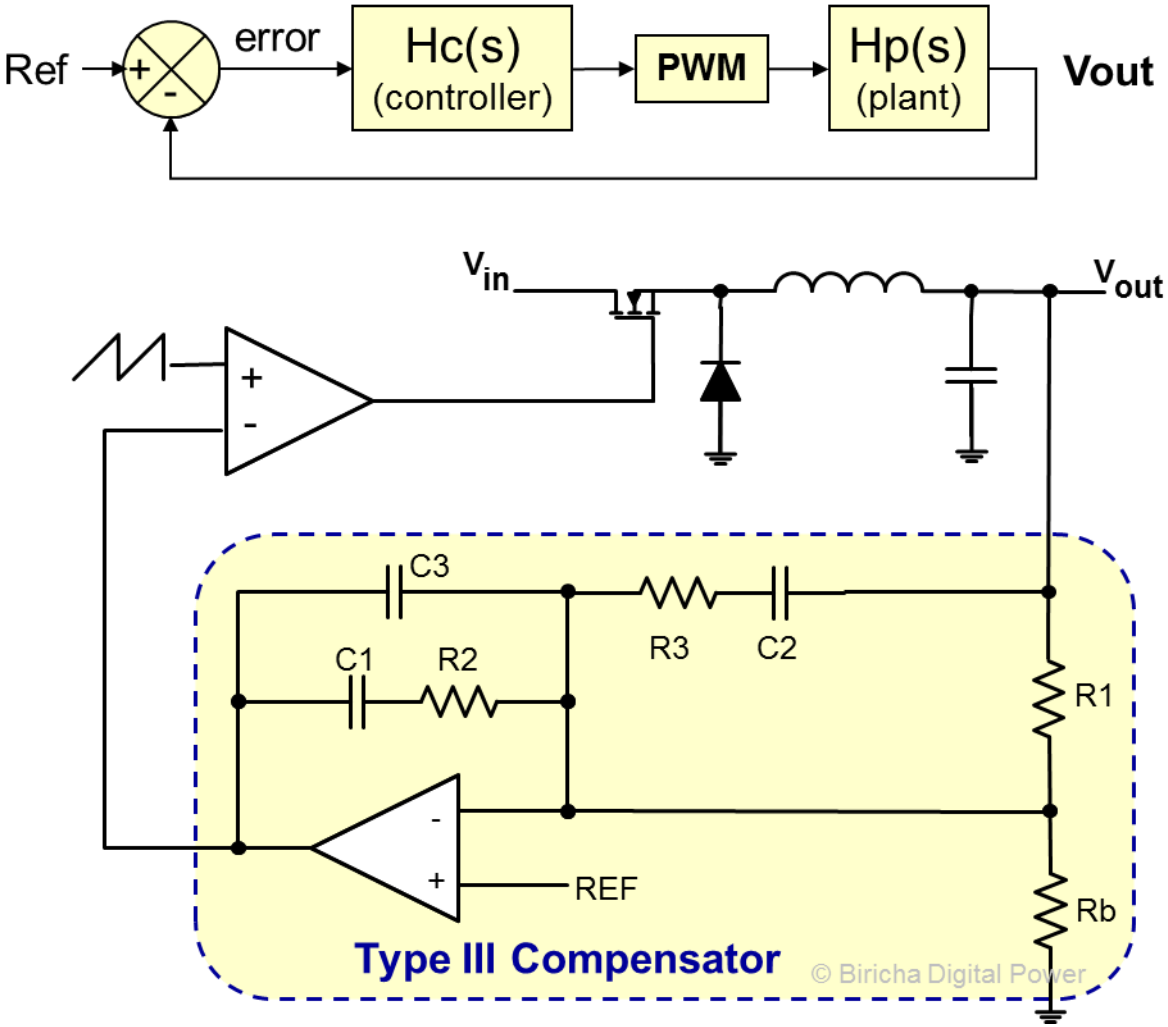
A Generic Buck Converter in Analog World



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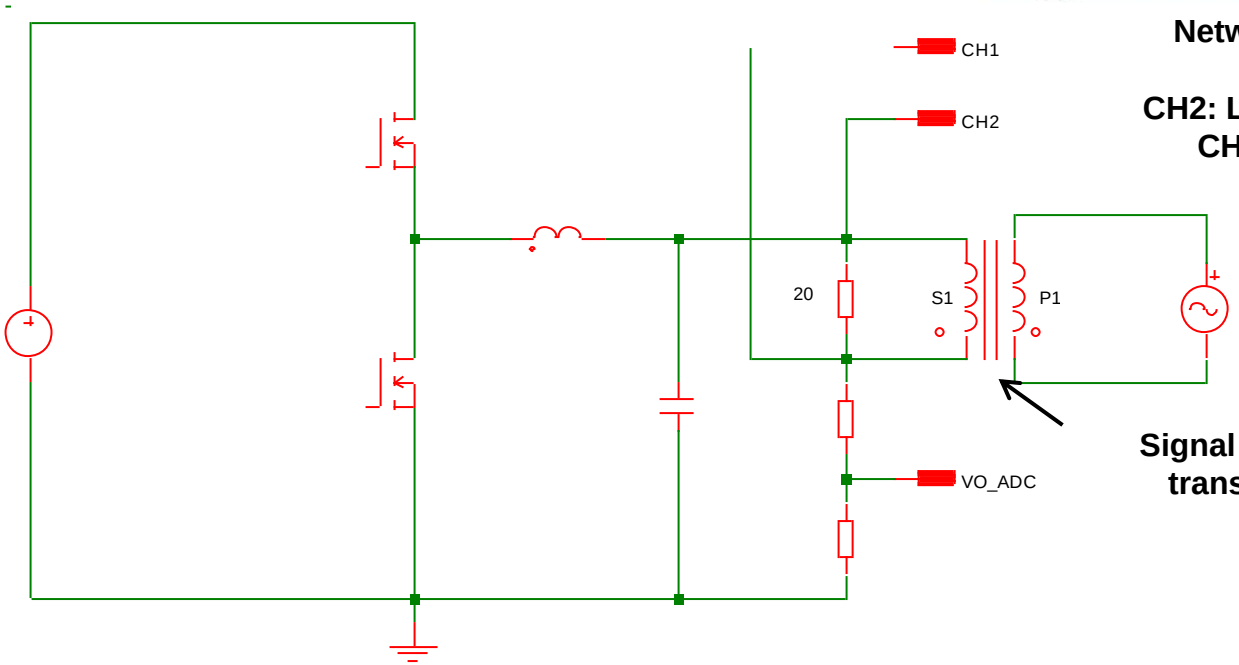
Measurement of Power Supply Stability – Network Analyzer

$$Loop\,Gain(dB) = 20\log\left(\frac{amp(CH2)}{amp(CH1)}\right)$$

$$Loop\,Phase(^\circ) = phase(CH2) - phase(CH1)$$



Network Analyzer Input Channels
CH2: Loop response signal
CH1: Injected signal

Network Analyzer Variable Frequency Source

Signal injection transformer

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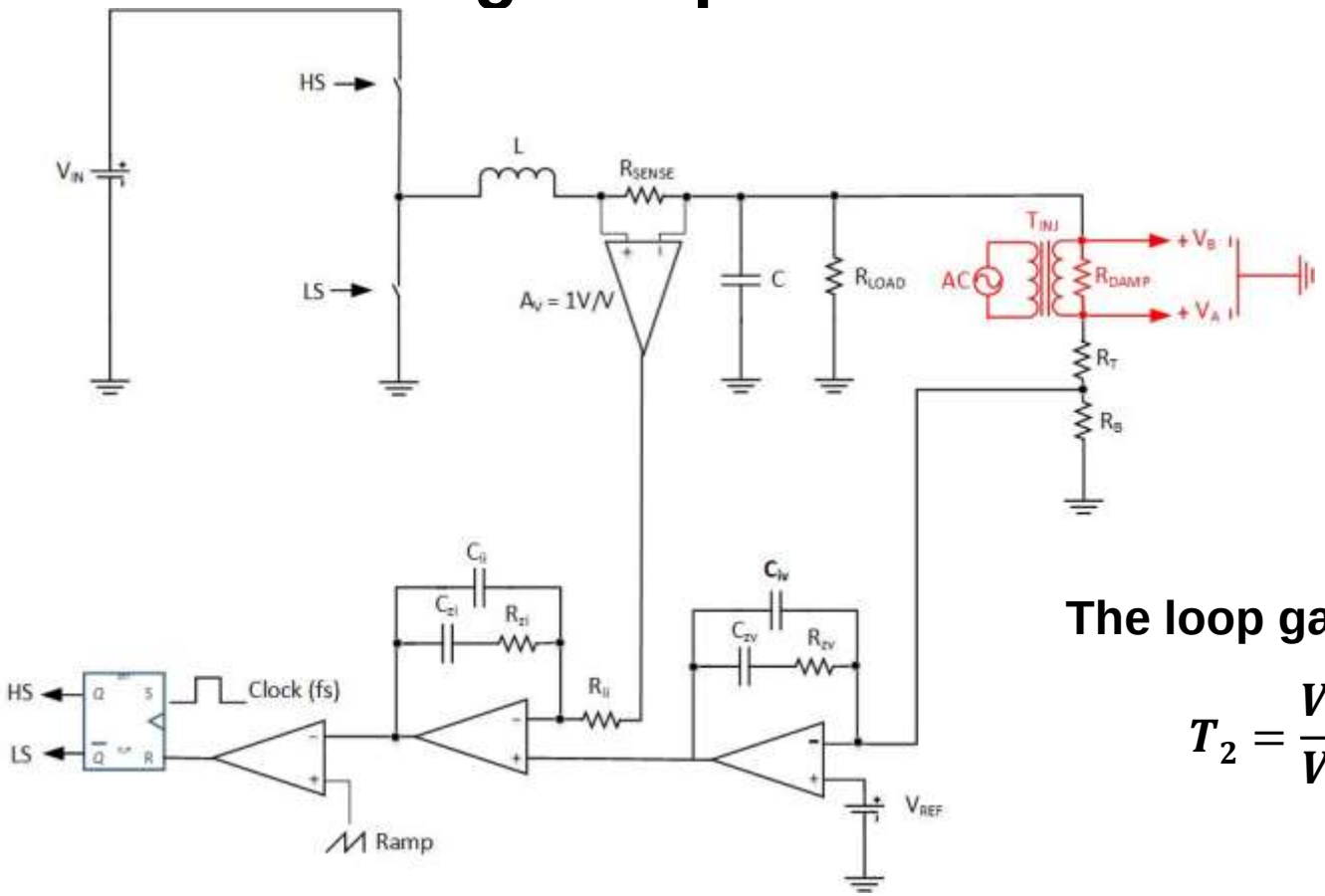
Analog Injection Example

- **Measure the voltage loop**



The loop gain T_2 is:

$$T_2 = \frac{V_B}{V_A}$$

- **Buck converter using average CMC**

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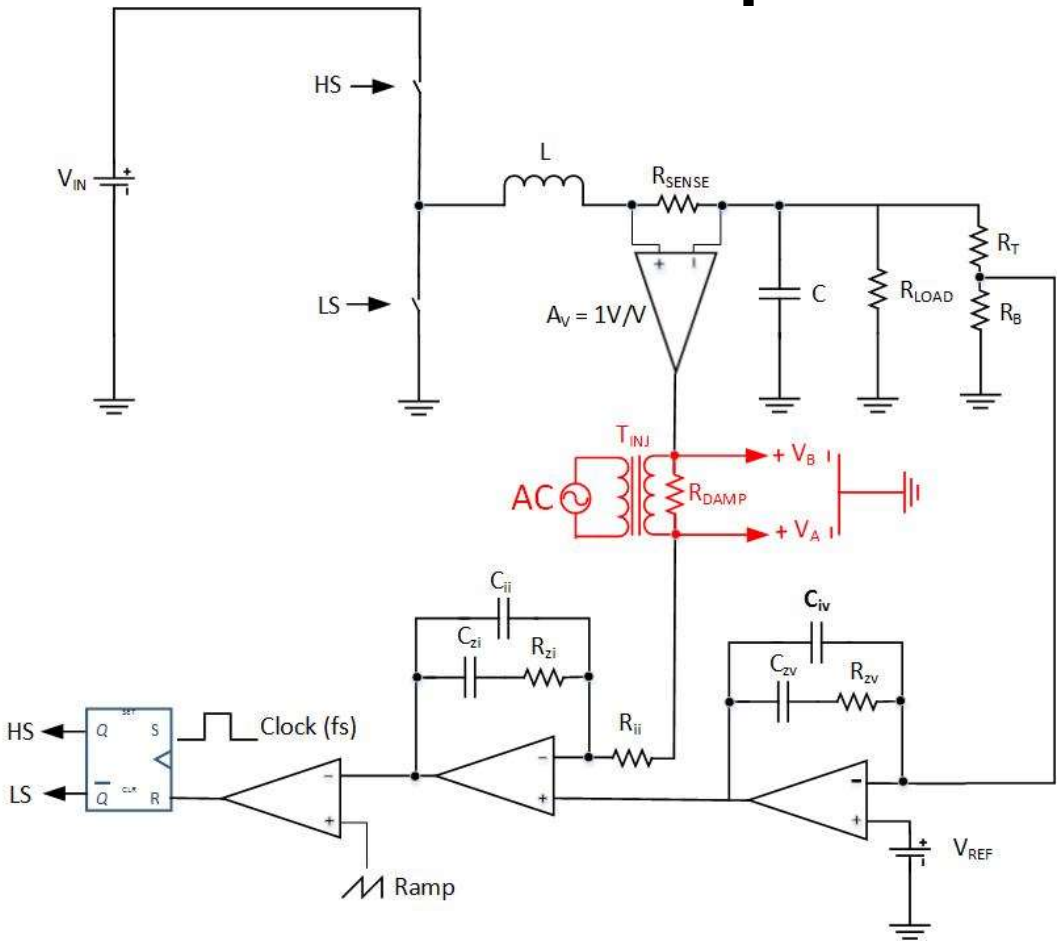
Analog Injection Example

- **Measure the current loop**



The loop gain T_3 is:

$$T_3 = \frac{V_B}{V_A}$$

- **Buck converter using average CMC**

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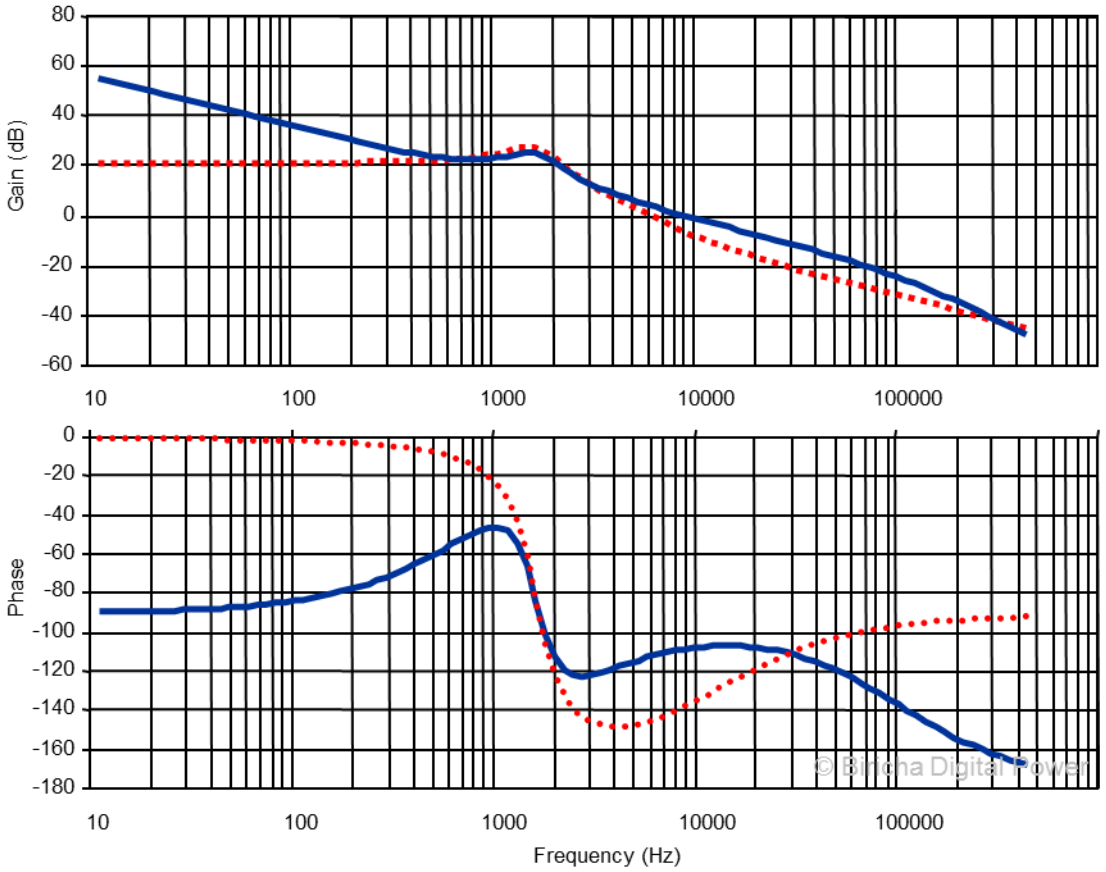
A Generic Buck Converter in Analog World

- **Red (dotted) Trace → Original power stage without compensation**
- **Blue (solid) Trace → Open loop gain after compensation**
- Using the transfer function and component values our analog type III compensator poles and zeros are selected such that:
  - Very high gain at DC, i.e. pole at origin
  - Fx = 10kHz as desired
  - $\phi M \cong 75o$
  - Slope of gain plot at Fx = 20dB/decade
  - GM better than 40dB



∴This power supply is stable → All we need to do is to convert our Hc(s) from analog (continuous time) to digital (discrete time)

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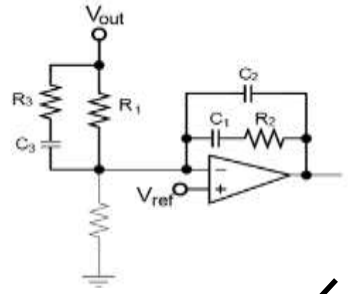
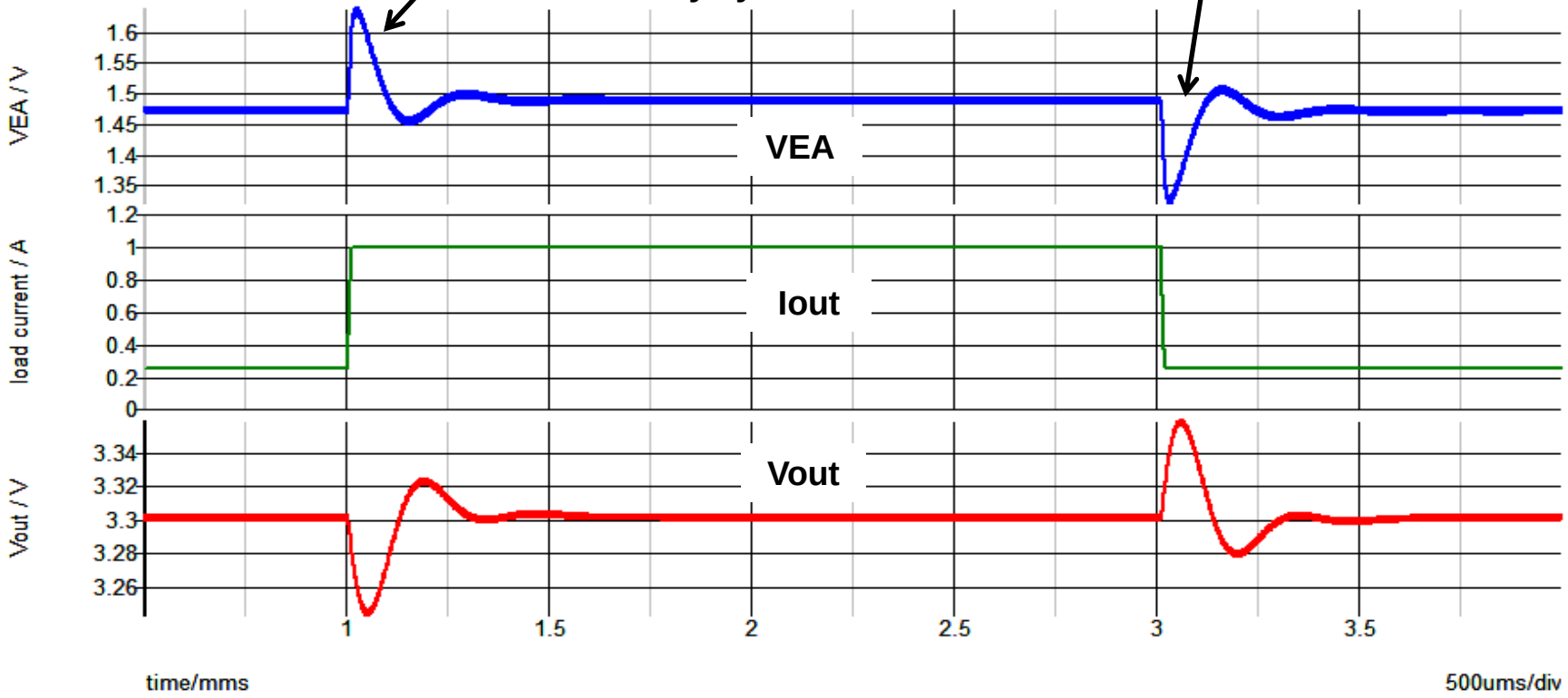
Analog Compensator Time Domain Operation



V_{EA}

VEA increases to react to load step – increasing VEA increases duty cycle

VEA decreases to react to load drop – decreasing VEA decreases duty cycle



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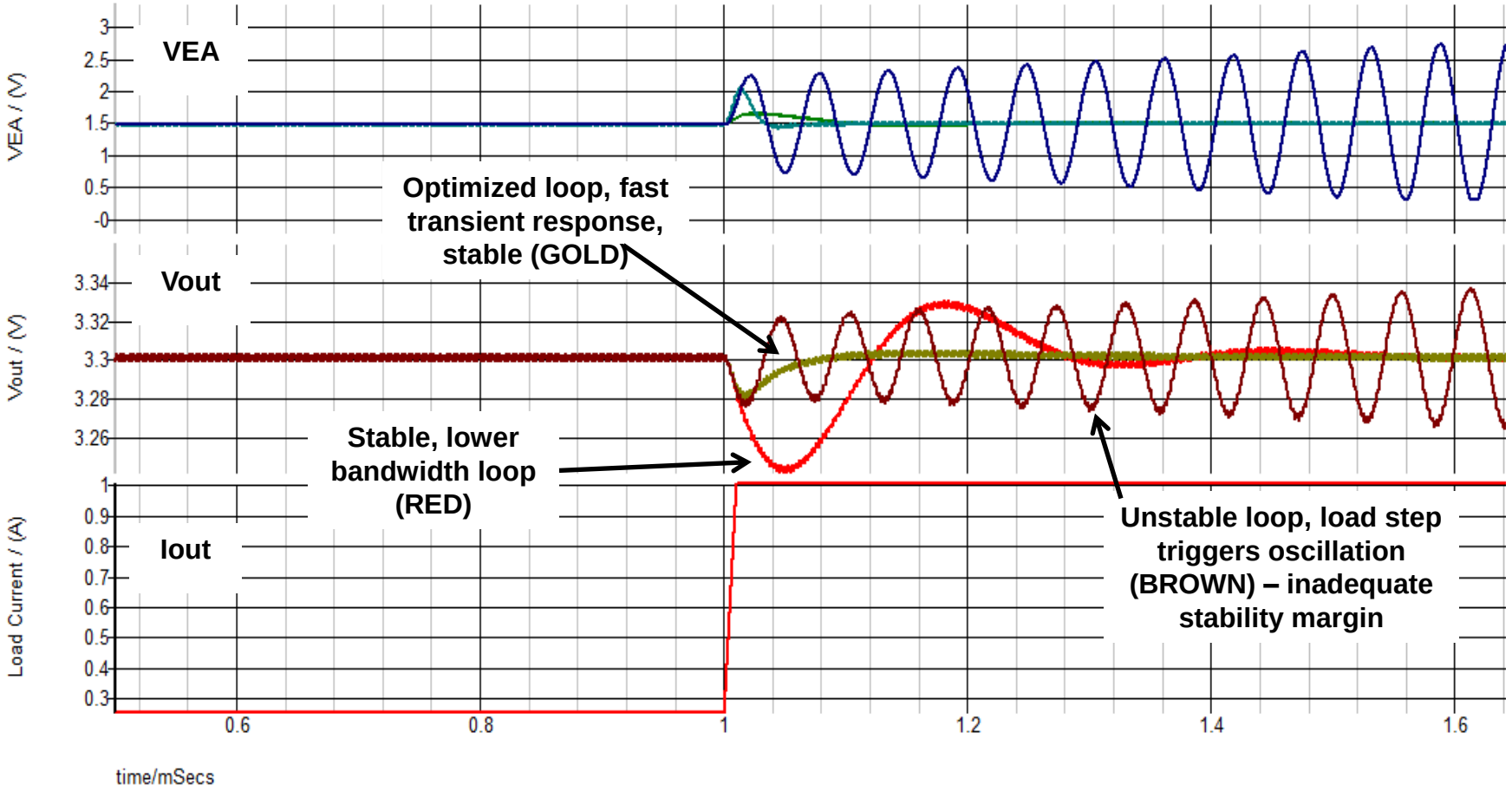
Analog Compensator Time Domain Response

RED – Lower loop BW



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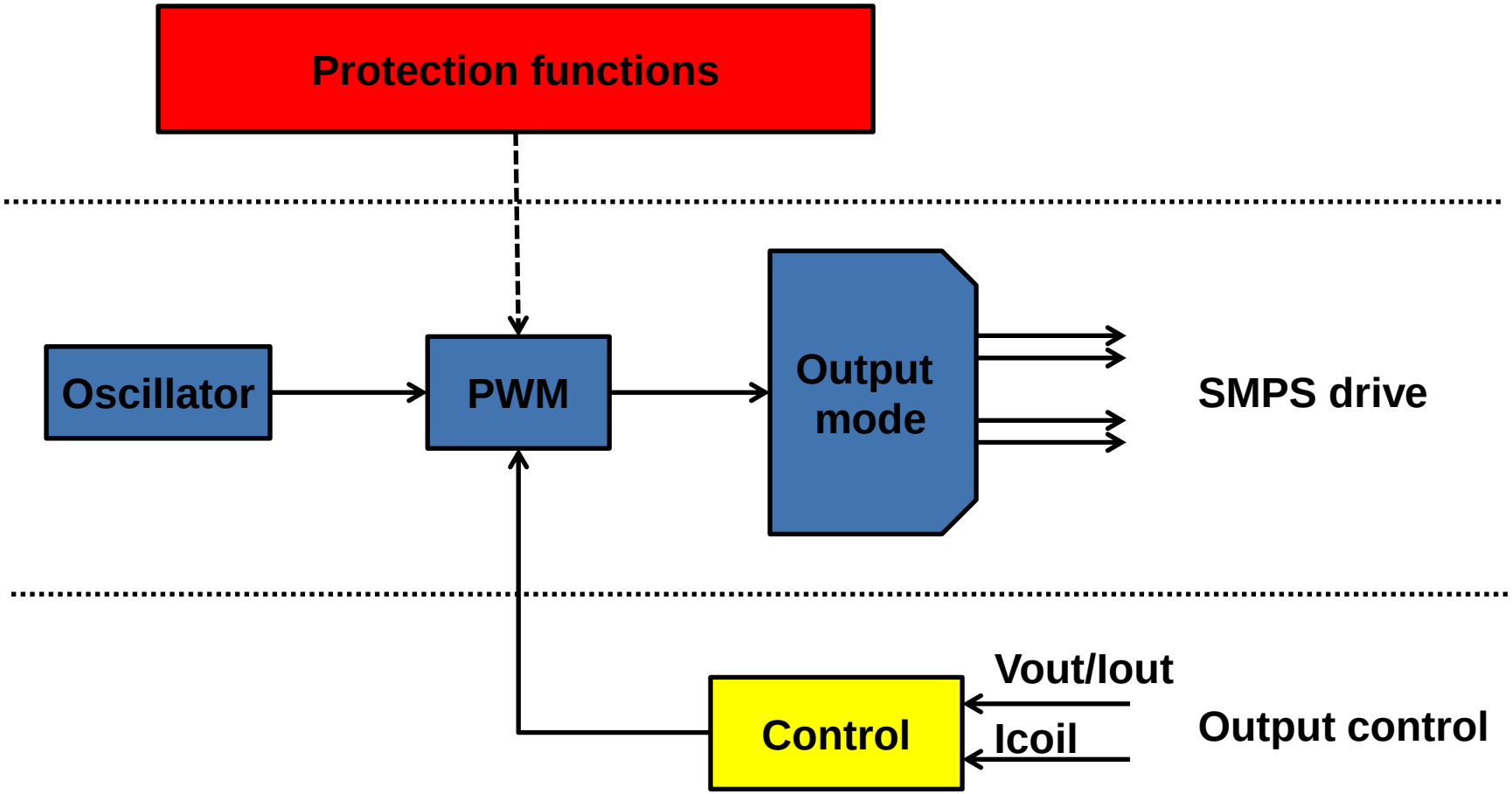
Basic SMPS Controllers



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SMPS drive

It generates one or more square waves to drive the power converter

- **One single PWM for Buck, Boost, Flyback, Sepic …**
- **Two PWMs for synchronous Buck, half bridge …**
- **Four PWMs for full bridge…**
- **Dead times/blanking**

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Control

- Measure the output
- Compare it with a reference value
- Interact with PWM in order to bring the output as close as possible to the reference

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Protection Functions

- **Over-voltage shutdown**
  - Monitors V_{in} and V_{out} & shuts down PWM if over voltage
- **Under-voltage lockout**
  - Monitors V_{in} & holds PWM off until $V_{in\text{-}min}$
- **Current Limit**
  - Limits output current/inductor current to I_{max}
- **Thermal Shutdown**
  - Monitor temperature and shutdown PWMs if over temp
- **Soft-Start**
  - At start-up it slowly bring to output to the reference value

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Additional Functions

- Slope Compensation (external transistor + RC)
- Continuous/Discontinuous switching
- Programmable output voltage/current
- Programmable current limit
- Programmable max duty cycle limit
- Over-temperature current limit/derating
- Power-up/down sequencing
- Switching Frequency dithering

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ASIC vs. MCU

- **ASIC**
  - **ASICs provide the basic functions**
  - **Most levels/timing are set with external components**
  - **Output modes were on-chip**
  - **Special functions used a mix of on chip and external**

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ASIC vs. MCU

- MCU + Core independent peripherals
  - Core Independent Peripherals (CIP) provide all control functions
  - Output modes are programmable via CIPs
  - Configuration are under real time control via software
  - Special functions use a mix of CIPs and software for complex, intelligent automated functions
- MCU only – Full digital
  - All the application is implemented in software

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Additional functions with a Microcontroller

- Monitoring/Protections
- Measurement of current, voltage, efficiency measurement & user interface
- Communications
- Talking to a controlling host

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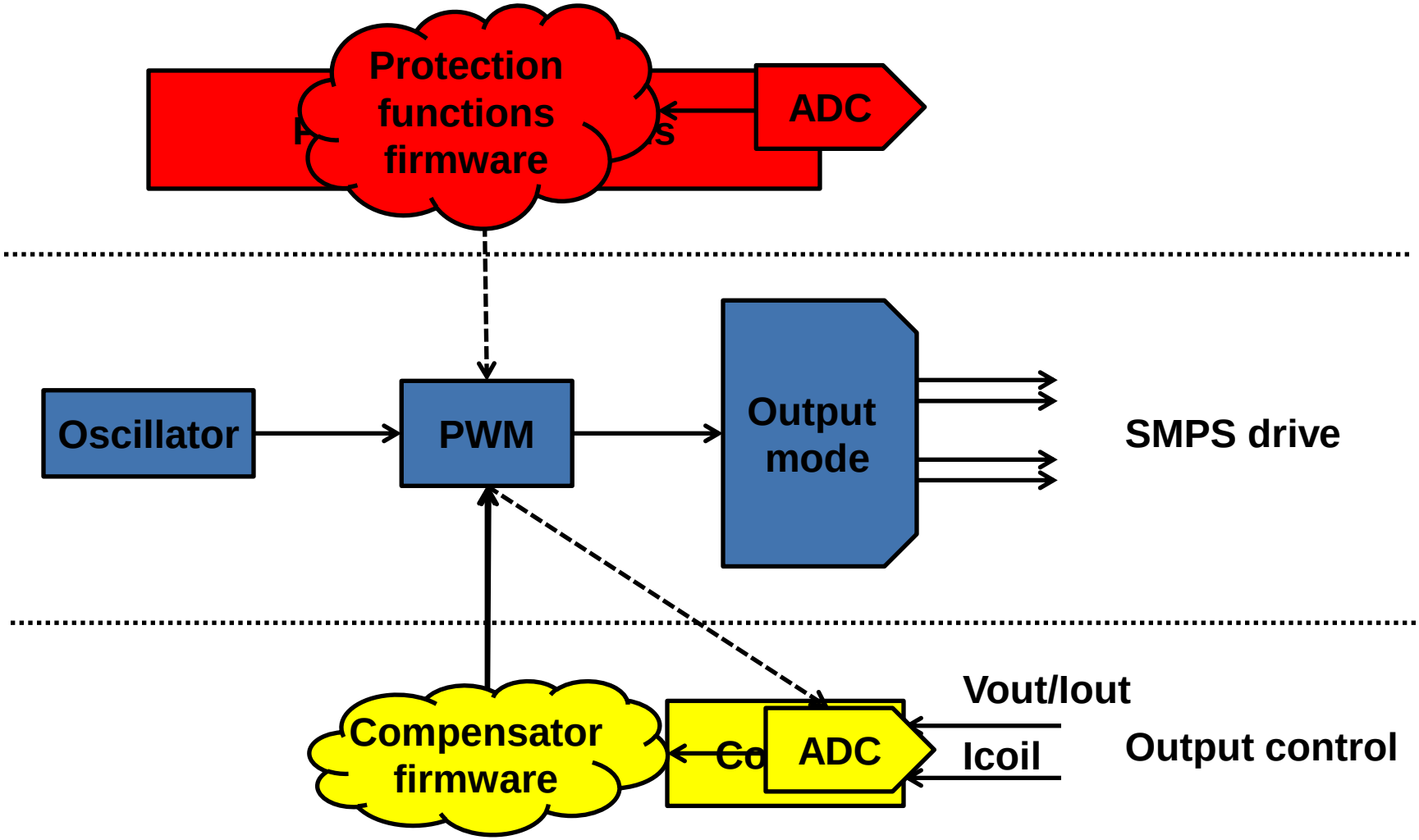
Full digital Controllers



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Resources for full digital control

- High resolution PWM → Output accuracy
- Fast ADC converter → Closed loop performances
- CPU speed → Closed loop performances

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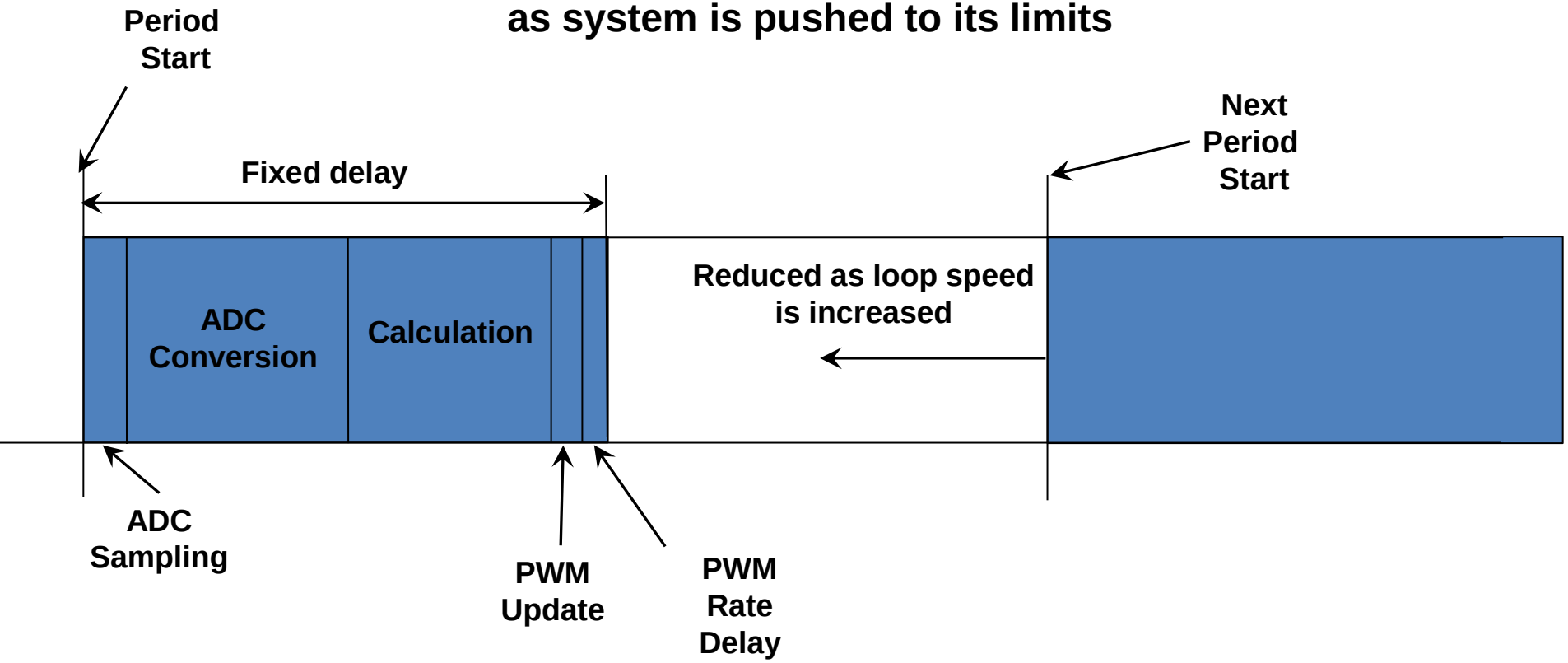
Processing Delay

Delay from sample time to actuation tends to Ts as system is pushed to its limits



Fcrossover ≅ Fcontrol/20

Rule of thumb

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Additional challenges

- **Phase margin loss:**

$$\Delta\Phi_{DEG} = -360° \times \frac{T_{sample}}{T_{crossover}}$$

- **Max PWM resolution is:**

$$PWM_{res} = \frac{f_{osc}}{f_{pwm}}$$ (8 bit with 32MHz and 100 kHz PWM)

- **No digital current mode**

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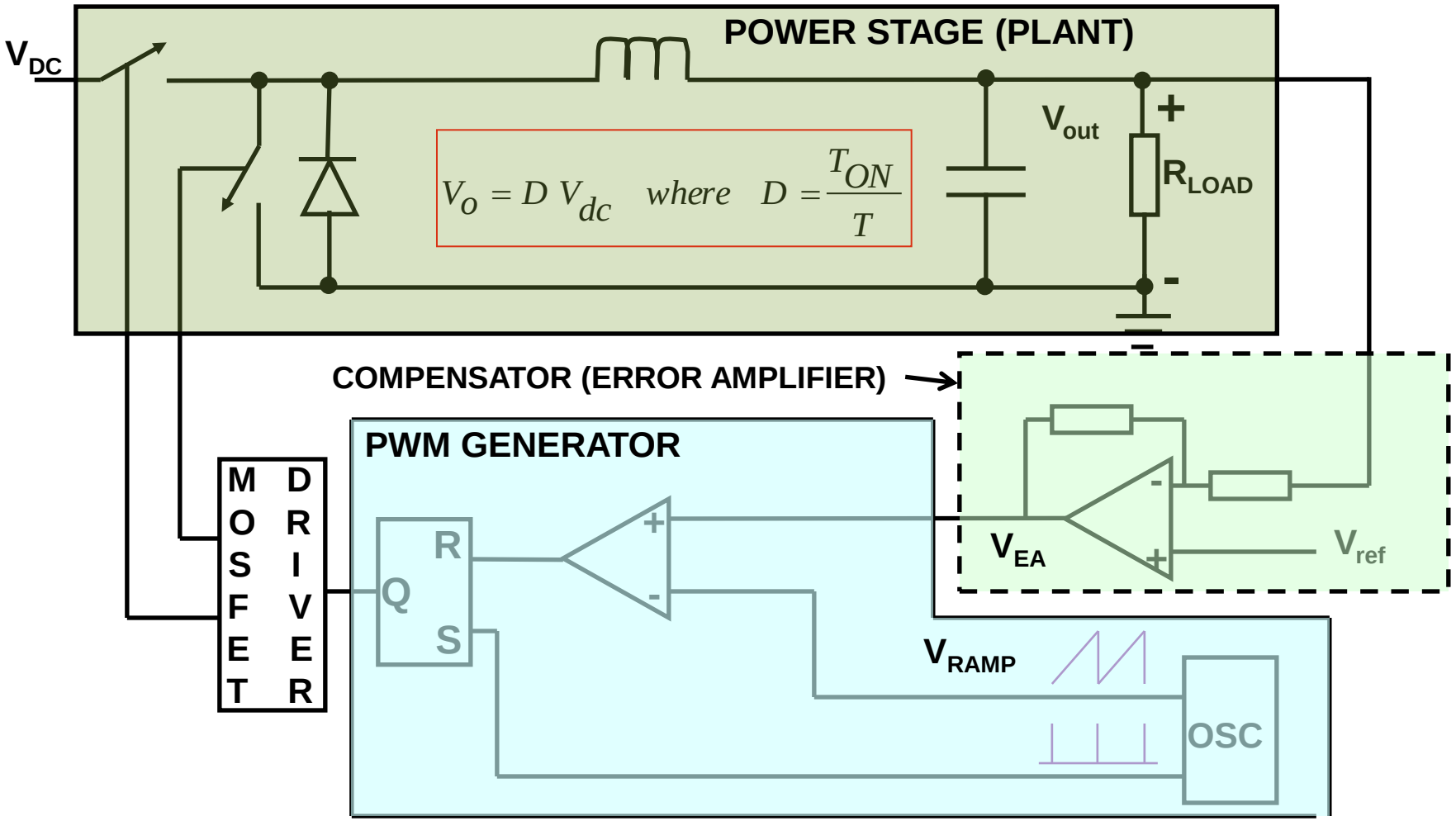
Analog Design Review

Analog World: Buck Converter - Voltage Mode



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Core Independent Peripherals

HE Flash

CLC

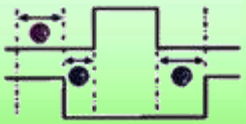
f x n/m

NCO

HCVD

ACT

PPS



CWG/COG

DC/DC
BLDC

PSMC

Slope Comp.

SMT

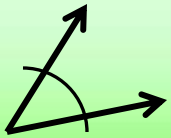
HLT

ZCD

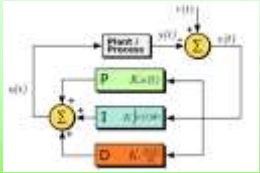
CRC-WWDT

16-bit
PWM

100mA



Angular Tmr



MACC

ADC²

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SMPS Modes of Operation

- **Voltage Mode**
  - Uses error voltage to control duty cycle
- **Current Mode**
  - Uses error voltage to control inductor current
- **Hysteretic Control**
  - On/Off control of fixed PWM based on output voltage
- **Proportional Control**
  - Proportional control of variable PWM based on output voltage and an active feedback filter (compensator)

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Voltage Mode Hysteretic

- **Control Blocks required for feedback control**
  - **A fixed duty cycle PWM**
  - **Reference Voltage**
  - **Comparator**
  - **Gating for control of on/off PWM**

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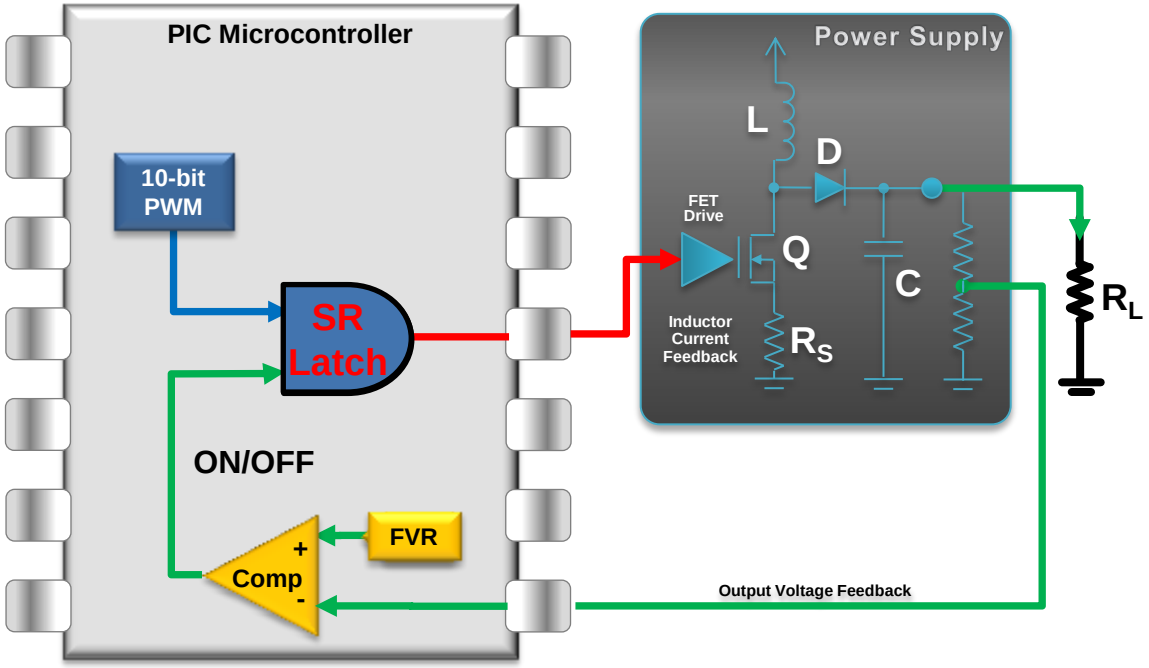
CIP Solution



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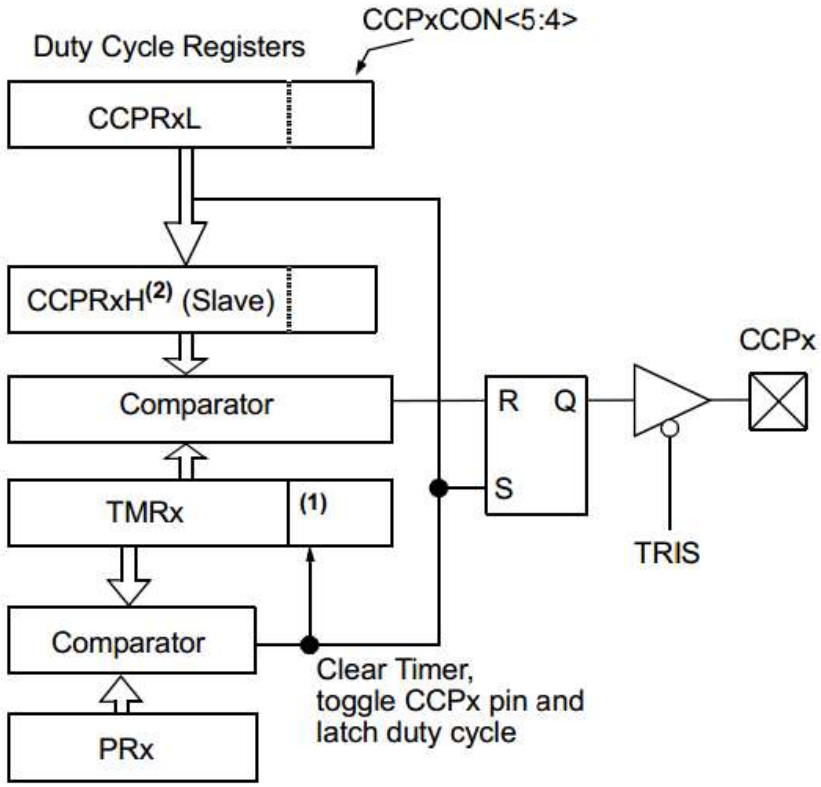
CCP

- 10-bit PWM
- Uses TMR2,4,6
- 8-bit period register
- 8 bit duty cycle in CCPRxL
- 2 bit duty cycle in CCPxCON



Note 1: The 8-bit timer TMRx register is concatenated with the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPRxH is a read-only register.

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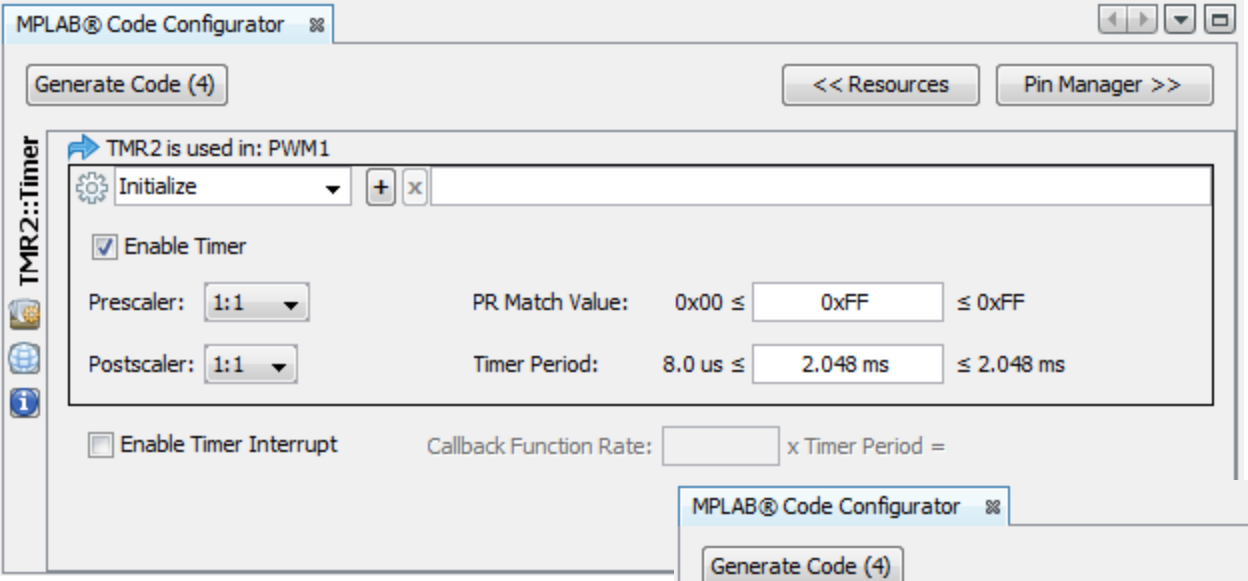
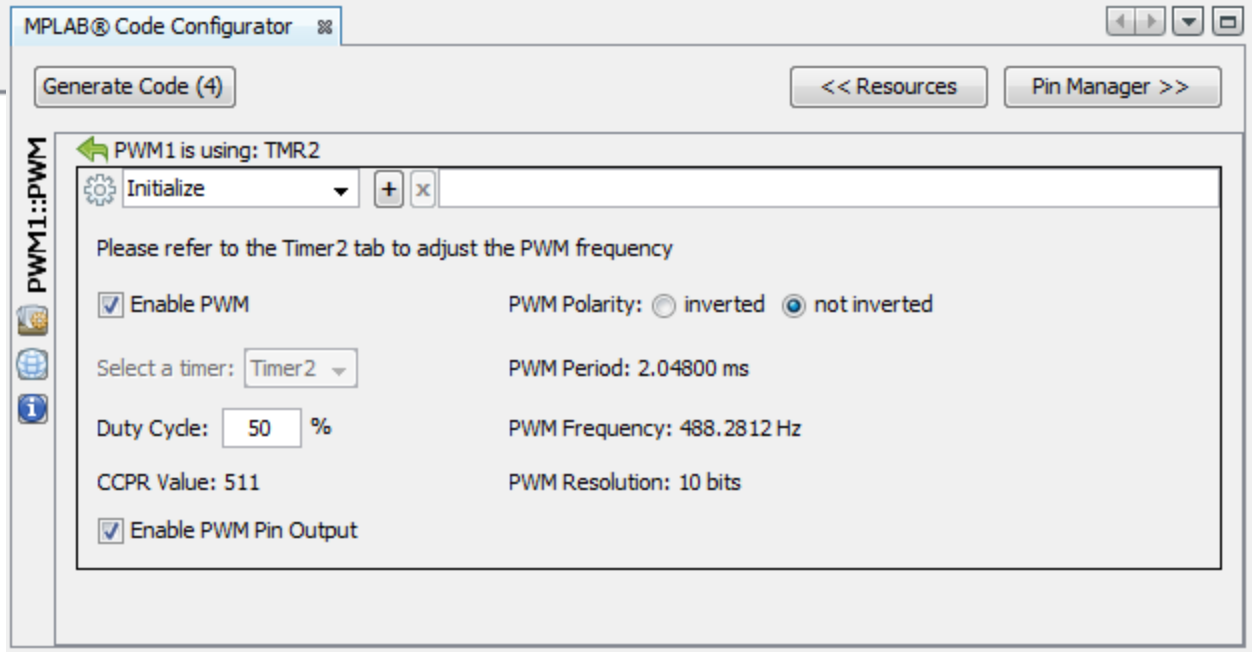
MCC - CCP





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HS Comparators

- Programmable input selection
- Programmable output polarity
- Programmable speed/power/Hyst
- Programmable and fixed voltage references
- Internal connections to PWM/COG/PRG/CLC/Op Amp/TMRs/DSM
- Interrupt on change
- External output

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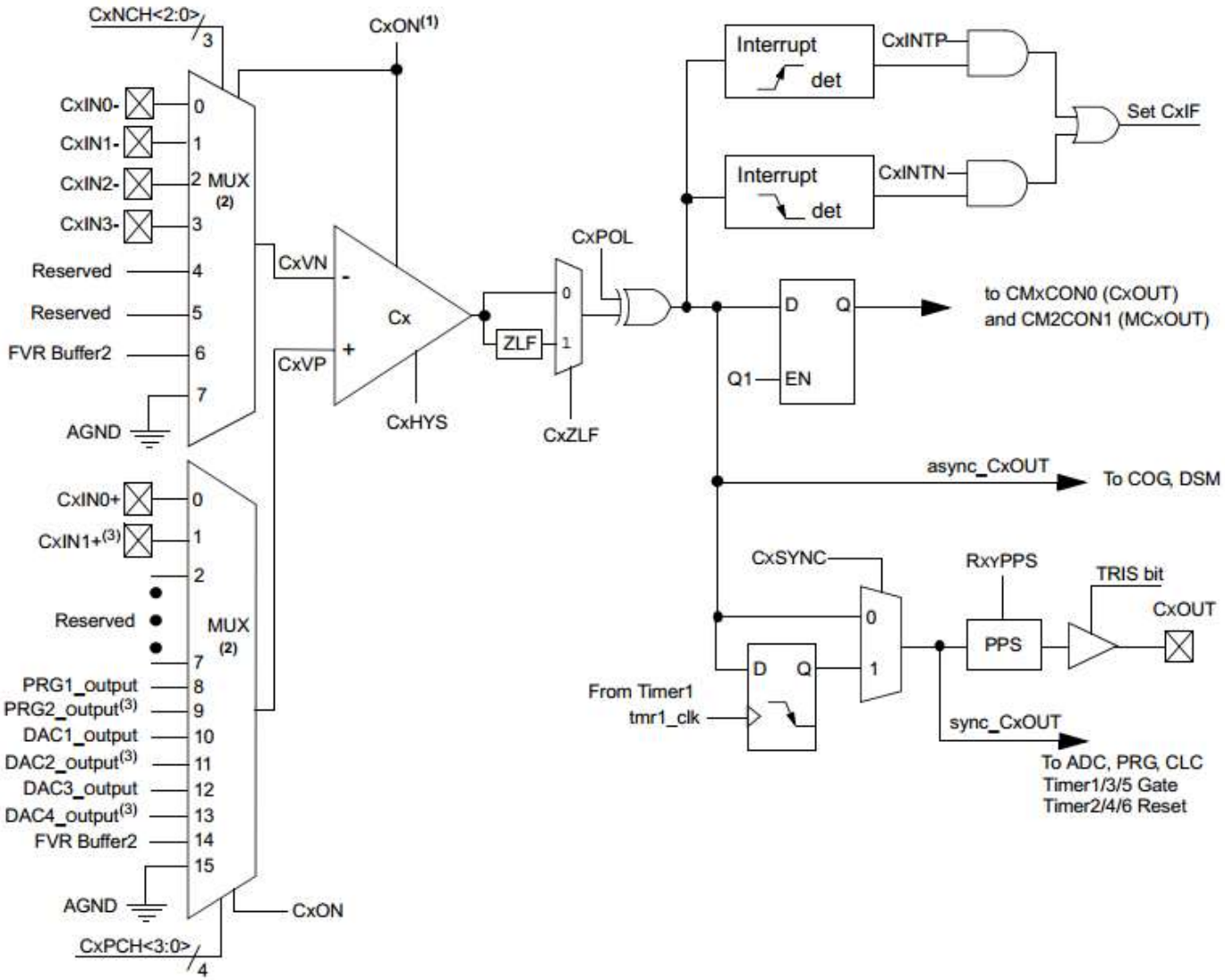
Comparators



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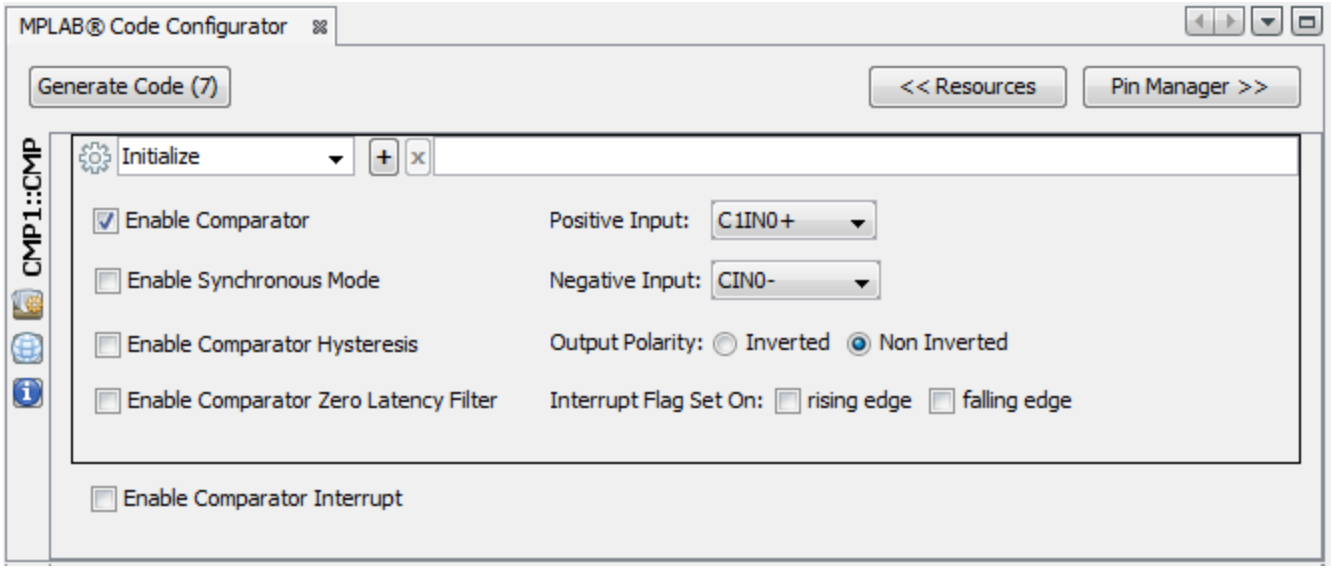
MCC - Comparator



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Configurable Logic Cells CLC

- Combinational logic
  - AND/NAND/AND-OR/AND-OR-INVERT/OR-XOR/OR-XNOR
- Latches
  - J-K w/RST, S-R, D latch w/SR, D Flop w/SR
- 38 selectable inputs
- Connections to CIPs, Clocks, Timers, GPIO, COGs, & each other
- Can be used for debug purposes

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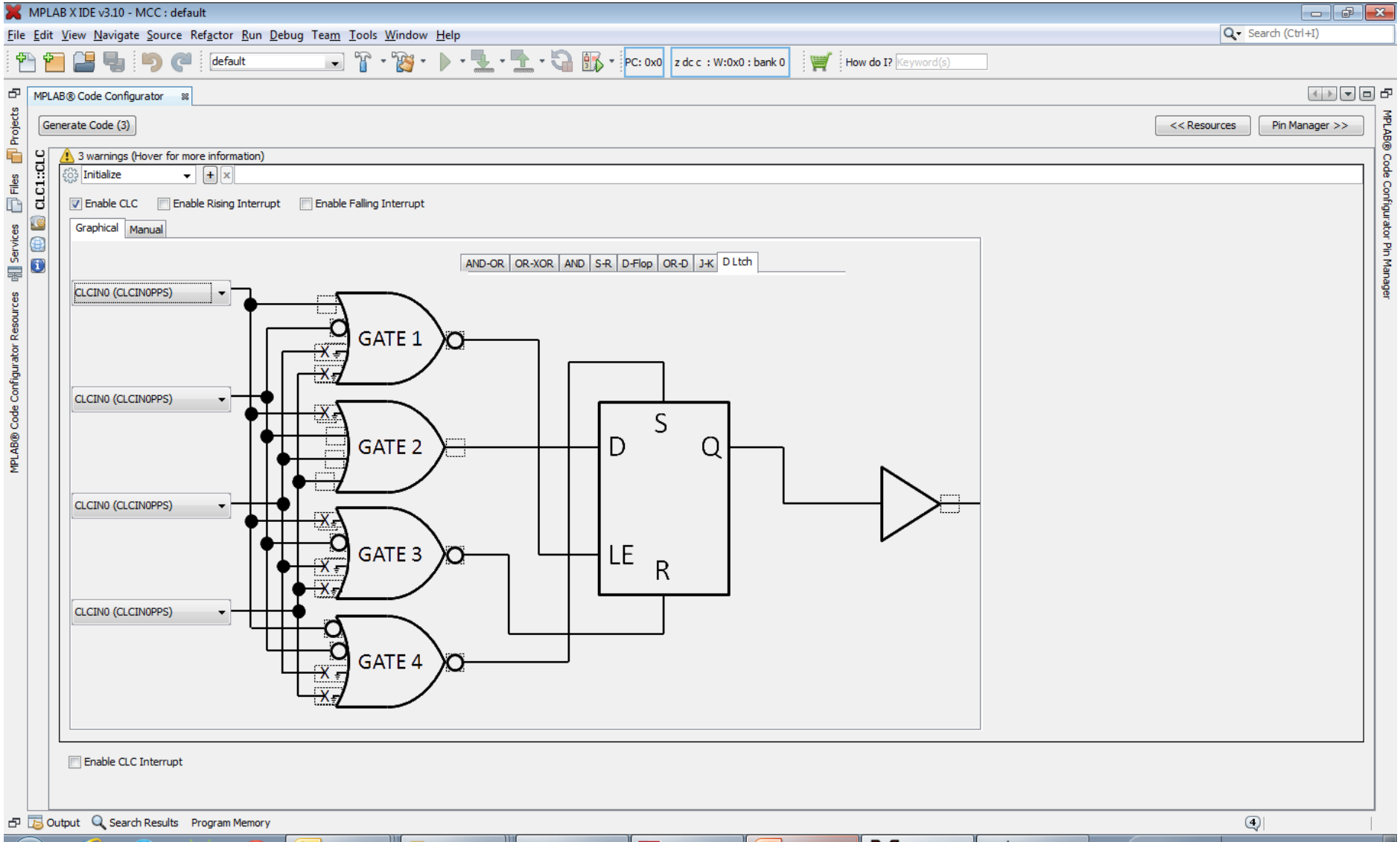
MCC - CLC



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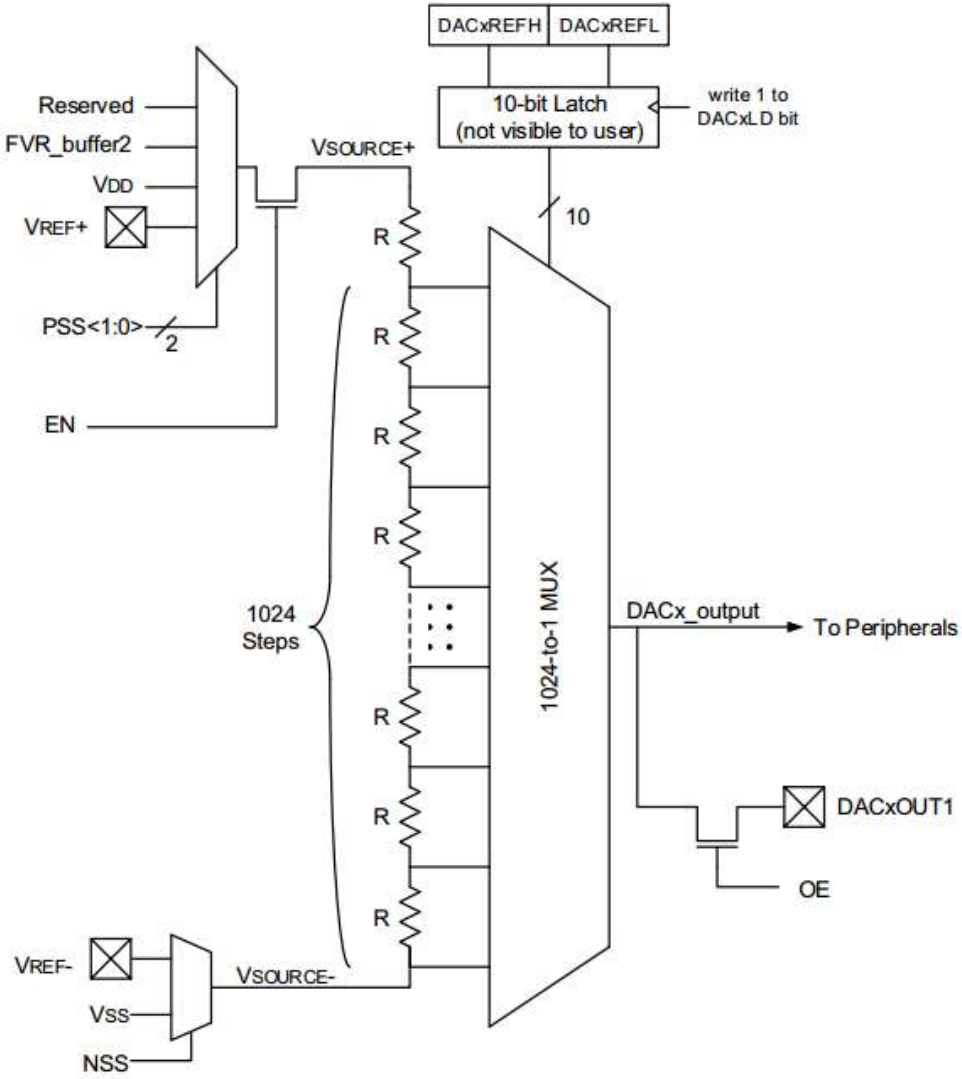
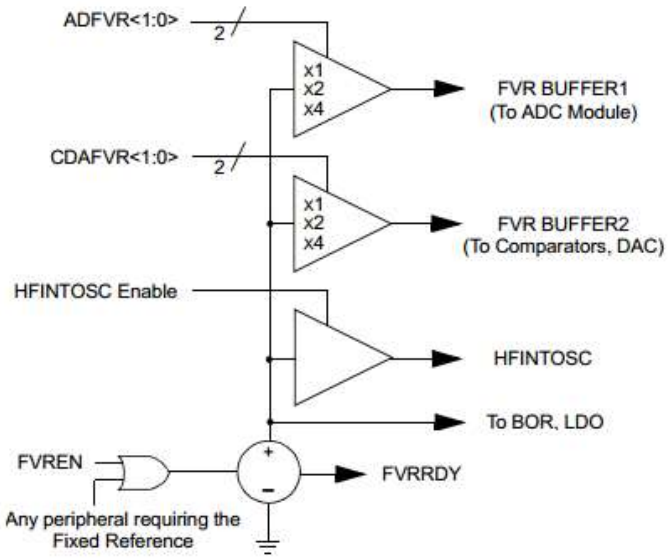
DAC & Fixed Voltage Reference (FVR)





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Voltage/Current Mode

- PWM is turned on by a timer and turned of by a comparator → same duty cycle resolution of an analog PWM
- Control loop is implemented using the internal opamp with an external compensation network → no need for high performance MCU for high speed calculations, and for high speed ADC
- Slope compensation for current mode uses an internal ramp generator + comparator → no external components
- Comparator measures the instantaneous current → no need for high speed ADC or fast CPU for digital slope compensation
- With an analog controller the crossover frequency my be in the range of $F_{sw}/10$

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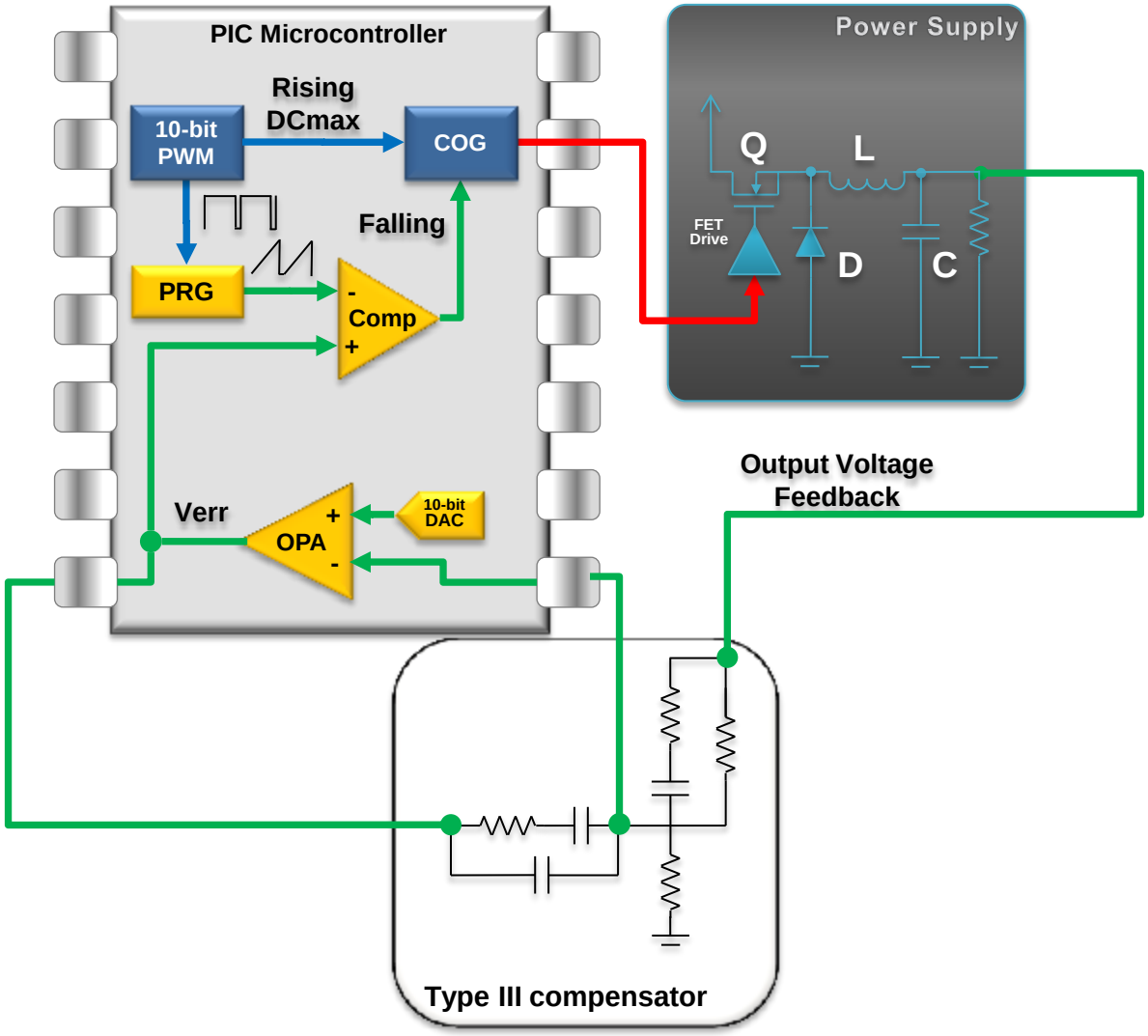
Voltage mode implementation



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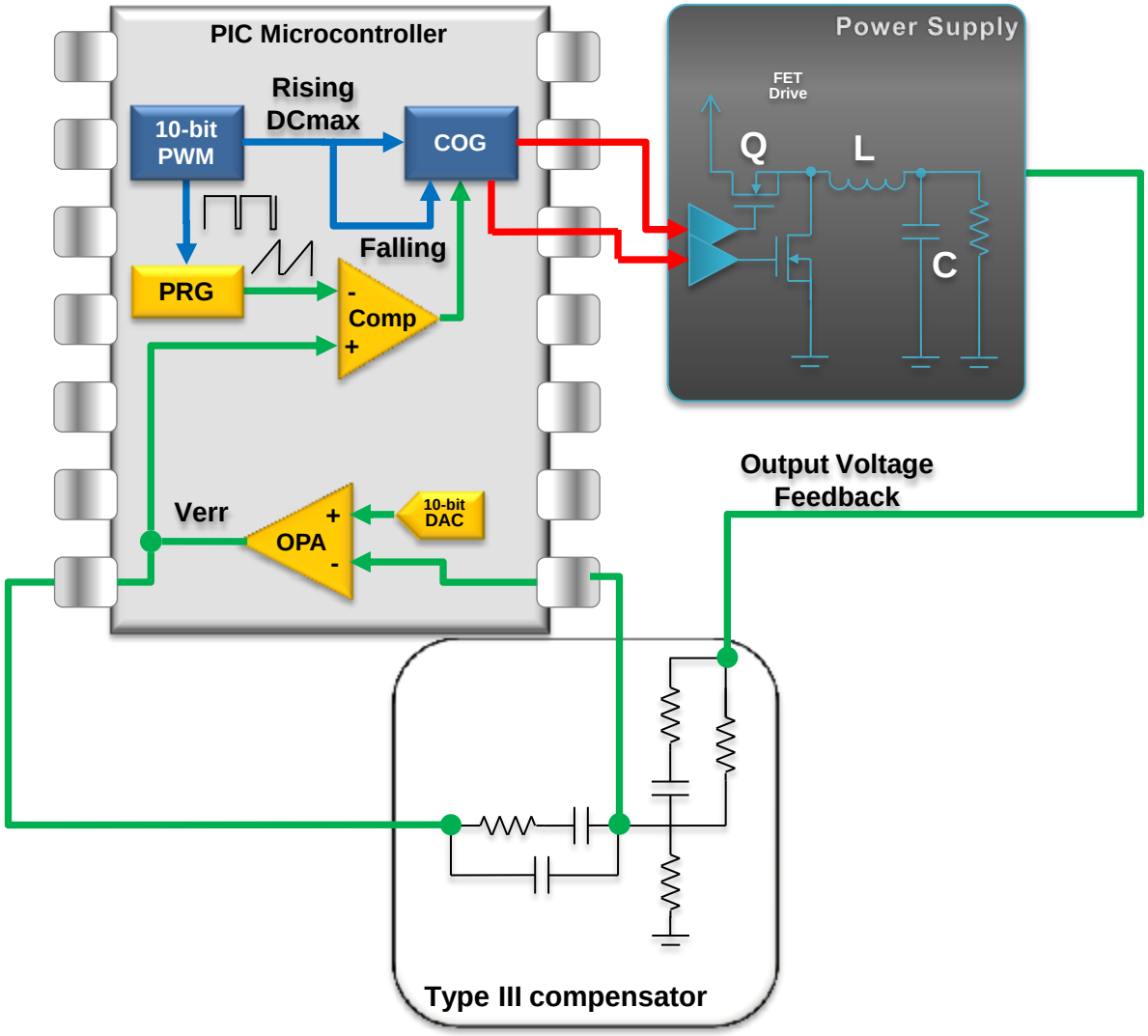
Voltage mode implementation



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Op Amps

- Low leakage inputs
- 2 MHz GBWP, CMRR 70dB typ
- Programmable inverting & non-inverting input selection
- Unity gain & output tristate over-ride
- Multiple over-ride sources

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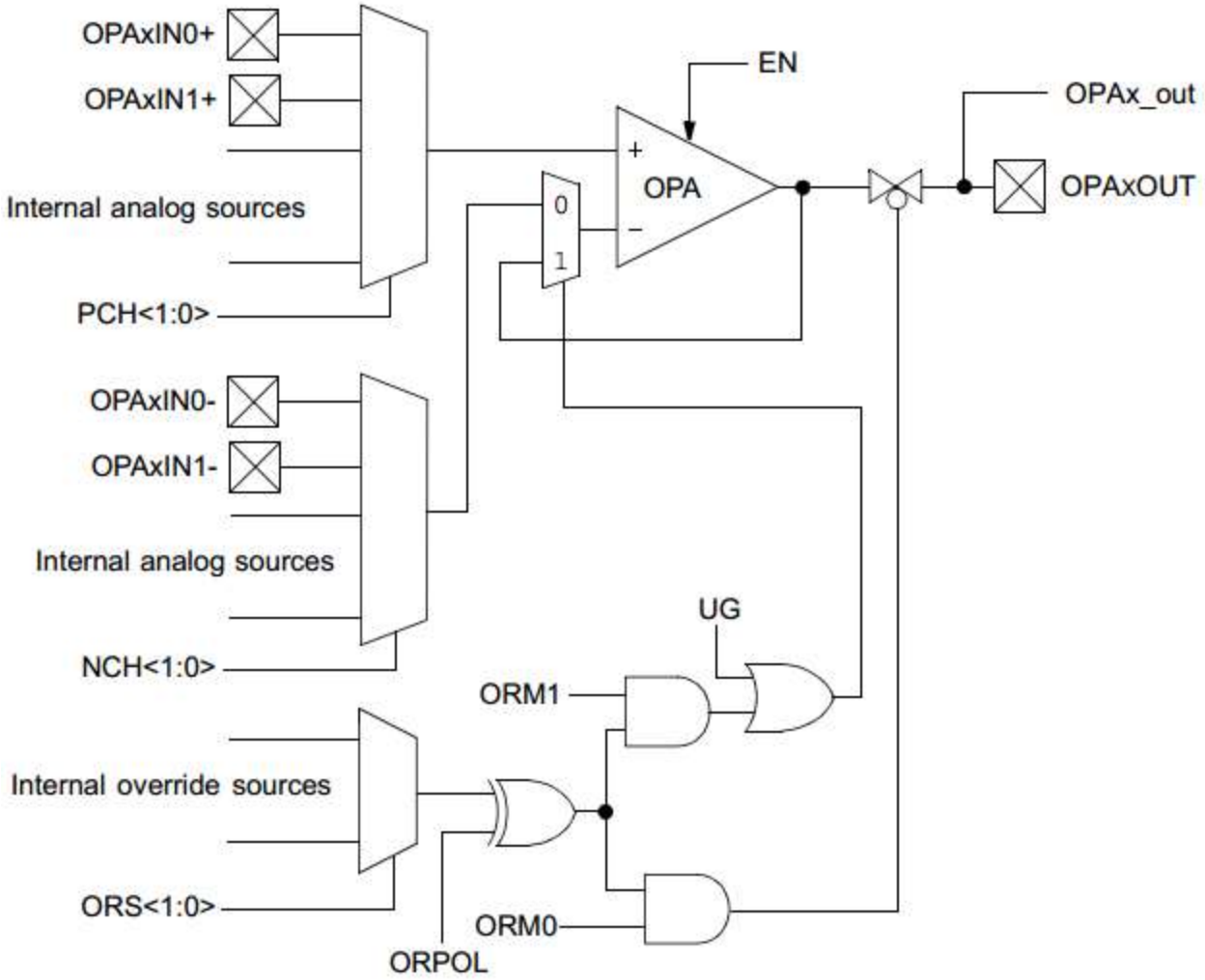
Op Amp



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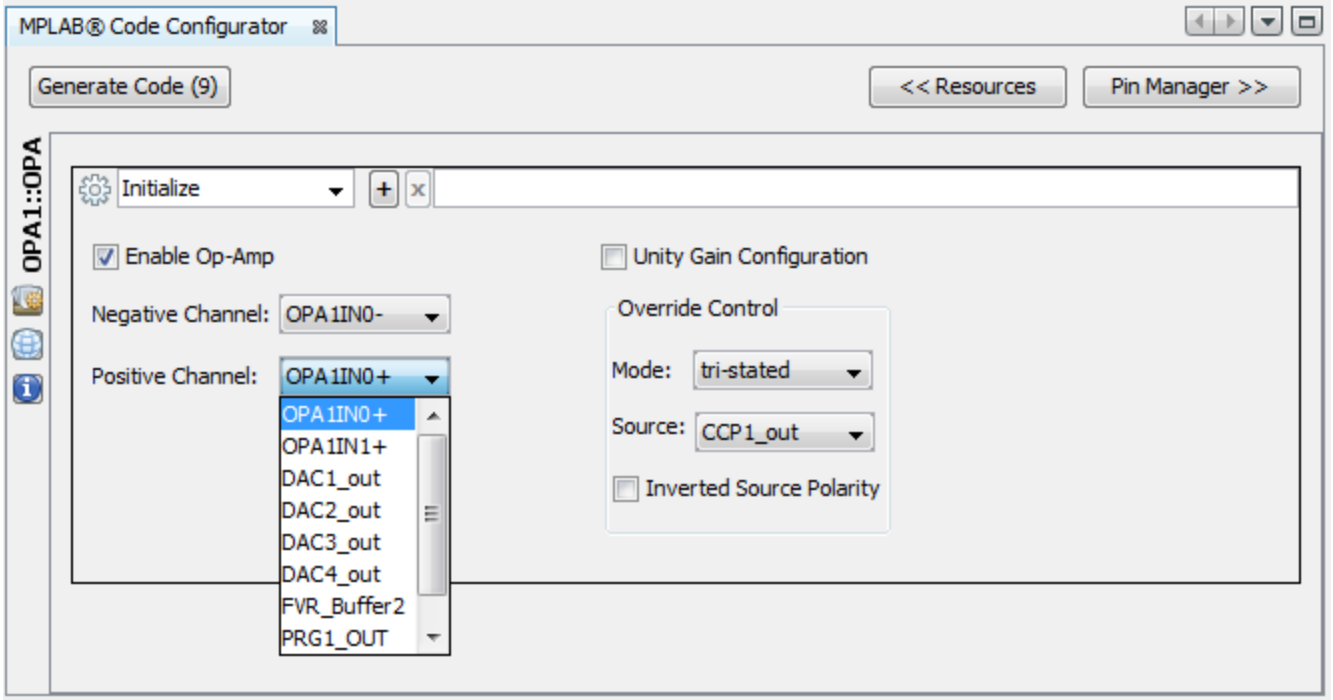
MCC - OPA



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Programmable Ramp Generator (PRG)

- Linear positive & negative ramp
- Programmable current source/sink
- Int/ext reference voltage select
- Int/ext timing source select
- 3 modes
  - Falling voltage (slope compensation)
  - Rising voltage (for voltage mode)
  - Alternating rising/falling voltage

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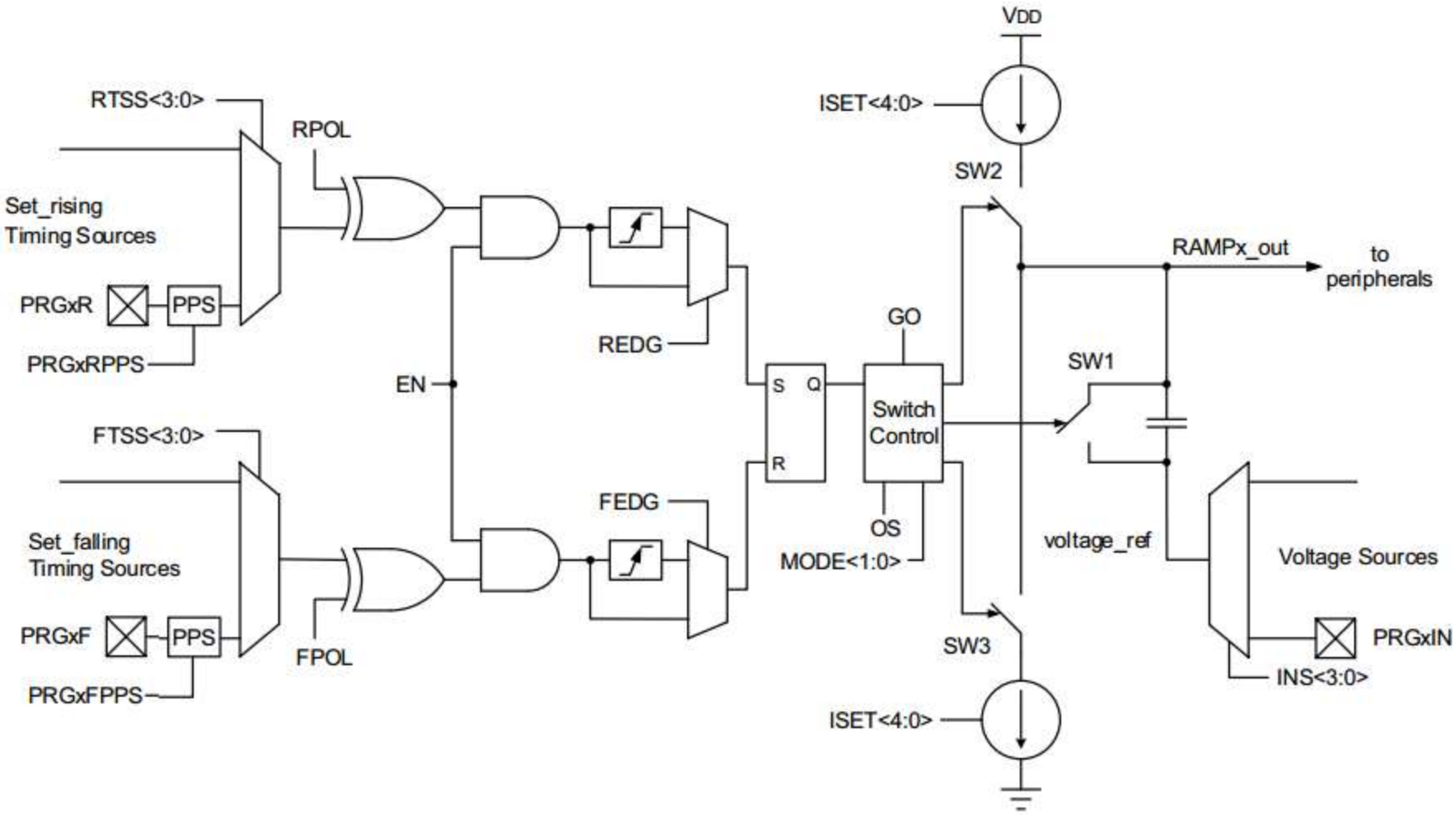
Programmable Ramp Generator (PRG)



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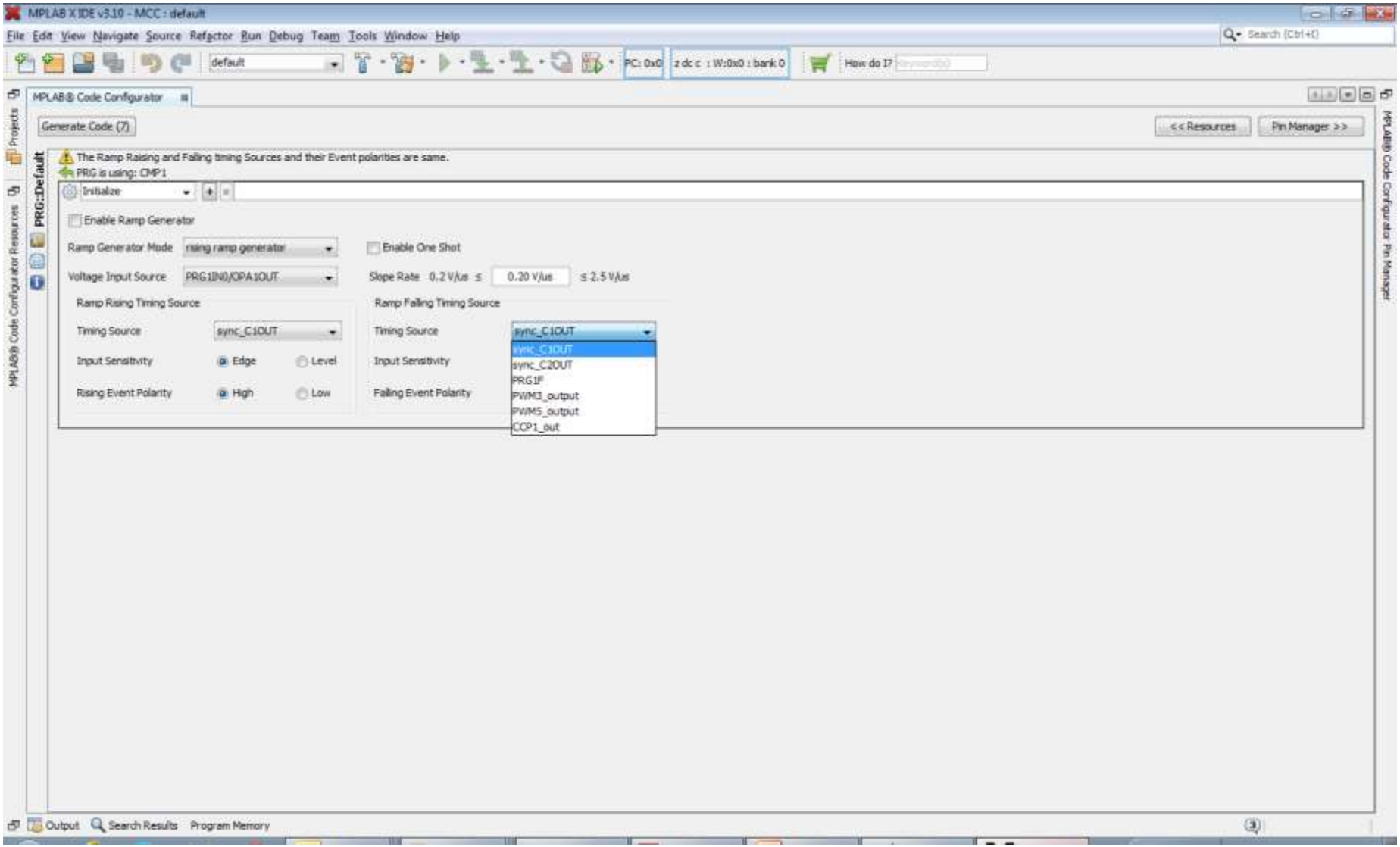
MCC - PRG



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Complimentary output generator (COG)

- **Six mode:**
  1. **Steered mode**
  2. **Synced steered mode**
  3. **Half Bridge**
  4. **Full Bridge (for/rev)**
  5. **Push Pull**
- **Independent rise/fall events with edge/level select**
- **Phase delay, Dead time, Blanking**
- **Auto-shutdown with pin override, high, low, or high-Z**

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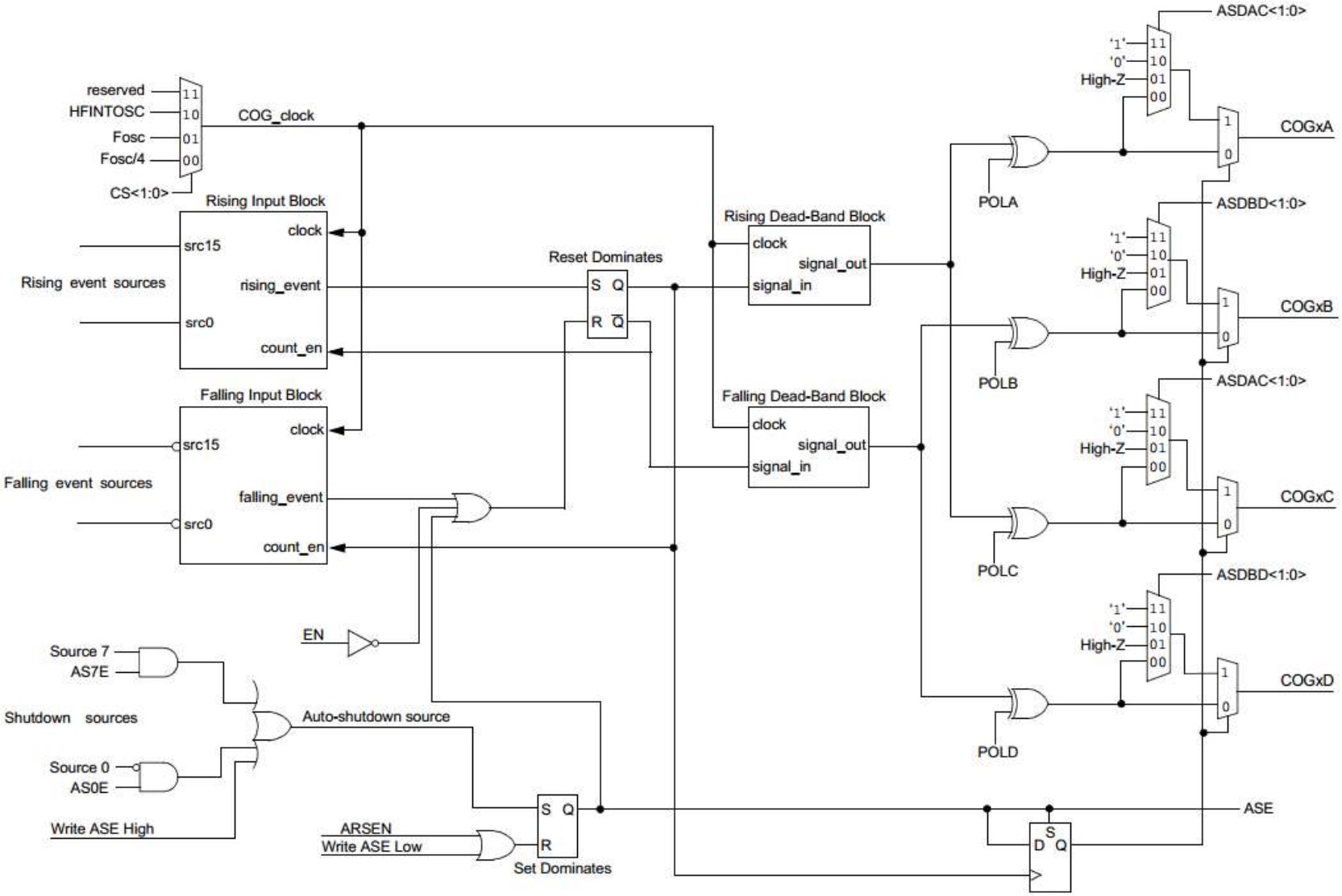
COG



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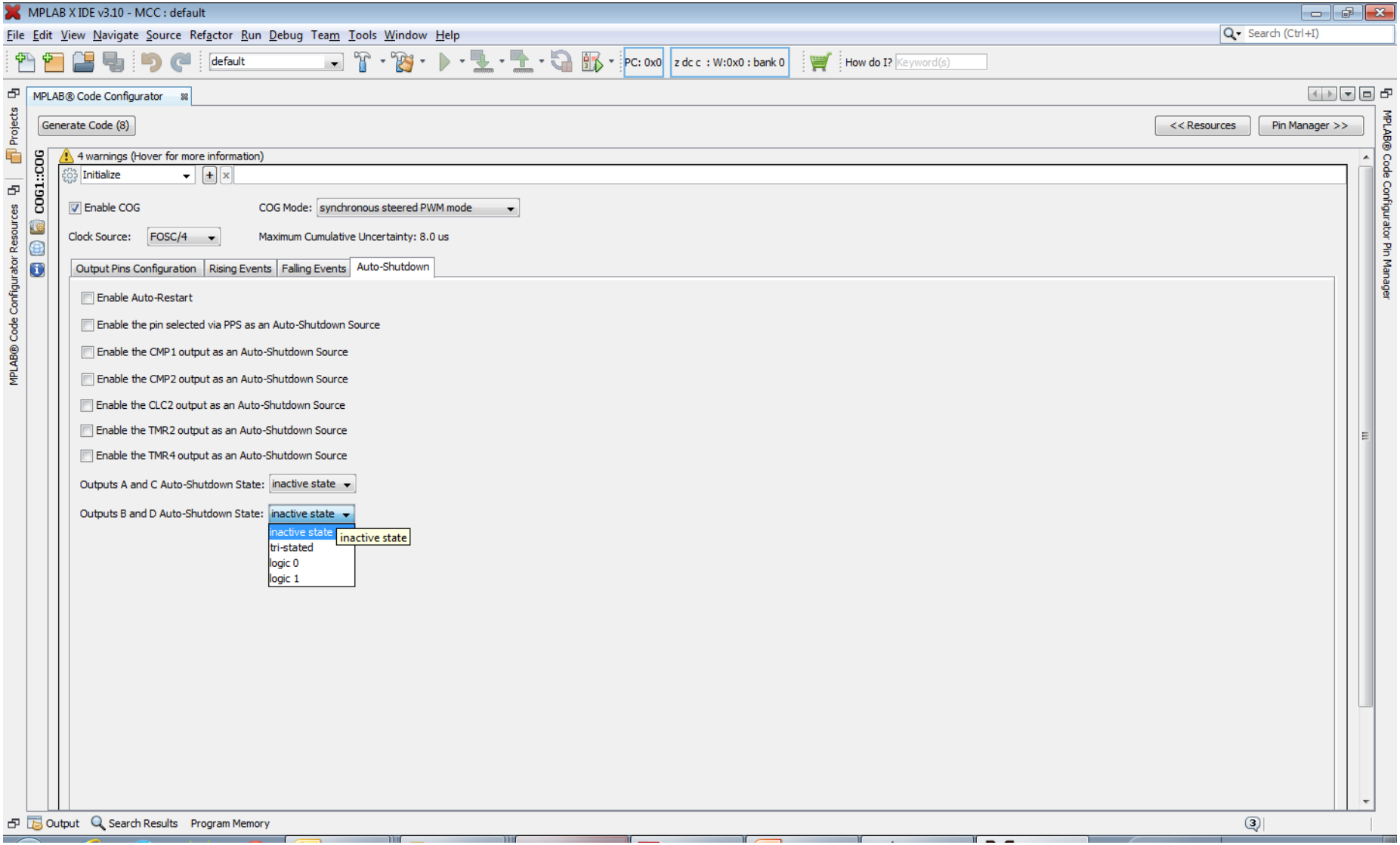
MCC - COG



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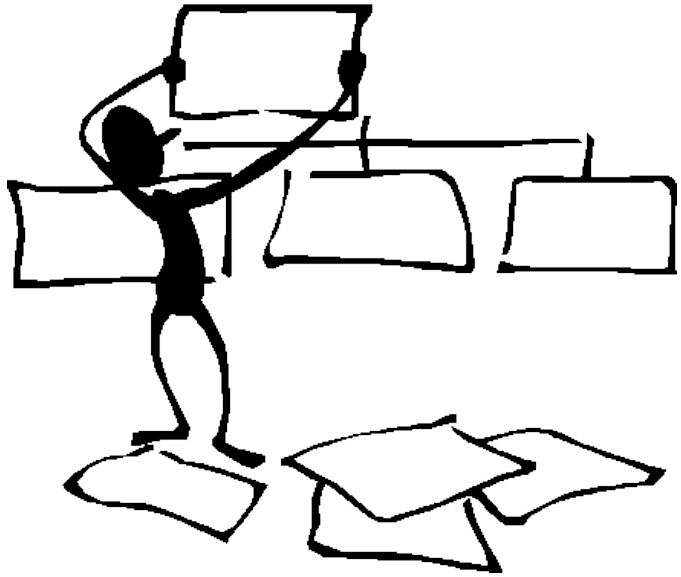
Current Mode

In addition to Voltage mode:

- A inner current loop need to be added
- Slope compensation is needed because the current loop is instable if the DC is greater than 50%
- Ramp generator to implement slope compensation



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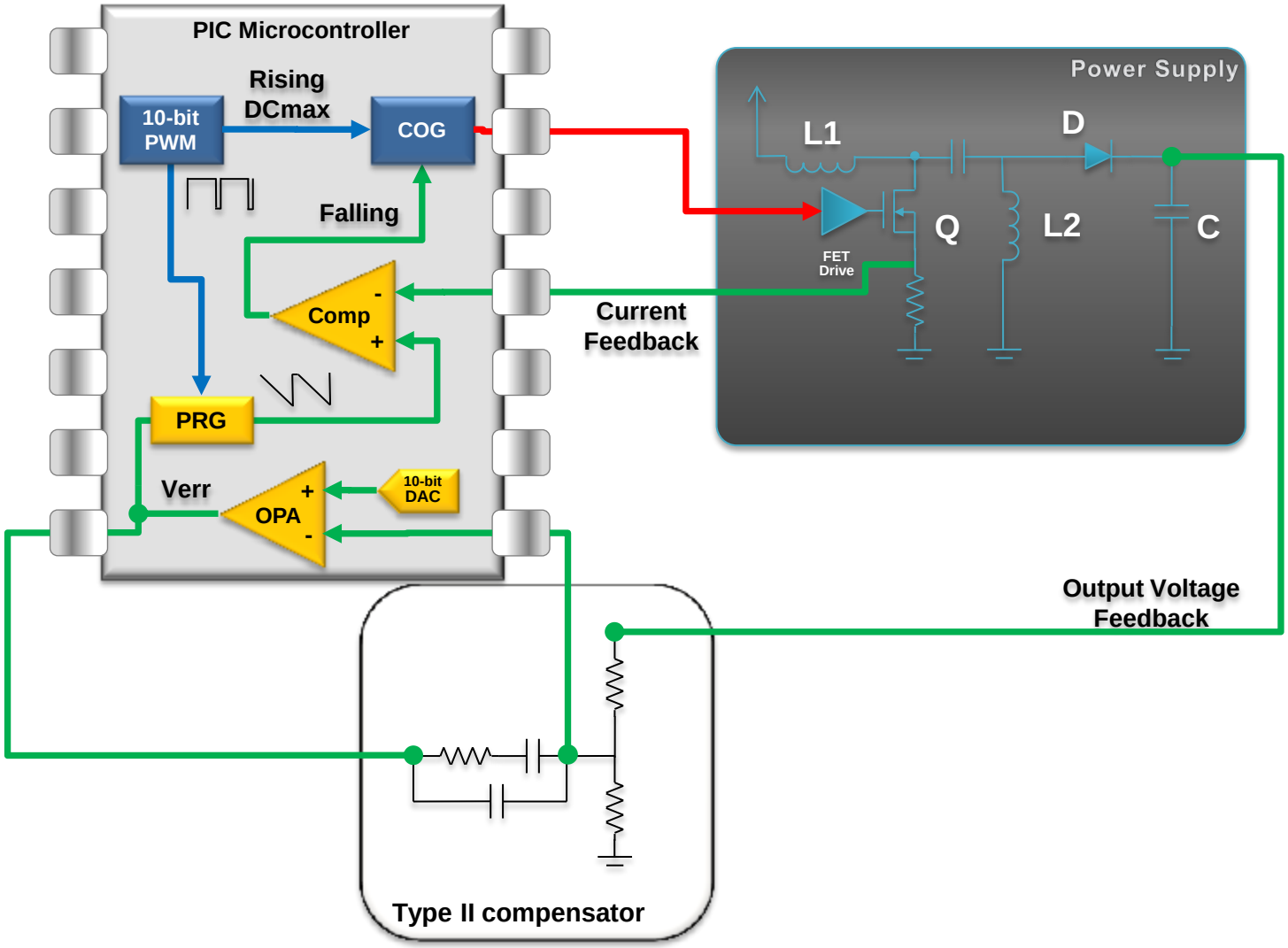
Current mode implementation



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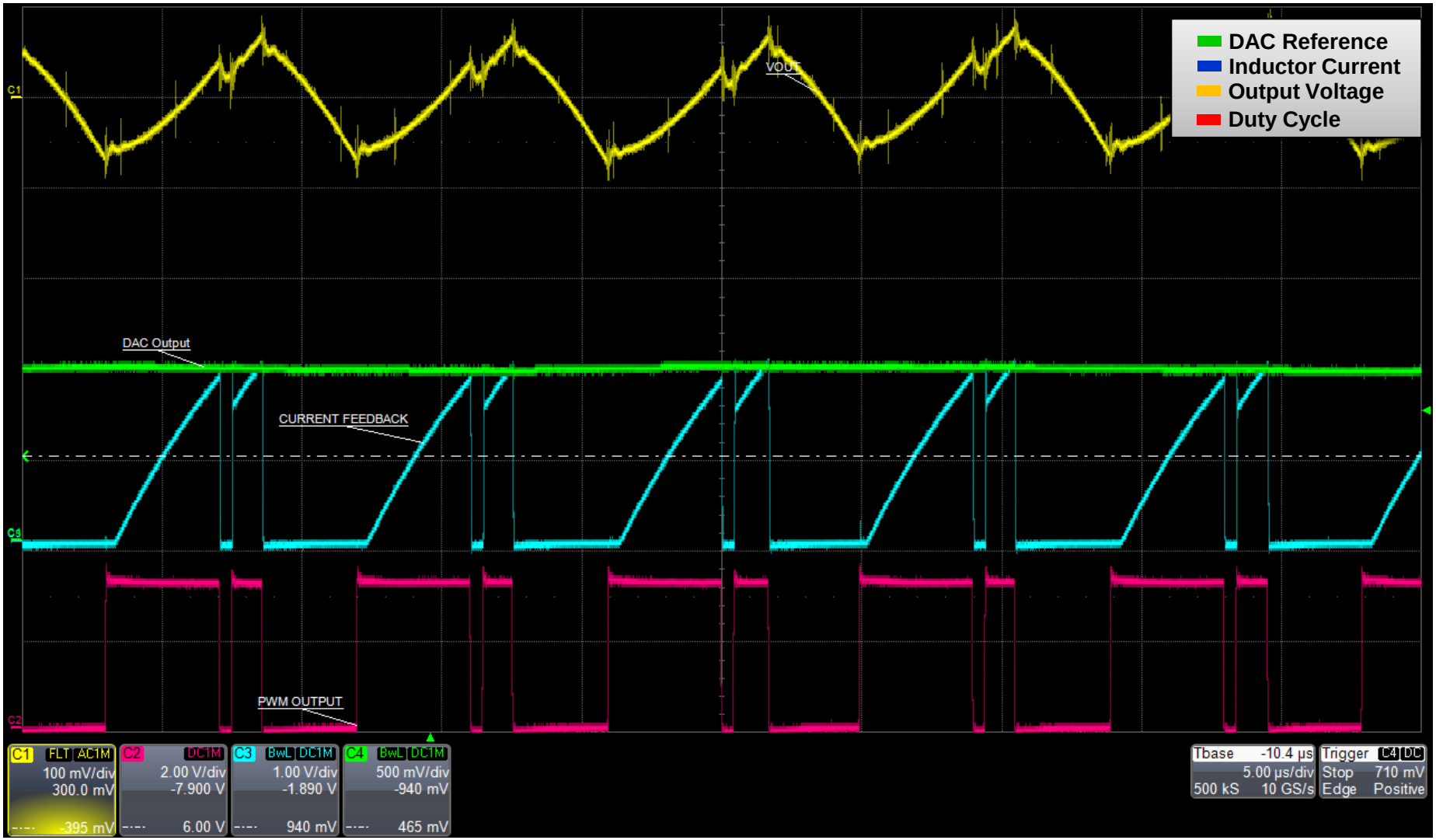
Sub Harmonic Oscillations in the Time Domain



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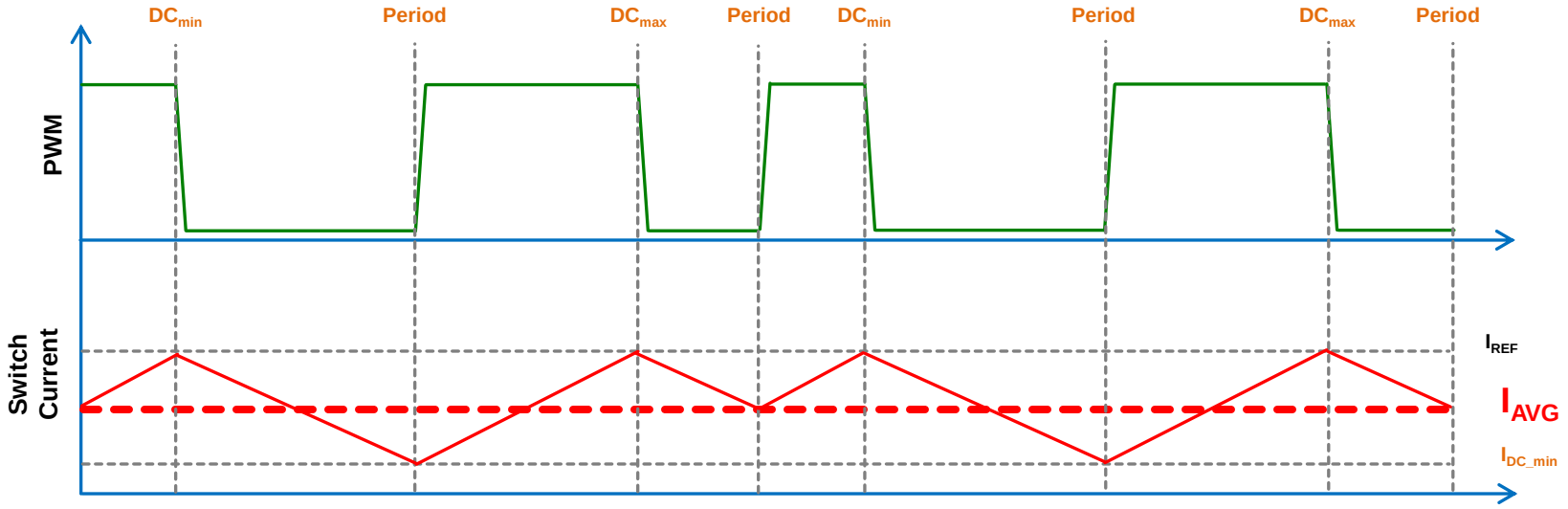
Sub Harmonic Oscillation Phenomenon

- **During steady state operation the average output voltage/current still looks constant from outside and no/very little regulation is available**



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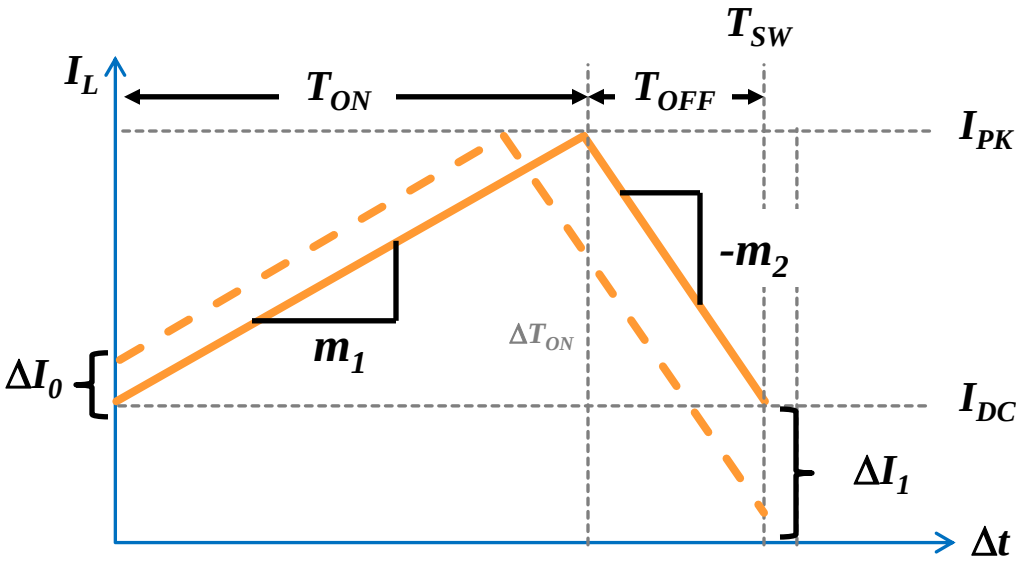
Determining Slope Factors

- The slopes of the perturbed current waveform can be considered to be parallel to the expected, ideal waveform
- So the ratios between ΔI_0 and ΔI_1, T_{ON} and T_{OFF} and m_1 and m_2 can be set in ***fixed relations***



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Determining Slope Factors – Inductor Current –

- **Ideally balanced waveform:**

$$I_{PK} = m_1 \times T_{ON} + I_{DC}$$
$$I_{PK} = m_2 \times T_{OFF} + I_{DC}$$

with

$$T_{ON} = D \times T_{SW}$$
$$T_{OFF} = (1 - D) \times T_{SW}$$

- **In Steady State:**

$$\frac{m_2}{m_1} = \frac{D}{1 - D}$$

- **Perturbed waveform:**

$$I_{PK} = \Delta I_0 + m_1 \times (T_{ON} - \Delta T_{ON}) + I_{DC}$$
$$I_{PK} - m_2 \times (T_{OFF} + \Delta T_{ON}) = \Delta I_1 + I_{DC}$$

with $\frac{\Delta I_0}{\Delta I_1} = -\frac{m_1}{m_2}$

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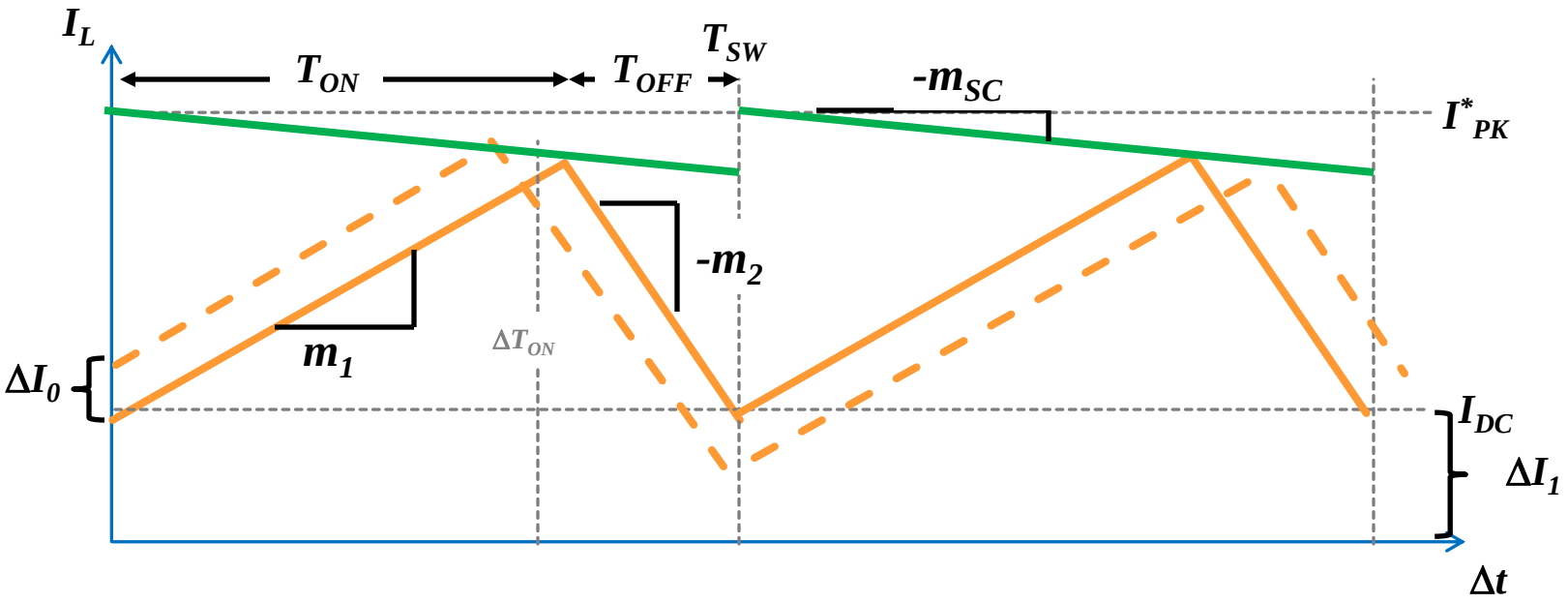
Determining Slope Factors – Compensation Ramp –

- To bring the current back in balance, the reference voltage will be decreased over time (subtractive compensation)
- The required V_{REF} de-rating slope $-m_{SC}$ has to be derived from the rising and falling current slopes m_1 and $-m_2$



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Determining Slope Factors – Compensation Ramp –

- The number of cycles ***n*** required to reach its maximum amplitude can be determined by

$$\Delta I_n = \left(-\frac{m_2}{m_1} \right)^n \Delta I_0$$

- By introducing the compensation ramp $-m_{SC}$, we get

$$\Delta I_n = \left(-\frac{m_2 - m_{SC}}{m_1 + m_{SC}} \right)^n \Delta I_0$$

- **Critical** compensation can be achieved, when

$$\left| \frac{m_2 - m_{SC}}{m_1 + m_{SC}} \right| < 1$$

and so we get

$$m_{SC} = \frac{1}{2}(m_2 - m_1)$$

Design Target for maximum dynamic range

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Determining Slope Factors

- **Assuming a constant inductance L, the slopes are proportional to the voltage across the inductor**
- **For different types of converters we can therefore determine the following slope ratios**

Converter Type	m_1L	m_2L	$m_{SC}L$
Buck	V_{IN} - V_{OUT}	V_{OUT}	> V_{OUT} - 0.5 V_{IN}
Boost	V_{IN}	V_{OUT} - V_{IN}	> 0.5 V_{OUT} - V_{IN}
Buck-Boost	V_{IN}	V_{OUT}	> 0.5 (V_{OUT} – V_{IN})

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Sub Harmonic Oscillations in the Frequency Domain

- **Control to Output Transfer Function:**

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{R}{R_i} \frac{1}{1+\frac{RT_s}{L}\left[m_c D' - 0.5\right]} F_p(s) F_h(s)$$

Where

$$F_h(s) = \frac{1}{1+\frac{s}{\omega_n Q}+\frac{s^2}{\omega_n^2}} \qquad F_p(s) = \frac{1+sCR_c}{1+\frac{s}{\omega_p}}$$

$$Q = \frac{1}{\pi(m_c D' - 0.5)} \qquad \omega_n = \frac{\pi}{T_s}$$

A New, Continuous-Time Model For Current-Mode Control (Raymond **B.** Ridley)

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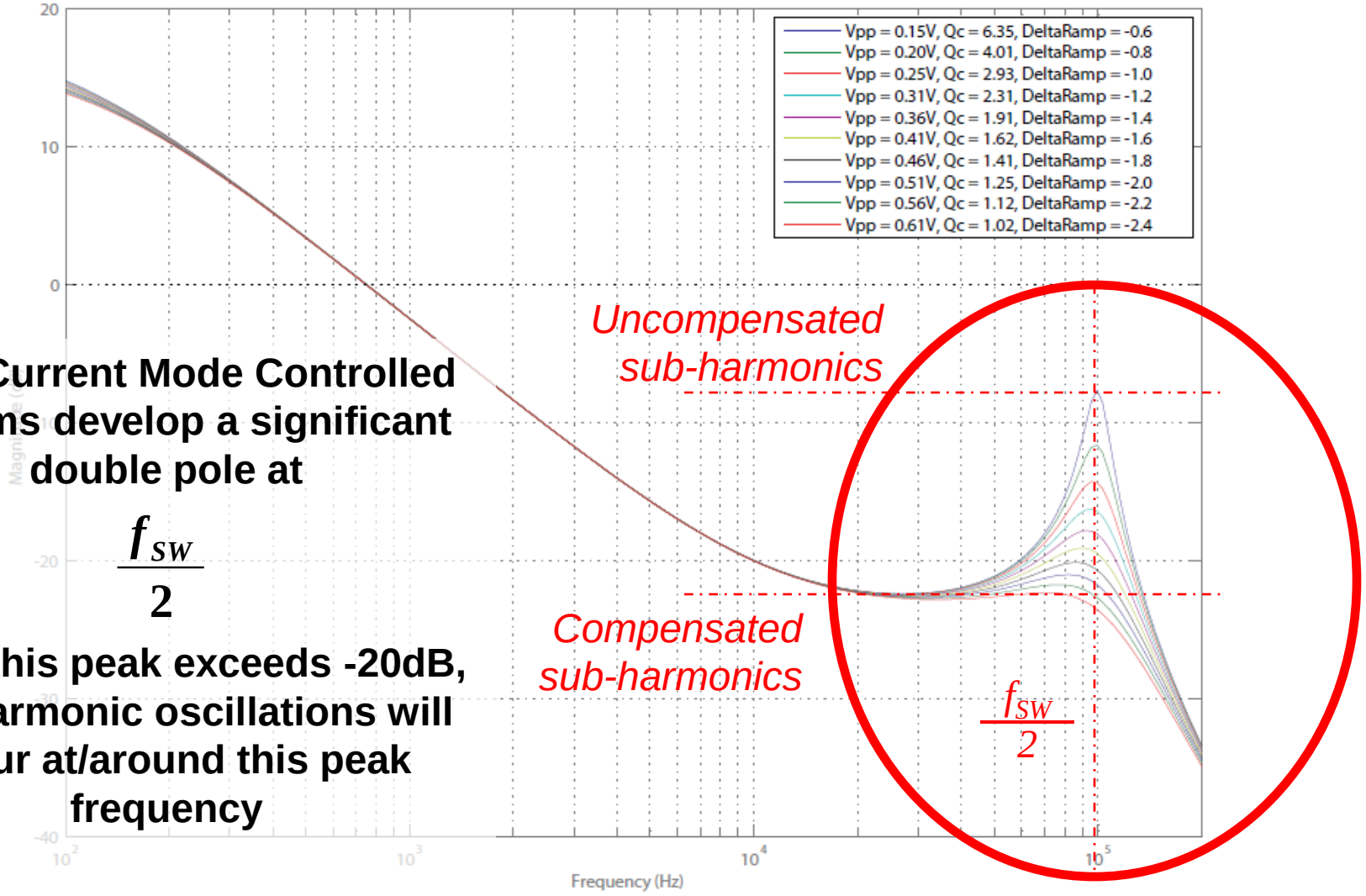
Sub Harmonic Oscillation

Peak Current Mode Controlled systems develop a significant double pole at

$$\frac{f_{SW}}{2}$$

When this peak exceeds -20dB, sub harmonic oscillations will occur at/around this peak frequency



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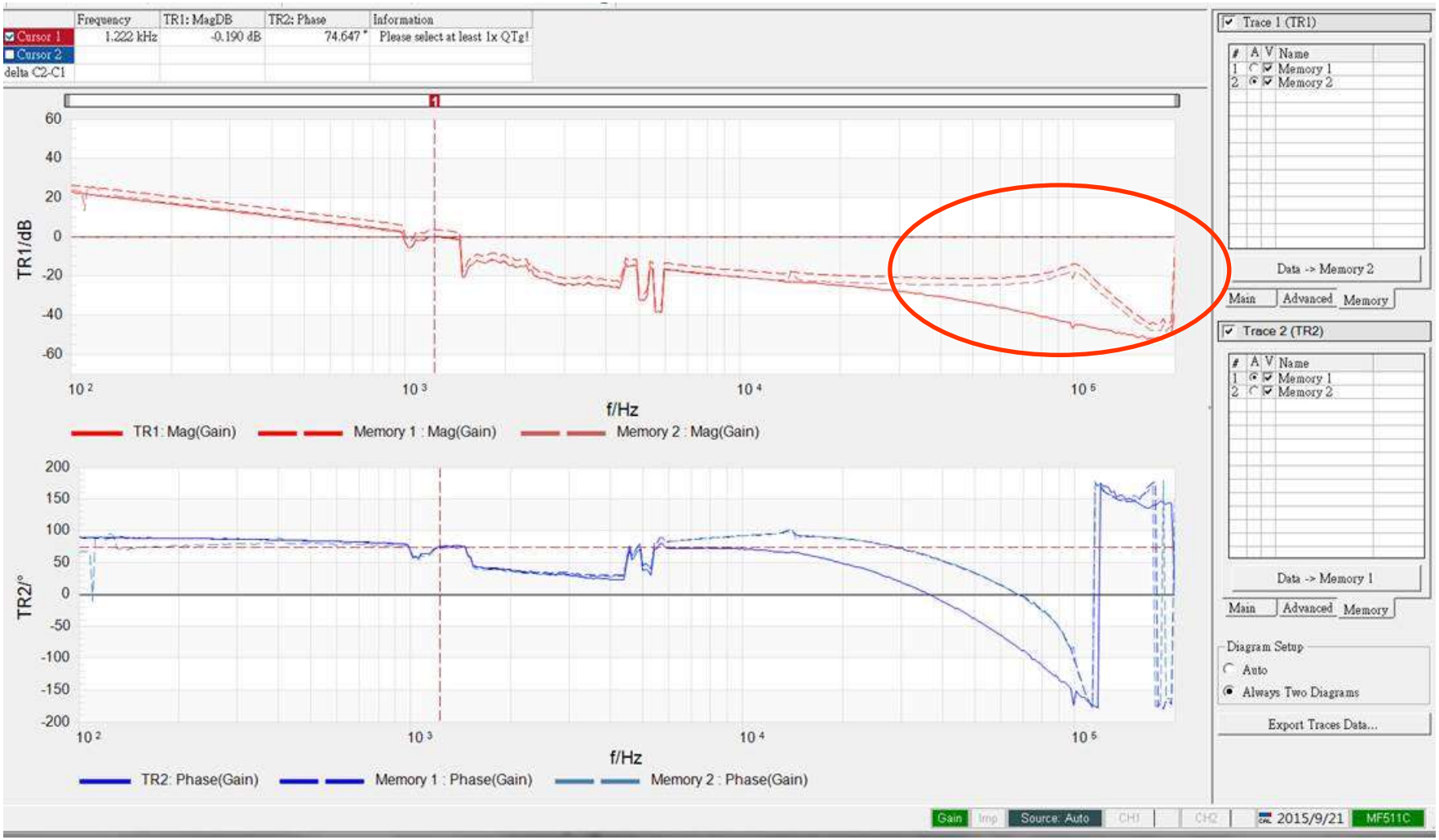
Real Case Study



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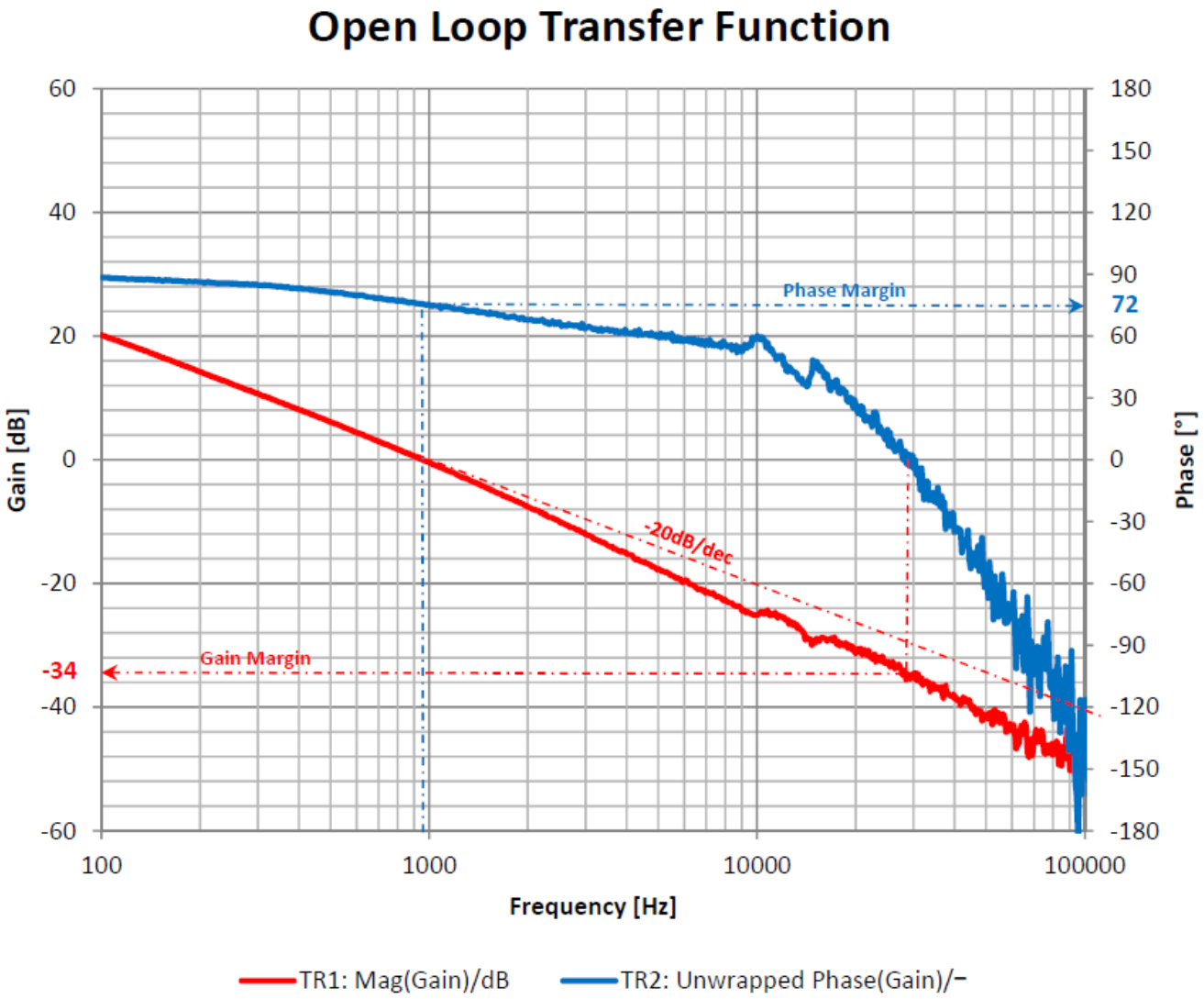
Real Case Study



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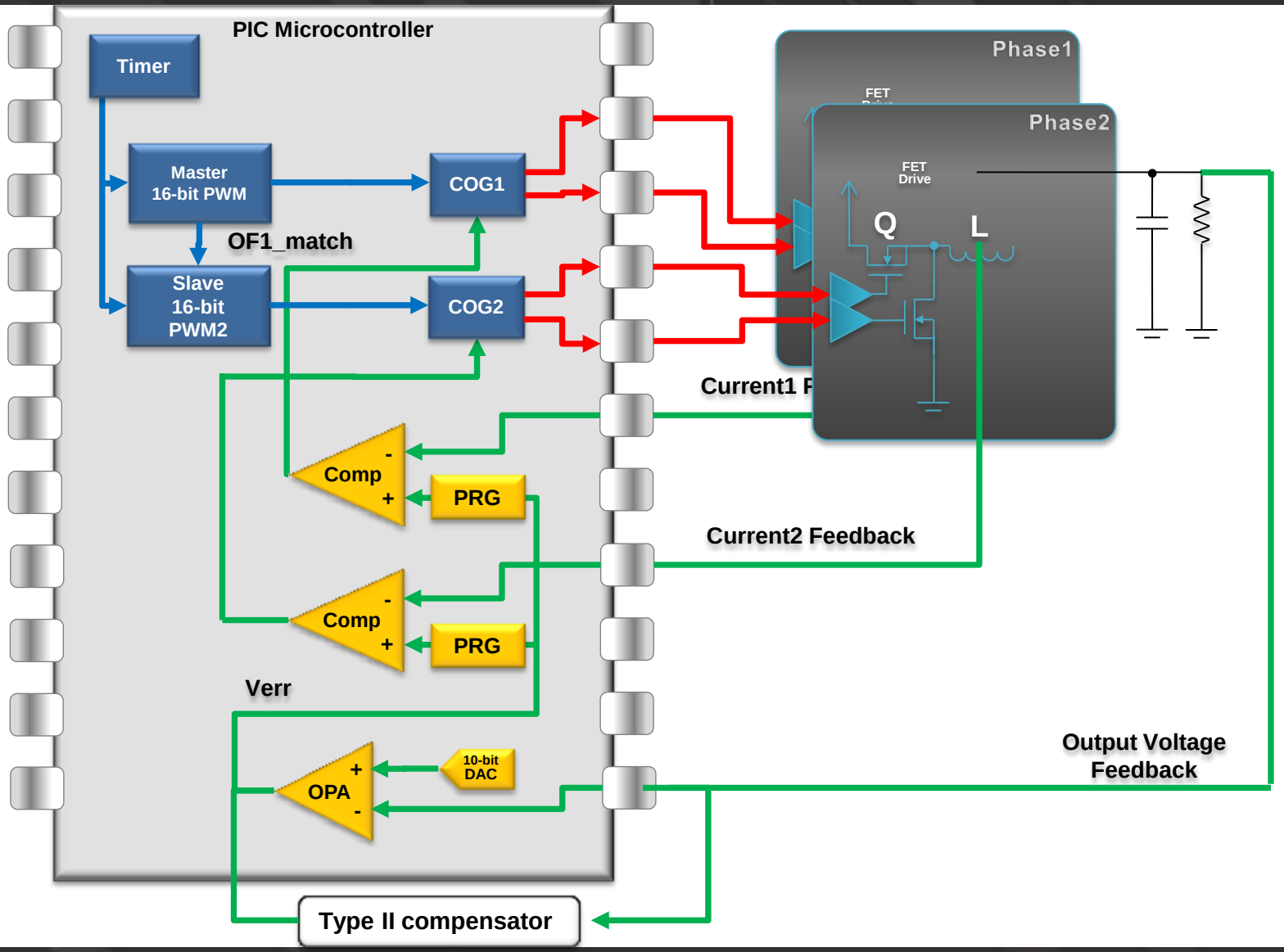
Interleaved topology



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16-bit PWM

- 16-bit PMW with Phase, duty cycle, period, and offset event controls
- Four modes of operation
  - Standard, Set on Match, Toggle on Match, Center Aligned
- Four offset modes
  - Independent, Slave run on Sync start, One-shot with Sync Start, Continuous run with Sync start & TMR reset

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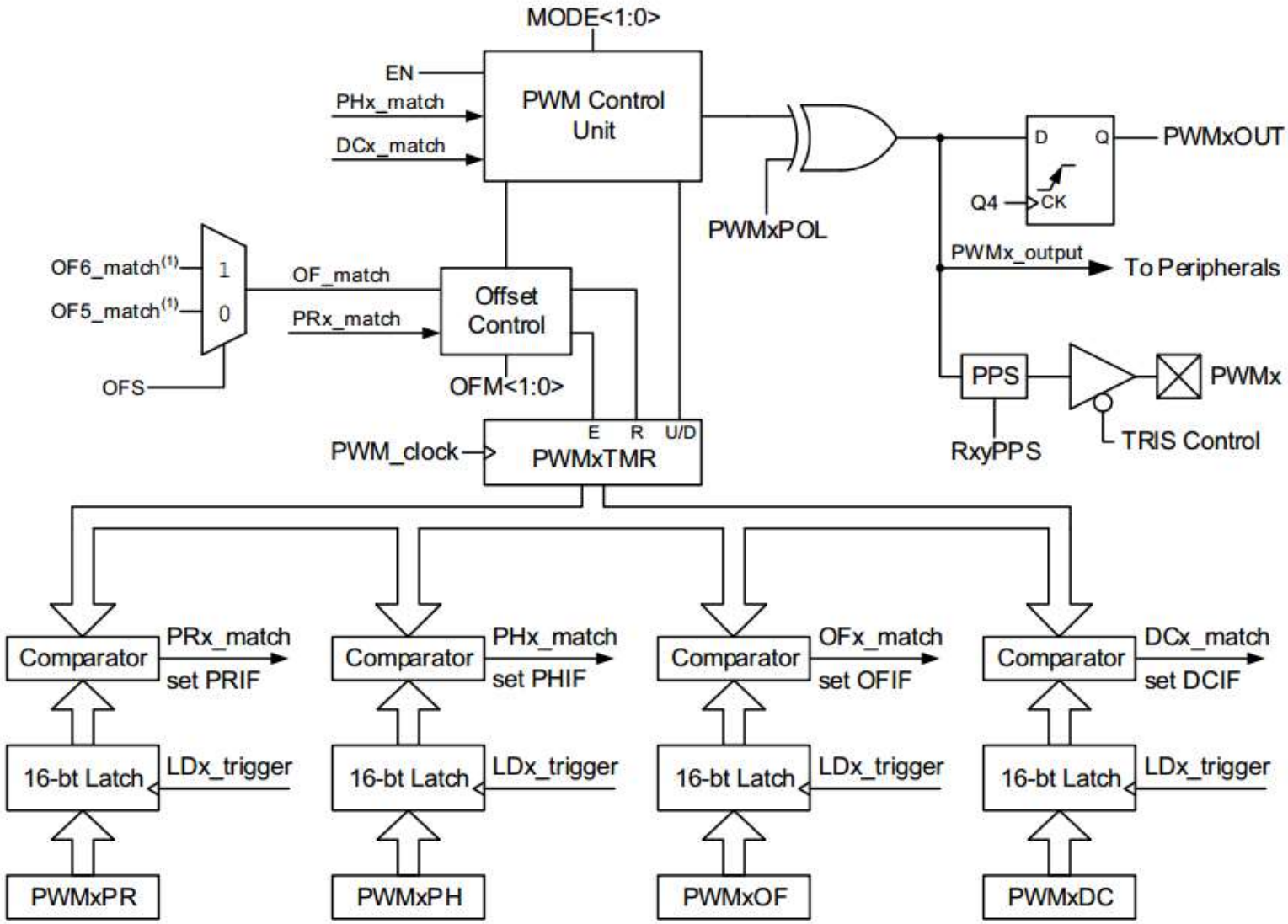
16-bit PWM



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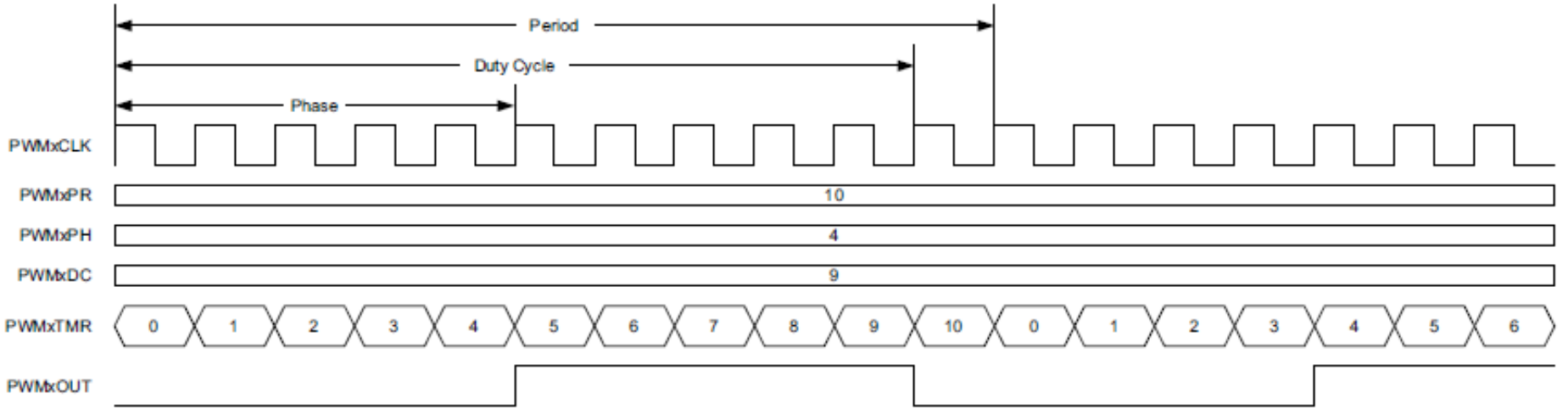
Operation Mode

- **Standard**



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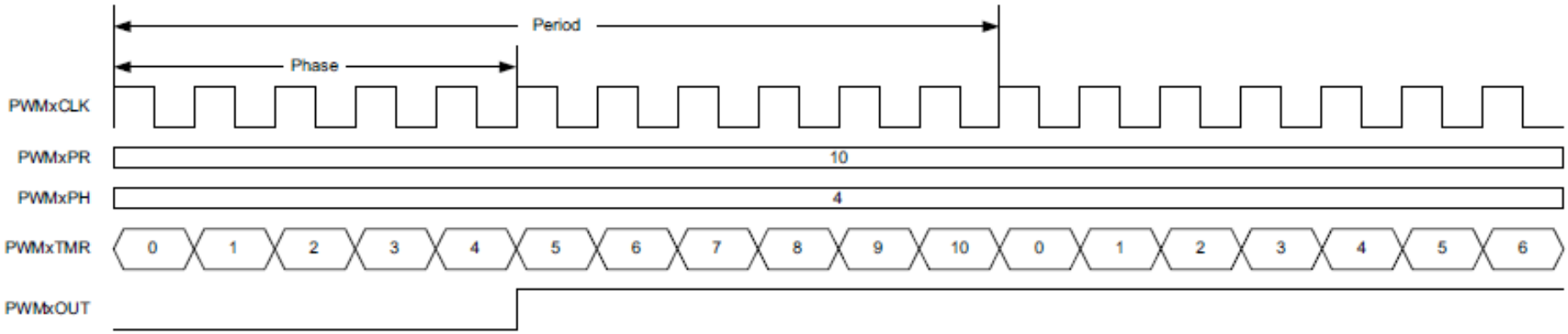
Operation Mode

- **Set on Match**



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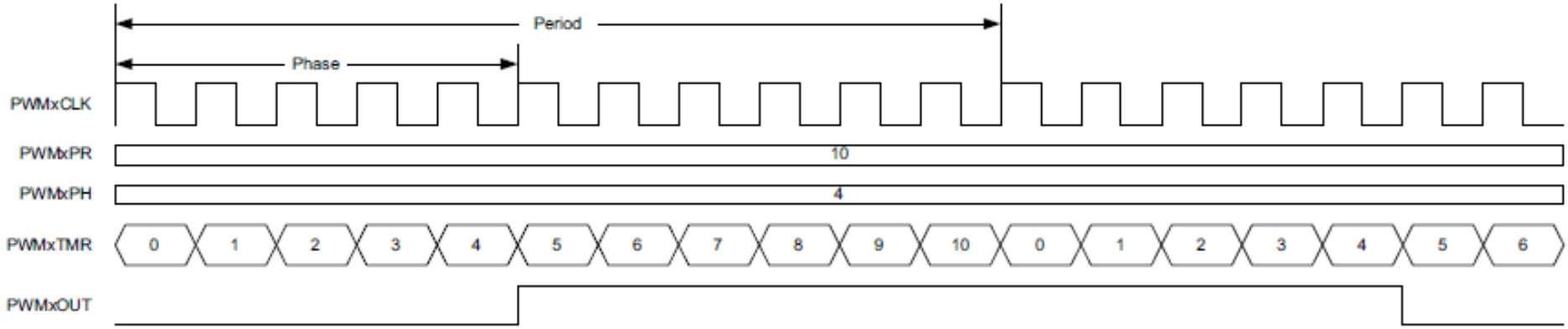
Operation Mode

- **Toggle on Match**



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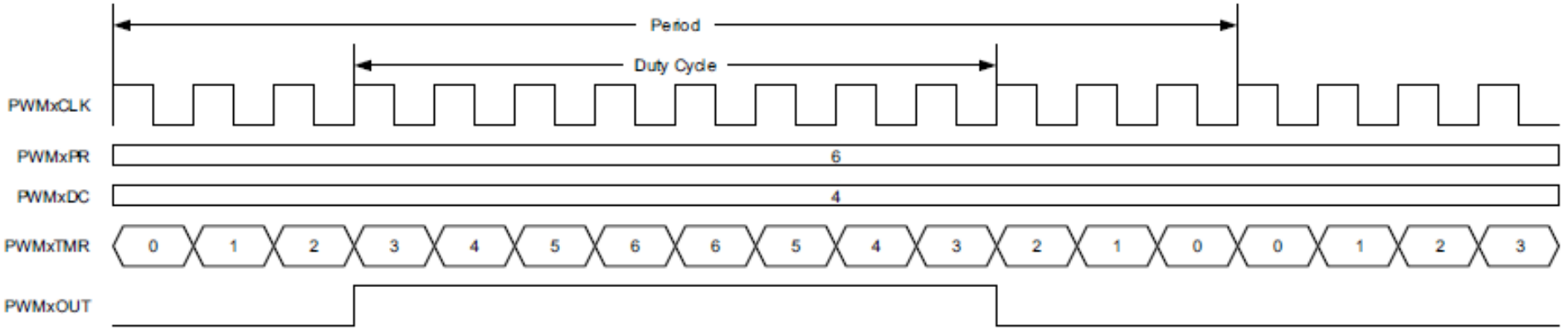
Operation Mode

- **Center Aligned**



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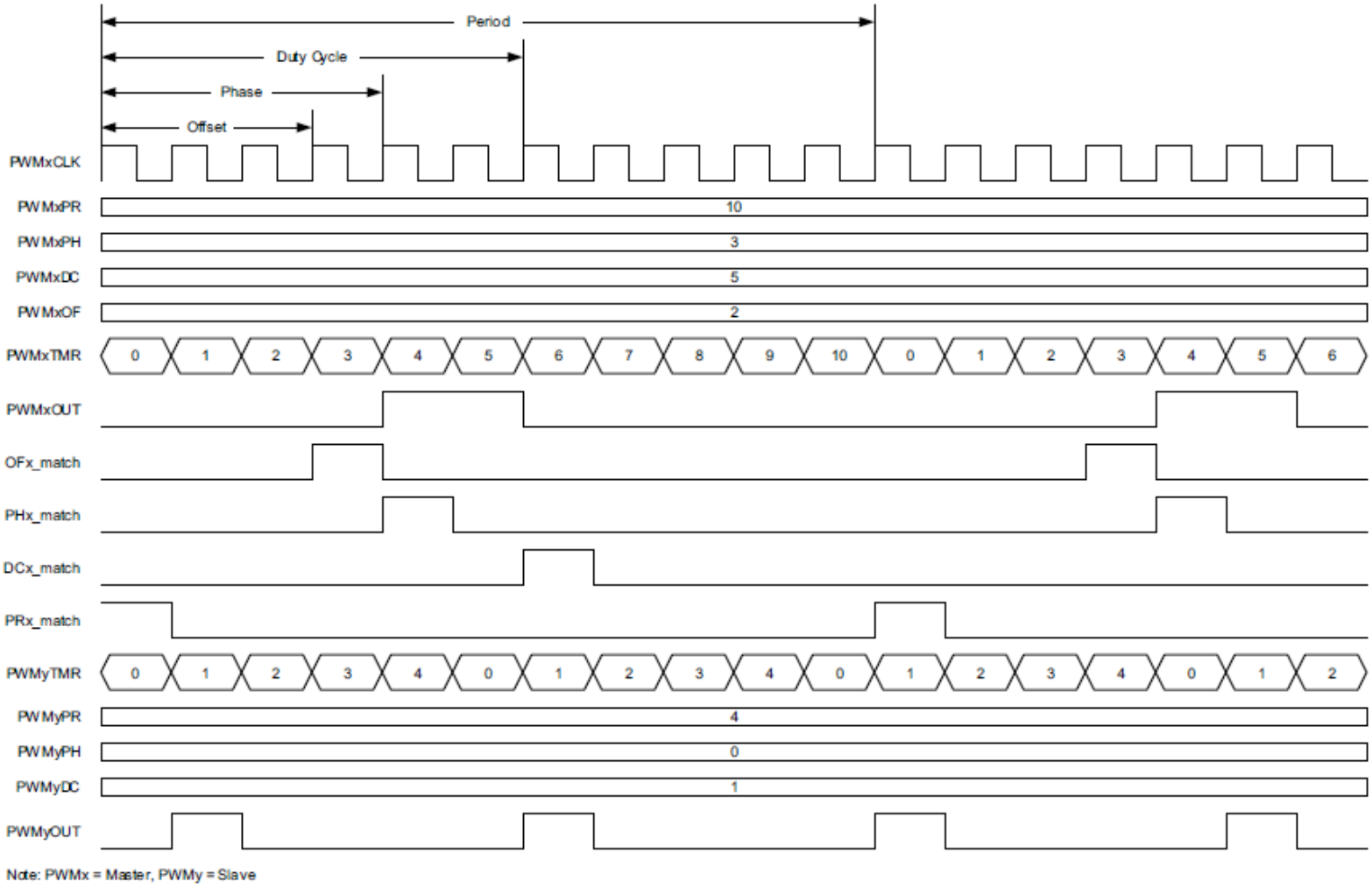
Offset Mode

- **Independent Run Mode**



Note: PWMx = Master, PWMy = Slave

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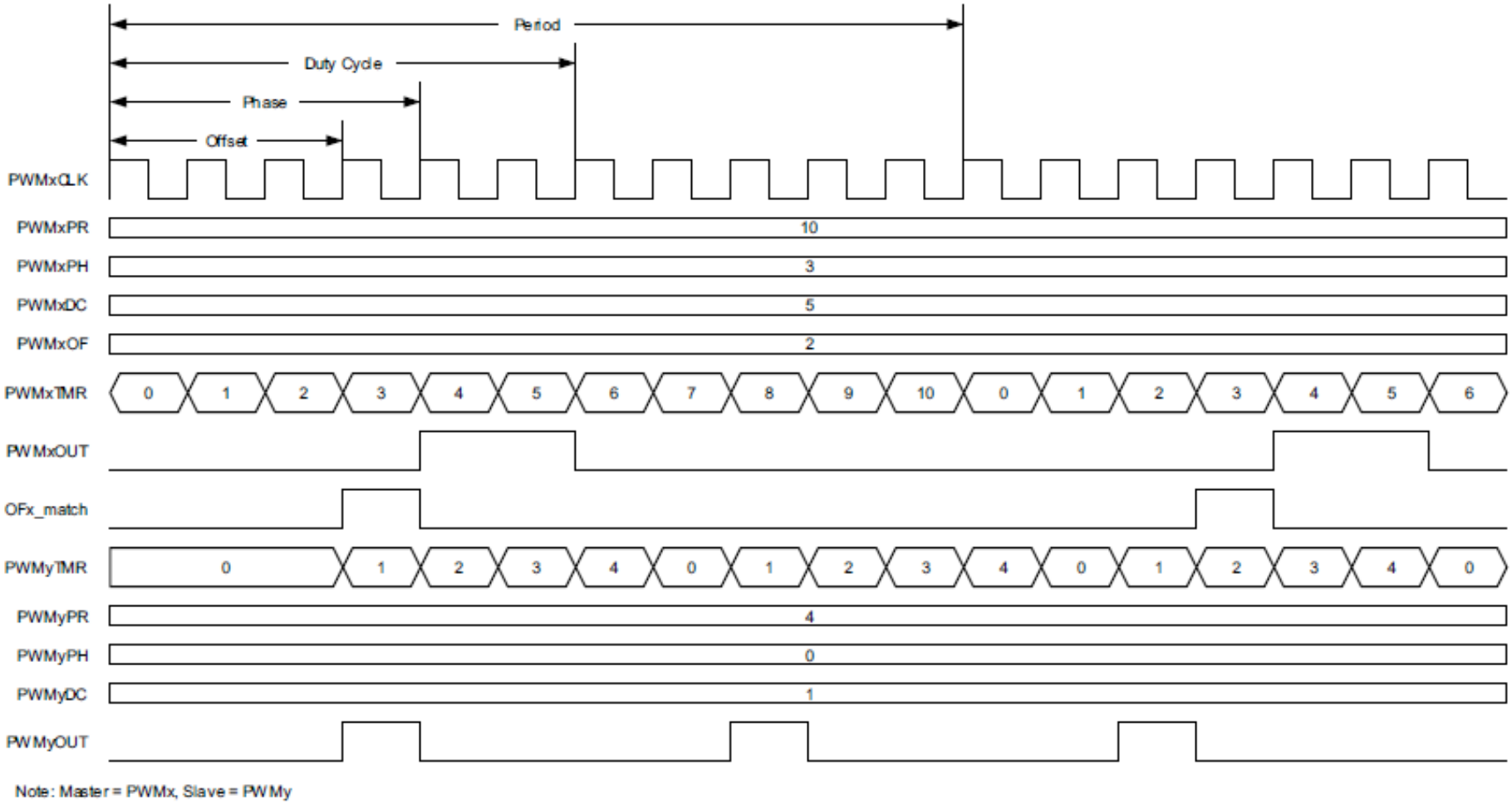
Offset Mode

- **Slave Run Mode with Sync Start**



Note: Master = PWMx, Slave = PWMy

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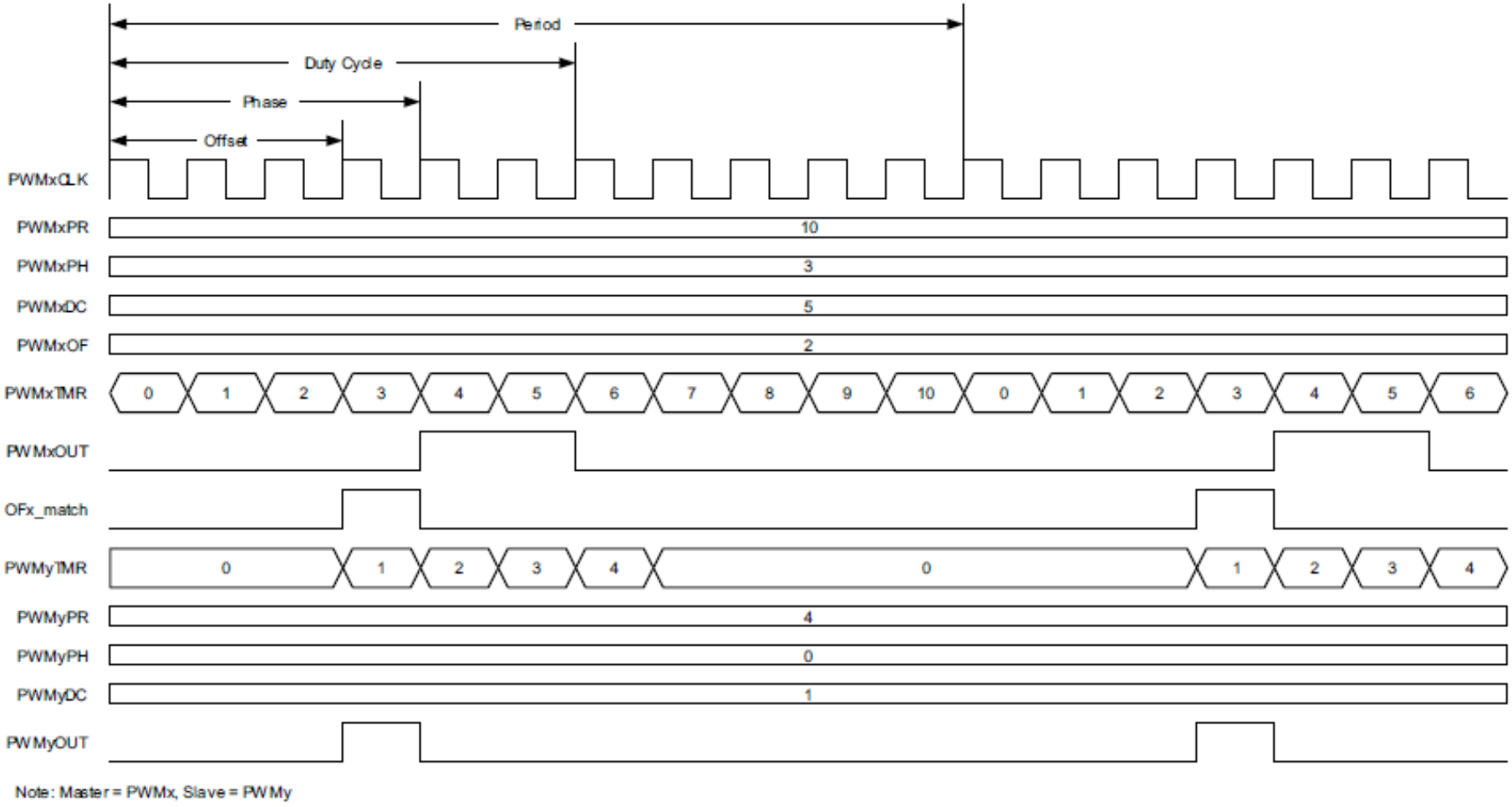
Offset Mode

- **One-Shot Slave Mode With Sync Start**



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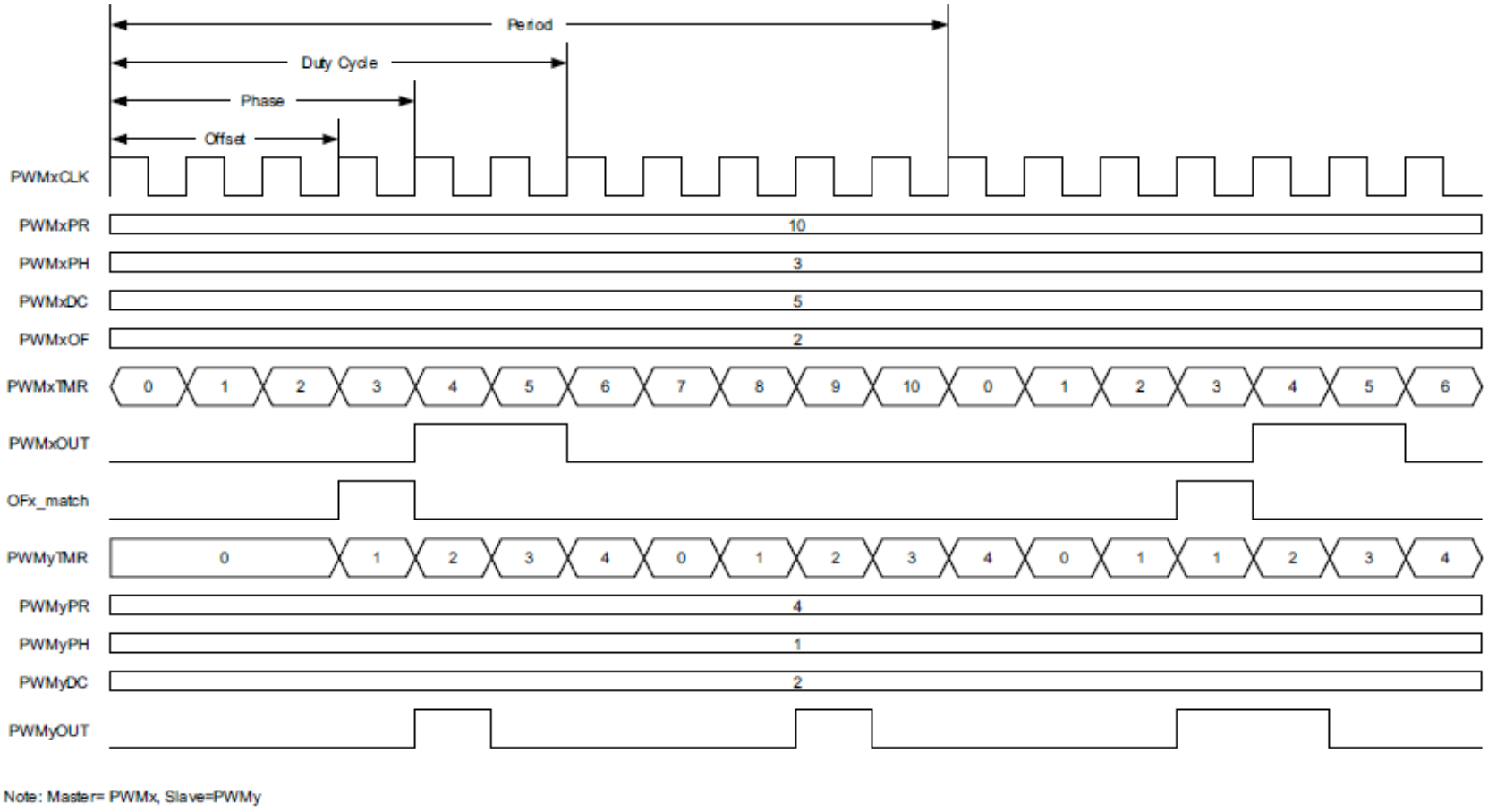
Offset Mode

- **Con. Run Slave Mode With Sync Start And Timer Reset**



Note: Master= PWMx, Slave=PWMy

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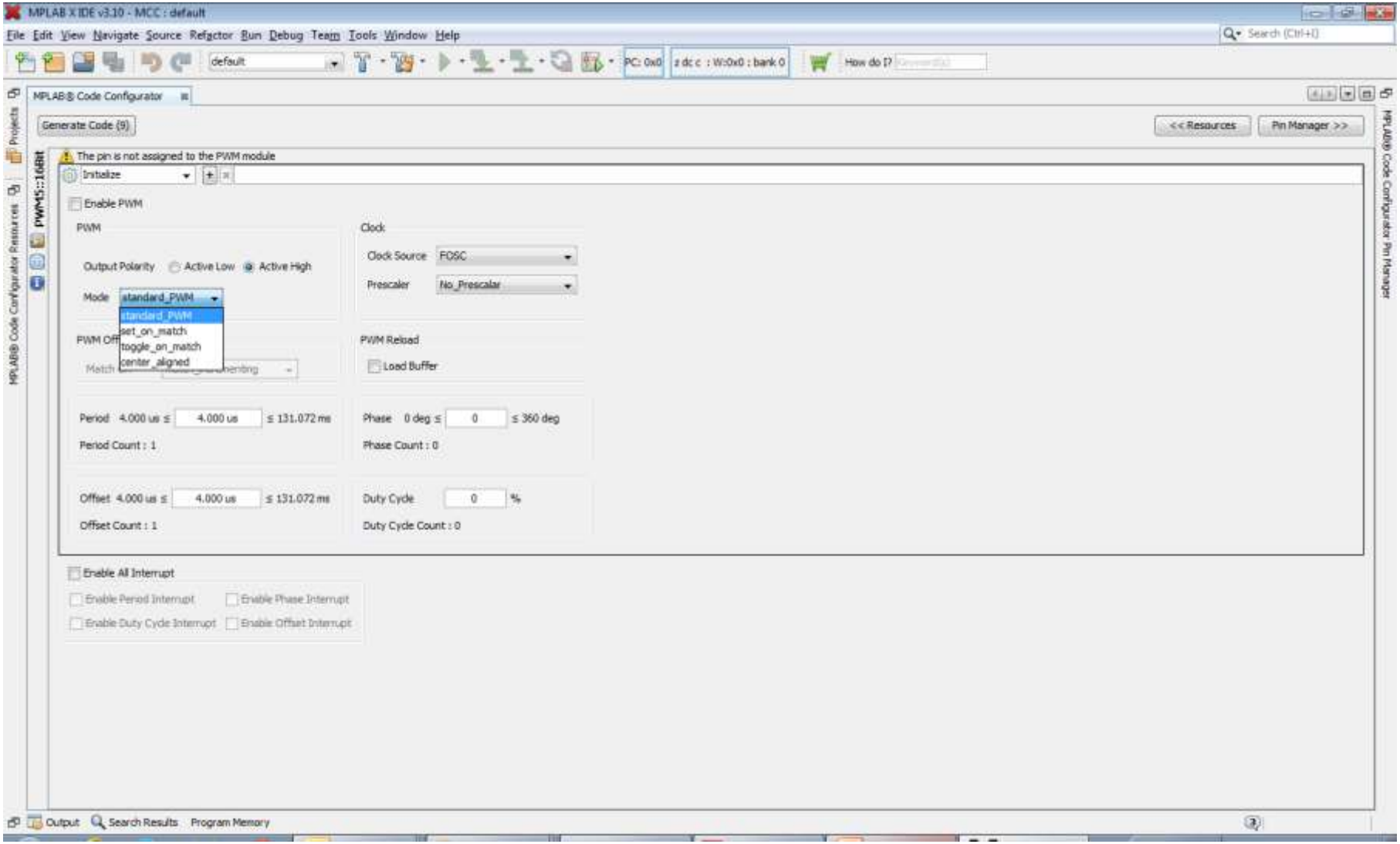
MCC – 16bit PWM



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The Power of Peripheral Pin Select

- Move functions
  - For improved layout
  - For improved noise isolation
- Switch drive peripherals on the fly
  - Add new digital connections
  - Generation of virtual test points
  - Swap output drivers for topology change
  - Move resources between SMPS channels

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Agenda

- Analog Design Review
  - Plant Transfer Function
  - Analyze stability & Design Compensator
- Analog control vs. full digital control
- Different topologies and control strategies using the core independent peripherals
- **Protection functions examples**
- Summary

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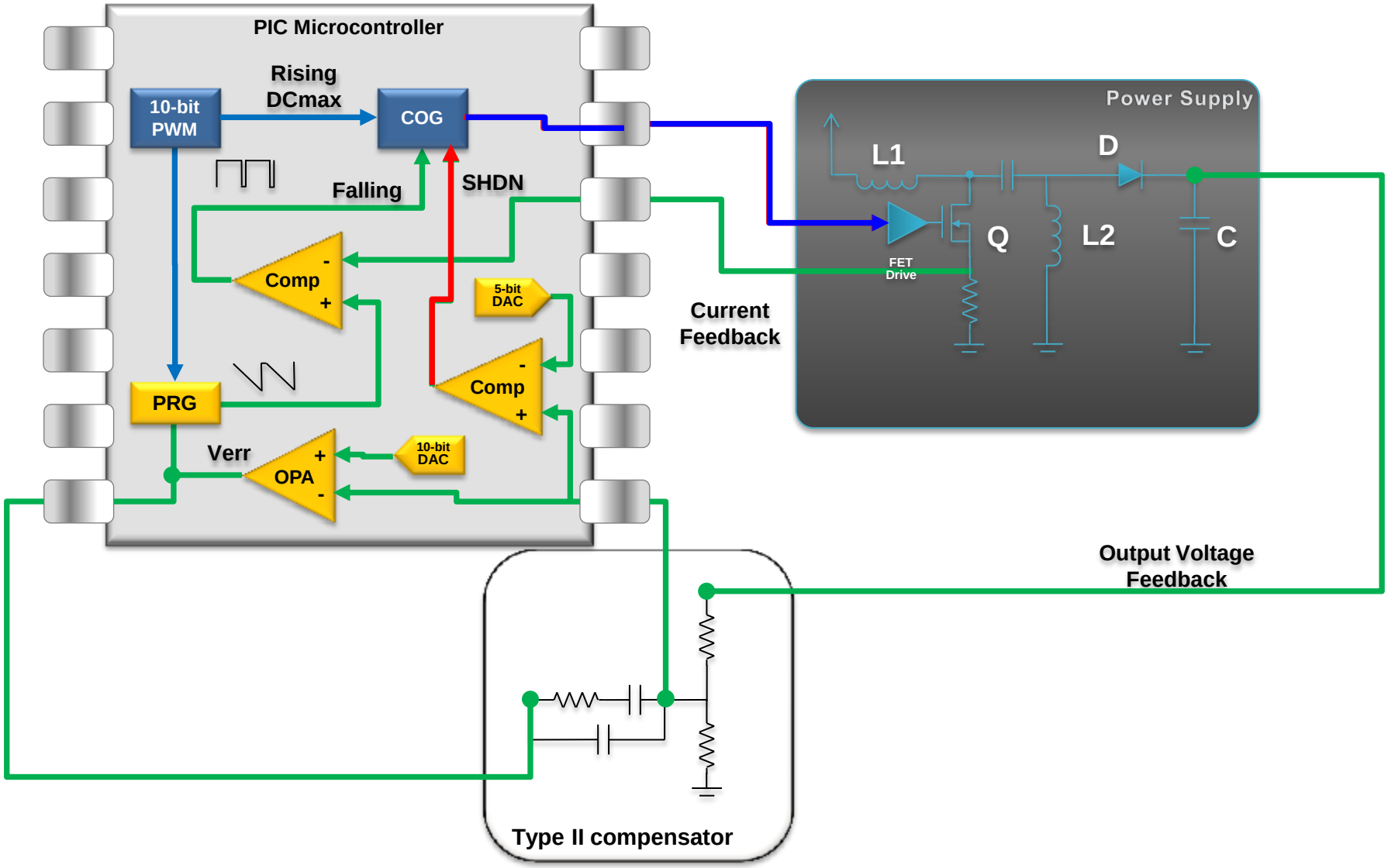
Output Over Voltage



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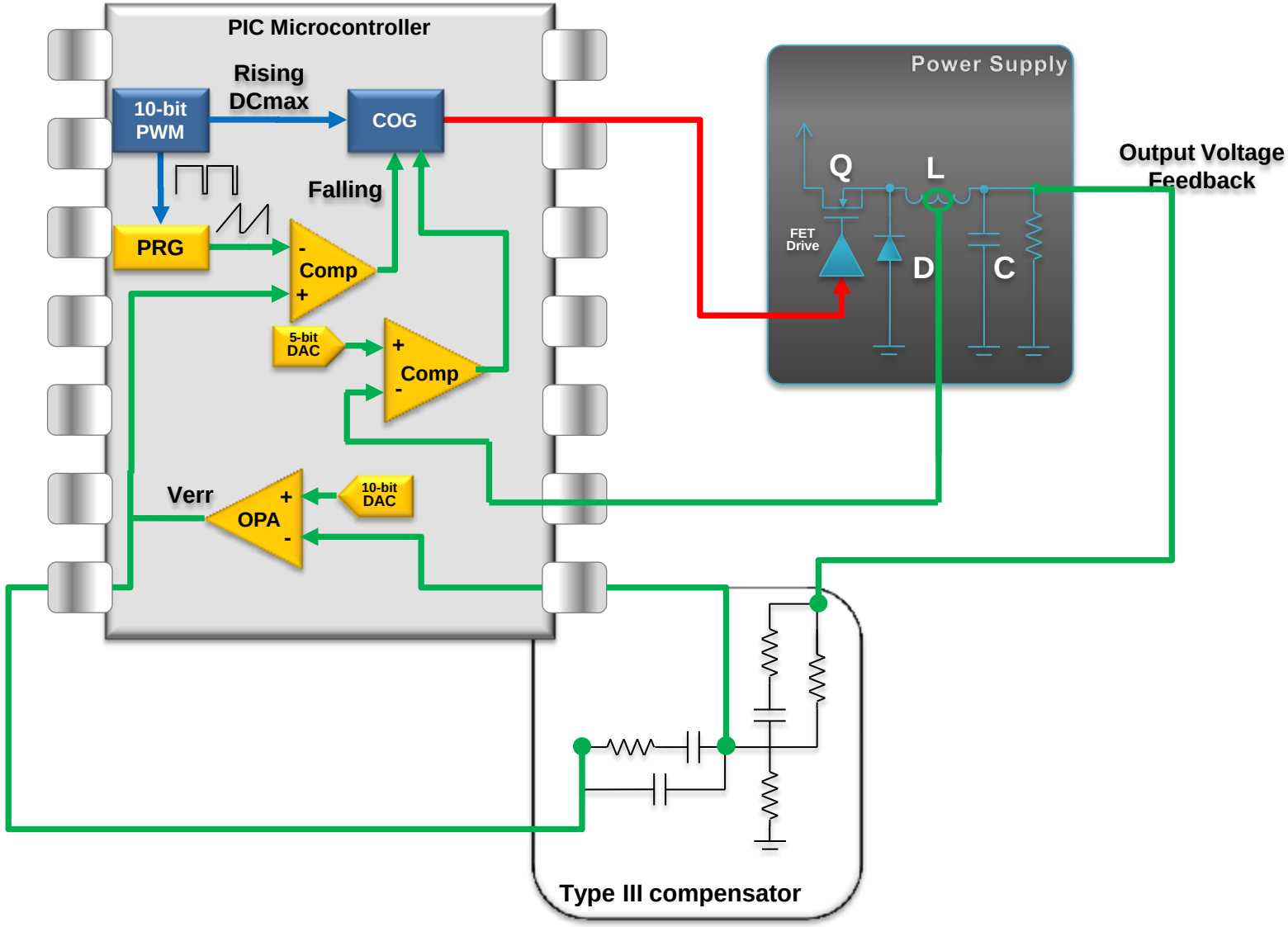
Max Current Limit Voltage Mode



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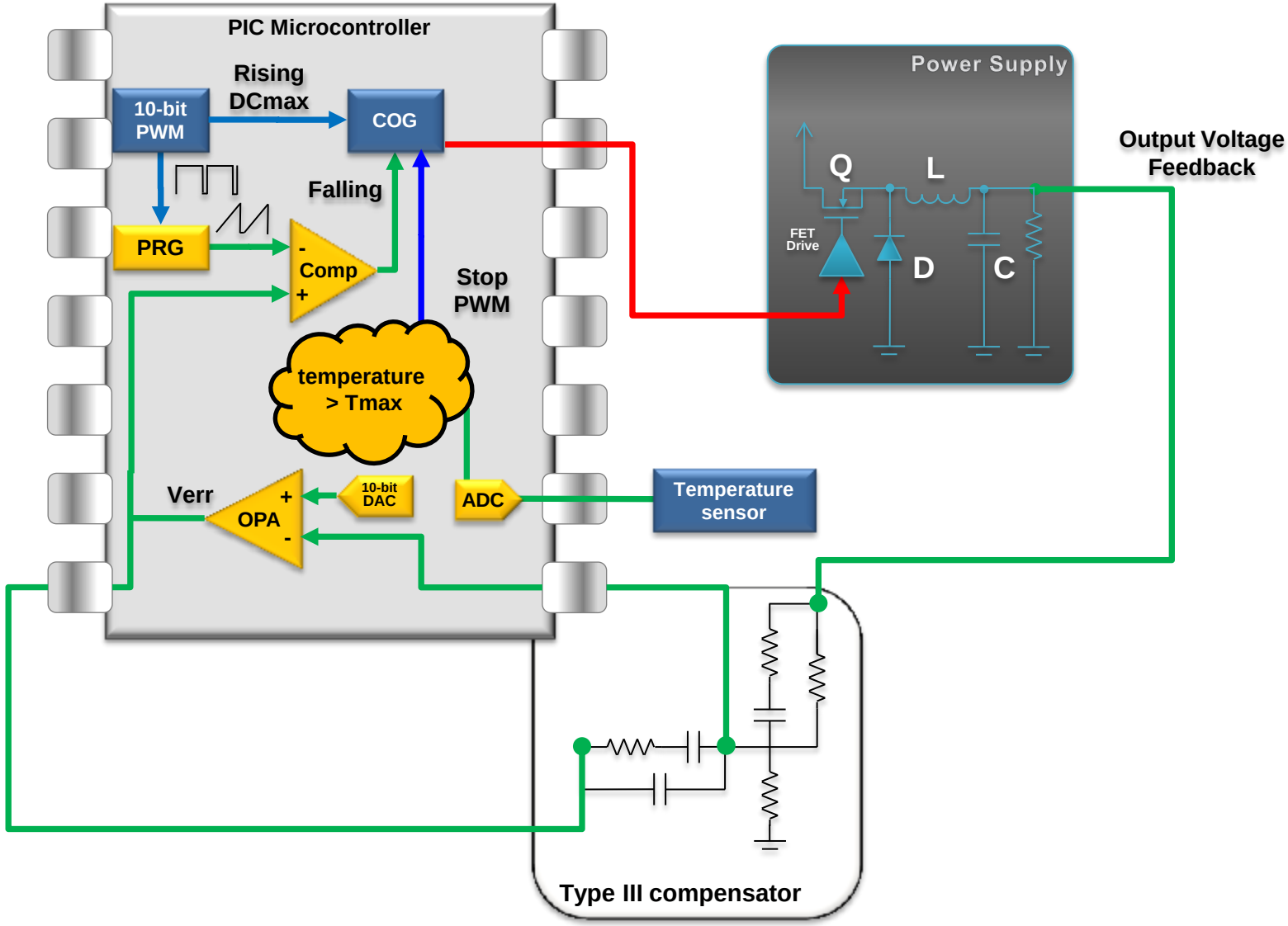
Over Temperature Shutdown



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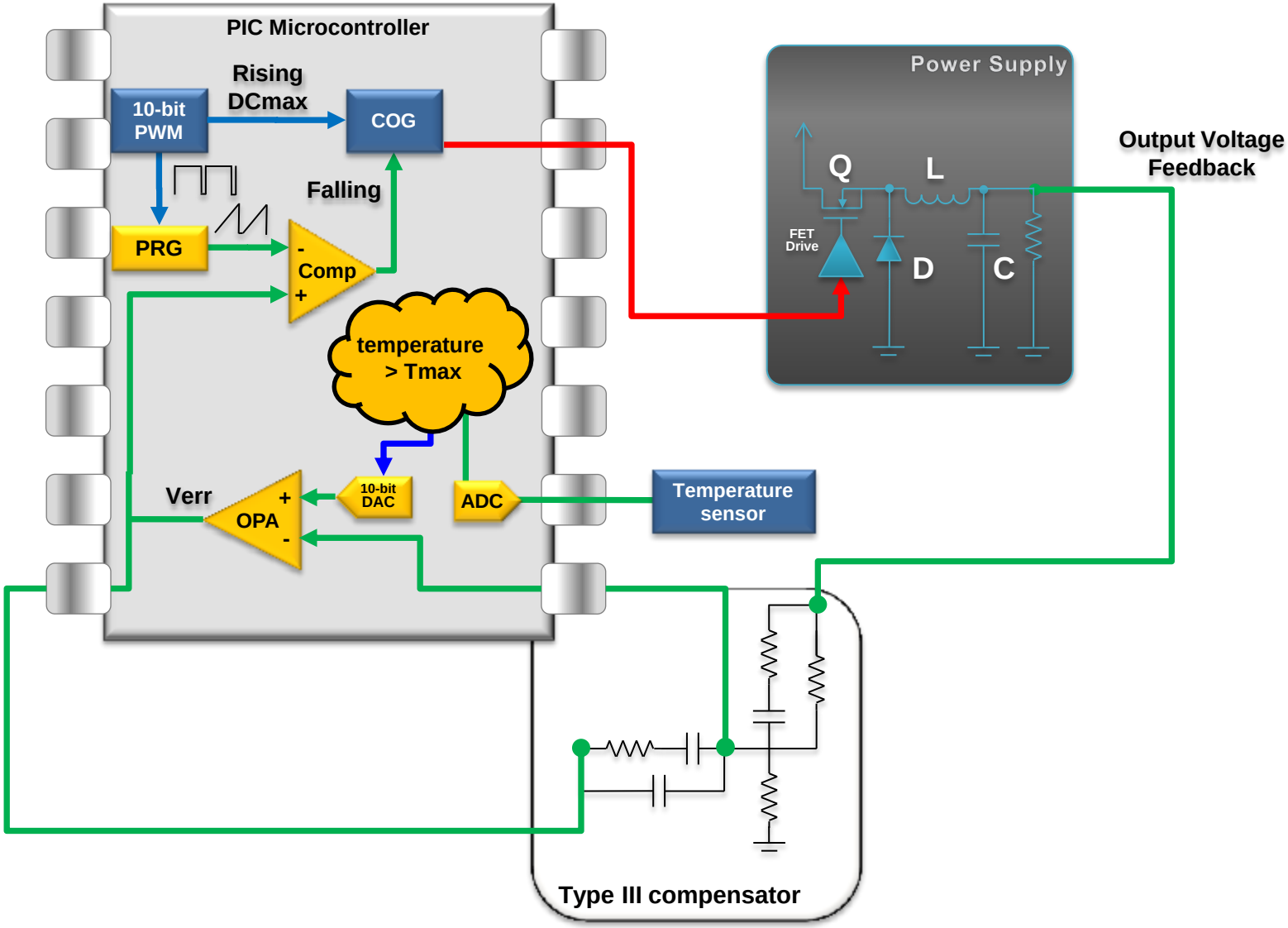
Over Temperature Derating



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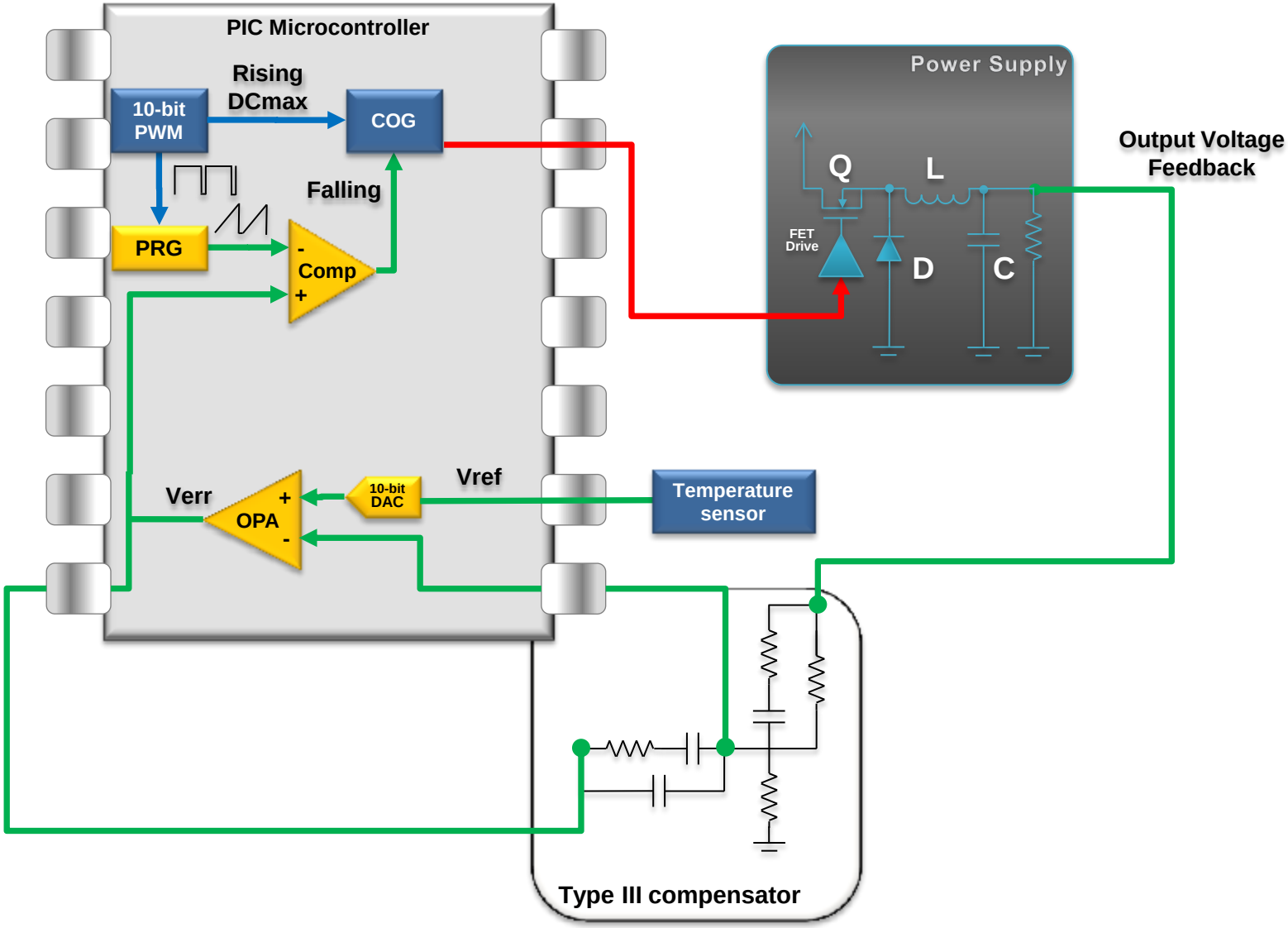
Over Temperature Derating



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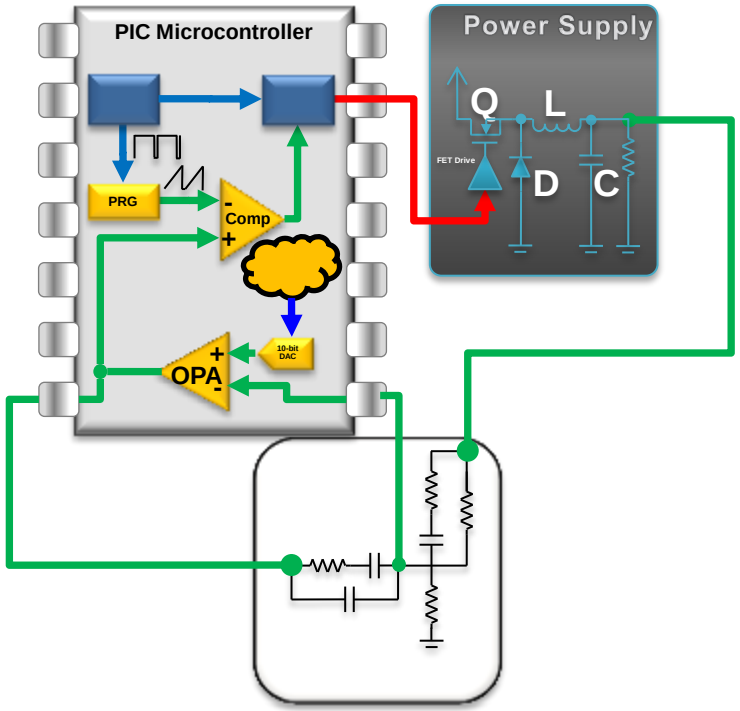
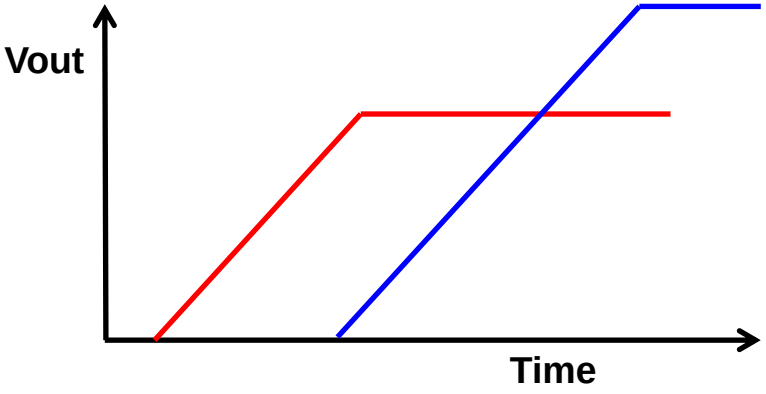
Soft-Start – Power sequencing

- DAC is set to a value very close to 0
- The control loop is turned on
- Using a timer or just a for loop, DAC is slowly increased up to the reference value





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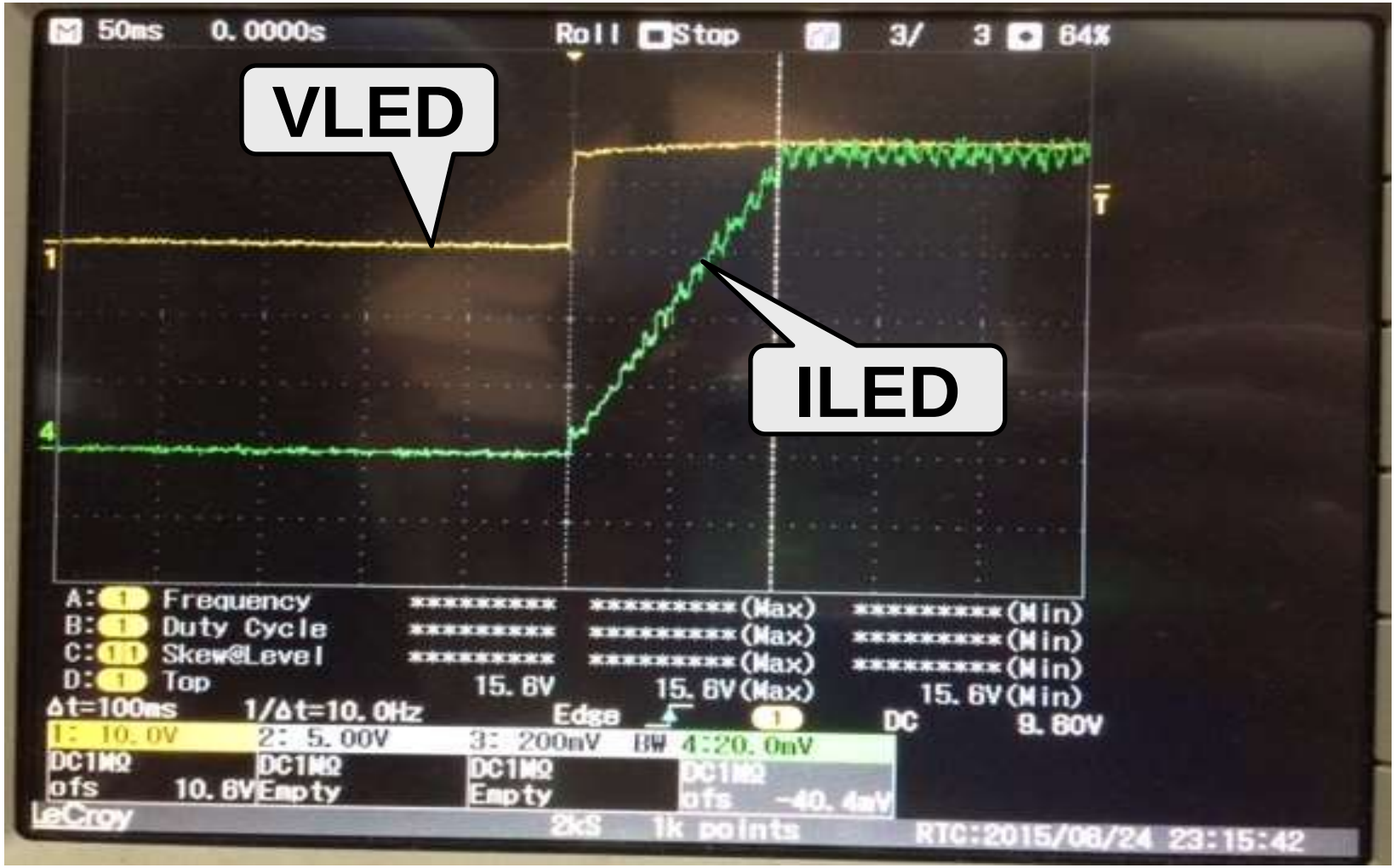
Soft-Start – LED Current



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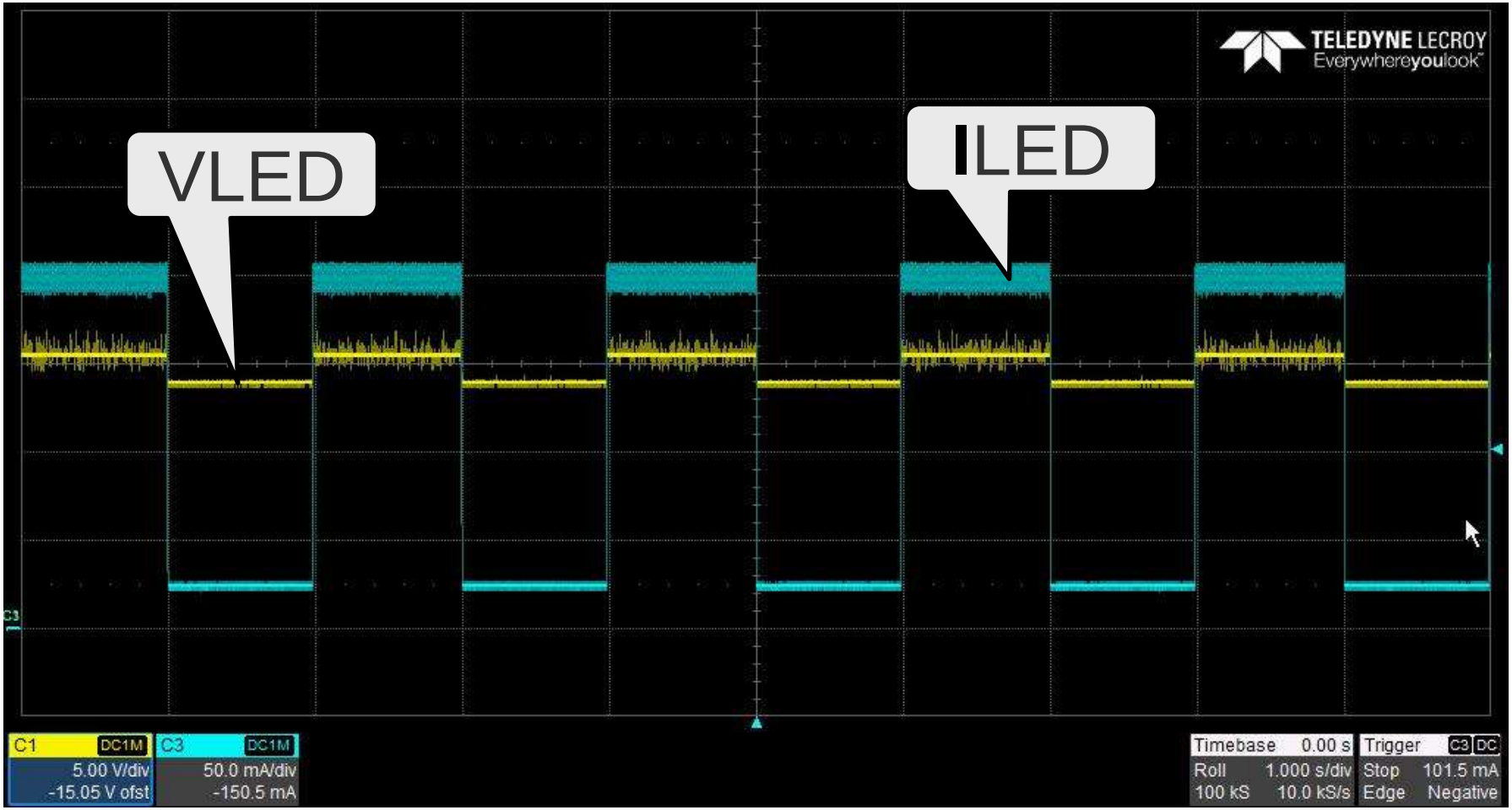
Dimming Control



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Frequency Dithering

- Timer 0 generates a periodic interrupt
- On the interrupt a pseudo random number is generated
- The random number is loaded into the OSCTUNE register

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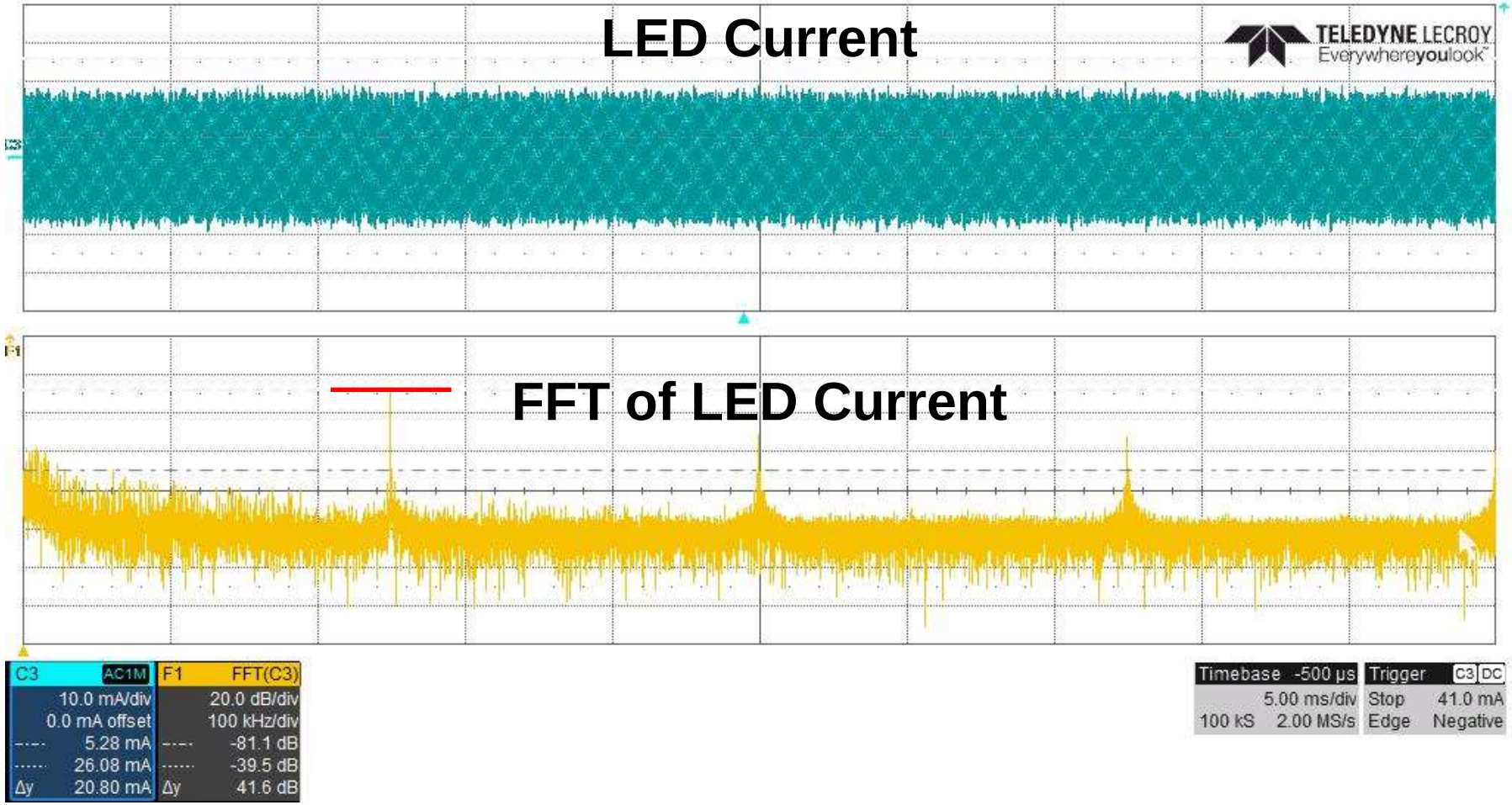
Frequency Dithering

On Board Testing without PWM Dithering



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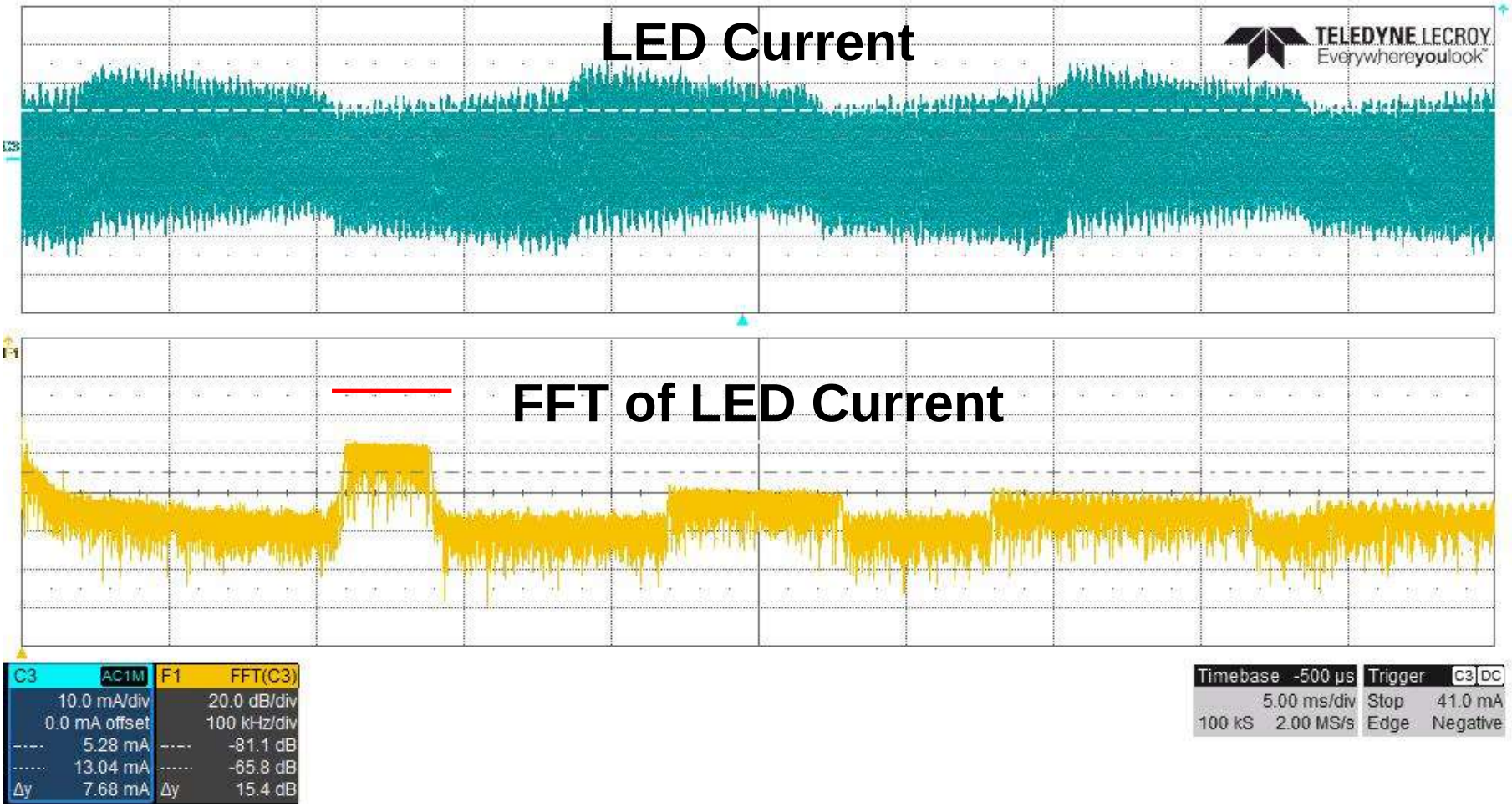
Frequency Dithering

On Board Testing with PWM Dithering



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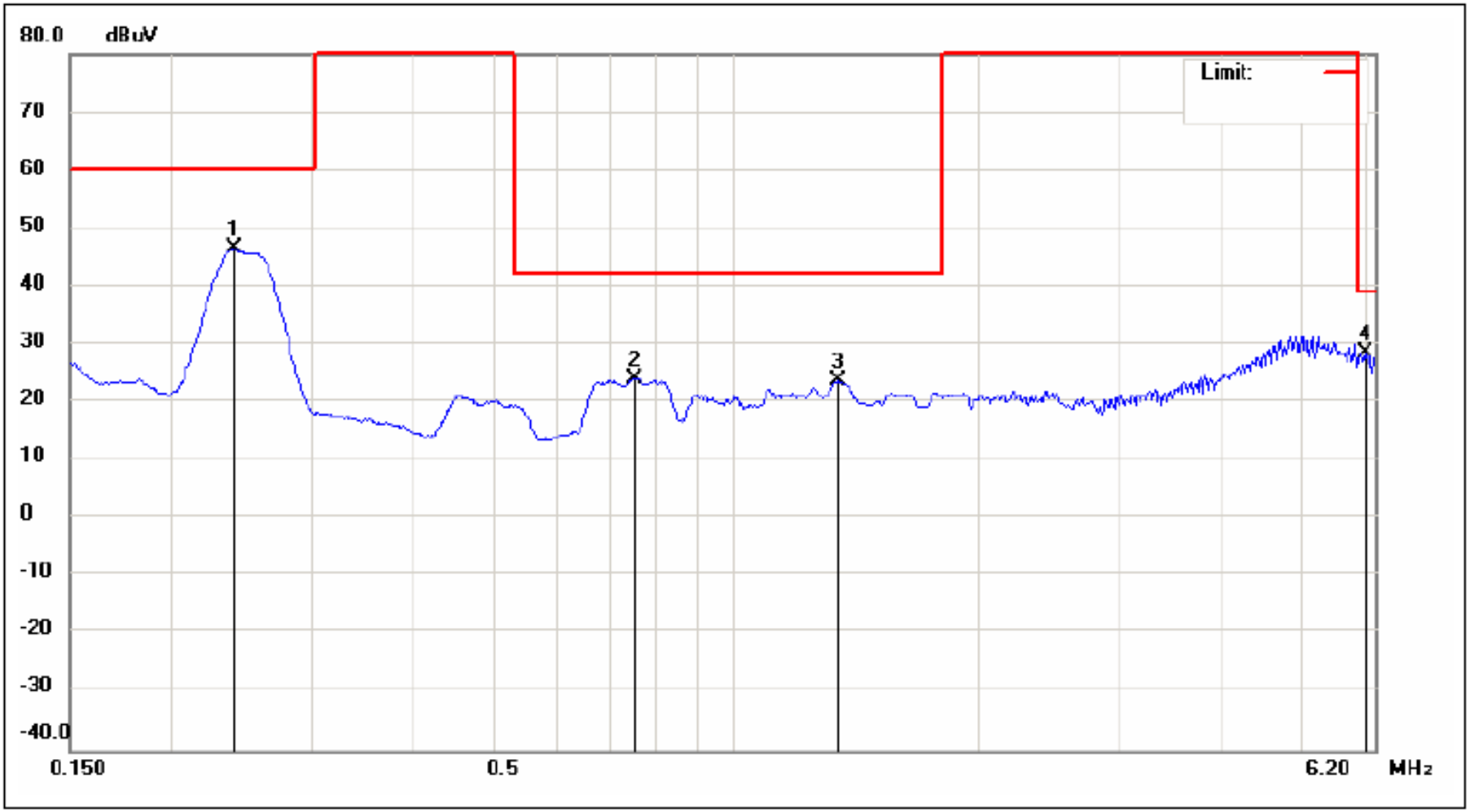
Frequency Dithering



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Monitoring Performance

- 10-bit ADC with connections to all of the analog signals
- Comparator interrupts on change
- Timer 1 gate for measuring pulse width, duty cycle, event timing
- 8-bit processor with advanced PIC16F1XXX processor
  - Enhanced instruction set for data manipulation

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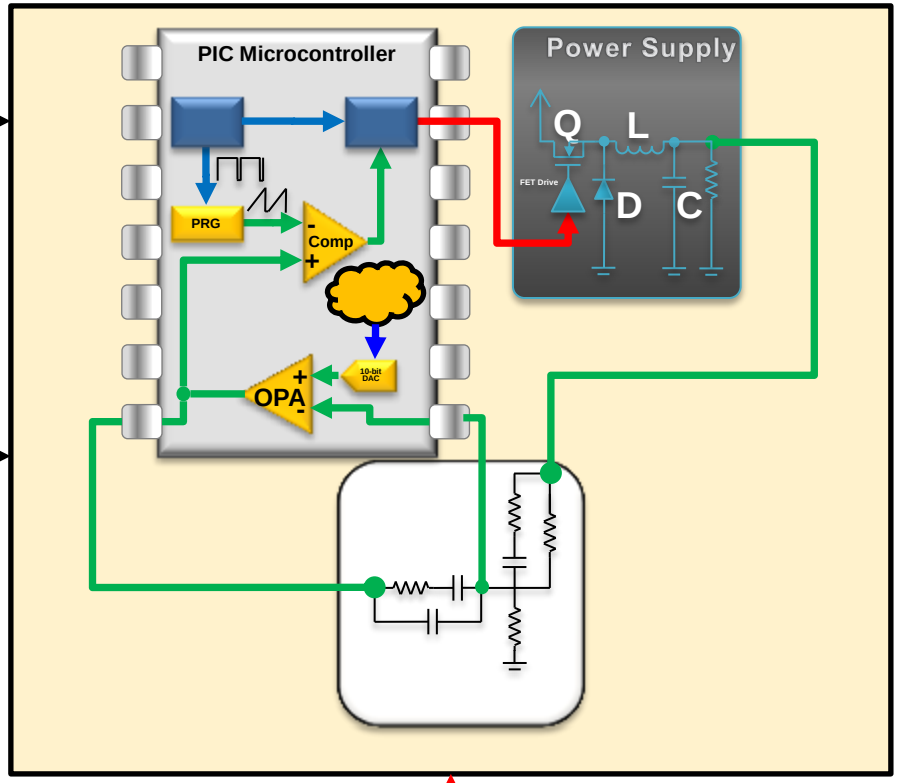
User interface - Communication

I/Os

AN INs



IOs/UART/I2C-PMBus…

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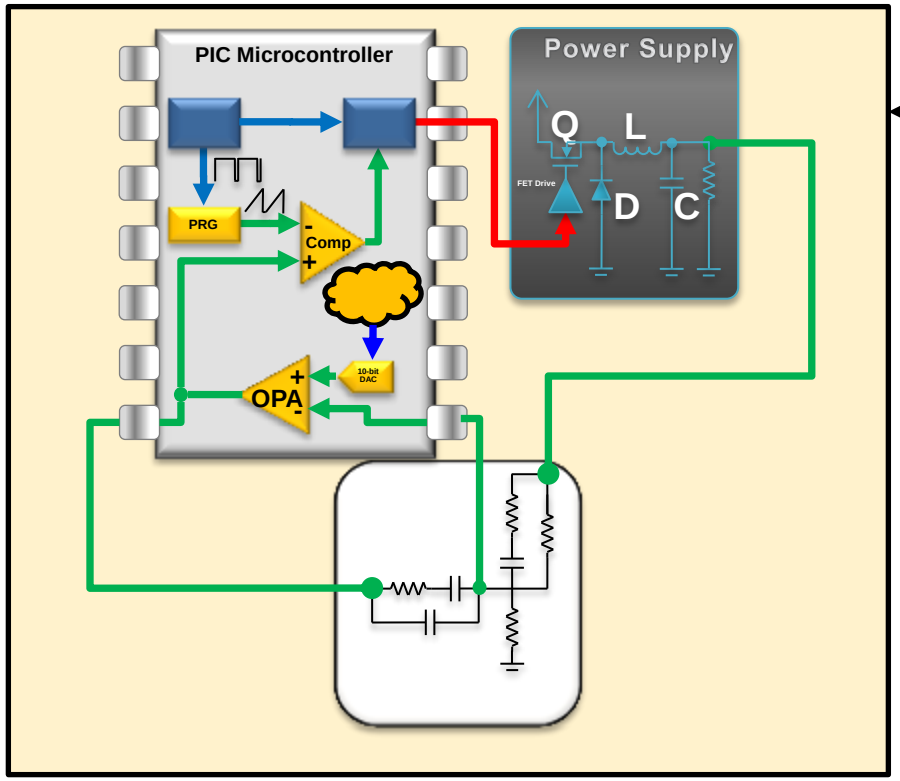
User interface - Communication



UART

WiFi / Bluetooth

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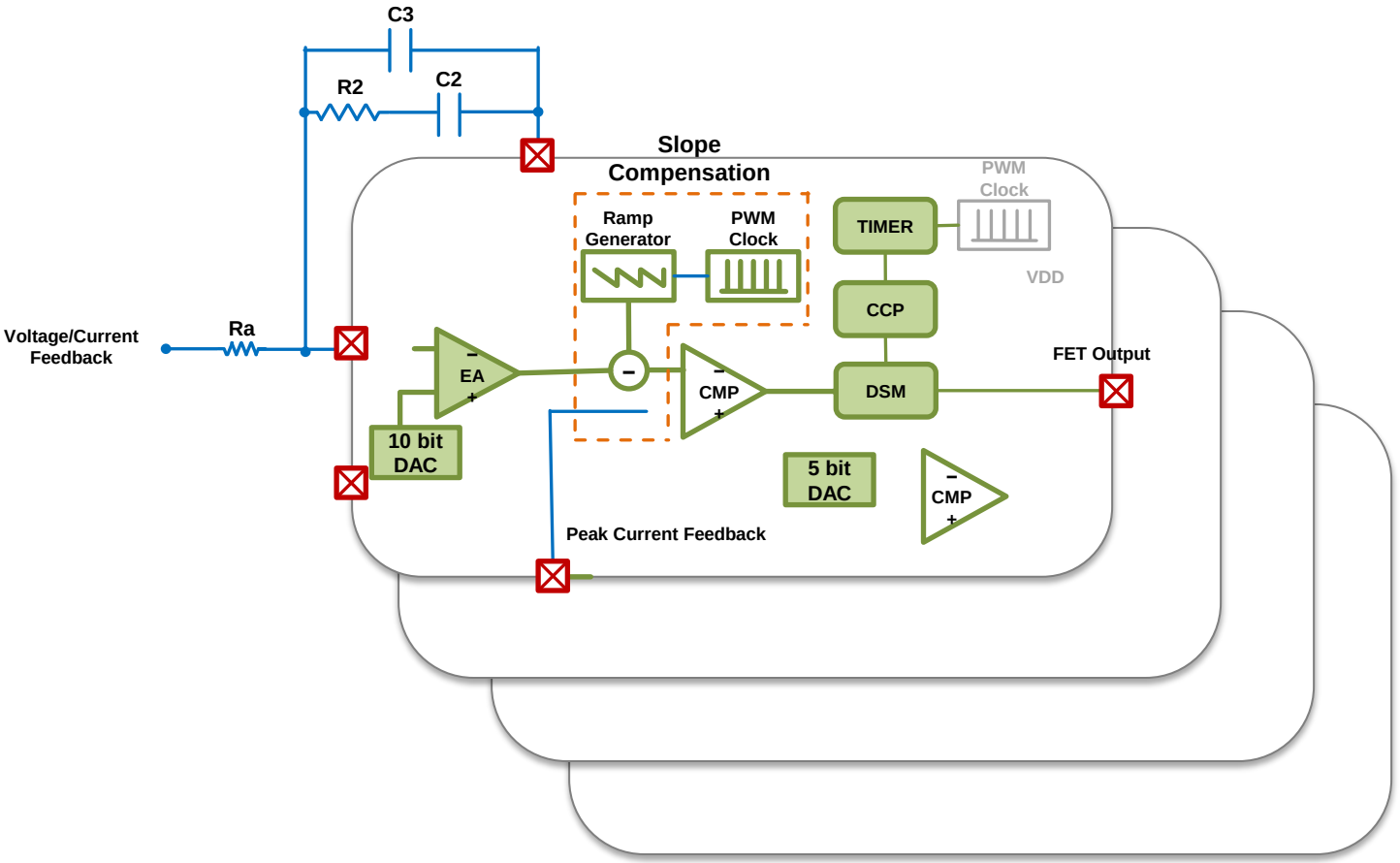
1,2,3 and 4 Channel Drive



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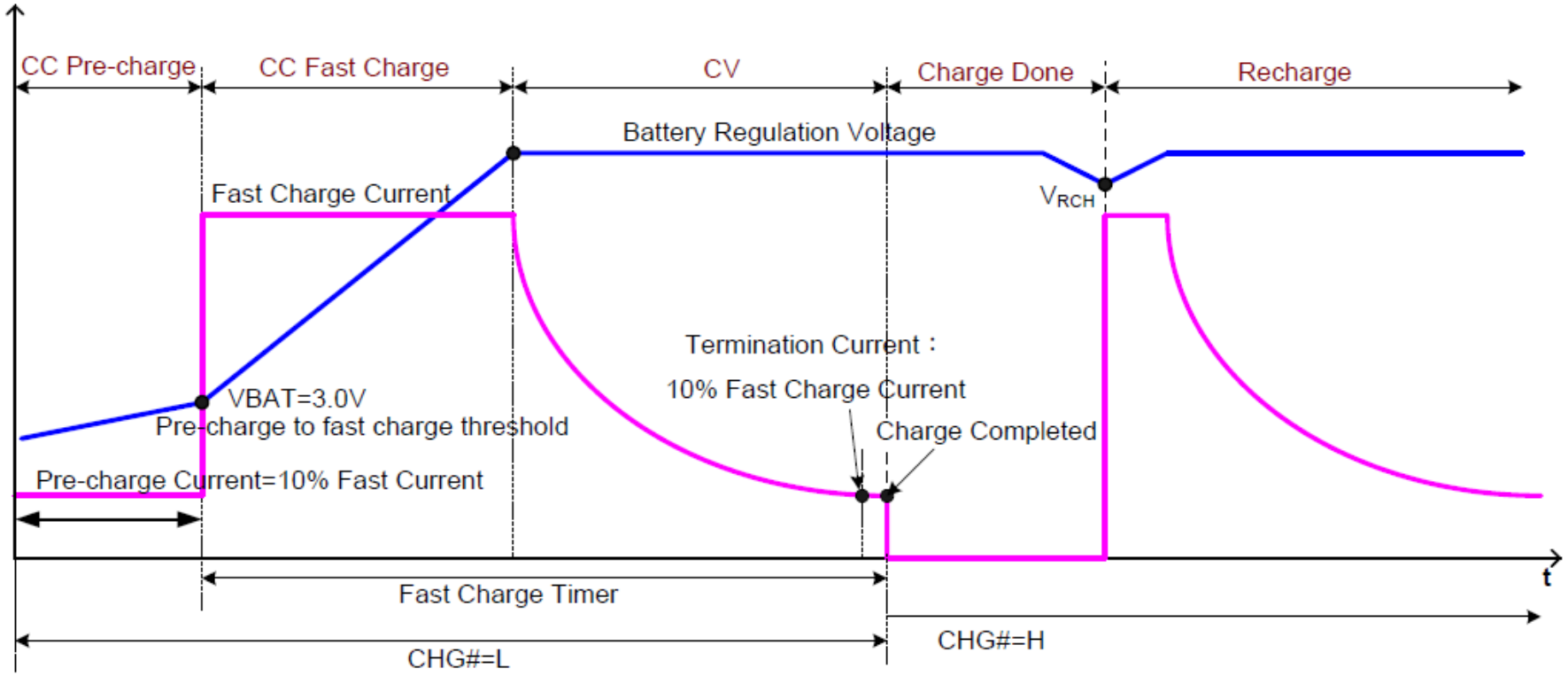
Battery Charger Application



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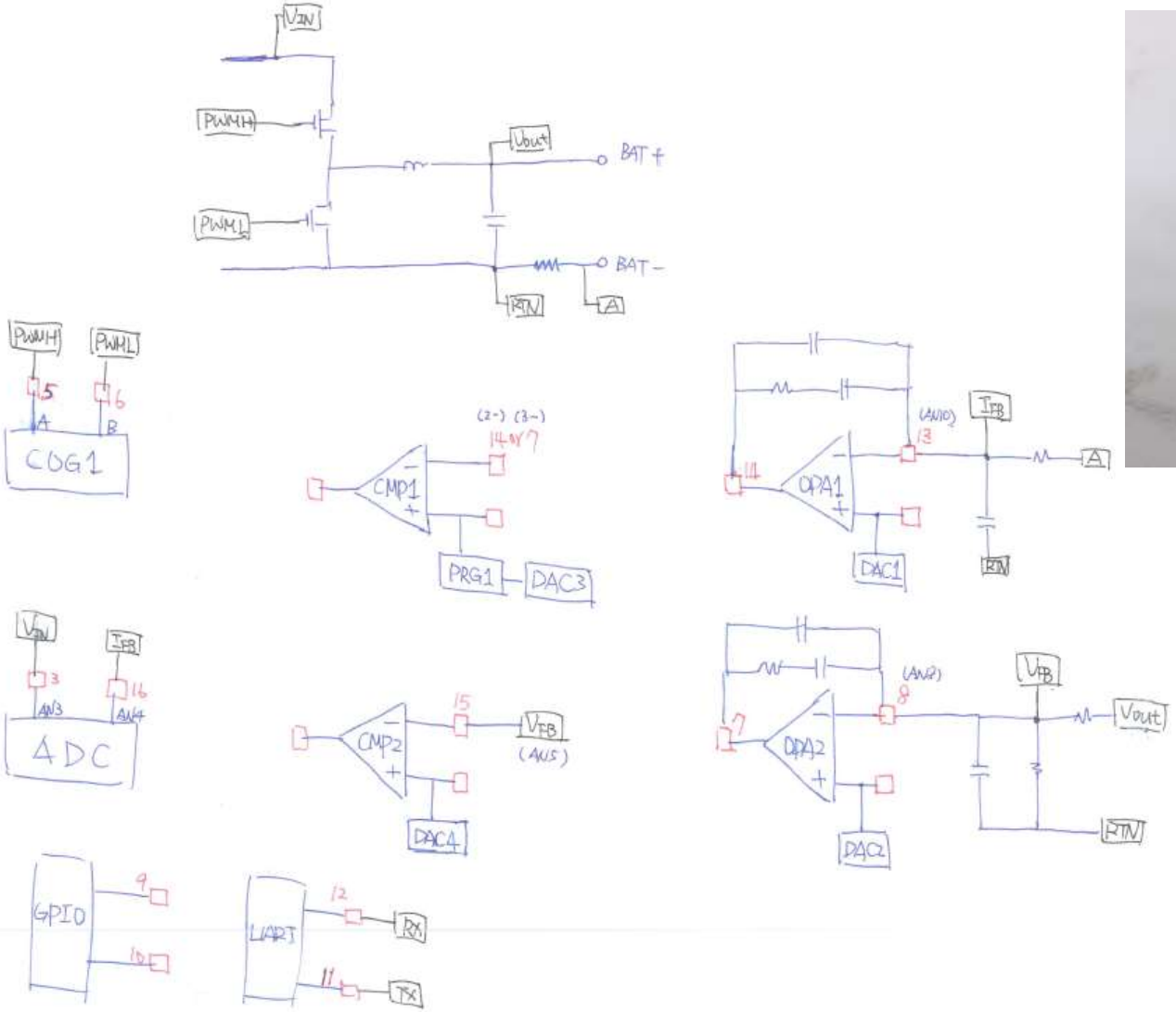
CIP Block Diagram



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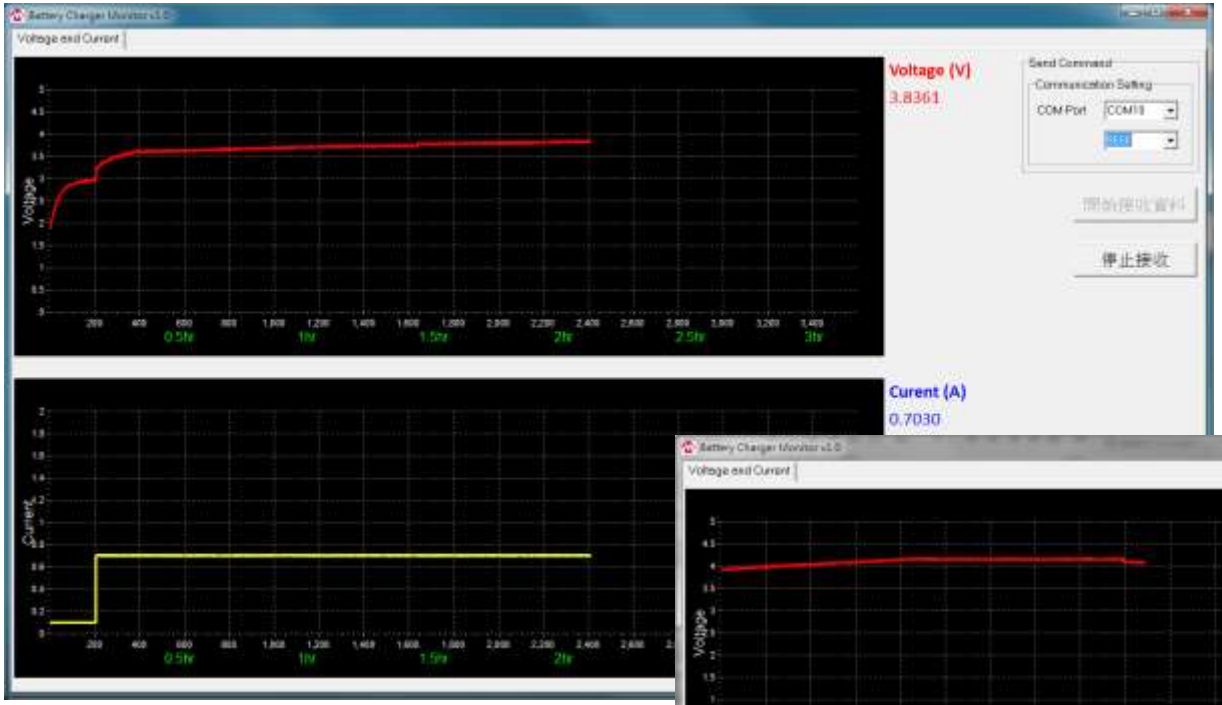
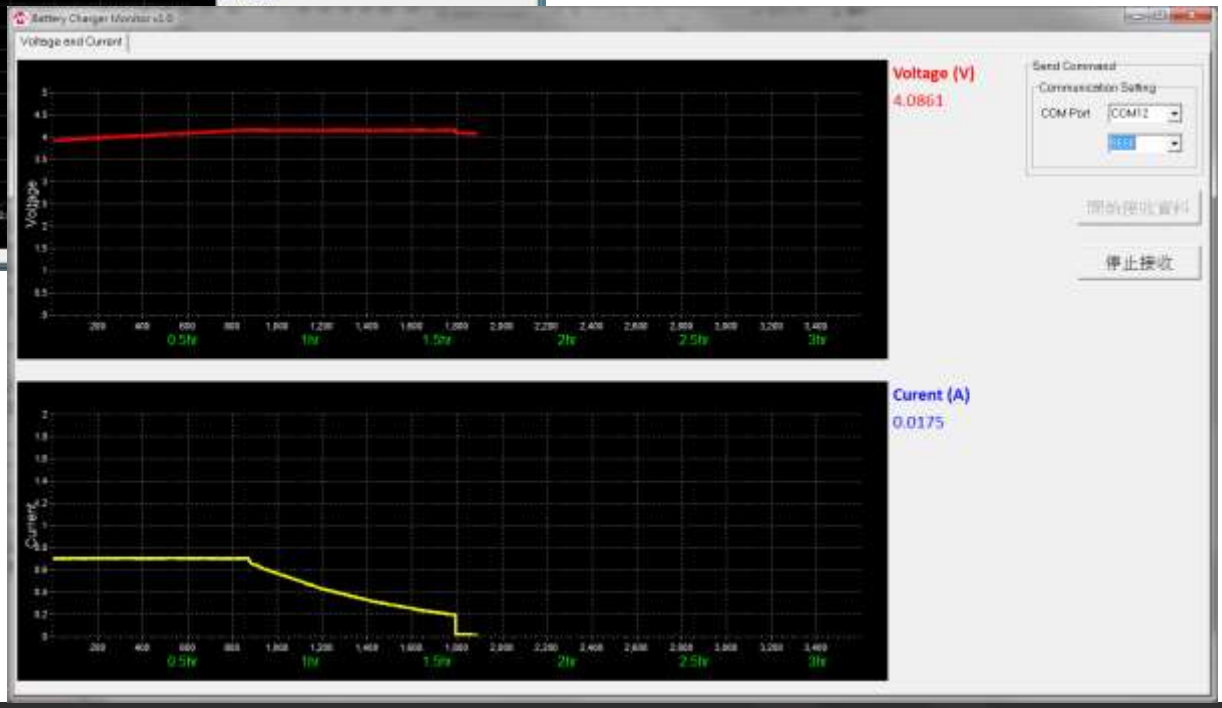
Charger Test Waveform



CC to CV.MOV



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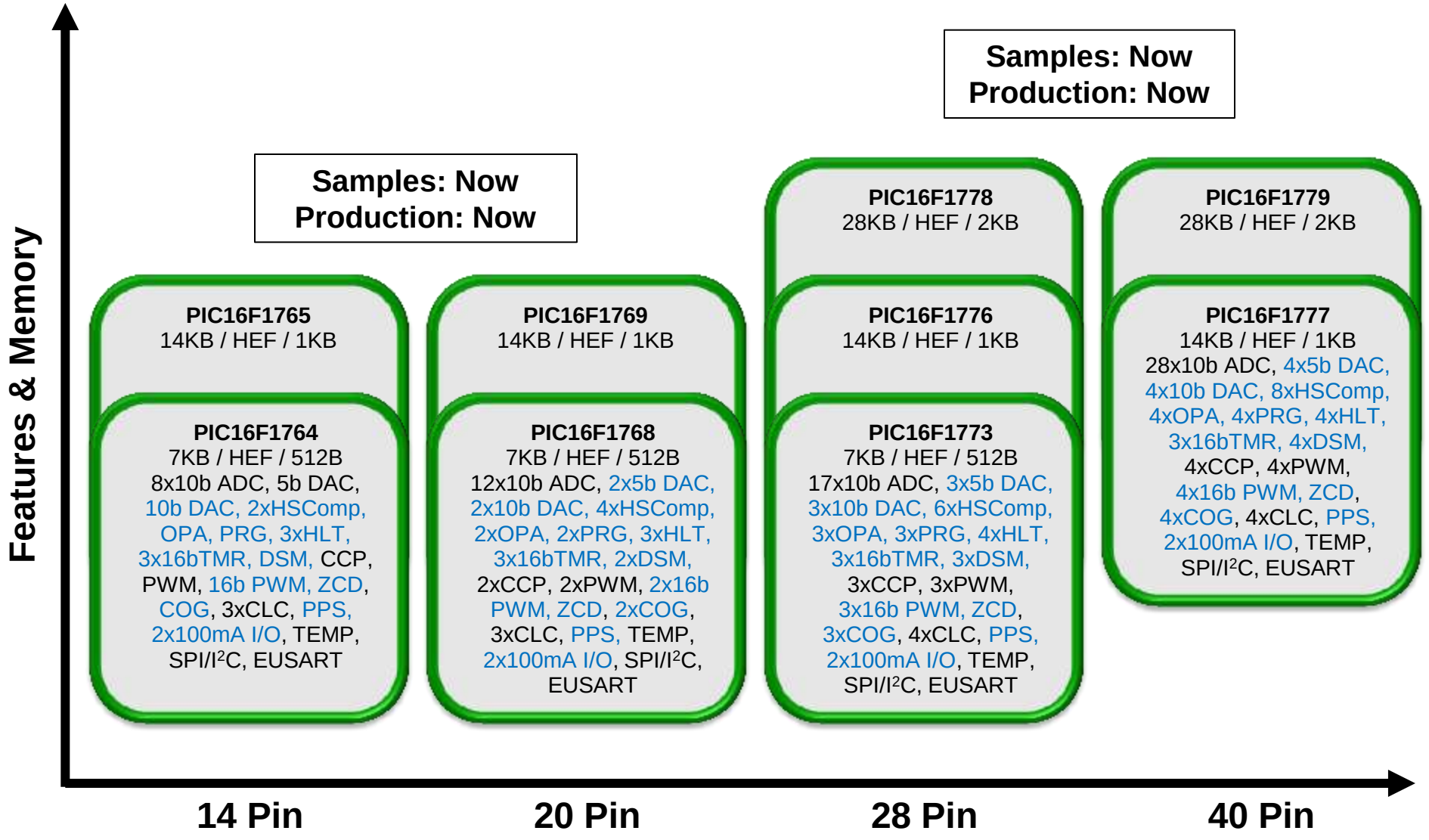
PIC16(L)F176X/7X

Multi Channel SMPS with LED Dimming Engine



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Core Independent Peripherals Integration Quick Reference Guide

Product Family	Pin Count	Program Flash Memory (KB)	Peripheral Function Focus																																				
			Intelligent Analog									Waveform Control							Timing and Measurements**								Logic and Math			Safety and Monitoring			Communications				User Interface			Low Power and System Flexibility				
			ADC (# of bits)	Comp	HSComp	DAC (# of bits)	HC I/O (mA)	OPA	PRG	SlopeComp	ZCD	CCP/ECCP	10-bit PWM	16-bit PWM	PSMC (16-bit PWM)	COG	CWG	NCO	DSM	AngTMR	HLT (8-bit)	PSMC (16-bit)	16-bit PWM (16-bit)	NCO (20-bit)	SMT (24-bit)	RTCC	TEMP	CLC	MULT	MathACC	CRC/SCAN	HLT	WWDT	EUSART/AUSART	I²C™/SPI	USB with ACT	LIN Capable	mTouch® Sensing	HCVD	LCD	HEF	PPS	IDLE and PMD	DOZE	XLP
PIC10(L)F3XX	6	384–896 B	8										✓				✓	✓							✓			✓									✓								
PIC16F527/570	20–28	1.5–3	8	✓				✓																													✓								
PIC1X(L)F150X	8–20	1.75–14	10	✓		5							✓				✓	✓						✓			✓							✓	✓		✓	✓			✓				✓
PIC16(L)F151X/2X	28–64	3.5–28	10									✓												✓			✓							2	2		✓	✓			✓				✓
PIC12LF1552	8	3.5	10																					✓										✓			✓	✓		✓				
PIC16LF1554/9	14–20	7–14	Dual 10										✓											✓			✓							✓	✓		✓	✓	✓		✓				✓
PIC16(L)F145X	14–20	14	10	✓									✓				✓									✓								✓	✓	✓	✓	✓							✓
PIC1X(L)F157X	8–20	1.75–14	10	✓		5								✓			✓						✓				✓							✓			✓	✓			✓	✓			
PIC1X(HV)F752/53	8–14	1.75–3.5	10		✓	5/9	50	✓		✓		✓				✓					✓											✓				✓								
PIC16(L)F182X/4X	8–20	3.5–14	10	✓								✓							✓							✓								✓	✓		✓	✓							✓
PIC1X(L)F1612/3	8–14	3.5	10	✓		8					✓	✓					✓				✓				✓						✓	✓	✓					✓						✓
PIC16(L)F161X	14–20	7–14	10	✓		8	100				✓	✓	✓				✓			✓	✓				✓		✓			✓	✓	✓	✓	✓		✓	✓			✓	✓			✓
PIC16(L)F170X/1X	14–40	3.5–28	10		✓	5/8		✓			✓	✓	✓			✓		✓						✓			✓							✓	✓		✓	✓			✓	✓			✓
PIC16(L)F176X/7X	14–40	7–28	10		✓	5/10	100	✓	✓		✓	✓	✓	✓		✓			✓		✓		✓				✓					✓		✓	✓		✓	✓			✓	✓			✓
PIC16(L)F178X	28–40	3.5–28	12		✓	5/8		✓				✓			✓							✓					✓							✓	✓		✓	✓							✓
PIC16(L)F183XX	8–20	3.5–14	10	✓		5						✓	✓				✓	✓	✓					✓			✓							✓	2		✓	✓				✓	✓	✓	✓
PIC16(L)F188XX	28–40	7–56	10*	✓		5					✓	✓	✓				✓	✓	✓		✓			✓	✓		✓			✓	✓	✓		✓	2		✓	✓	✓			✓	✓	✓	✓
PIC16(L)F193X/4X	28–64	7–28	10	✓								✓														✓								✓	2		✓	✓		✓					✓
PIC18(L)FXXK20	28–40	8–64	10	✓								✓														✓		✓						✓	✓		✓	✓				✓			✓
PIC18(L)FXXK22	20–80	8–128	10	✓		5						✓													✓		✓							2	2		✓	✓				✓			✓
PIC18(L)FXXK40	28–64	16–128	10*	✓		5					✓	✓	✓				✓		✓		✓						✓			✓	✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
PIC18(L)FXXK42	28–64	16–128	10*	✓		5					✓	✓		✓			✓	✓	✓		✓		✓	✓	✓	✓		✓		✓	✓	✓	2	2		✓	✓	✓			✓	✓	✓	✓	✓
PIC18(L)FXXJ94	64–100	32–128	12	✓								✓													✓			✓						4	2	✓	✓	✓		✓		✓	✓		✓
PIC18(L)FXXK50	20–40	8–32	10	✓		5						✓														✓			✓						✓	✓	✓	✓	✓				✓			✓

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INTELLIGENT ANALOG: Sensor Interfacing and Signal Conditioning	
ADC: Analog-to-Digital Converter	General purpose 8-/10-/12-bit ADC
ADC with MATHPAK: Advanced Analog-to-Digital Converter with Math Package	General purpose 10-/12-bit ADC with automated analog signal analysis (ex. oversampling, averaging, etc.)
CC I/O: Constant-Current I/O	Constant-current source I/O with fixed output up to 10 mA
Comp: Comparator	General purpose rail-to-rail comparator
DAC: Digital-to-Analog Converter	Programmable voltage reference with multiple internal and external connections
HC I/O: High-Current I/O	Up to 50 mA or 100 mA current drive on select I/O pins
HSComp: High-Speed Comparator	General purpose rail-to-rail comparator with < 50 ns response time
OPA: Operational Amplifier	General purpose op amp for internal and external signal source conditioning
PRG: Programmable Ramp Generator	Analog ramp generator (with slope compensation) for current/voltage mode power supplies
SlopeComp: Slope Compensation	Slope compensation for Peak Current Mode power supplies
VREF: Voltage Reference	Stable fixed voltage reference for use with integrated analog peripherals
ZCD: Zero Cross Detect	AC high-voltage zero crossing detection for simplifying TRIAC control, synchronized switching control and timing
WAVEFORM CONTROL: PWM Drive and Waveform Generation	
CCP/ECCP: (Enhanced) Capture Compare PWM	1. CCP/ECCP: 10-bit PWM control with 16-bit capture and compare 2. ECCP: Addition of auto shutdown control
COG: Complementary Output Generator	Automated complementary output with control of key parameters such as programmable rising/falling edge events, polarity, phase, precision dead-band, blanking and auto shutdown
CWG: Complementary Waveform Generator	Automated complementary output with control of key parameters such as dead-band and auto shutdown
DSM: Data Signal Modulator	Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms
NCO: Numerically Controlled Oscillator and 20-bit Timer Counter	1. Precision linear frequency generator (@ 50% duty cycle) with 0.0001% step size of source input clock frequency 2. General purpose 20-bit timer/counter
PSMC: Programmable Switch Mode Controller and 16-bit Timer/Counter	1. 16-bit PWM with dedicated 64 MHz clock source and event triggering 2. Automated complementary output with control of key parameters such as programmable rising/falling edge events, polarity, phase, precision dead-band, blanking and auto shutdown 3. General purpose 16-bit timer/counter
PWM: Pulse Width Modulation	General purpose 10-bit PWM control
16-bit PWM: Standalone 16-bit PWM and 16-bit Timer/Counter	1. High-resolution 16-bit PWM with edge- and center-aligned modes 2. General purpose 16-bit timer/counter
TIMING AND MEASUREMENTS: Signal Measurement with Timing and Counter Control	
AngTMR: Angular Timer	Phase angle timer for measurement and control of rotational and periodic events (ex. motor, AC mains, TRIAC, etc.)
CTMU: Charge Time Measurement Unit	Time measurement unit that provides method for temperature sensing, time measurements (down to 1 ns) and mTouch* sensing
HLT: Hardware Limit Timer and 8-bit Timer/Counter	1. Hardware monitoring for missed periodic events and fault detection 2. General purpose 8-bit timer/counter with external reset capabilities
NCO: Numerically Controlled Oscillator and 20-bit Timer/Counter	1. Precision linear frequency generator (@ 50% duty cycle) with 0.0001% step size of source input clock frequency 2. General purpose 20-bit timer/counter
PSMC: Programmable Switch Mode Controller and 16-bit Timer/Counter	1. 16-bit PWM with dedicated 64 MHz clock source and event triggering 2. Automated complementary output with control of key parameters such as programmable rising/falling edge events, polarity, phase, precision dead-band, blanking and auto shutdown 3. General purpose 16-bit timer/counter
RTCC: Real-Time Clock/Calendar	Maintains accurate clock and calendar timing with external 32.768 kHz crystal
SMT: 24-bit Signal Measurement Timer and 24-bit Timer/Counter	1. Accurate measurement of any digital signal including period, duty cycle, time of flight; instantaneous vs. average measurements 2. General purpose 24-bit timer/counter
TEMP: Temperature Indicator	Provides relative temperature measurements utilizing the ADC
8-/16-bit Timer	General purpose 8-/16-bit timer/counter
16-bit PWM: Standalone 16-bit PWM and 16-bit Timer/Counter	1. High-resolution 16-bit PWM with edge- and center-aligned modes 2. General purpose 16-bit timer/counter

LOGIC AND MATH: Customizable Logic and Math Functions	
CLC: Configurable Logic Cell	1. Integrated combinational and sequential logic 2. Customer interconnection and re-routing of digital peripherals
MULT: Hardware Multiplier	MULTIPLY function of two 8-bit values with 16-bit result
MathACC: Math Accelerator	1. MULTIPLY, ADD, ACCUMULATE functions of 8-/16-bit values with 35-bit result 2. Calculates a 16-bit PID function based on configurable K_P, K_I, K_D constants with a 34-bit result
SAFETY AND MONITORING: Hardware Monitoring and Fault Detection	
CRC/SCAN: Cyclical Redundancy Check with Memory Scan	1. Automatically calculates CRC checksum of Program/DataEE memory for NVM integrity 2. General purpose 16-bit CRC for use with memory and communications data
HLT: Hardware Limit Timer and 8-bit Timer/Counter	1. Hardware monitoring for missed periodic events and fault detection of external hardware 2. General purpose 8-bit timer/counter with external reset capabilities
WWDT: Windowed Watch Dog Timer	System supervisory circuit that generates a reset when software timing anomalies are detected within a configurable critical window
COMMUNICATIONS: General, Industrial, Lighting and Automotive	
ACT: Active Clock Tuning for Crystal-Free USB	1. Auto-tuning of internal oscillator when connected to USB host (eliminates need for external crystal) 2. Tunes internal oscillator to match accuracy of external clock source
CAN: Controller Area Network	Industrial- and automotive-centric communication bus
LIN: Local Interconnect Network	1. Industrial- and automotive-centric communication bus 2. Support for LIN when using the EUSART
EUSART/AUSART: Enhanced/Addressable Universal Asynchronous Receiver Transceiver	1. General purpose serial communications 2. Support for LIN when using the EUSART
I²C™: Inter-Integrated Circuit	General purpose 2-wire serial communications
SPI: Serial Peripheral Interface	General purpose 4-wire serial communications
USB: Universal Serial Bus	Support for full-speed USB 2.0 device profiles
USER INTERFACE: Capacitive Touch Sensing and LCD Control	
HCVD: Hardware Capacitive Voltage Divider	Simplifies implementation and reduces overhead of mTouch sensing applications
LCD: Liquid Crystal Display	Highly integrated segmented LCD controller
mTouch: Microchip Proprietary Capacitive Touch Technology	1. Capacitive sensing for touch buttons and sliders 2. Capacitive sensing for system measurements and detection (ex. water level, intrusion detection, etc.)
LOW POWER AND SYSTEM FLEXIBILITY: XLP Low-Power Technology, Peripheral and Interconnects	
DOZE: Power Saving Mode	Ability to run the CPU core slower than the system clock used by the internal peripherals
HEF: High-Endurance Flash	128B Non-volatile data storage with high-endurance 100k E/W cycles
IDLE: Power Saving Mode	Ability to put the CPU core to sleep while the internal peripherals continue to operate from the system clock
PMD: Peripheral Module Disable	Peripheral power disable hardware to minimize power consumption of unused peripherals
PPS: Peripheral Pin Select	I/O pin remapping of digital peripherals for greater design flexibility and improved EMI board layout
XLP: eXtreme Low Power Technology	Industry-leading low power technology (LF variants only, unless otherwise noted)

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Summary

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