Section 19. Comparator

HIGHLIGHTS

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19.1 INTRODUCTION

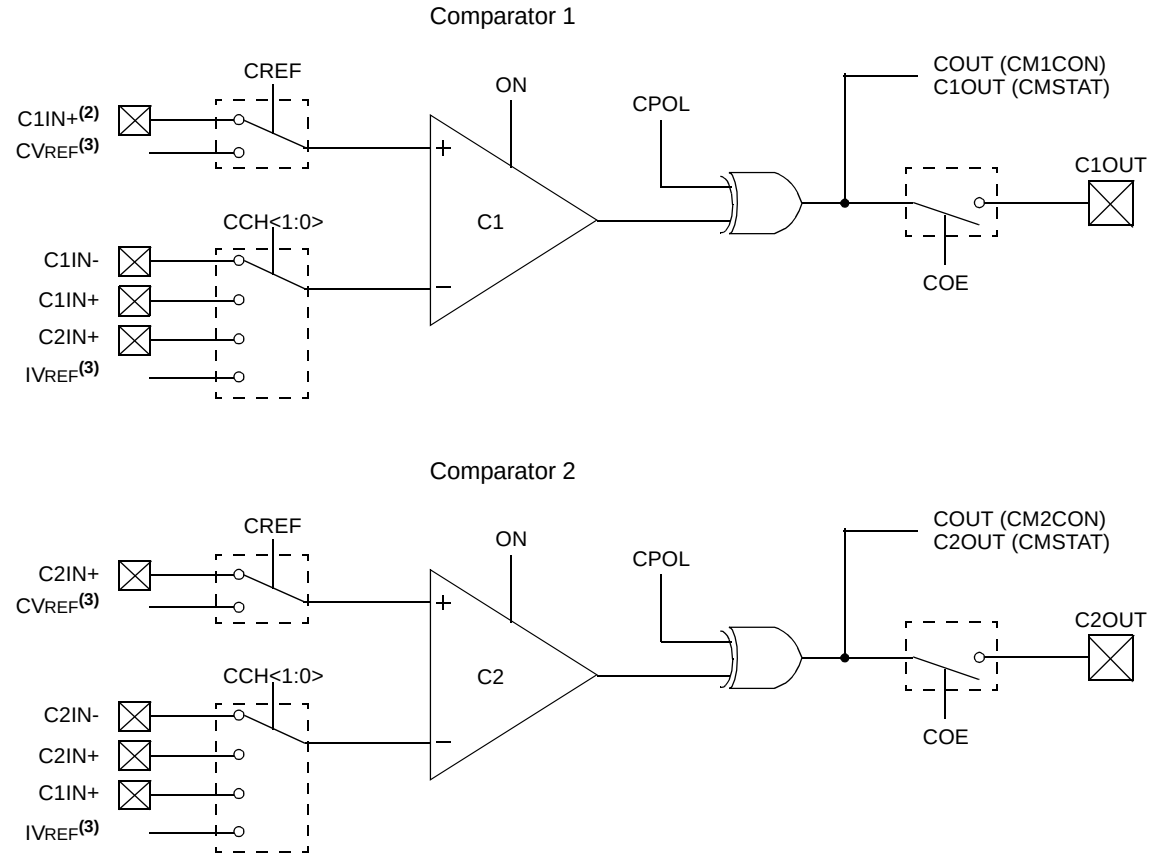
The PIC32MX Analog Comparator module contains one or more comparator(s) that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-Chip Internal Absolute Voltage Reference (IVREF)
  - Comparator Voltage Reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the comparator module is shown in Figure 19-1.

Figure 19-1: Comparator Block Diagram



Note 1: IVref is the internal 1.2V reference.

2: On USB variants, when USB is enabled, this pin is controlled by the USB module and therefore is not available as a comparator input.

3: Internally connected.

19.2 COMPARATOR CONTROL REGISTERS

Note: Each PIC32MX device variant may have one or more Comparator modules. An 'x' used in the names of pins, control/Status bits and registers denotes the particular module. Refer to the specific device data sheets for more details.

A Comparator module consists of the following Special Function Registers (SFRs):

- CMxCON: Comparator Control Register for Module 'x'
- CMxCONCLR, CMxCONSET, CMxCONINV: Atomic Bit Write-only Manipulation Registers for CMxCON
- CMSTAT: Comparator Status Register
- CMSTATCLR, CMSTATSET, CMSTATINV: Atomic Bit Write-only Manipulation Registers for CMSTAT

The Comparator module also has the following interrupt control registers:

- IFS1: Interrupt Flag Status Register
- IFS1CLR, IFS1SET, IFS1INV: Atomic Bit Manipulation Write-only Registers for IFS1
- IEC1: Interrupt Enable Control Register
- IEC1CLR, IEC1SET, IEC1INV: Atomic Bit Manipulation Write-only Registers for IEC1
- IPC7: Interrupt Priority Control Register
- IPC7CLR, IPC7SET, IPC7INV: Atomic Bit Write-only Manipulation Registers for IPC7

The following table provides a brief summary of all Comparator-related registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 19-1: Comparator SFRs Summary

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CM1CON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	COE	CPOL	—	—	—	—	COUT
	7:0	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
CM1CONCLR	31:0	Write clears selected bits in CM1CON, read yields undefined value							
CM1CONSET	31:0	Write sets selected bits in CM1CON, read yields undefined value							
CM1CONINV	31:0	Write inverts selected bits in CM1CON, read yields undefined value							
CM2CON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	COE	CPOL	—	—	—	—	COUT
	7:0	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
CM2CONCLR	31:0	Write clears selected bits in CM2CON, read yields undefined value							
CM2CONSET	31:0	Write sets selected bits in CM2CON, read yields undefined value							
CM2CONINV	31:0	Write inverts selected bits in CM2CON, read yields undefined value							
CMSTAT	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	—	FRZ	SIDL	—	—	—	—	—
	7:0	—	—	—	—	—	—	C2OUT	C1OUT
CMSTATCLR	31:0	Write clears selected bits in CMSTAT, read yields undefined value							
CMSTATSET	31:0	Write sets selected bits in CMSTAT, read yields undefined value							
CMSTATINV	31:0	Write inverts selected bits in CMSTAT, read yields undefined value							

Table 19-1: Comparator SFRs Summary (Continued)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
IFS1	31:24	—	—	—	—	—	—	USBIF	FCEIF
	23:16	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF
	15:8	RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF
	7:0	SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF
IFS1CLR	31:0	Clears the selected bits in IFS1, read yields undefined value							
IFS1SET	31:0	Sets the selected bits in IFS1, read yields undefined value							
IFS1INV	31:0	Inverts the selected bits in IFS1, read yields undefined value							
IEC1	31:24	—	—	—	—	—	—	USBIE	FCEIE
	23:16	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE
	15:8	RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE
	7:0	SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE
IEC1CLR	31:0	Clears the selected bits in IEC1, read yields undefined value							
IEC1SET	31:0	Sets the selected bits in IEC1, read yields undefined value							
IEC1INV	31:0	Inverts the selected bits in IEC1, read yields undefined							
IPC7	31:24	—	—	—	SPI2IP<2:0>			SP2IS<1:0>	
	23:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>	
	15:8	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>	
	7:0	—	—	—	PMPIP<2:0>			PMPIS<1:0>	
IPC7CLR	31:0	Clears the selected bits in IPC7, read yields undefined value							
IPC7SET	31:0	Sets the selected bits in IPC7, read yields undefined value							
IPC7INV	31:0	Inverts the selected bits in IPC7, read yields undefined value							

Register 19-1: CM1CON: Comparator 1 Control Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	r-x	r-x	R-0
ON	COE	CPOL	—	—	—	—	COUT
bit 15							bit 8

R/W-1	R/W-1	r-x	R/W-0	r-x	r-x	R/W-1	R/W-1
EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **Reserved:** Write ‘0’; ignore read

bit 15 **ON:** Comparator ON bit

1 = Module is enabled. Setting this bit does not affect the other bits in this register.
0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register.

Note: When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output C1OUT pin
0 = Comparator output is not driven on the output C1OUT pin

bit 13 **CPOL:** Comparator Output Inversion bit

1 = Output is inverted
0 = Output is not inverted

Note: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

bit 12 **Reserved:** Write ‘0’; ignore read

bit 11-9 **Reserved:** Write ‘0’; ignore read

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a ‘1’
0 = Output of the Comparator is a ‘0’

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
00 = Comparator interrupt generation is disabled

bit 5 **Reserved:** Write ‘0’; ignore read

Register 19-1: CM1CON: Comparator 1 Control Register (Continued)

bit 4 **CREF:** Comparator 1 Positive Input Configure bit
1 = Comparator non-inverting input is connected to the internal CV_{REF}
0 = Comparator non-inverting input is connected to the C1IN+ pin

bit 3-2 **Reserved:** Write '0'; ignore read

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator 1
11 = Comparator inverting input is connected to the IV_{REF}
10 = Comparator inverting input is connected to the C2IN+ pin
01 = Comparator inverting input is connected to the C1IN+ pin
00 = Comparator inverting input is connected to the C1IN- pin

Register 19-2: CM1CONCLR: Comparator Control Clear Register

Write clears selected bits in CM1CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in CM1CON**

A write of '1' in one or more bit positions clears the corresponding bit(s) in CM1CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM1CONCLR = 0x00008001` clears bits 15 and 0 in CM1CON register.

Register 19-3: CM1CONSET: Comparator Control Set Register

Write sets selected bits in CM1CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in CM1CON**

A write of '1' in one or more bit positions sets the corresponding bit(s) in CM1CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM1CONSET = 0x00008001` sets bits 15 and 0 in CM1CON register.

Register 19-4: CM1CONINV: Comparator Control Invert Register

Write inverts selected bits in CM1CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in CM1CON**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in CM1CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM1CONINV = 0x00008001` inverts bits 15 and 0 in CM1CON register.

Register 19-5: CM2CON: Comparator 2 Control Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	r-x	r-x	R-0
ON	COE	CPOL	—	—	—	—	COUT
bit 15							bit 8

R/W-1	R/W-1	r-x	R/W-0	r-x	r-x	R/W-1	R/W-1
EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **Reserved:** Write ‘0’; ignore read

bit 15 **ON:** Comparator ON bit
1 = Module is enabled. Setting this bit does not affect the other bits in this register.
0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register.
Note: When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is driven on the output C2OUT pin
0 = Comparator output is not driven on the output C2OUT pin

bit 13 **CPOL:** Comparator Output Inversion bit
1 = Output is inverted
0 = Output is not inverted
Note: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

bit 12 **Reserved:** Write ‘0’; ignore read

bit 11-9 **Reserved:** Write ‘0’; ignore read

bit 8 **COUT:** Comparator Output bit
1 = Output of the Comparator is a ‘1’
0 = Output of the Comparator is a ‘0’

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
00 = Comparator interrupt generation is disabled

bit 5 **Reserved:** Write ‘0’; ignore read

Register 19-5: CM2CON: Comparator 2 Control Register (Continued)

bit 4 **CREF:** Comparator 1 Positive Input Configure bit
1 = Comparator non-inverting input is connected to the internal CV_{REF}
0 = Comparator non-inverting input is connected to the C2IN+ pin

bit 3-2 **Reserved:** Write '0'; ignore read

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator 2
11 = Comparator inverting input is connected to the IV_{REF}
10 = Comparator inverting input is connected to the C1IN+ pin
01 = Comparator inverting input is connected to the C2IN+ pin
00 = Comparator inverting input is connected to the C2IN- pin

Register 19-6: CM2CONCLR: Comparator Control Clear Register

Write clears selected bits in CM2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in CM2CON**

A write of '1' in one or more bit positions clears corresponding bit(s) in CM2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM2CONCLR = 0x00008001` clears bits 15 and 0 in CM2CON register.

Register 19-7: CM2CONSET: Comparator Control Set Register

Write sets selected bits in CM2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in CM2CON**

A write of '1' in one or more bit positions sets corresponding bit(s) in CM2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM2CONSET = 0x00008001` sets bits 15 and 0 in CM2CON register.

Register 19-8: CM2CONINV: Comparator Control Invert Register

Write inverts selected bits in CM2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in CM2CON**

A write of '1' in one or more bit positions inverts corresponding bit(s) in CM2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CM2CONINV = 0x00008001` inverts bits 15 and 0 in CM2CON register.

Register 19-9: CMSTAT: Comparator Control Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	R/W-0	R/W-0	r-x	r-x	r-x	r-x	r-x
—	FRZ	SIDL	—	—	—	—	—
bit 15							bit 8

r-x	r-x	r-x	r-x	r-x	r-x	R-0	R-0
—	—	—	—	—	—	C2OUT	C1OUT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-15 **Reserved:** Write ‘0’; ignore read

bit 14 **FRZ:** Freeze Control bit
1 = Freeze operation when CPU enters Debug Exception mode
0 = Continue operation when CPU enters Debug Exception mode
Note: FRZ is writable in Debug Exception mode only. It always reads ‘0’ in Normal mode.

bit 13 **SIDL:** Stop in IDLE Control bit
1 = All Comparator modules are disabled in IDLE mode
0 = All Comparator modules continue to operate in the IDLE mode

bit 12-2 **Reserved:** Write ‘0’; ignore read

bit 1 **C2OUT:** Comparator Output bit
1 = Output of Comparator 2 is a ‘1’
0 = Output of Comparator 2 is a ‘0’

bit 0 **C1OUT:** Comparator Output bit
1 = Output of Comparator 1 is a ‘1’
0 = Output of Comparator 1 is a ‘0’

Register 19-10: CMSTATCLR: Comparator Control Clear Register

Write clears selected bits in CMSTAT, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in CMSTAT**

A write of '1' in one or more bit positions clears corresponding bit(s) in CMSTAT register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CMSTATCLR = 0x00002000` clears bit 13 in CMSTAT register.

Register 19-11: CMSTATSET: Comparator Control Set Register

Write sets selected bits in CMSTAT, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in CMSTAT**

A write of '1' in one or more bit positions sets corresponding bit(s) in CMSTAT register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CMSTATSET = 0x00002000` sets bit 13 in CMSTAT register.

Register 19-12: CMSTATINV: Comparator Control Invert Register

Write inverts selected bits in CMSTAT, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in CMSTAT**

A write of '1' in one or more bit positions inverts corresponding bit(s) in CMSTAT register, and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `CMSTATINV = 0x00002000` inverts bit 13 in CMSTAT register.

Register 19-13: IFS1: Interrupt Flag Status Register 1(1)

r-x	r-x	r-x	r-x	r-x	r-x	R/W-0	R/W-0
—	—	—	—	—	—	USBIF	FCEIF
bit 31							bit 24

r-0	r-0	r-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 4 **CMP2IF:** Comparator 2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CMP1IF:** Comparator 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the comparator.

Register 19-14: IEC1: Interrupt Enable Control Register 1(1)

r-x	r-x	r-x0	r-x	r-x	r-x	R/W-0	R/W-0
—	—	—	—	—	—	USBIE	FCEIE
bit 31							bit 24

r-0	r-0	r-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 4 **CMP2IE:** Comparator 2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **CMP1IE:** Comparator 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the comparator.

Register 19-15: IPC7: Interrupt Priority Control Register 7(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	SPI2IP<2:0>			SPI2IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CMP2IP<2:0>			CMP2IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CMP1IP<2:0>			CMP1IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PMPIP<2:0>			PMPIS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20-18 **CMP2IP<2:0>:** Comparator 2 Interrupt Priority bits
- 111 = Interrupt Priority is 7
- 110 = Interrupt Priority is 6
- 101 = Interrupt Priority is 5
- 100 = Interrupt Priority is 4
- 011 = Interrupt Priority is 3
- 010 = Interrupt Priority is 2
- 001 = Interrupt Priority is 1
- 000 = Interrupt is disabled

bit 17-6 **CMP2IS<1:0>:** Comparator 2 Interrupt Subpriority bits
- 11 = Interrupt Subpriority is 3
- 10 = Interrupt Subpriority is 2
- 01 = Interrupt Subpriority is 1
- 00 = Interrupt Subpriority is 0

bit 12-10 **CMP1IP<2:0>:** Comparator 1 Interrupt Priority bits
- 111 = Interrupt Priority is 7
- 110 = Interrupt Priority is 6
- 101 = Interrupt Priority is 5
- 100 = Interrupt Priority is 4
- 011 = Interrupt Priority is 3
- 010 = Interrupt Priority is 2
- 001 = Interrupt Priority is 1
- 000 = Interrupt is disabled

bit 9-8 **CMP1IS<1:0>:** Comparator 1 Interrupt Subpriority bits
- 11 = Interrupt Subpriority is 3
- 10 = Interrupt Subpriority is 2
- 01 = Interrupt Subpriority is 1
- 00 = Interrupt Subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the comparator.

19.3 COMPARATOR OPERATION

19.3.1 Comparator Configuration

The Comparator module has a flexible input and output configuration to allow the module to be tailored to the needs of the application. The PIC32MX Comparator module has individual control over the enables, output inversion, output on I/O pin and input selections. The VIN+ pin of each comparator can select from an input pin or the CVREF. The VIN- input of the comparator can select from one of 3 input pins or the IVREF. In addition, the module has two individual comparator event generation control bits. These control bits can be used for detecting when the output of an individual comparator changes to a desired state or changes states.

If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay (refer to the device data sheet for more information).

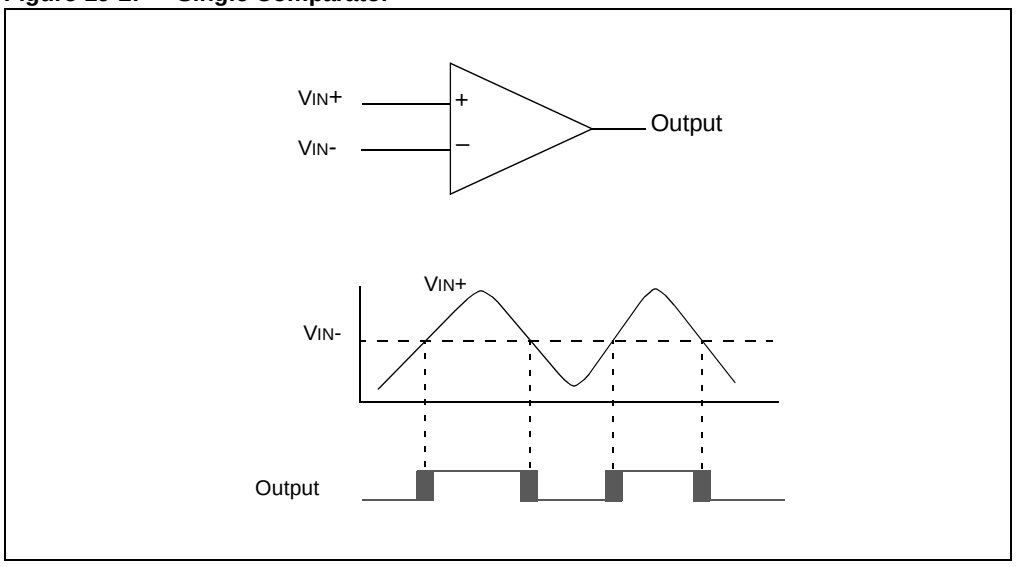
Note:	Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may be generated.

A single comparator is shown in the upper portion of Figure 19-2. The lower portion represents the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input at VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in the lower portion of Figure 19-2 demonstrates the uncertainty that is due to input offsets and the response time of the comparator.

19.3.2 Comparator Inputs

Depending on the comparator Operating mode, the inputs to the comparators may be from two input pins or a combination of an input pin and one of two internal voltage references. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is set or cleared according to the result of the comparison (see Figure 19-2).

Figure 19-2: Single Comparator



19.3.2.1 External Reference Signal

An external voltage reference may be used with the comparator by using the output of the reference as an input to the comparator. Refer to the device data sheet for input voltage limits.

19.3.2.2 Internal Reference Signals

The CVREF module and the IVREF can be used as inputs to the comparator (see Figure 19-1). The CVREF provides a user-selectable voltage for use as a comparator reference. Refer to **Section 20, "Comparator Voltage Reference"** of this manual for more information on this module. The IVREF has a fixed 1.2V output that does not change with the device supply voltage. Refer to the device data sheet for specific details and accuracy of this reference.

19.3.3 Comparator Response Time

Response time is the minimum amount of time that elapses from the moment a change is made in the input voltage to a comparator to the moment that the output reflects the new level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (see the device data sheet for detailed information).

19.3.4 Comparator Outputs

The comparator output is read through the CMSTAT register and the COUT bit (CM2CON<8> or CM1CON<8>). This bit is read-only. The comparator output may also be directed to an I/O pin via the CxOUT bit; however, the COUT bit is still valid when the signal is routed to a pin. For the comparator output to be available on the CxOut pin, the associated TRIS bit for the output pin must be configured as an output. When the COUT signal is routed to a pin the signal is the unsynchronized output of the comparator.

The output of the comparator has a degree of uncertainty. The uncertainty of each of the comparators is related to the input offset voltage and the response time, as stated in the specifications. The lower portion of Figure 19-2 provides a graphical representation of this uncertainty.

The comparator output bit COUT provides the latched sampled value of the comparator's output when the register was read. There are two common methods used to detect a change in the comparator output:

- Software polling
- Interrupt generation

19.3.4.1 Software Polling Method of Comparator Event Detection

Software polling of COUT is performed by periodically reading the COUT bit. This allows the output to be read at uniform time intervals. A change in the comparator output is not detected until the next read of the COUT bit. If the input signal changes at a rate faster than the polling, a brief change in output may not be detected.

19.3.4.2 Interrupt Generation Method of Comparator Event Detection

Interrupt generation is the other method for detecting a change in the comparator output. The Comparator module can be configured to generate an interrupt when the COUT bit changes.

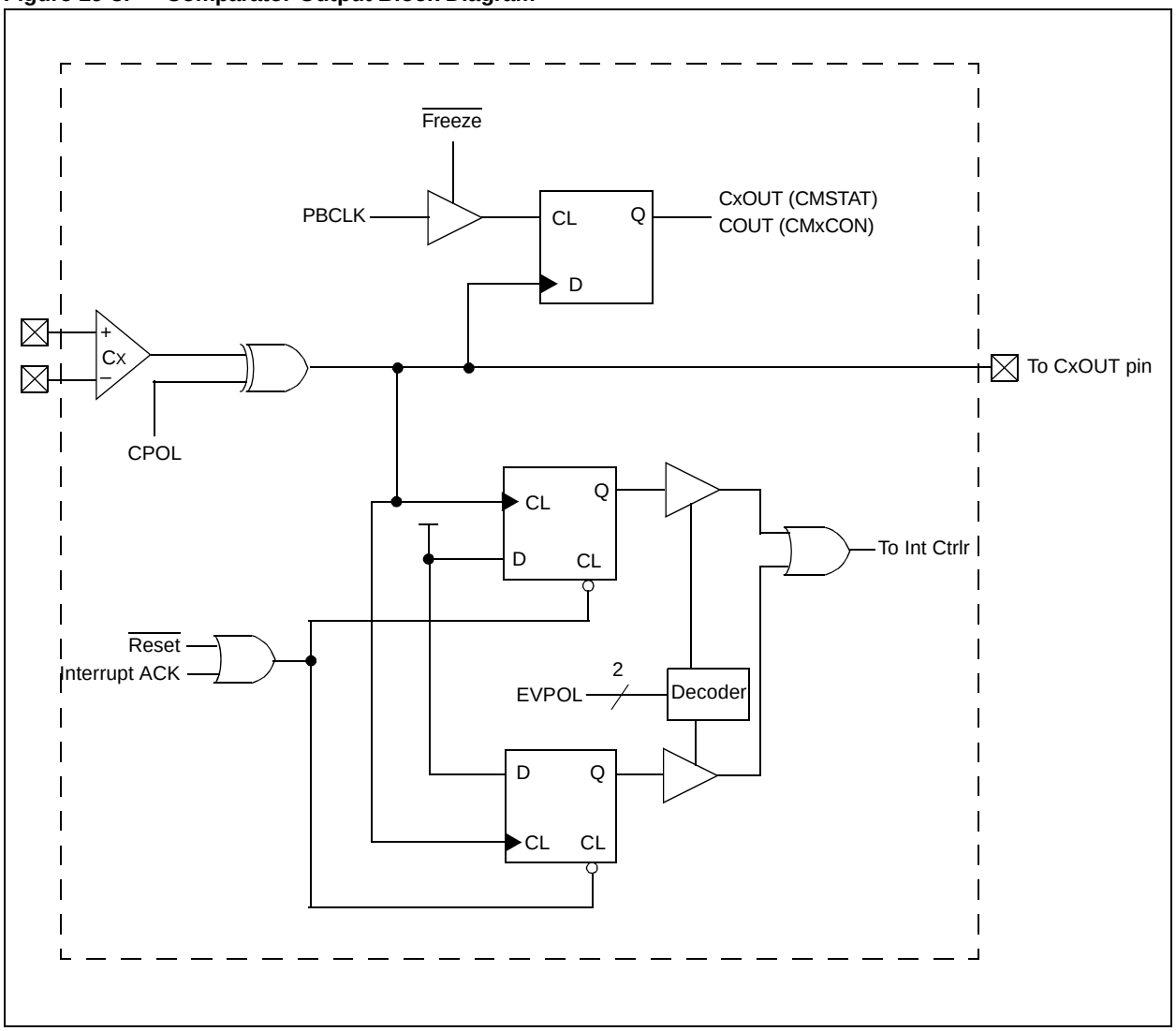
An interrupt will be generated when the comparator's output changes (subject to the interrupt priorities). This method responds more rapidly to changes than the software polling method; however, rapidly changing signals will cause an equally large number of interrupts. This can cause interrupt loading and potentially undetected interrupts due to new interrupts being generated while the previous interrupt is still being serviced or even before the interrupt can be serviced. If the input signal changes rapidly, reading the COUT bit in the Interrupt Service Routine may yield a different result than the one that generated the Interrupt. This is due to the COUT bit representing the value of the comparator output when the bit was read and not the value that caused the interrupt.

Comparator output and interrupt generation is illustrated in Figure 19-3.

19.3.4.3 Changing the Polarity of Comparator Outputs

The polarity of the comparator outputs can be changed using the CPOL bit (CM1CON<13>). CPOL appears below the comparator Cx on the left side of Figure 19-3.

Figure 19-3: Comparator Output Block Diagram



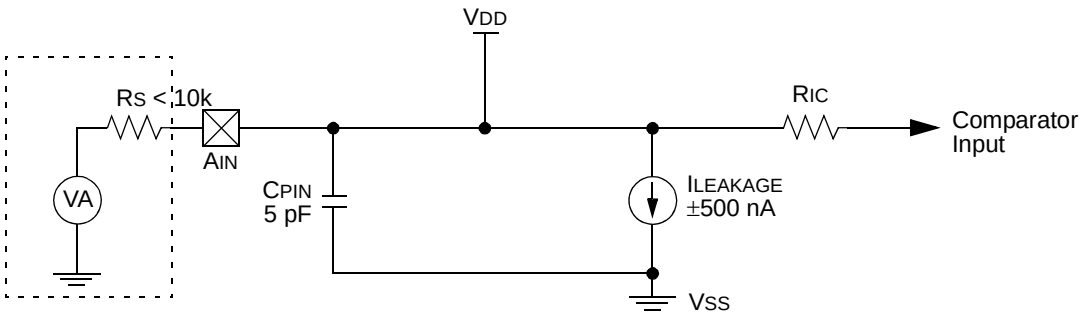
19.3.5 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 19-4. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current. See the device data sheet for input voltage limits. If a pin is to be shared by two or more analog inputs that are to be used simultaneously, the loading effects of all the modules involved must be taken into consideration. This loading may reduce the accuracy of one or more of the modules connected to the common pin. This may also require a lower source impedance than is stated for a single module with exclusive use of a pin in analog mode.

Notes: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

Figure 19-4: Comparator Analog Input Model



Legend:	CPIN	=	Input Capacitance
	ILEAKAGE	=	Leakage Current at the pin due to various junctions
	RIC	=	Interconnect Resistance
	RS	=	Source Impedance
	VA	=	Analog Voltage

19.4 INTERRUPTS

Each of the available comparators has a dedicated interrupt bit, CMPxIF (IFS1<3 or 4>), and a corresponding interrupt enable/mask bit, CMPxIE (IEC1<3 or 4>). These bits are used to determine the source of an interrupt and to enable or disable an individual interrupt source. The priority level of each of the channels can also be set independently of the other channels.

The CMPxIF bit is set when the CMPx channel detects a predefined match condition that is defined as an event generating an interrupt. The CMPxIF bit will then be set without regard to the state of the corresponding CMPxIE bit. The CMPxIF bit can be polled by software if desired.

The CMPxIE bit controls the interrupt generation. If the CMPxIE bit is set, the CPU will be interrupted whenever a comparator interrupt event occurs and the corresponding CMPxIF bit will be set (subject to the priority and subpriority as outlined below).

It is the responsibility of the user's software routine that services a particular interrupt to clear the appropriate interrupt flag bit before the service routine is complete.

The priority of each comparator channel can be set independently via the CMPxIP<2:0> bits. This priority defines the priority group to which the interrupt source will be assigned. The priority groups range from a value of 7 (the highest priority), to a value of 0 (which does not generate an interrupt). An interrupt being serviced will be preempted by an interrupt in a higher priority group.

The subpriority bits allow setting the priority of an interrupt source within a priority group. The values of the subpriority bit OCxIS<1:0> range from 3 (the highest priority), to 0 (the lowest priority). An interrupt within the same priority group but having a higher subpriority value will preempt a lower subpriority interrupt that is in progress.

The priority group and subpriority bits allow more than one interrupt source to share the same priority and subpriority. If simultaneous interrupts occur in this configuration, the natural order of the interrupt sources within a priority/subgroup pair determine the interrupt generated. The natural priority is based on the vector numbers of the interrupt sources. The lower the vector number, the higher the natural priority of the interrupt. Any interrupts that were overridden by natural order will then generate their respective interrupts based on priority, subpriority, and natural order, after the interrupt flag for the current interrupt is cleared.

After an enabled interrupt is generated, the CPU will jump to the vector assigned to that interrupt (refer to Table 19-2). The vector number for the interrupt is the same as the natural order number. The CPU will then begin executing code at the vector address. The user's code at this vector address should perform any application-specific operations required, such as reloading the duty cycle, clear the interrupt flag CMPxIF, and then exit. Refer to the vector address table details in **Section 8. "Interrupts"** for more information on interrupts.

Table 19-2: Typical Comparator Interrupt Vectors for Various Offsets with EBASE = 0x8000:0000

Interrupt	Vector	IRQ Number	Vector Address IntCtl.VS = 0x01	Vector Address IntCtl.VS = 0x02	Vector Address IntCtl.VS = 0x04	Vector Address IntCtl.VS = 0x08	Vector Address IntCtl.VS = 0x10
CMP1	29	35	8000 0660	8000 0AC0	8000 1380	8000 2500	8000 4800
CMP2	30	36	8000 0680	8000 0B00	8000 1400	8000 2600	8000 4A00

Example 19-1: Comparator Initialization with Interrupts Enabled Code Example

```
                          // Configure both comparators to generate an interrupt on any
                          // output transition
CM1CON  = 0xC0D0;         // Initialize Comparator 1
                          // Comparator enabled, output enabled, interrupt on any output
                          // change, inputs: CVref, C1IN-
CM2CON  = 0xA0C2;         // Initialize Comparator 2
                          // Comparator enabled, output enabled, interrupt on any output
                          // change, inputs: C2IN+, C1IN+

                          // Enable interrupts for Comparator modules and set priorities
                          // Set priority to 7 & sub priority to 3
IPC7SET = 0x00000700;     // Set CMP1 interrupt sub priority
IFS1CLR = 0x00000008;     // Clear the CMP1 interrupt flag
IEC1SET = 0x00000008;     // Enable CMP1 interrupt

IPC7SET = 0x00070000;     // Set CMP2 interrupt sub priority
IFS1CLR = 0x000000010;    // Clear the CMP2 interrupt flag
IEC1SET = 0x000000010;    // Enable CMP2 interrupt
```

Example 19-2: Comparator ISR Code Example

```
                          // Insert user code here

void__ISR(_COMPARATOR_2_VECTOR, ipl7) Cmp2_IntHandler (void)
{
                          // Insert user code here
    IFS1CLR = 0x00000010; // Clear the CMP2 interrupt flag
}

void__ISR(_COMPARATOR_1_VECTOR, ipl7) Cmp1_IntHandler (void)
{
                          // Insert code user here
    IFS1CLR = 0x00000008; // Clear the CMP1 interrupt flag
}
```

19.5 I/O PIN CONTROL

The Comparator module shares pins with port input/output control and in some cases with other modules. The following conditions must be provided to configure a pin for use by the comparator:

- Any modules sharing the pin must be disabled
- Comparator must be configured to use the desired pin
- TRIS bit corresponding to the pin must be a '1'
- Comparator must be enabled (refer to Table 19-3)
- Corresponding AD1PCFG bit must be a '0'.

  The comparator controls pin function for the desired comparator via the following bits in the CMxCON register: CREF, CCH<1:0>, and COE. The TRIS bit corresponding to any analog input pin for the comparator must be '1'. This disables the digital input buffer for the pin. When a pin is selected as analog output the digital output driver is disabled. The TRIS bit corresponding to the CxOUT pin must be a '0' if the comparator digital output is to be used.

Table 19-3: Pins Associated with a Comparator

Pin Name	Module Control	Controlling Bit Field	Required TRIS Bit Setting	Pin Type	Buffer Type	Description
C1IN+	ON	CVR_{EF}(1), CCH<1:0>(1), CCH<1:0>(2), AD1PCFG	Input	A, I	—	Analog Input for C1IN+
C1IN-	ON	CCH<1:0>(1), AD1PCFG	Input	A, I	—	Analog Input for C1IN-
C2IN+	ON	CVR_{EF}(2), CCH<1:0>(1), CCH<1:0>(2), AD1PCFG	Input	A, I	—	Analog Input for C2IN+
C2IN-	ON	CCH<1:0>(2), AD1PCFG	Input	A, I	—	Analog Input for C2IN-
C1OUT	ON	COE(1)	Output	D, O	—	Digital Output of the C1
C2OUT	ON	COE(2)	Output	D, O	—	Digital Output of the C2

Legend:
ST = Schmitt Trigger input with CMOS levels, I = Input, O = Output, A = Analog, D = Digital

Note 1: In CM1CON register
2: In CM2CON register

For example, if Comparator 1 is to use two external inputs C1IN+ and C1IN-, with an inverting output to a pin that does not generate an interrupt, the following configuration steps would be performed.

- Configure the TRIS Bits:
  - TRIS = Output – configures the C1IN+ and C1IN- pins as digital outputs to disable the digital input buffer.

    The output driver will be disabled when the pin is selected as an analog input by the module.
  - TRIS = Output – enables the output driver for the C1OUT signal.
- Set the CM1CON bits:
  - CREF (CM1CON<4>) = 0 – selects C1IN+ as a analog input to the comparator.
  - CCH<1:0> (CM1CON<1:0>) = 00 – selects C1IN- as an analog input (C2IN+ and C2IN- are available for use by other modules or general purpose I/O that share the pin).
  - CPOL (CM1CON <13>) = 1 – selects inverted output mode.
  - COE (CM1CON<14>) = 1 – enables the output of the comparator to be available at the C1OUT pin.
  - EVPOL<1:0> (CM1CON<7:6>) = 00 – disables interrupt generation.
  - ON (CM1CON <15>) = 1 – enables the module.

    ON is always set after the preceding bits are set.

19.6 OPERATION IN POWER-SAVING AND DEBUG MODES

Note:	In this manual, a distinction is made between a power mode as it is used in a specific module and a power mode as it is used by the device, e.g., Sleep mode of the Comparator and SLEEP mode of the CPU. To indicate which type of power mode is intended, upper- and lower-case letters (Sleep, Idle, Debug) signify a module power mode and all upper-case letters (SLEEP, IDLE, DEBUG) signify a device power mode.

19.6.1 Comparator Operation During IDLE Mode

When a comparator is active and the device is placed in IDLE mode, the comparator remains active and interrupts are generated (if enabled); if SIDL = 1 (CMSTAT<13>), the comparators are disabled in IDLE mode.

19.6.2 Comparator Operation During SLEEP Mode

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional (if enabled). This interrupt will wake up the device from SLEEP mode (when enabled). Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators: ON = 0 (CMxCON<15>), prior to entering SLEEP mode. If the device wakes up from SLEEP mode, the contents of the CMxCON register are not affected. See **Section 10. "Power-Saving Modes"** in this manual for additional information on SLEEP.

19.6.3 Comparator Operation in DEBUG Mode

The FRZ bit (CMSTAT<14>) determines whether the Comparator module will run or stop while the CPU is executing debug exception code (i.e., application is halted) in DEBUG mode. When FRZ = 0, the Comparator module continues to run even when application is halted in DEBUG mode. When FRZ = 1 and application is halted in DEBUG mode, the module will freeze its operations and make no changes to the state of the Comparator module. The module will resume its operation after the CPU resumes execution.

Note:	The FRZ bit is readable and writable only when the CPU is executing in Debug Exception mode. In all other modes, the FRZ bit reads as '0'. If FRZ bit is changed during DEBUG mode, the new value does not take effect until the current Debug Exception mode is exited and re-entered. During the Debug Exception mode, the FRZ bit reads the state of the peripheral when entering DEBUG mode.

19.7 EFFECTS OF A RESET

All Resets force the CMxCON registers to its Reset state, causing the comparator modules to be turned off (CMxCON<15> = 0). However, the input pins multiplexed with analog input sources are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the AD1PCFG register.

19.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32MX device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator module are:

Title	Application Note #
No related application notes at this time	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32MX family of devices.

19.9 REVISION HISTORY

Revision A (October 2007)

This is the initial released version of this document.

Revision B (October 2007)

Updated document to remove Confidential status.

Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x.

Revision D (May 2008)

Revised Figure 19-1; Revised Registers 19-1, 19-5, 19-13, 19-14, 19-15; Revised Example 19-2; Revised Section 19.5, pin names; Change Reserved bits from “Maintain as” to “Write”; Added Note to ON bit (CM1CON/CM2CON Registers).

NOTES:

