Section 16. Output Compare

HIGHLIGHTS

This section of the manual contains the following topics:

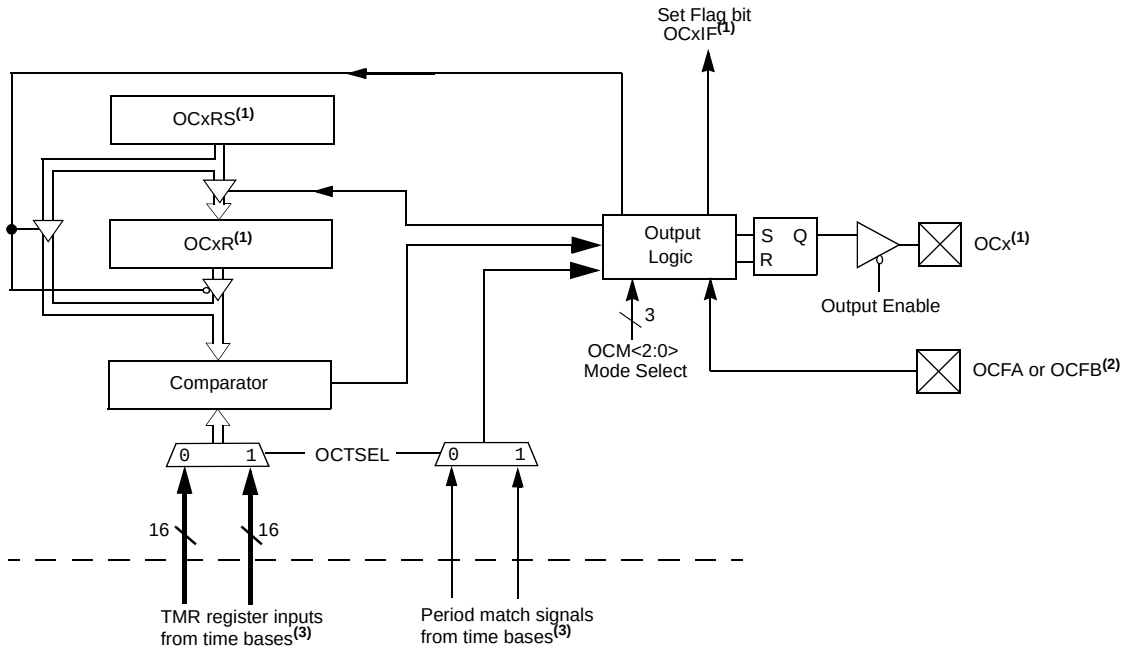
16.1 INTRODUCTION

The Output Compare module is primarily used to generate a single pulse or a train of pulses in response to selected time base events.

The following are some of the key features of the Output Compare module:

- Multiple output compare modules in a device
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Programmable interrupt generation on compare event
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16 or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

Figure 16-1: Output Compare Module Block Diagram



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels 1 through 5.

2: OCFA pin controls OC1-OC4 channels. OCFB pin controls OC5 channels.

3: Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit time base. Refer to the device data sheet for the time bases associated with the module.

16.2 OUTPUT COMPARE REGISTERS

Note: Each PIC32MX device variant may have one or more Output Compare modules. An 'x' used in the names of pins, control/Status bits and registers denotes the particular module. Refer to the specific device data sheets for more details.

Each Output Compare module consists of the following Special Function Registers (SFRs):

- OCxCON: Control register for the OCMP module 'x'
  OCxCONCLR, OCxCONSET, OCxCONINV: Atomic Bit Manipulation Write-only Registers for OCxCON
- OCxR: Data register for the module 'x'
  OCxRCLR, OCxRSET, OCxRINV: Atomic Bit Manipulation Write-only Registers for OCxR
- OCxRS: Secondary data register for the module 'x'
  OCxRSCLR, OCxRSSET, OCxRSINV: Atomic Bit Manipulation Write-only Registers for OCxRS
- T2CON: Time Base Register
  T2CONCLR, T2CONSET, T2CONINV: Atomic Bit Manipulation Write-only Registers for T2CON
- T3CON: Time Base Register
  T3CONCLR, T3CONSET, T3CONINV: Atomic Bit Manipulation Write-only Registers for T3CON
- TMR2: Timer Register
  TTMR2CLR, TMR2SET, TMR2INV: Atomic Bit Manipulation Write-only Registers for TMR2
- TMR3: Timer Register
  TMR3CLR, TMR3SET, TMR3INV: Atomic Bit Manipulation Write-only Registers for TMR3
- PR2: Period 2 Register
  PR2CLR, PR2SET, PR2INV: Atomic Bit Manipulation Write-only Registers for PR2
- PR3: Period 3 Register
  PR3CLR, PR3SET, PR3INV: Atomic Bit Manipulation Write-only Registers for PR3

Each timer module also has the following associated bits for interrupt control:

- OC5IF, OC4IF, OC3IF, OC2IF, OC1IF: Interrupt Flag Status Bits – in IFS0 INT Register
- OC5IE, OC4IE, OC3IE, OC2IE, OC1IE: Interrupt Enable Control Bits – in IEC0 INT Register
- OC1IP<2:0>: Interrupt Priority Control Bits – in IPC1 INT Registers
- OC1IS<1:0>: Interrupt Subpriority Control Bits – in IPC1 INT Registers
- OC2IP<2:0>: Interrupt Priority Control Bits – in IPC2 INT Registers
- OC2IS<1:0>: Interrupt Subpriority Control Bits – in IPC2 INT Registers
- OC3IP<2:0>: Interrupt Priority Control Bits – in IPC3 INT Registers
- OC3IS<1:0>: Interrupt Subpriority Control Bits – in IPC3 INT Registers
- OC4IP<2:0>: Interrupt Priority Control Bits – in IPC4 INT Registers
- OC4IS<1:0>: Interrupt Subpriority Control Bits – in IPC4 INT Registers
- OC5IP<2:0>: Interrupt Priority Control Bits – in IPC5 INT Registers
- OC5IS<1:0>: Interrupt Subpriority Control Bits – in IPC5 INT Registers

The following table summarizes all Output-Compare-related registers. Corresponding registers appear after the summary, followed by a detailed description of each register.

Table 16-1: Output Compare SFR Summary

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
OCxCON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	FRZ	SIDL	—	—	—	—	—
	7:0	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>		
OCxCONCLR	31:0	Write clears selected bits in OCxCON; read yields an undefined value							
OCxCONSET	31:0	Write sets selected bits in OCxCON; read yields an undefined value							
OCxCONINV	31:0	Write inverts selected bits in OCxCON; read yields an undefined value							
OCxR	31:24	OCxR<31:24>							
	23:16	OCxR<23:16>							
	15:8	OCxR<15:8>							
	7:0	OCxR<7:0>							
OCxRCLR	31:0	Write clears selected bits in OCxR; read yields an undefined value							
OCxRSET	31:0	Write sets selected bits in OCxR; read yields an undefined value							
OCxRINV	31:0	Write inverts selected bits in OCxR; read yields an undefined value							
OCxRS	31:24	OCxRS<31:24>							
	23:16	OCxRS<23:16>							
	15:8	OCxRS<15:8>							
	7:0	OCxRS<7:0>							
OCxRSCLR	31:0	Write clears selected bits in OCxRS; read yields an undefined value							
OCxRSSET	31:0	Write sets selected bits in OCxRS; read yields an undefined value							
OCxRSINV	31:0	Write inverts selected bits in OCxRS; read yields an undefined value							
IFS0	31:24	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF
	23:16	SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF
	15:8	INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC3IF	T2IF
	7:0	INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF
IFS0CLR	31:0	Write clears the selected bits in IFS0, read yields undefined value							
IFS0SET	31:0	Write sets the selected bits in IFS0, read yields undefined value							
IFS0INV	31:0	Write inverts the selected bits in IFS0, read yields undefined value							
IEC0	31:24	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE
	23:16	SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE
	15:8	INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE
	7:0	INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE
IEC0CLR	31:0	Write clears the selected bits in IEC0, read yields undefined value							
IEC0SET	31:0	Write sets the selected bits in IEC0, read yields undefined value							
IEC0INV	31:0	Write inverts the selected bits in IEC0, read yields undefined value							
IPC1	31:24	—	—	—	INT1IP<2:0>			INT1IS<1:0>	
	23:16	—	—	—	OC1IP<2:0>			OC1IS<1:0>	
	15:8	—	—	—	IC1IP<2:0>			IC1IS<1:0>	
	7:0	—	—	—	T1IP<2:0>			T1IS<1:0>	
IPC1CLR	31:0	Write clears the selected bits in IPC1, read yields undefined value							
IPC1SET	31:0	Write sets the selected bits in IPC1, read yields undefined value							
IPC1INV	31:0	Write inverts the selected bits in IPC1, read yields undefined value							

Table 16-1: Output Compare SFR Summary (Continued)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
IPC2	31:24	—	—	—	INT2IP<2:0>			INT2IS<1:0>	
	23:16	—	—	—	OC2IP<2:0>			OC2IS<1:0>	
	15:8	—	—	—	IC2IP<2:0>			IC2IS<1:0>	
	7:0	—	—	—	T2IP<2:0>			T2IS<1:0>	
IPC2CLR	31:0	Write clears the selected bits in IPC2, read yields undefined value							
IPC2SET	31:0	Write sets the selected bits in IPC2, read yields undefined value							
IPC2INV	31:0	Write inverts the selected bits in IPC2, read yields undefined value							
IPC3	31:24	—	—	—	INT3IP<2:0>			INT3IS<1:0>	
	23:16	—	—	—	OC3IP<2:0>			OC3IS<1:0>	
	15:8	—	—	—	IC3IP<2:0>			IC3IS<1:0>	
	7:0	—	—	—	T3IP<2:0>			T3IS<1:0>	
IPC3CLR	31:0	Write clears the selected bits in IPC3, read yields undefined value							
IPC3SET	31:0	Write sets the selected bits in IPC3, read yields undefined value							
IPC3INV	31:0	Write inverts the selected bits in IPC3, read yields undefined value							
IPC4	31:24	—	—	—	INT4IP<2:0>			INT4IS<1:0>	
	23:16	—	—	—	OC4IP<2:0>			OC4IS<1:0>	
	15:8	—	—	—	IC4IP<2:0>			IC4IS<1:0>	
	7:0	—	—	—	T4IP<2:0>			T4IS<1:0>	
IPC4CLR	31:0	Write clears the selected bits in IPC4, read yields undefined value							
IPC4SET	31:0	Write sets the selected bits in IPC4, read yields undefined value							
IPC4INV	31:0	Write inverts the selected bits in IPC4, read yields undefined value							
IPC5	31:24	—	—	—	SPI1IP<2:0>			SPI1IS<1:0>	
	23:16	—	—	—	OC5IP<2:0>			OC5IS<1:0>	
	15:8	—	—	—	IC5IP<2:0>			IC5IS<1:0>	
	7:0	—	—	—	T5IP<2:0>			T5IS<1:0>	
IPC5CLR	31:0	Write clears the selected bits in IPC5, read yields undefined value							
IPC5SET	31:0	Write sets the selected bits in IPC5, read yields undefined value							
IPC5INV	31:0	Write inverts the selected bits in IPC5, read yields undefined value							
T2CON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	FRZ	SIDL	—	—	—	—	—
	7:0	TGATE	TCKPS<2:0>			T32	—	TCS	—
T2CONCLR	31:0	Write clears selected bits in T2CON; read yields undefined value							
T2CONSET	31:0	Write sets selected bits in T2CON; read yields undefined value							
T2CONINV	31:0	Write inverts selected bits in T2CON; read yields undefined value							
T3CON	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	FRZ	SIDL	—	—	—	—	—
	7:0	TGATE	TCKPS<2:0>			—	—	TCS	—
T3CONCLR	31:0	Write clears selected bits in T3CON; read yields undefined value							
T3CONSET	31:0	Write sets selected bits in T3CON; read yields undefined value							
T3CONINV	31:0	Write inverts selected bits in T3CON; read yields undefined value							

Table 16-1: Output Compare SFR Summary (Continued)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
TMR2	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	TMRx<15:8>							
	7:0	TMRx<7:0>							
TMR2CLR	31:0	Write clears selected bits in TMRx, read yields undefined value							
TMR2SET	31:0	Write sets selected bits in TMRx, read yields undefined value							
TMR2INV	31:0	Write inverts selected bits in TMRx, read yields undefined value							
TMR3	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	TMRx<15:8>							
	7:0	TMRx<7:0>							
TMR3CLR	31:0	Write clears selected bits in TMRx, read yields undefined value							
TMR3SET	31:0	Write sets selected bits in TMRx, read yields undefined value							
TMR3INV	31:0	Write inverts selected bits in TMRx, read yields undefined value							
PR2	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	PR2<15:8>							
	7:0	PR2<7:0>							
PR2CLR	31:0	Write clears selected bits in PR2; read yields undefined value							
PR2SET	31:0	Write sets selected bits in PR2; read yields undefined value							
PR2INV	31:0	Write inverts selected bits in PR2; read yields undefined value							
PR3	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	PR3<15:8>							
	7:0	PR3<7:0>							
PR3CLR	31:0	Write clears selected bits in PR3; read yields undefined value							
PR3SET	31:0	Write sets selected bits in PR3; read yields undefined value							
PR3INV	31:0	Write inverts selected bits in PR3; read yields undefined value							

Register 16-1: OCxCON: Output Compare 'x' Control Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	r-x	r-x	r-x
ON	FRZ	SIDL	—	—	—	—	—
bit 15							bit 8

r-x	r-x	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	OC32	OCFLT	OCTSEL	OCM<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31-16 **Reserved:** Write '0'; ignore read

bit 15 **ON:** Output Compare Peripheral On bit
- 1 = Output Compare peripheral is enabled.
- 0 = Output Compare peripheral is disabled and not drawing current. SFR modifications are allowed. The status of other bits in this register are not affected by setting or clearing this bit.

Note: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

bit 14 **FRZ:** Freeze in Debug Exception Mode bit
- 1 = Freeze operation when CPU enters Debug Exception mode
- 0 = Continue operation when CPU enters Debug Exception mode

Note: FRZ is writable in Debug Exception mode only, it is forced to '0' in normal mode.

bit 13 **SIDL:** Stop in IDLE Mode bit
- 1 = Discontinue operation when CPU enters IDLE mode
- 0 = Continue operation in IDLE mode

bit 12-6 **Reserved:** Write '0'; ignore read

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisions to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(1)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

Note: This bit is only used when OCM<2:0> = '111'.

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this OCMP module
- 0 = Timer2 is the clock source for this OCMP module

Refer to the device data sheet for specific time bases available to the Output Compare module.

Note 1: Reads as '0' in modes other than PWM mode.

Register 16-1: OCxCON: Output Compare 'x' Control Register (Continued)

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: Reads as '0' in modes other than PWM mode.

Register 16-2: OCxCONCLR: Output Compare 'x' Control Clear Register

R/W-x	
Write clears selected bits in OCxCON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in OCxCON**

A write of '1' in one or more bit positions clears the corresponding bit(s) in OCxCON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxCONCLR = 0x00008001` will clear bits 15 and 0 in the OCxCON register.
`localValue = OCxCONCLR` will yield an undefined value.

Register 16-3: OCxCONSET: Output Compare 'x' Control Set Register

R/W-x	
Write sets selected bits in OCxCON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in OCxCON**

A write of '1' in one or more bit positions sets the corresponding bit(s) in OCxCON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxCONSET = 0x00008001` will set bits 15 and 0 in the OCxCON register.
`localValue = OCxCONSET` will yield an undefined value.

Register 16-4: OCxCONINV: Output Compare 'x' Control Invert Register

R/W-x	
Write inverts selected bits in OCxCON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in OCxCON**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in OCxCON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxCONINV = 0x00008001` will invert bits 15 and 0 in the OCxCON register.
`localValue = OCxCONINV` will yield an undefined value.

Register 16-5: OCxR: Output Compare 'x' Compare Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCR<31:24>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCR<23:16>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31-16 **OCxR<31:16>:** Upper 16 bits of 32-bit compare value, when OC32 (OCxCON<5>) = 1

bit 15-0 **OCxR<15:0>:** Lower 16 bits of 32-bit compare value or entire 16 bits of 16-bit compare value when OC32 = 0

Register 16-6: OCxRCLR: Output Compare 'x' Compare Clear Register

R/W-x	
Write clears selected bits in OCxR, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in OCxR**

A write of '1' in one or more bit positions clears the corresponding bit(s) in OCxR register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRCLR = 0x00008001` will clear bits 15 and 0 in the OCxR register.
`localValue = OCxRCLR` will yield an undefined value.

Register 16-7: OCxRSET: Output Compare 'x' Compare Set Register

R/W-x	
Write sets selected bits in OCxR, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in OCxR**

A write of '1' in one or more bit positions sets the corresponding bit(s) in OCxR register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRSET = 0x00008001` will set bits 15 and 0 in the OCxR register.
`localValue = OCxRSET` will yield an undefined value.

Register 16-8: OCxRINV: Output Compare 'x' Compare Invert Register

R/W-x	
Write inverts selected bits in OCxR, read yields undefined value	
bit 31	bit 0

31-0 **Inverts selected bits in OCxR**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in OCxR register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRINV = 0x00008001` will invert bits 15 and 0 in the OCxR register.
`localValue = OCxRINV` will yield an undefined value.

Register 16-9: OCxRS: Output Compare x Secondary Compare Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRS<31:24>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRS<23:16>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRS<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRS<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **OCxRS<31:16>:** Upper 16 bits of 32-bit compare value when OC32 (OCxCON<5>) = 1

bit 15-0 **OCxRS<15:0>:** Lower 16 bits of 32-bit compare value or entire 16 bits of 16-bit compare value when OC32 = 0

Register 16-10: OCxRSCLR: Output Compare 'x' Secondary Compare Clear Register

R/W-x	
Write clears selected bits in OCxRS, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in OCxRS**

A write of '1' in one or more bit positions clears the corresponding bit(s) in OCxRS register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRSCLR = 0x00008001` will clear bits 15 and 0 in the OCxRS register.
`localValue = OCxRSCLR` will yield an undefined value.

Register 16-11: OCxRSSET: Output Compare 'x' Secondary Compare Set Register

R/W-x	
Write sets selected bits in OCxRS, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in OCxRS**

A write of '1' in one or more bit positions sets the corresponding bit(s) in OCxRS register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRSSET = 0x00008001` will set bits 15 and 0 in the OCxRS register.
`localValue = OCxRSSET` will yield an undefined value.

Register 16-12: OCxRSINV: Output Compare 'x' Secondary Compare Invert Register

R/W-x	
Write inverts selected bits in OCxRS, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in OCxRS**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in OCxRS register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Examples: `OCxRSINV = 0x00008001` will invert bits 15 and 0 in the OCxRS register.
`localValue = OCxRSINV` will yield an undefined value.

Register 16-13: IFS0: Interrupt Flag Status Register 0(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	SPI1EIF
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1IF	OC1IF	IC1IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF
bit 7							bit 0

Legend:			
R = readable bit	W = writable bit	P = programmable	r = reserved bit
U = unimplemented bit, read as '0'		-n = bit value at POR: ('0', '1', x = unknown)	

bit 22 **OC5IF:** Output Compare 5 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 18 **OC4IF:** Output Compare 4 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 14 **OC3IF:** Output Compare 3 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 10 **OC2IF:** Output Compare 2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 6 **OC1IF:** Output Compare 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-14: IEC0: Interrupt Enable Control Register 0(1)

I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE	SPI1EIE
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE
bit 7							bit 0

Legend:			
R = readable bit	W = writable bit	P = programmable	r = reserved bit
U = unimplemented bit, read as '0'		-n = bit value at POR: ('0', '1', x = unknown)	

bit 22 **OC5IE:** Output Compare 5 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **OC4IE:** Output Compare 4 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 14 **OC3IE:** Output Compare 3 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 10 **OC2IE:** Output Compare 2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **OC1IE:** Output Compare 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-15: IPC1: Interrupt Priority Control Register 1(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IP<2:0>			INT1IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OC1IP<2:0>			OC1IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IC1IP<2:0>			IC1IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	T1IP<2:0>			T1IS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20-18 **OC1IP<2:0>:** Output Compare 1 Interrupt Priority bits
- 111 = Interrupt priority is 7
- 110 = Interrupt priority is 6
- 101 = Interrupt priority is 5
- 100 = Interrupt priority is 4
- 011 = Interrupt priority is 3
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **OC1IS<1:0>:** Output Compare 1 Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-16: IPC2: Interrupt Priority Control Register 2(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT2IP<2:0>			INT2IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OC2IP<2:0>			OC2IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IC2IP<2:0>			IC2IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	T2IP<2:0>			T2IS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20 - 18 **OC2IP<2:0>:** Output Compare 2 Interrupt Priority bits

111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 17-16 **OC2IS<1:0>:** Output Compare 2 Interrupt Subpriority bits

11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-17: IPC3: Interrupt Priority Control Register 3(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT3IP<2:0>			INT3IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OC3IP<2:0>			OC3IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IC3IP<2:0>			IC3IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	T3IP<2:0>			T3IS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20-18 **OC3IP<2:0>:** Output Compare 3 Interrupt Priority bits
- 111 = Interrupt priority is 7
- 110 = Interrupt priority is 6
- 101 = Interrupt priority is 5
- 100 = Interrupt priority is 4
- 011 = Interrupt priority is 3
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **OC3IS<1:0>:** Output Compare 3 Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-18: IPC4: Interrupt Priority Control Register 4(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4IP<2:0>			INT4IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OC4IP<2:0>			OC4IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IC4IP<2:0>			IC4IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	T4IP<2:0>			T4IS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20-18 **OC4IP<2:0>:** Output Compare 4 Interrupt Priority bits

111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 17-16 **OC4IS<1:0>:** Output Compare 4 Interrupt Subpriority bits

11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-19: IPC5: Interrupt Priority Control Register 5(1)

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	SPI1IP<2:0>			SPI1IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OC5IP<2:0>			OC5IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	IC5IP<2:0>			IC5IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	T5IP<2:0>			T5IS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 20-18 **OC5IP<2:0>:** Output Compare 5 Interrupt Priority bits
- 111 = Interrupt priority is 7
- 110 = Interrupt priority is 6
- 101 = Interrupt priority is 5
- 100 = Interrupt priority is 4
- 011 = Interrupt priority is 3
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **OC5IS<1:0>:** Output Compare 5 Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

Note 1: Shaded bit names in this Interrupt register control other PIC32MX peripherals and are not related to the output compare module.

Register 16-20: T2CON: Time Base Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	r-x	r-x	r-x
ON	FRZ	SIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	r-x	R/W-0	r-x
TGATE	TCKPS<2:0>			T32	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 15 **ON:** TMR2 On bit

1 = Peripheral is enabled
0 = Peripheral is disabled

Note: When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

bit 14 **FRZ:** Freeze in Debug Exception Mode bit

1 = Freeze operation when CPU is in Debug Exception mode
0 = Continue operation even when CPU is in Debug Exception mode

Note: FRZ is writable in Debug Exception mode only, it is forced to ‘0’ in normal mode.

bit 13 **SIDL:** Stop in IDLE Mode bit

1 = Discontinue operation when device enters IDLE mode
0 = Continue operation even in IDLE mode

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored and reads as ‘0’
When TCS = ‘0’:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits

111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **T32:** 32-bit Timer Mode Select bits

1 = TMR2 and TMR3 form a 32-bit timer
0 = TMR2 and TMR3 are separate 16-bit timers

Register 16-20: T2CON: Time Base Register (Continued)

bit 1 **TCS:** TMR2 Clock Source Select bit

1 = External clock from T2CK pin

0 = Internal peripheral clock

Register 16-21: T2CONCLR: Time Base Register

R/W-x	
Write clears selected bits in T2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in T2CON**

A write of '1' in one or more bit positions clears the corresponding bit(s) in T2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T2CONCLR = 0x00008000` will clear bit 15 in the T2CON register.

Register 16-22: T2CONSET: Output Compare 'x' Secondary Compare Set Register

R/W-x	
Write sets selected bits in T2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in T2CON**

A write of '1' in one or more bit positions sets the corresponding bit(s) in T2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T2CONSET = 0x00008000` will set bit 15 in the T2CON register.

Register 16-23: T2CONINV: Output Compare 'x' Secondary Compare Invert Register

R/W-x	
Write inverts selected bits in T2CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in T2CON**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in T2CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T2CONINV = 0x00008000` will invert bit 15 in the T2CON register.

Register 16-24: TMR2: Timer Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 15-0 **TMR2<15:0>:** Timer Count Register

16-bit mode:
These bits represent the complete 16-bit timer count.

32-bit mode (Timer Type B only):
Timer2 and Timer4
These bits represent the least significant half word (16 bits) of the 32-bit timer count.

Register 16-25: TMR2CLR: Timer Clear Register

Write clears selected bits in TMR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in TMR2**

A write of '1' in one or more bit positions clears the corresponding bit(s) in TMR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR2CLR = 0x00008001` will clear bits 15 and 0 in TMR2 register.

Register 16-26: TMR2SET: Timer Set Register

Write sets selected bits in TMR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in TMR2**

A write of '1' in one or more bit positions sets the corresponding bit(s) in TMR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR2SET = 0x00008001` will set bits 15 and 0 in TMR2 register.

Register 16-27: TMR2INV: Timer Invert Register

Write inverts selected bits in TMR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in TMR2**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in TMR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR2INV = 0x00008001` will invert bits 15 and 0 in TMR2 register.

Register 16-28: PR2: Period Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **PR<31:16>:** Unimplemented

bit 15-0 **PR<15:0>:** 16-bit Timer2 period match value. Provides lower half of the 32-bit period match value when Timer2 and Timer3 are configured to form a 32-bit timer.

Register 16-29: PR2CLR: Period 2 Clear Register

R/W-x	
Write clears selected bits in PR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in PR2**

A write of '1' in one or more bit positions clears the corresponding bit(s) in PR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR2CLR = 0x00008001` will clear bits 15 and 0 in the PR2 register.

Register 16-30: PR2SET: Period 2 Set Register

R/W-x	
Write sets selected bits in PR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in PR2**

A write of '1' in one or more bit positions sets the corresponding bit(s) in PR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR2SET = 0x00008001` will set bits 15 and 0 in the PR2 register.

Register 16-31: PR2INV: Period 2 Invert Register

R/W-x	
Write inverts selected bits in PR2, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in PR2**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in PR2 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR2INV = 0x00008001` will invert bits 15 and 0 in the PR2 register.

Register 16-32: T3CON: Time Base Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	r-x	r-x	r-x
ON	FRZ	SIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	r-0	r-x	R/W-0	r-x
TGATE	TCKPS<2:0>			—	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 15 **ON:** TMR3 On bit

1 = Peripheral is enabled
0 = Peripheral is disabled

Note: When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

bit 14 **FRZ:** Freeze in Debug Exception Mode bit

1 = Freeze operation when CPU is in Debug Exception mode
0 = Continue operation even when CPU is in Debug Exception mode

Note: FRZ is writable in Debug Exception mode only, it is forced to ‘0’ in normal mode.

bit 13 **SIDL:** Stop in IDLE Mode bit

1 = Discontinue operation when device enters IDLE mode
0 = Continue operation even in IDLE mode

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored and reads ‘0’
When TCS = ‘0’:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits

111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 1 **TCS:** TMR3 Clock Source Select bit

1 = External clock from T3CK pin
0 = Internal peripheral clock

Register 16-33: T3CONCLR: Time Base Register

R/W-x	
Write clears selected bits in T3CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in T3CON**

A write of '1' in one or more bit positions clears the corresponding bit(s) in T3CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T3CONCLR = 0x00008000` will clear bit 15 in the T3CON register.

Register 16-34: T3CONSET: Output Compare 'x' Secondary Compare Set Register

R/W-x	
Write sets selected bits in T3CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in T2CON**

A write of '1' in one or more bit positions sets the corresponding bit(s) in T3CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T3CONSET = 0x00008000` will set bit 15 in the T3CON register.

Register 16-35: T3CONINV: Output Compare 'x' Secondary Compare Invert Register

R/W-x	
Write inverts selected bits in T3CON, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in T3CON**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in T3CON register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `T3CONINV = 0x00008000` will invert bit 15 in the T3CON register.

Register 16-36: TMR3: Timer Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 15-0 **TMR3<15:0>:** Timer Count Register

16-bit mode:
These bits represent the complete 16-bit timer count.

32-bit mode (Timer Type B only):
Timer3 and Timer5
These bits represent the most significant half word (16 bits) of the 32-bit timer count.

Register 16-37: TMR3CLR: Timer Clear Register

Write clears selected bits in TMR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in TMR3**

A write of '1' in one or more bit positions clears the corresponding bit(s) in TMR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR3CLR = 0x00008001` will clear bits 15 and 0 in TMR3 register.

Register 16-38: TMR3SET: Timer Set Register

Write sets selected bits in TMR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in TMR3**

A write of '1' in one or more bit positions sets the corresponding bit(s) in TMR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR3SET = 0x00008001` will set bits 15 and 0 in TMR3 register.

Register 16-39: TMR3INV: Timer Invert Register

Write inverts selected bits in TMR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in TMR3**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in TMR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `TMR3INV = 0x00008001` will invert bits 15 and 0 in TMR3 register.

Register 16-40: PR3: Period 3 Register

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **PR<31:16>:** Unimplemented

bit 15-0 **PR<15:0>:** 16-bit Timer3 period match value. Provides upper half of the 32-bit period match value when Timer 2 and Timer3 are configured to form a 32-bit timer.

Register 16-41: PR3CLR: Period 3 Clear Register

R/W-x	
Write clears selected bits in PR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Clears selected bits in PR3**

A write of '1' in one or more bit positions clears the corresponding bit(s) in PR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR3CLR = 0x8001` will clear bits 15 and 0 in the PR3 register.

Register 16-42: PR3SET: Period 3 Set Register

R/W-x	
Write sets selected bits in PR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Sets selected bits in PR3**

A write of '1' in one or more bit positions sets the corresponding bit(s) in PR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR3SET = 0x00008001` will set bits 15 and 0 in the PR3 register.

Register 16-43: PR3INV: Period 3 Invert Register

R/W-x	
Write inverts selected bits in PR3, read yields undefined value	
bit 31	bit 0

bit 31-0 **Inverts selected bits in PR3**

A write of '1' in one or more bit positions inverts the corresponding bit(s) in PR3 register and does not affect unimplemented or read-only bits. A write of '0' will not affect the register.

Example: `PR3INV = 0x00008001` will invert bits 15 and 0 in the PR3 register.

16.3 OPERATION

Each Output Compare module has the following modes of operation:

- Single Compare Match mode
  - With output drive high
  - With output drive low
  - With output drive toggles
- Dual Compare Match mode
  - With single output pulse
  - With continuous output pulses
- Simple Pulse-Width Modulation mode
  - Without fault protection input
  - With fault protection input

Notes: It is required that the user turn off the Output Compare module (i.e., clear OCM<2:0> (OCxCON<2:0>)) before switching to a new mode. Changing modes while the module is in operation may produce unexpected results.

In this section, a reference to any SFRs associated with the selected timer source is indicated by a 'y' suffix. For example, PR2 is the Period register for the selected timer source, while TyCON is the Timer Control register for the selected timer source.

16.3.1 Single Compare Match Mode

When control bits OCM<2:0> (OCxCON<2:0>) are set to '001', '010' or '011', the selected output compare channel is configured for one of three Single Output Compare Match modes. The compare time base must also be enabled.

In the Single Compare mode, the OCxR register is loaded with a value and is compared to the selected incrementing timer register, TMRy. On a compare match event, one of the following events will take place:

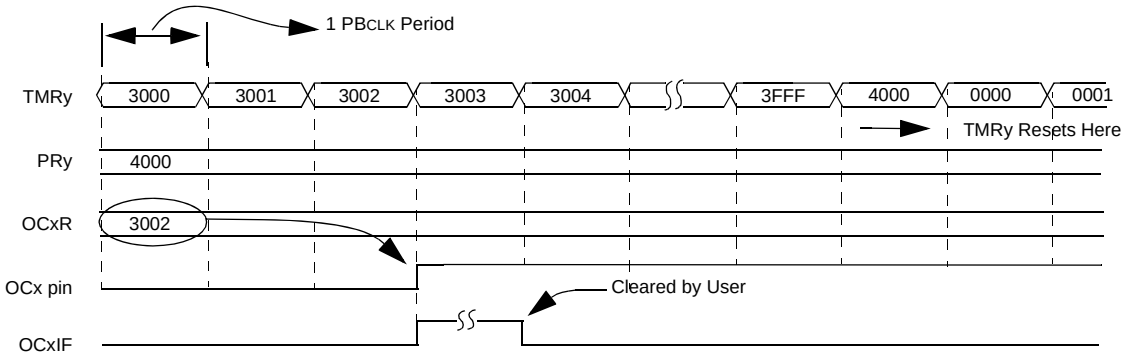
- Compare forces OCx pin high; initial state of pin is low. Interrupt is generated on the single compare match event.
- Compare forces OCx pin low; initial state of pin is high. Interrupt is generated on the single compare match event.
- Compare toggles OCx pin. Toggle event is continuous and an interrupt is generated for each toggle event.

16.3.1.1 Compare Mode Output Driven High

To configure the Output Compare module for this mode, set control bits OCM<2:0> = '001'. The compare time base must also be enabled. Once this Compare mode has been enabled, the output pin, OCx, will be driven low and remain low until a match occurs between the TMRy and OCxR registers. Please note the following key timing events (refer to Figure 16-2):

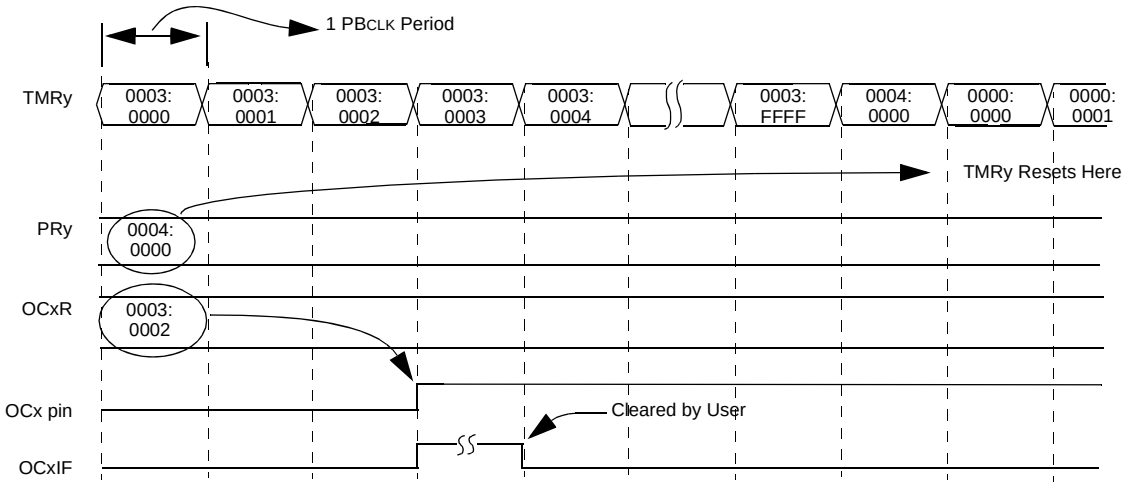
- The OCx pin is driven high one peripheral clock after the compare match occurs between the compare time base and the OCxR register. The OCx pin will remain high until a mode change has been made or the module is disabled.
- The compare time base will count up to the value contained in the associated period register and then reset to 0x0000 on the next PBCLK.
- The respective channel interrupt flag, OCxIF (refer to the IFS0 register for the position of the interrupt flag bit for each of the Output Compare channels), is asserted when the OCx pin is driven high.

Figure 16-2: Single Compare Mode: Set OCx High on Compare Match Event (16-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-3: Single Compare Mode: Set OCx High on Compare Match Event (32-Bit Mode)



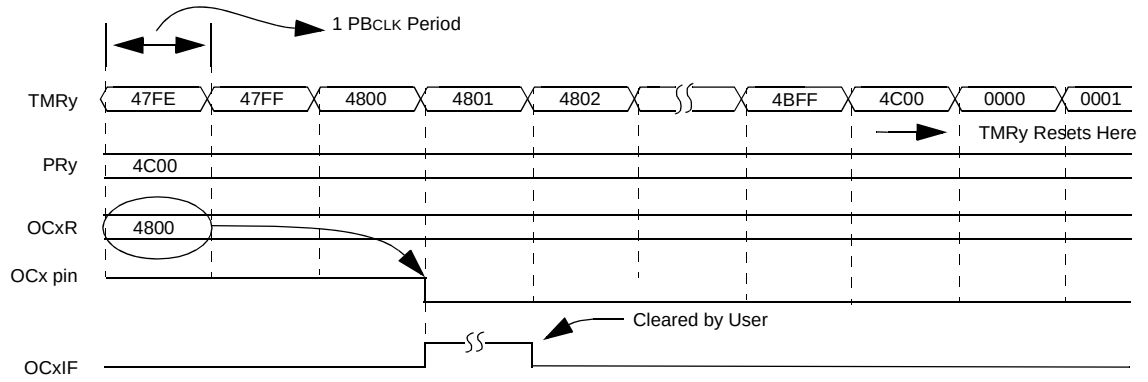
Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

16.3.1.2 Compare Mode Output Driven Low

To configure the output compare module for this mode, set control bits OCM<2:0> = '010'. The compare time base must also be enabled. Once this Compare mode has been enabled, the output pin, OCx, will be driven high and remain high until a match occurs between the Timer and OCxR registers. Please note the following key timing events (refer to Figure 16-4):

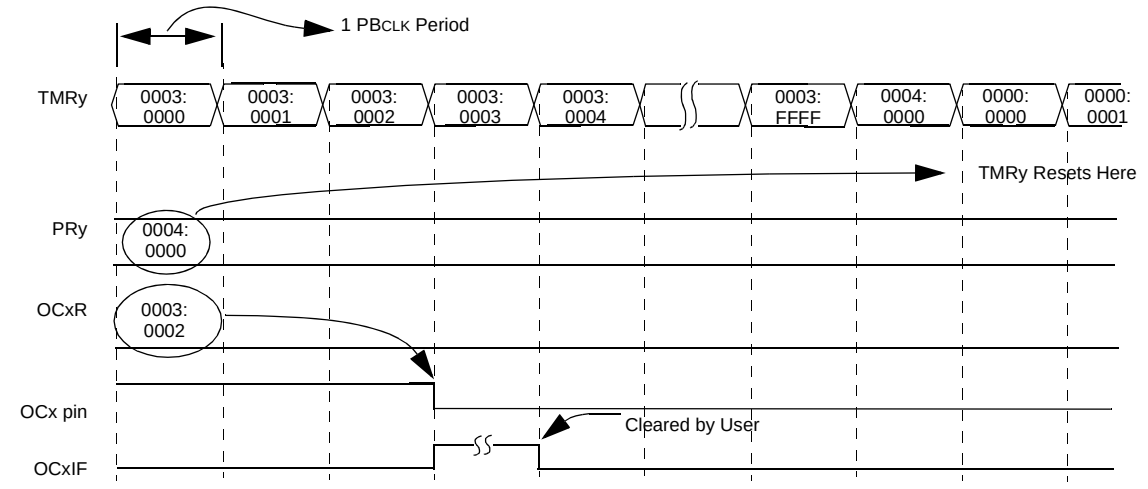
- The OCx pin is driven low one PBCLK after the compare match occurs between the compare time base and the OCxR register. The OCx pin will remain low until a mode change has been made or the module is disabled.
- The compare time base will count up to the value contained in the associated period register and then reset to 0x0000 on the next PBCLK .
- The respective channel interrupt flag, OCxIF, is asserted when the OCx pin is driven low.

Figure 16-4: Single Compare Mode: Force OCx Low on Compare Match Event (16-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-5: Single Compare Mode: Set OCx Low on Compare Match Event (32-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

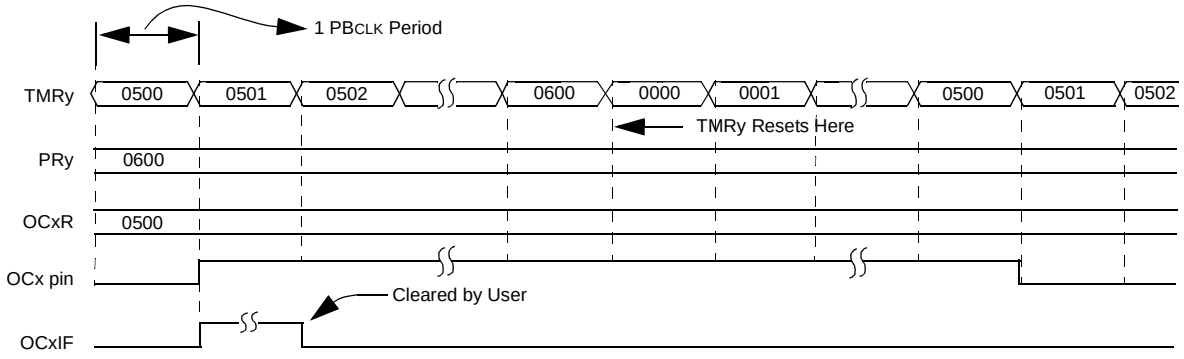
16.3.1.3 Single Compare Mode Toggle Output

To configure the Output Compare module for this mode, set control bits OCM<2:0> = '011'. In addition, Timer2 or Timer3 must be selected and enabled. Once this Compare mode has been enabled, the output pin, OCx, will be initially driven low and then toggle on each and every subsequent match event between the Timer and OCxR registers. Please note the following key timing events (refer to Figure 16-6 and Figure 16-8):

- The OCx pin is toggled one PBCLK after the compare match occurs between the compare time base and the OCxR register. The OCx pin will remain at this new state until the next toggle event, or until a mode change has been made or the module is disabled.
- The compare time base will count up to the contents in the period register and then reset to 0x0000 on the next PBCLK .
- The respective channel interrupt flag, OCxIF, is asserted when the OCx pin is toggled.

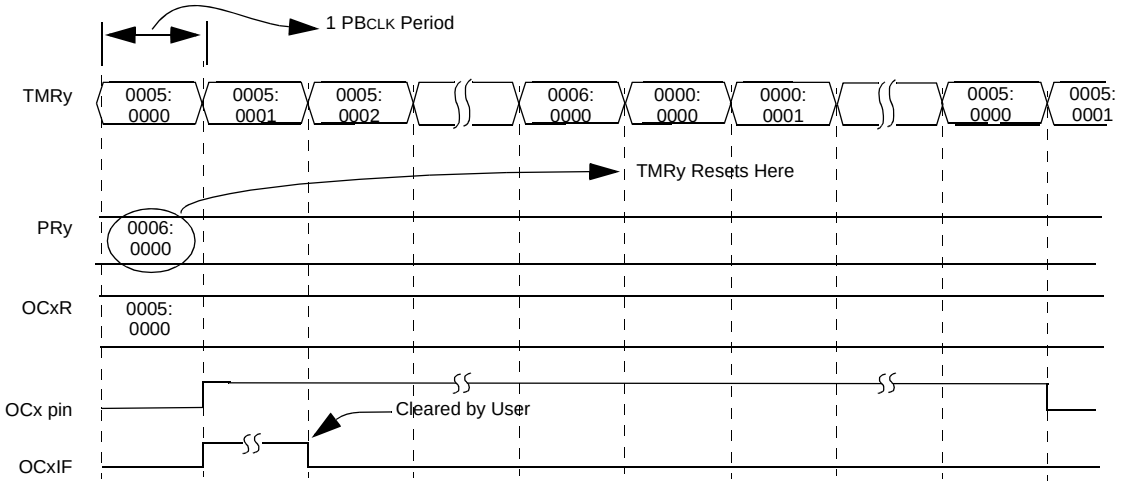
Note:	The internal OCx pin output logic is set to a logic '0' on a device Reset. However, the operational OCx pin state for the Toggle mode can be set by the user software. Example 16-1 shows a code example for defining the desired initial OCx pin state in the Toggle mode of operation.

Figure 16-6: Single Compare Mode: Toggle Output on Compare Match Event (16-Bit Mode)



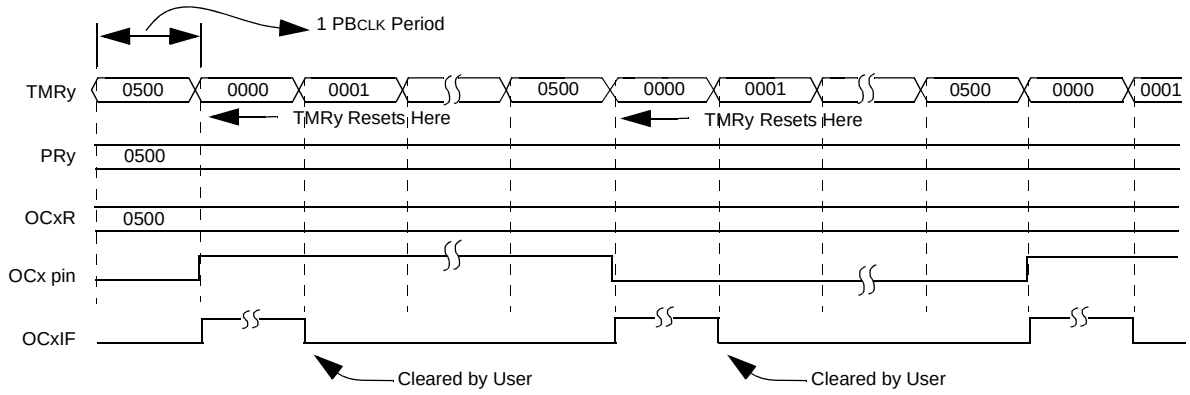
Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-7: Single Compare Mode: Toggle Output on Compare Match Event (32-Bit Mode)



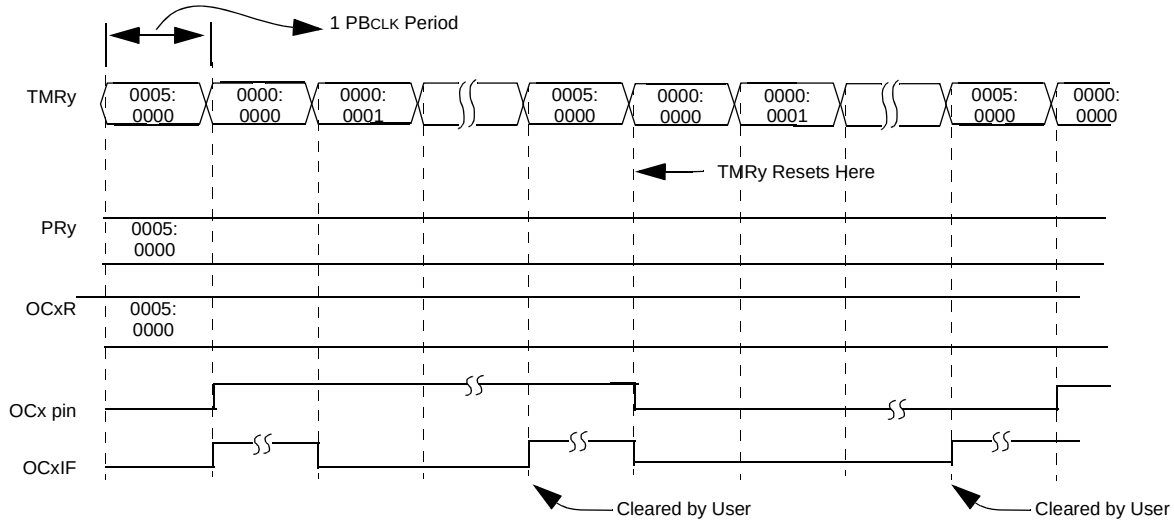
Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-8: Single Compare Mode: Toggle Output on Compare Match Event (PRy = OCxR, 16-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-9: Single Compare Mode: Toggle Output on Compare Match Event (PRy = OCxR, 32-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Example 16-1: Compare Mode Toggle Mode Pin State Setup (16-Bit Mode)

```
// The following code example illustrates how to define the initial
// OC1 pin state for the output compare toggle mode of operation.

                                    // Toggle mode with initial OC1 pin state set low

OC1CON = 0x0001;                    // Configure module for OC1 pin low, toggle high
OC1CONSET = 0x8000;                 // Enable OC1 module
```


Example 16-2: Compare Mode Toggle Mode Pin State Setup (32-Bit Mode)

```
// The following code example illustrates how to define the initial
// OC1 pin state for the output compare toggle mode of operation.

                                    // Toggle mode with initial OC1 pin state set low

OC1CON = 0x0021;                    // Configure module for OC1 pin low, toggle high,
                                    // 32-bit mode
OC1CONSET = 0x8000;                 // Enable OC1 module
```

Example 16-3 shows example code for the configuration and interrupt service of the Single Compare mode toggle event.

Example 16-3: Compare Mode Toggle Setup and Interrupt Servicing (16-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the toggle event and select Timer2 as the clock
// source for the compare time base.

T2CON = 0x0010;                     // Configure Timer2 for a prescaler of 2

OC1CON = 0x0000;                    // Turn off OC1 while doing setup.
OC1CON = 0x0003;                    // Configure for compare toggle mode
OC1R = 0x0500;                      // Initialize Compare Register 1
PR2 = 0x0500;                       // Set period

                                    // Configure int
IFS0CLR = 0x0040;                   // Clear the OC1 interrupt flag
IEC0SET = 0x040;                    // Enable OC1 interrupt
IPC1SET = 0x001C0000;               // Set OC1 interrupt priority to 7,
                                    // the highest level
IPC1SET = 0x00030000;               // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                  // Enable Timer 2
OC1CONSET = 0x8000;                 // Enable OC1

// Example code for Output Compare 1 ISR:

void __ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                   // Clear the OC1 interrupt flag
}
```

Example 16-4: Compare Mode Toggle Setup and Interrupt Servicing (32-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the toggle event and select the Timer2/Timer3 pair as
// the 32-bit as the clock source for the compare time base.

T2CON = 0x0018;                       // Configure Timer2 for 32-bit operation
                                      // with a prescaler of 2. The Timer2/Timer3
                                      // pair is accessed via registers associated
                                      // with the Timer2 register

OC1CON = 0x0000;                      // Turn off OC1 while doing setup.
OC1CON = 0x0023;                      // Configure for compare toggle mode
OC1R = 0x00500000;                    // Initialize Compare Register 1
PR2 = 0x00500000;                     // Set period (PR2 is now 32-bits wide)

                                      // configure int
IFS0CLR = 0x00000040;                 // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;                 // Enable OC1 interrupt
IPC1SET = 0x001C0000;                 // Set OC1 interrupt priority to 7,
                                      // the highest level
IPC1SET = 0x00030000;                 // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                    // Enable Timer2
OC1CONSET = 0x8000;                   // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR (_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntlHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                     // Clear the OC1 interrupt flag
}
```


16.3.2 Dual Compare Match Mode

When control bits OCM<2:0> = 100 or '101' (OCxCON<2:0>), the selected output compare channel is configured for one of two Dual Compare Match modes:

- Single Output Pulse mode
- Continuous Output Pulse mode

In the Dual Compare mode, the module uses both the OCxR and OCxRS registers for the compare match events. The OCxR register is compared against the incrementing timer count, TMRy, and the leading (rising) edge of the pulse is generated at the OCx pin on a compare match event. The OCxRS register is then compared to the same incrementing timer count, TMRy, and the trailing (falling) edge of the pulse is generated at the OCx pin on a compare match event.

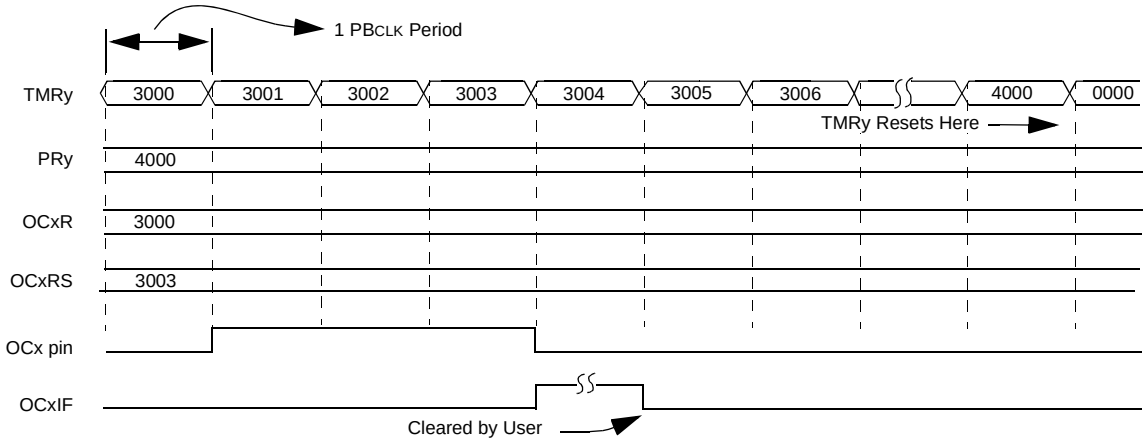
16.3.2.1 Dual Compare Mode: Single Output Pulse

To configure the Output Compare module for the Single Output Pulse mode, set control bits OCM<2:0> = 100. In addition, the compare time base must be selected and enabled. Once this mode has been enabled, the output pin, OCx, will be driven low and remain low until a match occurs between the time base and OCxR registers. Please note the following key timing events (refer to Figure 16-10 and Figure 16-12):

- The OCx pin is driven high one peripheral clock after the compare match occurs between the compare time base and the OCxR register. The OCx pin will remain high until the next match event occurs between the time base and the OCxRS register. At this time, the pin will be driven low. The OCx pin will remain low until a mode change has been made or the module is disabled.
- The compare time base will count up to the value contained in the associated period register and then reset to 0x0000 on the next instruction clock.
- If the time base period register contents are less than the OCxRS register contents, then no falling edge of the pulse is generated. The OCx pin will remain high until OCxRS <= PR2, or a mode change or Reset condition has occurred.
- The respective channel interrupt flag, OCxIF, is asserted when the OCx pin is driven low (falling edge of single pulse).

Figure 16-10 depicts the General Dual Compare mode generating a single output pulse. Figure 16-12 depicts another timing example where OCxRS > PR2. In this example, no falling edge of the pulse is generated because the compare time base resets before counting up to 0x4100.

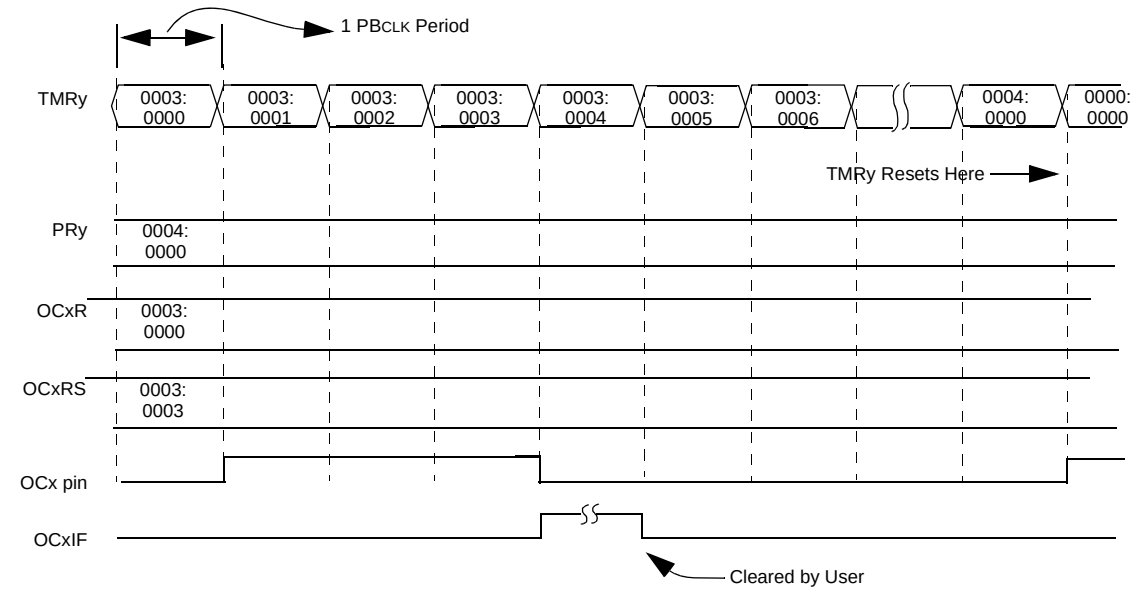
Figure 16-10: Dual Compare Mode (16-Bit Mode)



Note 1: An 'x' represents the output compare channel number. A 'y' represents the time base number.

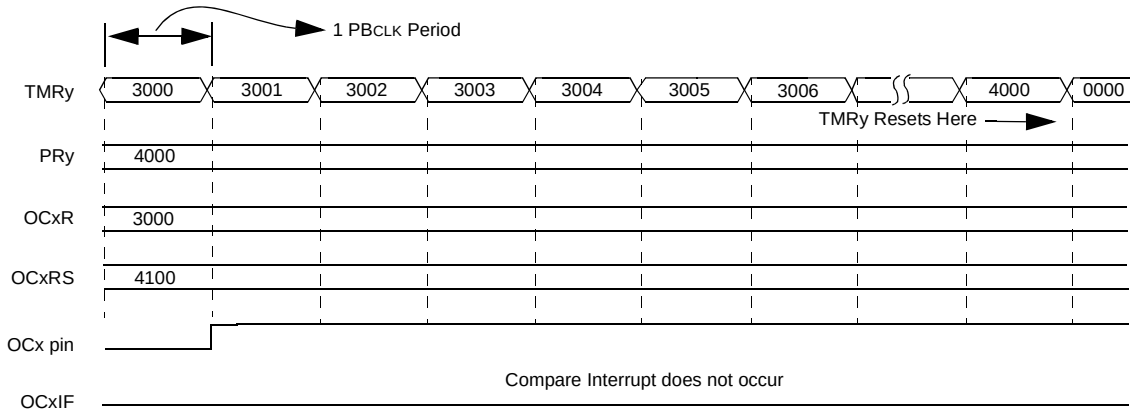
2: OCxR = Compare Register; OCxRS = Secondary Compare Register.

Figure 16-11: Dual Compare Mode (32-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

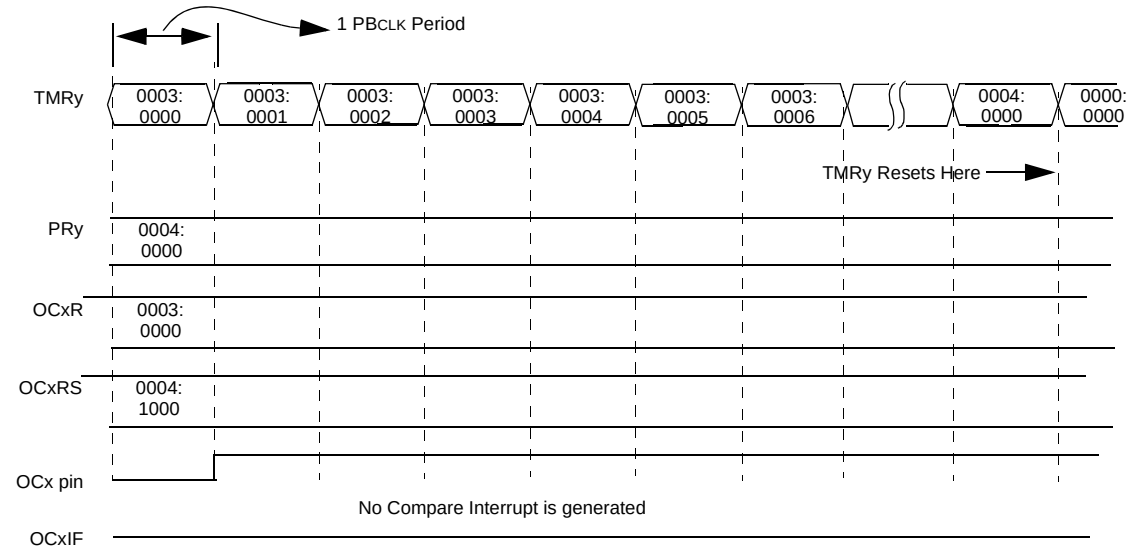
Figure 16-12: Dual Compare Mode: Single Output Pulse (OCxRS > PRy, 16-Bit Mode)



Note 1: An 'x' represents the output compare channel number. A 'y' represents the time base number.

2: OCxR = Compare Register; OCxRS = Secondary Compare Register.

Figure 16-13: Dual Compare Mode: Single Output Pulse (OCxRS > PRy, 32-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

16.3.2.2 Setup for Single Output Pulse Generation

When control bits OCM<2:0> (OCxCON<2:0>) are set to '100', the selected output compare channel initializes the OCx pin to the low state and generates a single output pulse.

To generate a single output pulse, the following steps are required (these steps assume the timer source is initially turned off, but this is not a requirement for the module operation):

1. Determine the peripheral clock cycle time.
2. Calculate the time to the rising edge of the output pulse relative to the TMRy start value (0x0000).
3. Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
4. Write the values computed in steps 2 and 3 above into the compare register, OCxR, and the secondary compare register, OCxRS, respectively.
5. Set the timer period register, PRy, to value equal to or greater than value in OCxRS, the secondary compare register.
6. Set OCM<2:0> = 100 and the OCTSEL (OCxCON<3>) bit to the desired timer source. The OCx pin state will now be driven low.
7. Set the ON (TyCON<15>) bit to '1', to enable the timer.
8. Upon the first match between TMRy and OCxR, the OCx pin will be driven high.
9. When the incrementing timer, TMRy, matches the secondary compare register, OCxRS, the second and trailing edge (high-to-low) of the pulse is driven onto the OCx pin. No additional pulses are driven onto the OCx pin and it remains at low. As a result of the second compare match event, the OCxIF interrupt flag bit is set, which will result in an interrupt (if it is enabled by setting the OCxIE bit). For further information on peripheral interrupts, refer to **Section 8. "Interrupts"**.
10. To initiate another single pulse output, change the timer and compare register settings, if needed, and then issue a write to set the OCM<2:0> (OCxCON<2:0>) bits to '100'. Disabling and re-enabling of the timer and clearing the TMRy register are not required, but may be advantageous for defining a pulse from a known event time boundary.

The Output Compare module does not have to be disabled after the falling edge of the output pulse. Another pulse can be initiated by rewriting the value of the OCxCON register.

Examples 16-5 and 16-6 show example code for configuration of the single output pulse event.

Example 16-5: Single Output Pulse Setup and Interrupt Servicing (16-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the single pulse event and select Timer2
// as the clock source for the compare time base.

T2CON = 0x0010;                       // Configure Timer2 for a prescaler of 2

OC1CON = 0x0000;                      // Turn off OC1 while doing setup.
OC1CON = 0x0004;                      // Configure for single pulse mode
OC1R = 0x3000;                        // Initialize primary Compare Register
OC1RS = 0x3003;                       // Initialize secondary Compare Register
PR2 = 0x3003;                         // Set period (PR2 is now 32-bits wide)

                                      // configure int
IFS0CLR = 0x00000040;                 // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;                 // Enable OC1 interrupt
IPC1SET = 0x001C0000;                 // Set OC1 interrupt priority to 7,
                                      // the highest level
IPC1SET = 0x00030000;                 // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                    // Enable Timer2
OC1CONSET = 0x8000;                   // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                     // Clear the OC1 interrupt flag
}
```

Example 16-6: Single Output Pulse Setup and Interrupt Servicing (32-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the single pulse event and select Timer2
// as the clock source for the compare time base.

T2CON = 0x0018;                     // Configure Timer2 for 32-bit operation
                                    // with a prescaler of 2. The Timer2/Timer3
                                    // pair is accessed via registers associated
                                    // with the Timer2 register

OC1CON = 0x0000;                    // Turn off OC1 while doing setup.
OC1CON = 0x0004;                    // Configure for single pulse mode
OC1R = 0x00203000;                  // Initialize primary Compare Register
OC1RS = 0x00203003;                 // Initialize secondary Compare Register
PR2 = 0x00500000;                   // Set period (PR2 is now 32-bits wide)

                                    // configure int
IFS0CLR = 0x00000040;               // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;               // Enable OC1 interrupt
IPC1SET = 0x001C0000;               // Set OC1 interrupt priority to 7,
                                    // the highest level
IPC1SET = 0x00030000;               // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                  // Enable Timer2
OC1CONSET = 0x8000;                 // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                   // Clear the OC1 interrupt flag
}
```


16.3.2.3 Special Cases for Dual Compare Mode Generating a Single Output Pulse

Depending on the relationship of the OCxR, OCxRS and PRy values, the output compare module has a few unique conditions which should be understood. These special conditions are specified in Table 16-2, along with the resulting behavior of the module.

Table 16-2: Special Cases for Dual Compare Mode Generating a Single Output Pulse

SFR Logical Relationship	Special Conditions	Operation	Output at OCx
PRy >= OCxRS and OCxRS > OCxR	OCxR = 0 Initialize TMRy = 0	In the first iteration of the TMRy counting from 0x0000 up to PRy, the OCx pin remains low; no pulse is generated. After the TMRy resets to zero (on period match), the OCx pin goes high due to match with OCxR. Upon the next TMRy to OCxRS match, the OCx pin goes low and remains there. The OCxIF bit will be set as a result of the second compare. There are two alternative initial conditions to consider: a. Initialize TMRy = 0 and set OCxR >= 1 b. Initialize TMRy = PRy (PRy > 0) and set OCxR = 0	Pulse will be delayed by the value in the PRy register, depending on setup
PRy >= OCxR and OCxR >= OCxRS	OCxR >= 1 and PRy >= 1	TMRy counts up to OCxR and on a compare match event (i.e., TMRy = OCxR), the OCx pin is driven to a high state. TMRy then continues to count and eventually resets on period match (i.e., PRy =TMRy). The timer then restarts from 0x0000 and counts up to OCxRS. On a compare match event (i.e., TMRy = OCxRS), the OCx pin is driven to a low state. The OCxIF bit will be set as a result of the second compare.	Pulse
OCxRS > PRy and PRy >= OCxR	None	Only the rising edge will be generated at the OCx pin. The OCxIF will not be set.	Rising edge/ transition to high
OCxR > PRy	None	Unsupported mode; timer resets prior to match condition.	Remains low

Note 1: In all the cases considered herein, the TMRy register is assumed to be initialized to 0x0000.

2: OCxR = Compare Register, OCxRS = Secondary Compare Register, TMRy = Timery Count and PRy = Timery Period Register.

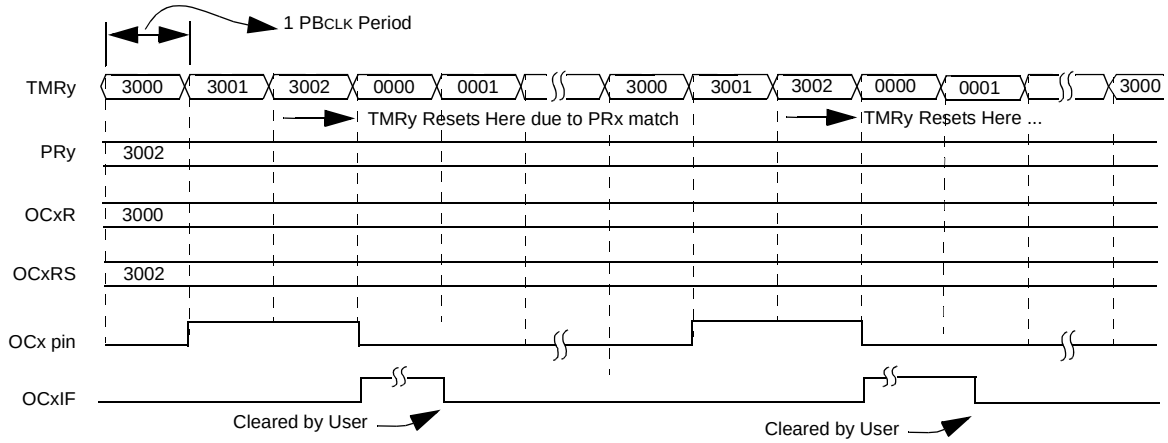
16.3.2.4 Dual Compare Mode: Continuous Output Pulses

To configure the output compare module for this mode, set control bits OCM<2:0> = '101'. In addition, the compare time base must be selected and enabled. Once this mode has been enabled, the output pin, OCx, will be driven low and remain low until a match occurs between the compare time base and OCxR register. Please note the following key timing events (refer to Figure 16-14 and Figure 16-16):

- The OCx pin is driven high one PBCLK after the compare match occurs between the compare time base and OCxR register. The OCx pin will remain high until the next match event occurs between the time base and the OCxRS register, at which time the pin will be driven low. This pulse generation sequence of a low-to-high and high-to-low edge will repeat on the OCx pin without further user intervention.
- Continuous pulses will be generated on the OCx pin until a mode change is made or the module is disabled.
- The compare time base will count up to the value contained in the associated period register and then reset to 0x0000 on the next instruction clock.
- If the compare time base period register value is less than the OCxRS register value, then no falling edge is generated. The OCx pin will remain high until OCxRS <= PRy, a mode change is made, or the device is reset.
- The respective channel interrupt flag, OCxIF, is asserted when the OCx pin is driven low (falling edge of single pulse).

General Dual Compare mode generating a continuous output pulse is illustrated in Figure 16-14. Figure 16-16 depicts another timing example where OCxRS > PRy. In this example, no falling edge of the pulse is generated, because the time base will reset before counting up to the contents of OCxRS.

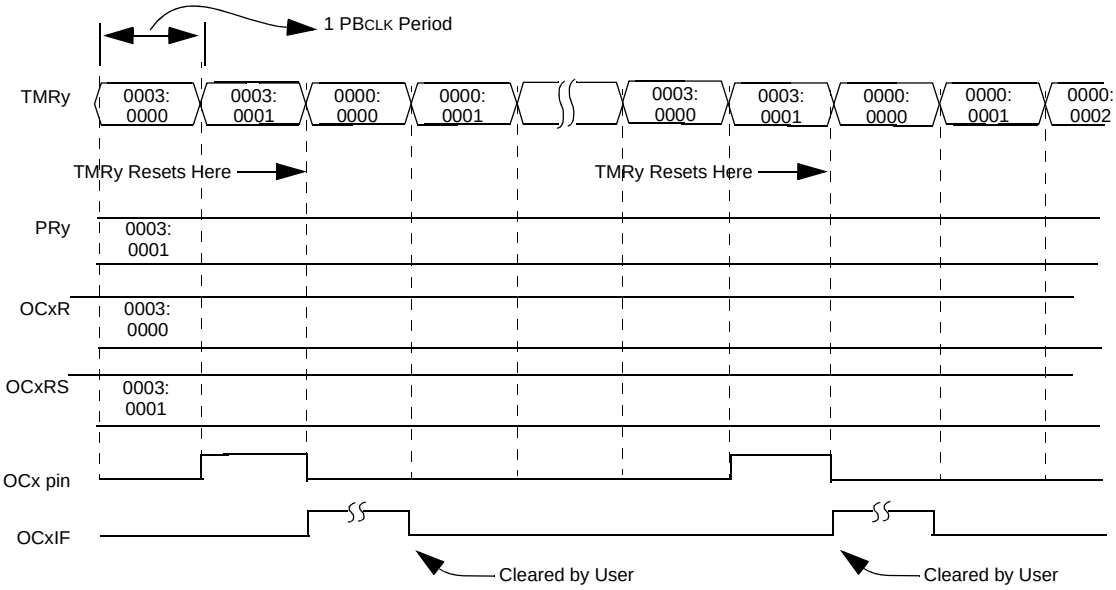
Figure 16-14: Dual Compare Mode: Continuous Output Pulse (PRy = OCxRS, 16-Bit Mode)



Note 1: An 'x' represents the output compare channel number. A 'y' represents the time base number.

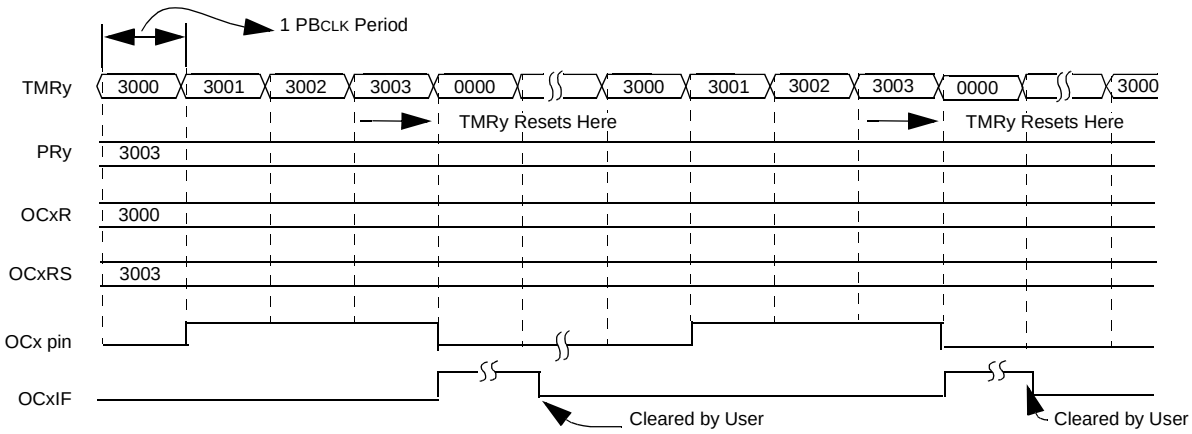
2: OCxR = Compare Register; OCxRS = Secondary Compare Register.

Figure 16-15: Dual Compare Mode: Continuous Output Pulse (PRy = OCxRS, 32-Bit Mode)



Note: An 'x' represents the output compare channel number. A 'y' represents the time base number.

Figure 16-16: Dual Compare Mode: Continuous Output Pulse (PRy = OCxRS, 16-Bit Mode)



Note 1: An 'x' represents the output compare channel number. A 'y' represents the time base number.

2: OCxR = Compare Register; OCxRS = Secondary Compare Register.

16.3.2.5 Setup for Continuous Output Pulse Generation

When control bits OCM<2:0> (OCxCON<2:0>) are set to '101', the selected output compare channel initializes the OCx pin to the low state and generates output pulses on each and every compare match event.

For the user to configure the module for the generation of a continuous stream of output pulses, the following steps are required (these steps assume the timer source is initially turned off, but this is not a requirement for the module operation):

1. Determine the peripheral clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
2. Calculate the time to the rising edge of the output pulse, relative to the TMRy start value (0x0000).
3. Calculate the time to the falling edge of the pulse, based on the desired pulse width and the time to the rising edge of the pulse.
4. Write the values computed in step 2 and 3 above into the compare register, OCxR, and the secondary compare register, OCxRS, respectively.
5. Set the timer period register, PRy, to a value equal to or greater than the value in OCxRS, the secondary compare register.
6. Set OCM<2:0> = '101' and the OCTSEL (OCxCON<3>) bit to the desired timer source (for 16-bit mode only). The OCx pin state will now be driven low.
7. Enable the compare time base by setting the TON (TyCON<15>) bit to '1'.
8. Upon the first match between TMRy and OCxR, the OCx pin will be driven high.
9. When the compare time base, TMRy, matches the secondary compare register, OCxRS, the second and trailing edge (high-to-low) of the pulse is driven onto the OCx pin.
10. As a result of the second compare match event, the OCxIF interrupt flag bit is set.
11. When the compare time base and the value in its respective period register match, the TMRy register resets to 0x0000 and resumes counting.
12. Steps 8 through 11 are repeated, and a continuous stream of pulses is generated, indefinitely. The OCxIF flag (refer to the IF0 register for the bit position of each channel's interrupt flag) is set on each OCxRS-TMRy compare match event.

Example 16-7 shows example code for configuration of the continuous output pulse event.

Example 16-7: Continuous Output Pulse Setup and Interrupt Servicing (16-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the continuous pulse event and select Timer2
// as the clock source for the compare time-base.

T2CON = 0x0010;                       // Configure Timer2 for a prescaler of 2

OC1CON = 0x0000;                      // disable OC1 module
OC1CON = 0x0005;                      // Configure OC1 module for Pulse output
OC1R = 0x3000;                        // Initialize Compare Register 1
OC1RS = 0x3003;                       // Initialize Secondary Compare Register 1
PR2 = 0x5000;                         // Set period


                                      // configure int
IFS0CLR = 0x00000040;                 // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;                 // Enable OC1 interrupt
IPC1SET = 0x001C0000;                 // Set OC1 interrupt priority to 7,
                                      // the highest level
IPC1SET = 0x00030000;                 // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                    // Enable Timer2
OC1CONSET = 0x8000;                   // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR= 0x0040;                      // Clear the OC1 interrupt flag
}
```

Example 16-8: Continuous Output Pulse Setup and Interrupt Servicing (32-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for interrupts on the continuous pulse event and select Timer2
// as the clock source for the compare time-base.

T2CON = 0x0018;                      // Configure Timer2 for 32-bit operation
                                     // with a prescaler of 2. The Timer2/Timer3
                                     // pair is accessed via registers associated
                                     // with the Timer2 register

OC1CON = 0x0000;                     // disable OC1 module
OC1CON = 0x0005;                     // Configure OC1 module for Pulse output
OC1R = 0x3000;                       // Initialize Compare Register 1
OC1RS = 0x3003;                      // Initialize Secondary Compare Register 1
PR2 = 0x00500000;                    // Set period (PR2 is now 32-bits wide)


                                     // configure int
IFS0CLR = 0x00000040;                // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;                // Enable OC1 interrupt
IPC1SET = 0x001C0000;                // Set OC1 interrupt priority to 7,
                                     // the highest level
IPC1SET = 0x00030000;                // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                   // Enable Timer2
OC1CONSET = 0x8000;                  // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                    // Clear the OC1 interrupt flag
}
```


16.3.2.6 Special Cases for Dual Compare Mode Generating Continuous Output Pulses

Depending on the relationship of the OCxR, OCxRS and PRy values, the output compare module may not provide the expected results. These special cases are specified in Table 16-3, along with the resulting behavior of the module.

Table 16-3: Special Cases for Dual Compare Mode Generating Continuous Output Pulses

SFR Logical Relationship	Special Conditions	Operation	Output at OCx
PRy >= OCxRS and OCxRS > OCxR	OCxR = 0 Initialize TMRy = 0	In the first iteration of the TMRy counting from 0x0000 up to PRy, the OCx pin remains low; no pulse is generated. After the TMRy resets to zero (on period match), the OCx pin goes high. Upon the next TMRy to OCxRS match, the OCx pin goes low. If OCxR = 0 and PRy = OCxRS, the pin will remain low for one clock cycle, then be driven high until the next TMRy to OCxRS match. The OCxIF bit will be set as a result of the second compare. There are two alternative initial conditions to consider: a. Initialize TMRy = 0 and set OCxR >= 1 b. Initialize TMRy = PRy (PRy > 0) and set OCxR = 0	Continuous pulses with the first pulse delayed by the value in the PRy register, depending on setup.
PRy >= OCxR and OCxR >= OCxRS	OCxR >= 1 and PRy >= 1	TMRy counts up to OCxR and on a compare match event (i.e., TMRy = OCxR), the OCx pin is driven to a high state. TMRy then continues to count and eventually resets on period match (i.e., PRy =TMRy). The timer then restarts from 0x0000 and counts up to OCxRS. On a compare match event (i.e., TMRy = OCxR), the OCx pin is driven to a low state. The OCxIF bit will be set as a result of the second compare.	Continuous pulses
OCxRS > PRy and PRy >= OCxR	None	Only one transition will be generated at the OCx pin until the OCxRS register contents have been changed to a value less than or equal to the period register contents (PRy). OCxIF is not set until then.	Rising edge/ transition to high
OCxR > PRy	None	Unsupported mode; Timer resets prior to match condition.	Remains low

Note 1: In all the cases considered herein, the TMRy register is assumed to be initialized to 0x0000.

2: OCxR = Compare Register, OCxRS = Secondary Compare Register, TMRy = Timery Count and PRy = Timery Period Register.

16.3.3 Pulse Width Modulation Mode

When control bits OCM<2:0> (OCxCON<2:0>) are set to '110' or '111', the selected output compare channel is configured for the PWM (Pulse-Width Modulation) mode of operation.

The following two PWM modes are available:

- PWM without Fault Protection Input
- PWM with Fault Protection Input

The OCFA or OCFB Fault input pin is utilized for the second PWM mode. In this mode, an asynchronous logic level '0' on the OCFx pin will cause the selected PWM channel to be shut down. (Refer to **16.3.3.1 "PWM with Fault Protection Input Pin"**.)

In PWM mode, the OCxR register is a read-only slave duty cycle register and OCxRS is a buffer register that is written by the user to update the PWM duty cycle. On every timer to period register match event (end of PWM period), the duty cycle register, OCxR, is loaded with the contents of OCxRS. The TyIF interrupt flag is asserted at each PWM period boundary.

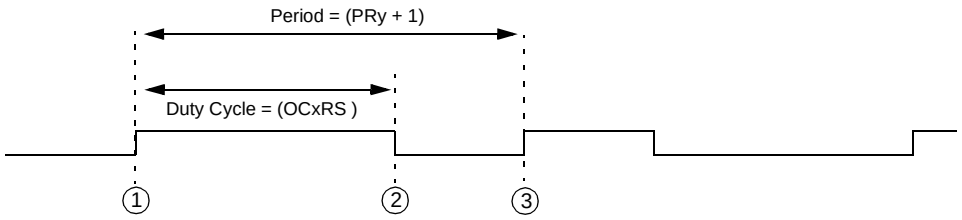
The following steps should be taken when configuring the output compare module for PWM operation:

1. Set the PWM period by writing to the selected timer period register (PRy).
2. Set the PWM duty cycle by writing to the OCxRS register.
3. Write the OxCR register with the initial duty cycle.
4. Enable interrupts, if required, for the timer and output compare modules. The output compare interrupt is required for PWM Fault pin utilization.
5. Configure the Output Compare module for one of two PWM Operation modes by writing to the Output Compare mode bits, OCM<2:0> (OCxCON<2:0>).
6. Set the TMRy prescale value and enable the time base by setting TON (TxCON<15>) = '1'.

Note:	The OCxR register should be initialized before the Output Compare module is first enabled. The OCxR register becomes a read-only duty cycle register when the module is operated in the PWM modes. The value held in OCxR will become the PWM duty cycle for the first PWM period. The contents of the duty cycle buffer register, OCxRS, will not be transferred into OCxR until a time base period match occurs.

An example PWM output waveform is shown in Figure 16-17.

Figure 16-17: PWM Output Waveform



1. Timery is cleared and the new duty cycle value is loaded from OCxRS into OCxR.
2. Timer value equals the value in the OCxR register; OCx Pin is driven low.
3. Timer overflow; value from OCxRS is loaded into OCxR; OCx pin is driven high. TyIF interrupt flag is asserted.

16.3.3.1 PWM with Fault Protection Input Pin

When the Output Compare mode bits, OCM<2:0> (OCxCON<2:0>), are set to '111', the selected output compare channel is configured for the PWM mode of operation. All functions described in **16.3.3 "Pulse Width Modulation Mode"** apply, with the addition of input Fault protection.

Fault protection is provided via the OCFA and OCFB pins. The OCFA pin is associated with the output compare channels 1 through 4, while the OCFB pin is associated with the output compare channel 5.

If a logic '0' is detected on the OCFA/OCFB pin, the selected PWM output pin(s) are placed in the high-impedance state. The user may elect to provide a pull-down or pull-up resistor on the PWM pin to provide for a desired state if a Fault condition occurs. The shutdown of the PWM output is immediate and is not tied to the device clock source. This state will remain until the following conditions are met:

- The external Fault condition has been removed
- The PWM mode is re-enabled by writing to the appropriate mode bits, OCM<2:0> (OCxCON<2:0>)

As a result of the Fault condition, the respective interrupt flag, OCxIF bit, is asserted and an interrupt will be generated, if enabled. Upon detection of the Fault condition, the OCFLT bit (OCxCON<4>) is asserted high (logic '1'). This bit is a read-only bit and will only be cleared once the external Fault condition has been removed and the PWM mode is re-enabled by writing to the appropriate mode bits, OCM<2:0> (OCxCON<2:0>).

Note:	The external Fault pins, if enabled for use, will continue to control the OCx output pins while the device is in SLEEP or IDLE mode.

16.3.3.2 PWM Period

The PWM period is specified by writing to PRy, the Timery period register. The PWM period can be calculated using the following formula:

Equation 16-1: Calculating the PWM Period

$$\text{PWM Period} = [(PR + 1) \bullet T_{PB} \bullet (\text{TMR Prescale Value})]$$

$$\text{PWM Frequency} = 1/[\text{PWM Period}]$$

The PWM period must not exceed the width of the Period Register for the selected mode, 16 bits for 16-bit mode or 32 bits for 32-bit mode. If the calculated period is too large, select a larger prescaler to prevent overflow. To maintain maximum PWM resolution, select the smallest prescaler that does not result in an overflow.

Note:	A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7 written into the PRy register will yield a period consisting of 8 time base cycles.

16.3.3.3 PWM Duty Cycle

The PWM duty cycle is specified by writing to the OCxRS register. The OCxRS register can be written to at any time, but the duty cycle value is not latched into OCxR until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation. In the PWM mode, OCxR is a read-only register.

Some important boundary parameters of the PWM duty cycle include the following:

- If the duty cycle register OCxR is loaded with 0x0000, the OCx pin will remain low (0% duty cycle).
- If OCxR is greater than PRy (timer period register), the pin will remain high (100% duty cycle).
- If OCxR is equal to PRy, the OCx pin will be low for one time base count value and high for all other count values.

See Figure 16-18 for PWM mode timing details. Table 16-4 through Table 16-9 show example PWM frequencies and resolutions for a device with the Peripheral Bus operating at a variety of frequencies.

Equation 16-2: Calculation for Maximum PWM Resolution

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{PB}}{F_{PWM} \bullet TMRy \bullet \text{Prescaler bits}}\right)}{\log_{10}(2)}$$

Equation 16-3: PWM Period and Duty Cycle Calculation

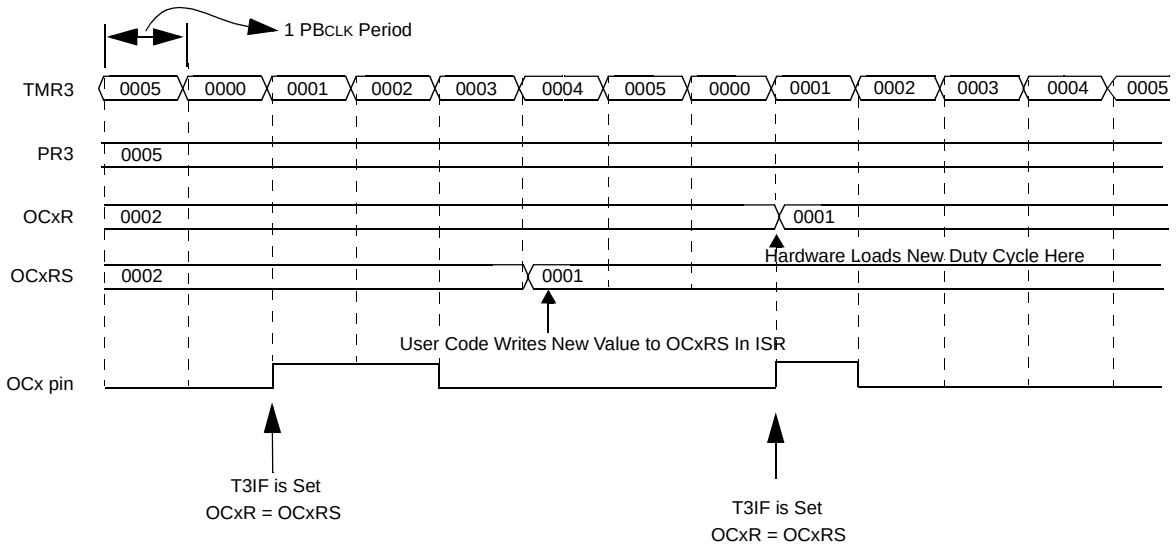
Desired PWM frequency is 52.08 kHz
F_{PB} = 10 MHz
Timer 2 prescale setting: 1:1

$1/52.08\ \text{kHz} = (PR2 + 1) \bullet T_{PB} \bullet (\text{Timer 2 prescale value})$
$19.20\ \mu s = (PR2 + 1) \bullet 0.1\ \mu s \bullet (1)$
$PR2 = 191$

Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz PWM frequency and a 10 MHz Peripheral Bus clock rate.

$1/52.08\ \text{kHz} = 2^{\text{PWM RESOLUTION}} \bullet 1/10\ \text{MHz} \bullet 1$
$19.20\ \mu s = 2^{\text{PWM RESOLUTION}} \bullet 100\ \text{ns} \bullet 1$
$192 = 2^{\text{PWM RESOLUTION}}$
$\log_{10}(192) = (\text{PWM Resolution}) \bullet \log_{10}(2)$
PWM Resolution = 7.6 bits

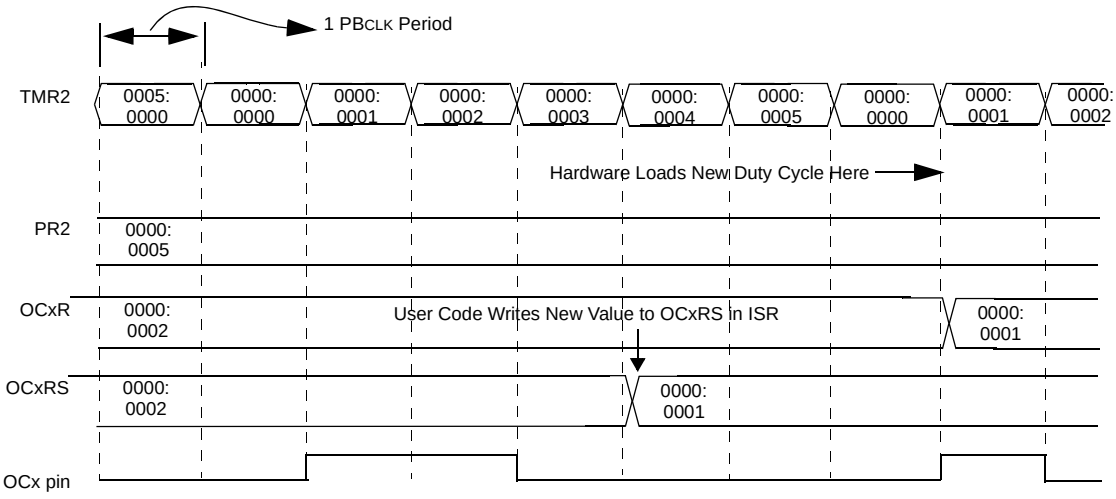
Figure 16-18: PWM Output Timing



Note 1: An 'x' represents the output compare channel number.

2: OCxR = Compare Register; OCxRS = Secondary Compare Register.

Figure 16-19: Dual Compare Mode: Continuous Output Pulse (PR2 = OCxRS, 32-Bit Mode)



Note: An 'x' represents the output compare channel number..

Table 16-4: Example PWM Frequencies and Resolutions with a 10 MHz (16-Bit Mode) Peripheral Bus Clock

PWM Frequency	19 Hz	153 Hz	305 Hz	2.44 kHz	9.77 kHz	78.1 kHz	313 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	0xFFFF	0xFFFF	0x7FFF	0x0FFF	0x03FF	0x007F	0x001F
Resolution (bits)	16	16	15	12	10	7	5

Table 16-5: Example PWM Frequencies and Resolutions with a 30 MHz (16-Bit Mode) Peripheral Bus Clock

PWM Frequency	58 Hz	458 Hz	916 Hz	7.32 kHz	29.3 kHz	234 kHz	938 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	0xFC8E	0xFFDD	0x7FEE	0x1001	0x03FE	0x007F	0x001E
Resolution (bits)	16	16	15	12	10	7	5

Table 16-6: Example PWM Frequencies and Resolutions with a 50 MHz (16-Bit Mode) Peripheral Bus Clock

PWM Frequency	57 Hz	458 Hz	916 Hz	7.32 kHz	29.3 kHz	234 kHz	938 kHz
Timer Prescaler Ratio	64	8	1	1	1	1	1
Period Register Value	0x349C	0x354D	0xD538	0x1AAD	0x06A9	0x00D4	0x0034
Resolution (bits)	13.7	13.7	15.7	12.7	10.7	7.7	5.7

Table 16-7: Example PWM Frequencies and Resolutions with a 50 MHz (16-Bit Mode) Peripheral Bus Clock

PWM Frequency	100 Hz	200 Hz	500 Hz	1 kHz	2 kHz	5 kHz	10 kHz
Timer Prescaler Ratio	8	8	8	1	8	1	1
Period Register Value (hex)	0xF423	0x7A11	0x30D3	0xC34F	0x0C34	0x270F	0x1387
Resolution (bits) (decimal)	15.9	14.9	13.6	15.6	11.6	13.3	12.3

Table 16-8: Example PWM Frequencies and Resolutions with a 50 MHz (16-Bit Mode) Peripheral Bus Clock

PWM Frequency	100 Hz	200 Hz	500 Hz	1 kHz	2 kHz	5 kHz	10 kHz
Timer Prescaler Ratio	8	4	2	1	1	1	1
Period Register Value (hex)	0xF423	0xF423	0xC34F	0x0C34F	0x61A7	0x270F	0x1387
Resolution (bits) (decimal)	15.9	15.9	15.6	15.6	14.6	13.3	12.3

Table 16-9: Example PWM Frequencies and Resolutions with a 50 MHz (32-Bit Mode) Peripheral Bus Clock

PWM Frequency	100 Hz	200 Hz	500 Hz	1 kHz	2 kHz	5 kHz	10 kHz
Timer Prescaler Ratio	1	1	1	1	1	8	1
Period Register Value (hex)	0x0007A11F	0x0003D08F	0x0001869F	0x0000C34F	0x000061A7	0x000004E1	0x00001387
Resolution (bits) (decimal)	18.9	17.9	16.6	15.6	14.6	10.3	12.3

Example 16-9 shows configuration and interrupt service code for the PWM mode of operation.

Example 16-9: PWM Mode Setup and Interrupt Servicing (16-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for PWM mode with FAULT pin disabled, a 50% duty cycle and a
// PWM frequency of 52.08 kHz at Fosc = 40 MHz. Timer2 is selected as
// the clock for the PWM time base and Timer2 interrupts
// are enabled.

OC1CON = 0x0000;                    // Turn off OC1 while doing setup.
OC1R = 0x0060;                      // Initialize primary Compare Register
OC1RS = 0x0060;                     // Initialize secondary Compare Register
OC1CON = 0x0006;                    // Configure for PWM mode
PR2 = 0x00BF;                       // Set period


                                    // configure int
IFS0CLR = 0x00000040;               // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;               // Enable OC1 interrupt
IPC1SET = 0x001C0000;               // Set OC1 interrupt priority to 7,
                                    // the highest level
IPC1SET = 0x00030000;               // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                  // Enable Timer2
OC1CONSET = 0x8000;                 // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                   // Clear the OC1 interrupt flag
}
```

Example 16-10: PWM Mode Setup and Interrupt Servicing (32-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for PWM mode with FAULT pin disabled, a 50% duty cycle and a
// PWM frequency of 52.08 kHz at Fosc = 40 MHz. Timer2 is selected as
// the clock for the PWM time base and Timer2 interrupts
// are enabled.

OC1CON = 0x0000;                    // Turn off OC1 while doing setup.
OC1R = 0x00600000;                  // Initialize primary Compare Register
OC1RS = 0x00600000;                 // Initialize secondary Compare Register
OC1CON = 0x0006;                    // Configure for single pulse mode
PR2 = 0x00600000;                   // Set period

                                    // configure int
IFS0CLR = 0x00000040;               // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;               // Enable OC1 interrupt
IPC1SET = 0x001C0000;               // Set OC1 interrupt priority to 7,
                                    // the highest level
IPC1SET = 0x00030000;               // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                  // Enable Timer2
OC1CONSET = 0x8000;                 // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
// insert user code here
IFS0CLR = 0x0040;                   // Clear the OC1 interrupt flag
}
```


16.4 INTERRUPTS

Each of the available output compare channels has a dedicated interrupt bit OCxIF, and a corresponding interrupt enable/mask bit OCxIE. These bits are used to determine the source of an interrupt and to enable or disable an individual interrupt source. The priority level of each of the channels can also be set independently of the other channels.

OCxIF is set when an output compare channel detects a predefined match condition that is defined as an event generating an interrupt. The OCxIF bit will then be set without regard to the state of the corresponding OCxIE bit. The OCxIF bit can be polled by software if desired.

The OCxIE bit is used to define the behavior of the Vector Interrupt Controller (VIC) when a corresponding OCxIF is set. When the OCxIE bit is clear, the VIC module does not generate a CPU interrupt for the event. If the OCxIE bit is set, the VIC module will generate an interrupt to the CPU when the corresponding OCxIF bit is set (subject to the priority and subpriority as outlined below).

It is the responsibility of the routine that services a particular interrupt to clear the appropriate interrupt flag bit before the service routine is complete.

The priority of each output compare channel can be set independently via the OCxIP<2:0> bits. This priority defines the priority group that the interrupt source will be assigned to. The priority groups range from a value of 7, the highest priority, to a value of 0, which does not generate an interrupt. An interrupt being serviced will be preempted by an interrupt in a higher priority group.

The subpriority bits allow setting the priority of an interrupt source within a priority group. The values of the subpriority, OCxIS<1:0>, range from 3, the highest priority, to 0, the lowest priority. An interrupt with the same priority group but having a higher subpriority value will preempt a lower subpriority interrupt that is in progress.

The priority group and subpriority bits allow more than one interrupt source to share the same priority and subpriority. If simultaneous interrupts occur in this configuration, the natural order of the interrupt sources within a priority/subpriority group pair determines the interrupt generated. The natural priority is based on the vector numbers of the interrupt sources. The lower the vector number, the higher the natural priority of the interrupt. any interrupts that were overridden by natural order will then generate their respective interrupts (based on priority, subpriority, and natural order) after the interrupt flag for the current interrupt is cleared.

After an enabled interrupt is generated, the CPU will jump to the vector assigned to that interrupt. The vector number for the interrupt is the same as the natural order number. The CPU will then begin executing code at the vector address. The user's code at this vector address should perform any operations required (such as reloading the duty cycle and clearing the interrupt flag), and then exit. Refer to **Section 8. "Interrupts"** for the vector address table details and for more information on interrupts.

16.5 I/O PIN CONTROL

When the output compare module is enabled, the I/O pin direction is controlled by the compare module. The compare module returns the I/O pin control back to the appropriate pin LAT and TRIS control bits when it is disabled.

When the PWM with Fault Protection Input mode is enabled, the OCFx Fault pin must be configured for an input by setting the respective TRIS SFR bit. The OCFx Fault input pin is not automatically configured as an input when the PWM fault mode is selected.

Table 16-10: Pins Associated with Output Compare Modules 1-5

Pin Name	Module Control	Pin Type	Buffer Type	Description
OC1	ON	O	—	Output Compare/PWM Channel 1
OC2	ON	O	—	Output Compare/PWM Channel 2
OC3	ON	O	—	Output Compare/PWM Channel 3
OC4	ON	O	—	Output Compare/PWM Channel 4
OC5	ON	O	—	Output Compare/PWM Channel 5
OCFA	ON	I	ST	PWM Fault Protection A Input (for Channels 1-4)
OCFB	ON	I	ST	PWM Fault Protection B Input (for Channel 5)

Legend: ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output

16.6 OPERATION IN POWER-SAVING AND DEBUG MODES

Note: In this manual, a distinction is made between a power mode as it is used in a specific module, and a power mode as it is used by the device, e.g., Sleep mode of the Comparator and SLEEP mode of the CPU. To indicate which type of power mode is intended, uppercase and lowercase letters (Sleep, Idle, Debug) signify a module power mode, and all uppercase letters (SLEEP, IDLE, DEBUG) signify a device power mode.

16.6.1 Output Compare Operation in SLEEP Mode

When the device enters SLEEP mode, the system clock is disabled. During SLEEP, the Output Compare modules will drive the pin to the same active state as driven prior to entering SLEEP. The module will then halt at this state.

For example, if the pin was high and the CPU entered the SLEEP state, the pin will stay high. Likewise, if the pin was low and the CPU entered the SLEEP state, the pin will stay low. In both cases, when the device wakes up, the Output Compare module will resume operation.

When the module is operating in PWM Fault mode, the asynchronous portions of the fault circuit remain active. If a fault is detected, the compare output enable signal is deasserted and OCFLT (OCxCON<4>) is set. If the corresponding interrupt is enabled, an interrupt will be generated and the device will wake-up from SLEEP.

16.6.2 Output Compare Operation in IDLE Mode

When the device enters IDLE mode, the system clock sources remain functional and the CPU stops executing code. The SIDL bit (OCxCON<13>) selects if the compare module will stop operation when the device enters IDLE mode or whether the module will continue normal operation in IDLE mode.

- If SIDL = 1, the module will discontinue operation in IDLE mode. The module will perform the same procedures when stopped in IDLE mode as it does for SLEEP mode.
- If SIDL = 0, the module will continue operation in IDLE only if the selected time base is set to operate in IDLE mode. The output compare channel(s) will operate during the CPU IDLE mode if the SIDL bit is a logic '0'. Furthermore, the time base must be enabled with the respective SIDL bit set to a logic '0'.

Note: The external Fault pins, if enabled for use, will continue to control the associated OCx output pins while the device is in SLEEP or IDLE mode.

- When the module is operating in PWM Fault mode, the asynchronous portions of the fault circuit remain active. If a fault is detected, the compare output enable signal is deasserted and OCFLT (OCxCON<4>) is set. If the corresponding interrupt is enabled, an interrupt will be generated and the device will wake-up from IDLE.

16.6.3 Output Compare Operation in DEBUG Mode

The FRZ bit (OCxCON<14>) determines whether the Output Compare module will run or stop while the CPU is executing Debug Exception code (i.e., the application is halted) in DEBUG mode. When FRZ = '0', the Output Compare module continues to run even when the application is halted in DEBUG mode. When FRZ = 1 and the application is halted in DEBUG mode, the module will freeze its operations and make no changes to the state of the Output Compare module. The module will resume its operation after the CPU resumes execution.

When the module is operating in PWM Fault mode, the asynchronous portions of the fault circuit remain active. If a fault is detected, the compare output enable signal is deasserted and OCFLT (OCxCON<4>) is set. If the corresponding interrupt is enabled, an interrupt will be generated.

Note: The FRZ bit is readable and writable only when the CPU is executing in Debug Exception mode. In all other modes, the FRZ bit reads as '0'. If FRZ bit is changed during DEBUG mode, the new value does not take effect until the current Debug Exception mode is exited and re-entered. During the Debug Exception mode, the FRZ bit reads the state of the peripheral when entering DEBUG mode.

16.7 EFFECTS OF VARIOUS RESETS

16.7.1 $\overline{\text{MCLR}}$ Reset

Following a $\overline{\text{MCLR}}$ event, the OCxCON, OCxR, and OCxRS registers for each Output Compare module are reset to a value of 0x00000000.

16.7.2 Power-on Reset

Following a Power-on (POR) event, the OCxCON, OCxR, and OCxRS registers for each Output Compare module are reset to a value of 0x00000000.

16.7.3 Watchdog Timer Reset

The status of the OCMP control registers after a Watchdog Timer (WDT) event depends on the operational mode of the CPU prior to the WDT event.

If the device is not in SLEEP, a WDT event will force the OCxCON, OCxR, and OCxRS registers to a Reset value of 0x00000000.

If the device is in SLEEP when a WDT event occurs, the contents of the OCxCON, OCxR and OCxRS register values are not affected.

16.8 OUTPUT COMPARE APPLICATION

This is an example application using the PWM mode of the Output Compare module to control the speed of a DC motor. The speed of the motor is controlled by changing the PWM duty cycle.

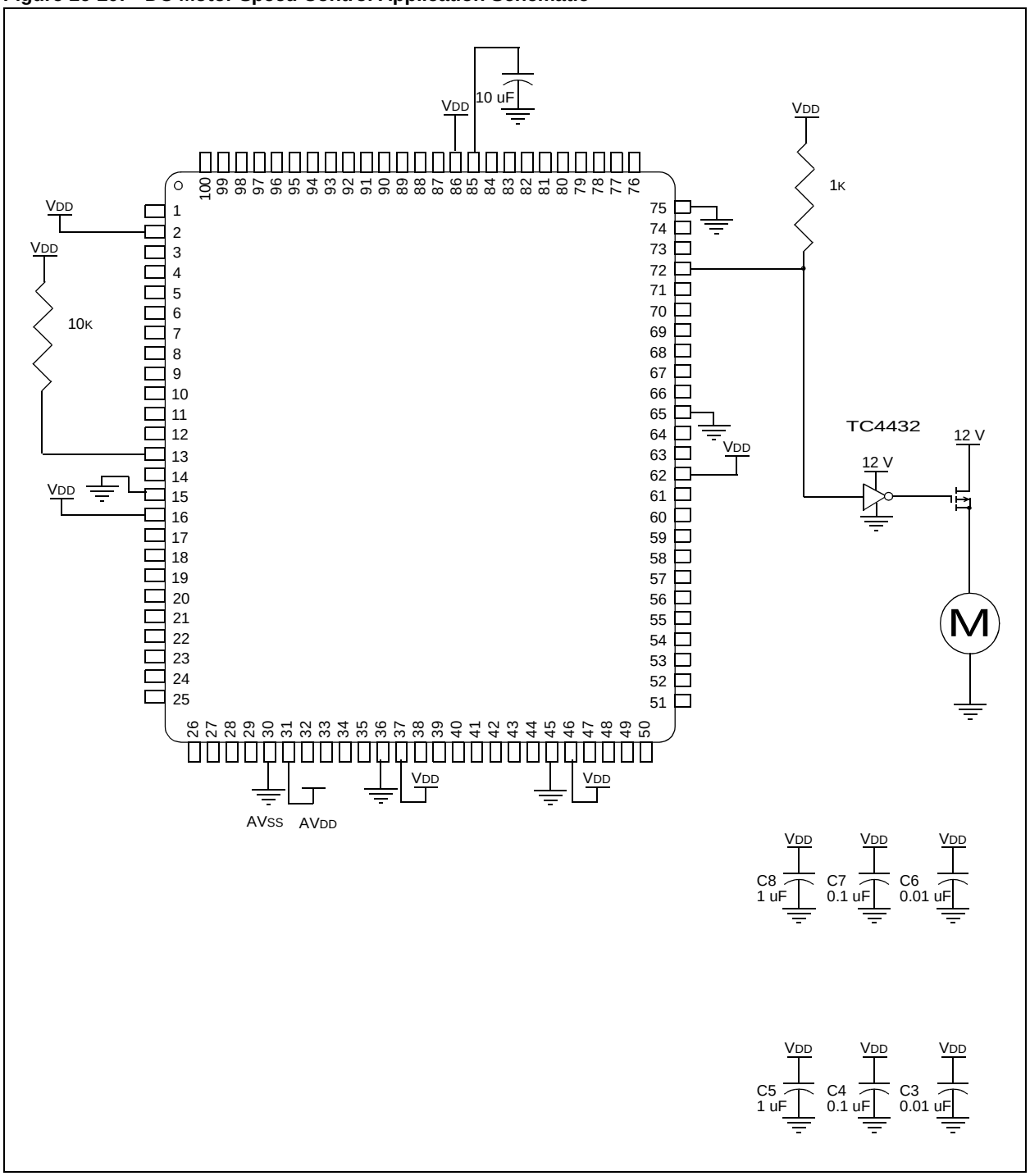
The circuit consists of the following:

- A PIC32MX device to generate the PWM.
- A TC4431 or equivalent MOSFET driver to drive the MOSFET.
- A MOSFET to drive the motor.
- A pull-up resistor is used to pull the input of the MOSFET driver high when the PIC32MX is in Reset. This prevents unwanted motor operation during start-up.
- A DC motor.

Example 16-11: PWM Mode Example Application (16-Bit Mode)

```
// The following code example will set the Output Compare 1 module
// for PWM mode w/o FAULT pin enabled, a 50% duty cycle and a
// PWM frequency of 52.08 kHz at FP = 40 MHz. Timer2 is selected as
// the clock for the PWM time base and Timer2 interrupts
// are enabled. This example ramps the PWM duty cycle from min to max, then
// from max to min and repeats. The rate at which the PWM duty cycle is
// changed can be adjusted by the rate at which the Timer2 overflows.
// The PWM period can be changed by writing a different value to the PR2
// register. If the PR2 value is adjusted the maximum PWM value will also
// have to be adjusted so that it is not greater than the PR2 value.

unsigned int Pwm;                       // variable to store calculated PWM value
unsigned char Mode = 0;                 // variable to determine ramp up or ramp down

OC1CON = 0x0000;                        // Turn off OC1 while doing setup.
OC1R = 0x0000;                          // Initialize primary Compare Register
OC1RS = 0x0000;                         // Initialize secondary Compare Register
OC1CON = 0x0006;                        // Configure for PWM mode
PR2 = 0xFFFF;                           // Set period

                                        // configure int
IFS0CLR = 0x00000040;                   // Clear the OC1 interrupt flag
IFS0SET = 0x00000040;                   // Enable OC1 interrupt
IPC1SET = 0x001C0000;                   // Set OC1 interrupt priority to 7,
                                        // the highest level
IPC1SET = 0x00030000;                   // Set Subpriority to 3, maximum

T2CONSET = 0x8000;                      // Enable Timer2
OC1CONSET = 0x8000;                     // Enable OC1

// Example code for Output Compare 1 ISR:

void__ISR(_OUTPUT_COMPARE_1_VECTOR, ipl7) OC1_IntHandler (void)
{
if ( Mode )
    {
        if ( Pwm < 0xFFFF )             // ramp up mode
        {
            Pwm ++;                     // If the duty cycle is not at max, increase
            OC1RS = Pwm;                // Write new duty cycle
        }
        else
        {
            Mode = 0;                   // PWM is at max, change mode to ramp down
        }
    }                                   // end of ramp up
    else
    {
        if ( !Pwm )                     // ramp down mode
        {
            Pwm --;                     // If the duty cycle is not at min, increase
            OC1RS = Pwm;                // Write new duty cycle
        }
        else
        {
            Mode = 1;                   // PWM is at min, change mode to ramp up
        }
    }                                   // end of ramp down

        // insert user code here
        IFS0CLR = 0x0040;               // Clear the OC1 interrupt flag
}
```

Figure 16-20: DC Motor Speed Control Application Schematic



16.9 DESIGN TIPS

Question 1: ***The Output Compare pin stops functioning even when the SIDL bit is not set. Why?***

Answer: This is most likely to occur when the SIDL bit (TxCON<13>) of the associated timer source is set. Therefore, it is the timer that actually goes into IDLE mode when the PWRSAV instruction is executed.

Question 2: ***Can I use the Output Compare modules with the selected time base configured for 32-bit mode?***

Answer: Yes. The timer can be used in 32-bit mode as a time base for the Output Compare modules by setting the T32 bit (TxCON<3>). For proper operation, the Output Compare module must be configured for 32-bit Compare mode by setting the OC32 bit (OCxCON<5>) for all Output Compare modules using the 32-bit timer as a time base.

16.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32MX device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Output Compare module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32MX family of devices.

16.11 REVISION HISTORY

Revision A (October 2007)

This is the initial released version of this document.

Revision B (October 2007)

Updated document to remove Confidential status.

Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x.

Revision D (June 2008)

Revised Registers 16-1, 16-20, 16-32; Revised Examples 16-3, 16-4, 16-5, 16-6, 16-7, 16-8, 16-9, 16-10, 16-11; Added TMR1 and TMR2 to Summary Table; Revised Section 16.3, Notes; Change Reserved bits from “Maintain as” to “Write”; Added Note to ON bit (0CxCON, T2CON, T3CON Registers).

NOTES:

