Section 9. Watchdog Timer (WDT) and Power-Saving Modes

HIGHLIGHTS

This section of the manual contains the following topics:

9.1 Introduction 9-2
9.2 Power-Saving Modes 9-2
9.3 Watchdog Timer (WDT) 9-7
9.4 Design Tips 9-11
9.5 Related Application Notes 9-12
9.6 Revision History 9-13

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Special Features"** and **"Power-Saving Features"** chapters in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

9.1 INTRODUCTION

This section describes the Watchdog Timer (WDT) and power-saving modes implemented in dsPIC33F/PIC24H devices. The dsPIC33F/PIC24H families offer a number of built-in capabilities that permit user-assigned applications to select the best balance of performance and low power consumption.

The WDT resets the device during software malfunction. It can also be used to wake the device from Sleep mode or Idle mode.

9.2 POWER-SAVING MODES

Power-saving features implemented in dsPIC33F/PIC24H devices include the following:

- System clock management
- Instruction-based power-saving modes (Sleep mode and Idle mode)
- Hardware-based Doze mode
- Peripheral module disable

9.2.1 System Clock Management

Reducing the system clock frequency results in power savings that are roughly proportional to the frequency reduction. The dsPIC33F/PIC24H devices provide an on-the-fly clock switching feature that allows the user-assigned application to optimize power consumption by dynamically changing the system clock frequency. For more information, refer to **Section 7. "Oscillator"** (DS70186).

9.2.2 Instruction-Based Power-Saving Modes

The dsPIC33F/PIC24H devices have two instruction-based power-saving modes. These modes can be entered by executing a special `PWRSAV` instruction. If an interrupt coincides with the execution of a `PWRSAV` instruction, the interrupt is delayed until the device fully enters Sleep mode or Idle mode. If the interrupt is a wake-up event, it will then wake-up the device and execute.

- **Sleep Mode:** In Sleep mode, the CPU, the system clock source, and the peripherals that operate on the system clock source are disabled. This is the lowest power mode for the device. The Wake-up from Sleep Flag bit (SLEEP) in the Reset Control register (RCON<3>) is set when the device enters Sleep mode.
- **Idle Mode:** In Idle mode, the CPU is disabled, but the system clock source continues to operate. The peripherals continue to operate but can optionally be disabled. The Wake-up from Idle Flag bit (IDLE) in the Reset Control register (RCON<2>) is set when the device enters Idle mode.

The SLEEP and IDLE status bits are cleared on Power-on Reset (POR) and Brown-out Reset (BOR). These bits can also be cleared in software. For more information, refer to **Section 8. "Reset"** (DS70192).

The assembly syntax of the PWRSAV instruction is shown in Example 9-1.

Example 9-1: PWRSAV Assembly Syntax

```
PWRSAV #SLEEP_MODE   ; Put the device into SLEEP mode
PWRSAV #IDLE_MODE    ; Put the device into IDLE mode
```

Note 1: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

2: Sleep mode does not change the state of the I/O pins.

9.2.2.1 SLEEP MODE

Sleep mode is the lowest current-consumption state. The characteristics of Sleep mode include the following:

- The Primary Oscillator (POSC) and Internal Fast RC (FRC) Oscillator are disabled.
- The Secondary Oscillator (SOSC) continues to run, if the Secondary Oscillator Enable bit (LPOSCEN) in the Oscillator Control register (OSCCON<1>) is set. For more information, refer to **Section 7. "Oscillator"** (DS70186).
- The WDT and the clock source Internal Low-Power RC (LPRC) Oscillator continue to run if the Watchdog Timer is enabled. For more information, see **9.3 "Watchdog Timer (WDT)"**.
- If the Voltage Regulator Standby During Sleep bit (VREGS) is cleared in the Reset Control register (RCON<8>), the internal voltage regulator enters Standby state. The voltage regulator consumes less current when in Standby state.
- The peripherals operating with the system clock are disabled.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode, because the system clock is disabled.

To minimize the current consumption in Sleep mode, perform the following action:

- Ensure that I/O pins do not drive resistive loads
- Ensure that I/O pins configured as inputs are not floating
- Disable the SOSC
- Disable the WDT
- Enable the voltage regulator to enter standby state in Sleep mode

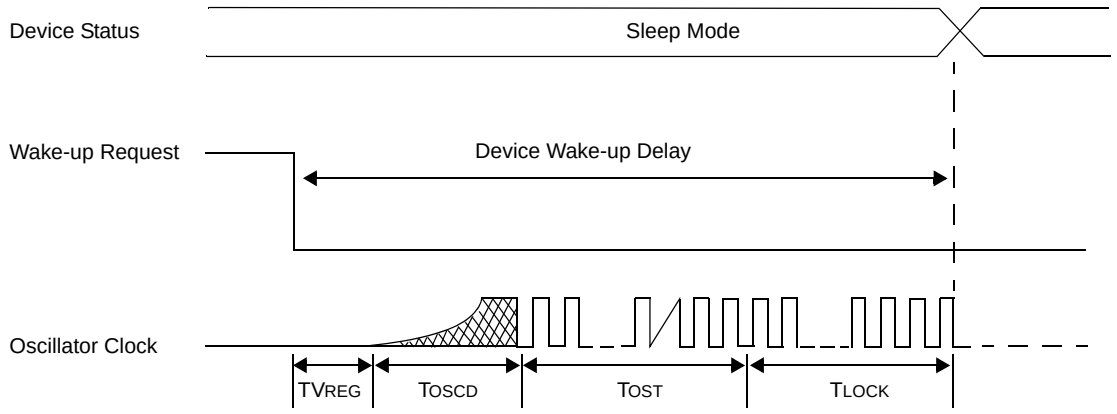
When the device exits Sleep mode, it restarts with the current clock source as indicated by the Current Oscillator Selection bits (COSC<2:0>) in the Oscillator Control register (OSCCON<14:12>).

9.2.2.1.1 Delay on Wake-up from Sleep Mode

Figure 9-1 illustrates the wake-up delay from Sleep mode. This delay consists of the voltage regulator delay and the oscillator delay.

- **Voltage regulator delay:** The time delay for the voltage regulator to transit from standby state to active state. This delay is required only if Standby mode is enabled for the voltage regulator.
- **Oscillator delay**: The time delay for the clock to be ready for various clock sources as given in Table 9-1. For more information, refer to **Section 7. "Oscillator"** (DS70186).

Figure 9-1: Wake-up Delay from Sleep Mode



Note 1: TVREG = Voltage regulator standby-to-active mode transition time (130 ms nominal).

2: TOSCD = Oscillator start-up delay (FRC = 1.1 ms nominal; LPRC = 70 ms nominal).

3: TOST = Oscillator start-up timer delay (1024 oscillator clock period).

4: TLOCK = PLL lock time (1 ms nominal), if PLL is enabled.

Table 9-1: Oscillator Delay

Oscillator Source	Oscillator Start-up Delay	Oscillator Start-up Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	TOSCD	—	—	TOSCD
FRCPLL	TOSCD	—	TLOCK	TOSCD + TLOCK
XT	TOSCD	TOST	—	TOSCD + TOST
HS	TOSCD	TOST	—	TOSCD + TOST
EC	—	—	—	—
XTPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
HSPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
ECPLL	—	—	TLOCK	TLOCK
SOSC	TOSCD	TOST	—	TOSCD + TOST
LPRC	TOSCD	—	—	TOSCD

Note 1: TOSCD = Oscillator start-up delay (1.1 µs max for FRC; 70 µs max for LPRC).
Crystal Oscillator start-up time varies with crystal characteristics, load capacitance and so on.

2: TOST = Oscillator start-up timer delay (1024 oscillator clock period).
For example, TOST = 102.4 µs for 10 MHz crystal and TOST = 32 ms for 32 kHz crystal.

3: TLOCK = PLL lock time (1 ms nominal), if PLL is enabled.

9.2.2.2 IDLE MODE

Idle mode has the following characteristics:

- CPU stops executing instructions
- System clock source remains active
- Peripheral modules, by default, continue to operate normally from the system clock source
- Peripherals can optionally be shut down using their Stop-in-Idle control bit, which is located in bit position 13 of the control register for most peripheral modules. The generic bit-field name format is “xxxSIDL” (where, “xxx” is the mnemonic name of the peripheral device). For more information, refer to the respective peripheral dsPIC33F/PIC24H Family Reference Manual sections, which are available from the Microchip web site (www.microchip.com).

When the device exits Idle mode, the CPU starts executing instructions within eight system clock cycles.

9.2.2.3 WAKE-UP FROM SLEEP MODE AND IDLE MODE

Sleep mode and Idle mode exit on the following events:

- Enabled interrupt event
- WDT time-out
- Reset from any source (POR, BOR and $\overline{\text{MCLR}}$)

9.2.2.3.1 Wake-up on Interrupt

An enabled interrupt event wakes the device from Sleep mode or Idle mode, which result in the following actions:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device wakes up and continues code execution from the instruction following the `PWRSAV` instruction that initiated Sleep mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device wakes up and the CPU exception process begins. Code execution continues from the first instruction of the ISR.

9.2.2.3.2 Wake-up on WDT Time-out

If enabled, the WDT continues to run during Sleep mode or Idle mode. When the WDT time-out occurs, the device wakes up and code execution continues from where the `PWRSAV` instruction was executed.

The Watchdog Timer Time-out Flag bit (WDTO) in the Reset Control register (RCON<4>) is set to indicate that the wake-up event is due to a WDT time-out.

9.2.2.3.3 Wake-up on Reset

A Reset from any source (POR, BOR and $\overline{\text{MCLR}}$) causes the device to exit Sleep mode or Idle mode, and begin executing from the Reset vector.

9.2.3 Hardware-based Doze Mode

The preferred strategy for reducing power consumption is to change clock speed and invoke Idle mode or Sleep mode. However, in certain circumstances this strategy is not practical. The following effects must be considered:

- Manipulating the system clock speed alters the communication peripheral baud rate and can introduce communication errors.
- Using an instruction-based power-saving mode (Idle mode/Sleep mode) stops processor execution.

Doze mode provides an alternate method to reduce power consumption. In Doze mode, the peripherals are clocked at the system clock frequency, whereas the CPU is clocked at a reduced speed.

Doze mode is enabled by setting the Doze Mode Enable bit (DOZEN) in the Clock Divisor register (CLKDIV<11>). The ratio between peripheral and CPU clock speed is determined by the Processor Clock Reduction Select bits (DOZE<2:0>) in the Clock Divisor register (CLKDIV<14:12>). There are eight possible configurations, ranging from 1:1 to 1:128, with 1:1 being the default.

The CPU automatically returns to full-speed operation on any interrupt when the Recover On Interrupt bit (ROI) is set in the Clock Divisor register (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

Note:	A `NOP` instruction must be executed immediately before entering Doze mode and immediately after exiting Doze mode. Failure to do so may result in unpredictable behavior.

9.2.4 Peripheral Module Disable

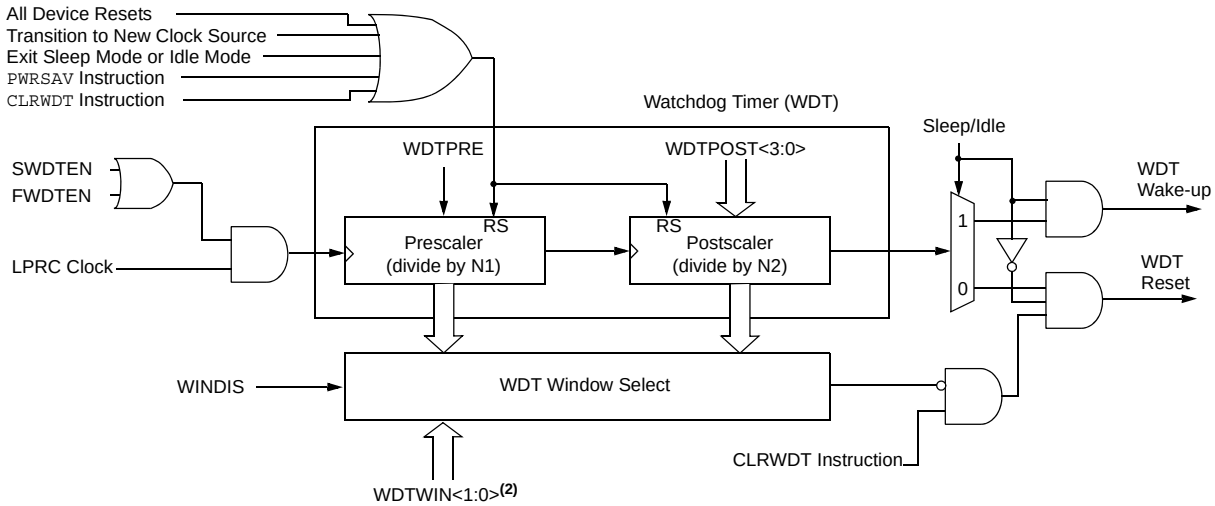
All the peripheral modules (except for I/O ports) in dsPIC33F/PIC24H devices have a control bit that can be selectively disabled to reduce power consumption. These bits, known as the Peripheral Module Disable bits (PMD), are generically named “xxxPMD” (where “xxx” is the mnemonic version of the module name). These bits are located in the PMDx Special Function Registers (SFRs). The PMD bit must be set to ‘`1`’ to disable the module. The PMD bit shuts down the peripheral, and effectively powering down all circuits and removing all clock sources. All of the peripherals are enabled by default. For PMD register details, refer to the specific device data sheet.

9.3 WATCHDOG TIMER (WDT)

The primary function of the WDT is to reset the device during software malfunction. It can also be used to wake the device from Sleep mode or Idle mode.

The WDT consists of a programmable prescaler and postscaler clocked with the LPRC Oscillator. The WDTO period is selected by configuring the prescaler and postscaler dividers. A block diagram of the WDT is illustrated in Figure 9-2.

Figure 9-2: WDT Block Diagram



Note 1: See Table 9-3 for the prescaler divider ratio (N1) and Table 9-4 for the postscaler divider ratio (N2).

2: Refer to the specific device data sheet for the availability of these bits.

9.3.1 WDT Operation

When enabled, the WDT increments until it overflows or a time-out occurs. A WDT time-out forces a device Reset, except during Sleep mode or Idle mode. To prevent a WDT time-out reset, the software must periodically clear the WDT using the `CLRWDT` instruction.

The WDT is also cleared when the device enters Sleep mode or Idle mode after executing the `PWRSAV` instruction. If the WDT expires during Sleep mode or Idle mode, the device wakes up and continues code execution from where the `PWRSAV` instruction was executed.

In either case, the WDTO bit in the Reset Control register (RCON<4>) is set to indicate that the device Reset or wake-up event is due to a WDT time-out.

If a Watchdog Timer Reset occurs while a Flash programming or erase operation is in progress, the Reset will remain pending until the Run-Time Self Programming (RTSP) cycle completes. Refer to **Section 5. "Flash Programming"** (DS70191) for more information.

9.3.1.1 ENABLING AND DISABLING THE WDT

The WDT is enabled or disabled by the Watchdog Timer Enable bit (FWDTEN) in the WDT Configuration register (FWDT<7>). When the FWDTEN bit is set, the WDT is always enabled. This is the default value for an erased device.

If the WDT bit is disabled in the FWDT register, the user-assigned application can optionally enable the WDT by setting the Software Enable/Disable of WDT bit (SWDTEN) in the Reset Control register (RCON<5>).

The SWDTEN control bit is cleared on any device reset. This bit allows the user-assigned application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

Note:	The WDT Configuration register (FWDT) values are written during device programming. For more information on the WDT configuration register, refer to **Section 25. "Device Configuration"** (DS70194).

9.3.1.2 WDT WINDOW

The WDT has an optional Windowed mode enabled by programming the Watchdog Timer Window Enable bit (WINDIS) in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared within an allowed window of the WDTO period, as illustrated in Figure 9-3 through Figure 9-6. If the WDT is cleared before the allowed window, a system Reset is generated immediately.

The Windowed mode is useful for resetting the device during unexpected quick or slow execution of a critical portion of the code. Table 9-2 lists all possible window options for devices with and without the WDTWIN<1:0> bits.

Table 9-2: Window Bit Options

WDTWIN<1:0>	Selected Allowed Window
Bits not implemented	25%
11	25%
10	37.50%
01	50%
00	75%

Figure 9-3: Windowed WDT When WDTWIN<1:0> = 11 or when the WDTWIN<1:0> Bits are not Implemented

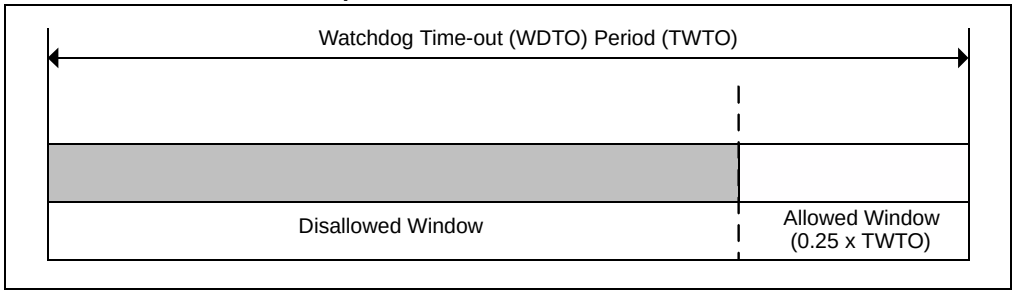


Figure 9-4: Windowed WDT When WDTWIN<1:0> = 10

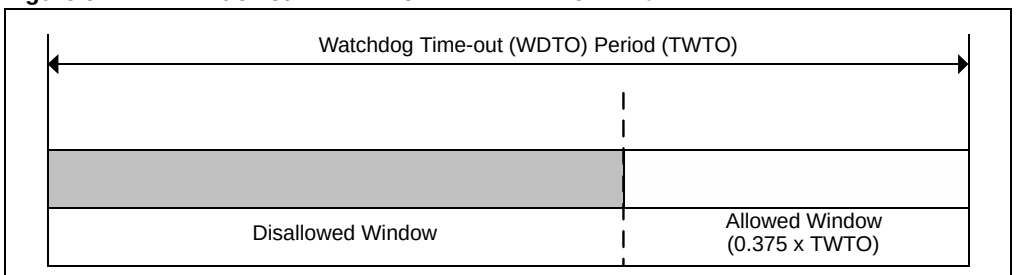


Figure 9-5: Windowed WDT When WDTWIN<1:0> = 01

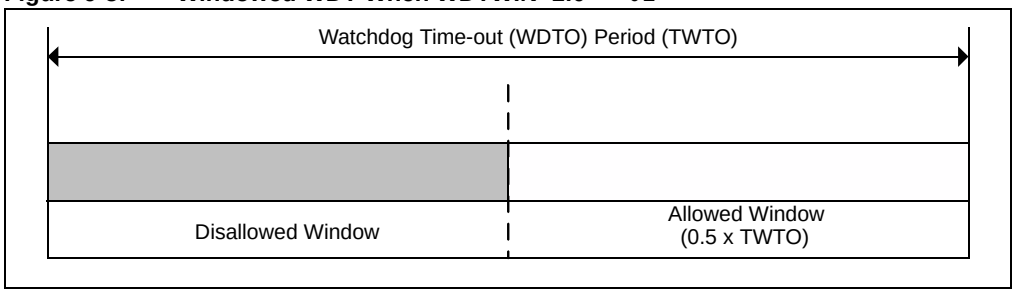
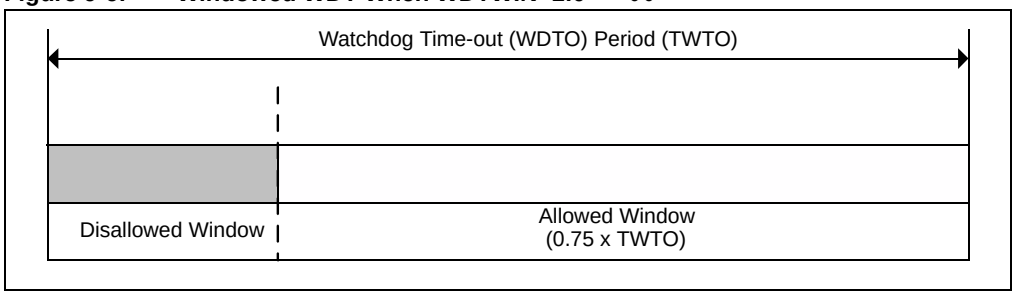


Figure 9-6: Windowed WDT When WDTWIN<1:0> = 00



9.3.2 WDTO Period Selection

The WDTO period is selected by programming the prescaler and postscaler dividers. The prescaler divider ratio is determined by the Watchdog Timer Prescaler bit (WDTPRE) in the WDT Configuration register (FWDT<4>).

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler divider ratio is determined by the Watchdog Timer Postscaler bits (WDTPOST<3:0>) in the WDT Configuration register (FWDT<3:0>), which provides 16 settings (from 1:1 to 1:32,768).

The WDT time-out value can be calculated using Equation 9-1.

Equation 9-1: WDT Time-out Period

$$T_{WTO} = (N1) \times (N2) \times (T_{LPRC})$$

Where,

$N1$ = Prescaler divider ratio (see Table 9-3)

$N2$ = Postscaler divider ratio (see Table 9-4)

T_{LPRC} = LPRC clock period

Note:	The WDT time-out period is directly related to the LPRC Oscillator frequency (32 kHz nominal). Refer to the specific device data sheet for the accuracy of the LPRC frequency over temperature and voltage variations.

Table 9-3 and Table 9-4 provide the WDT prescaler and postscaler divider settings.

Table 9-3: WDT Prescaler Divider Settings

Prescaler Setting (WDTPRE)	Prescaler Divider Ratio (N1)
0	32
1	128

Table 9-4: WDT Postscaler Divider Settings

Postscaler Setting (WDTPOST<3:0>)	Postscaler Divider Ratio (N2)
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

9.3.3 WDT Reset

The WDT is reset in the following circumstances:

- On any device Reset
- When a PWRSAV instruction is executed (i.e., Sleep mode or Idle mode is entered)
- When the WDT is enabled in software
- On the completion of a clock switch
- By a CLRWDT instruction during normal execution or during the last 25% of the WDT time-out period if WINDIS is '0'

9.3.4 Operation of WDT in Sleep Mode and Idle Mode

If enabled, the WDT continues to run during Sleep mode or Idle mode. When the WDT time-out occurs, the device wakes up and code execution continues from where the PWRSAV instruction was executed.

The WDT is useful for low-power system designs because it can be used to periodically wake the device from Sleep mode to check the system status and provide action, if necessary. The SWDTEN bit is very useful in this case. If the WDT is disabled during normal operation (FWDTEN = 0), the SWDTEN bit (RCON<5>) can be used to turn on the WDT before entering Sleep mode.

9.4 DESIGN TIPS

Question 1: ***The device resets even though I have inserted a*** `CLRWDT` ***instruction in my main software loop.***

Answer: Ensure that the software loop that contains the `CLRWDT` instruction meets the minimum specification of the WDT (not the typical value). Also, ensure that interrupt processing time has been accounted for.

Question 2: ***What should my software do before entering Sleep mode or Idle mode?***

Answer: Ensure that the sources intended to wake the device have their Interrupt Enable bits set. In addition, ensure that the particular source of interrupt can wake the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, ensure that the “stop-in-idle” control bit for each peripheral device is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. Refer to the individual peripheral sections in this manual for further details.

Question 3: ***How do I tell which peripheral woke the device from Sleep mode or Idle mode?***

Answer: You can poll the Interrupt Flag bits for each enabled interrupt source to determine the source of wake-up.

9.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Watchdog Timer (WDT) and power-saving modes include the following:

Title	Application Note #
Low-Power Design using PIC® Microcontrollers	AN606

Note: Visit Microchip Web site (www.microchip.com) for additional application notes and code examples for the dsPIC33F/PIC24H families of devices.

9.6 REVISION HISTORY

Revision A

This is the initial released version of this document.

Revision B (March 2010)

This revision incorporates the following updates:

- Merged the dsPIC33F and PIC24H family reference manual sections titled Section 9. Watchdog Timer (WDT) and Power-Saving Modes, into this single document
- Tables:
  - Updated the postscaler setting values in binary representation (see Table 9-4)
- Note:
  - Added a note with information to customers for utilizing family reference manual sections and data sheets as a joint reference (see note above **9.1 “Introduction”**)
  - Added a note on executing the `NOP` instruction in the Doze mode section (see **9.2.3 “Hardware-based Doze Mode”**)
- Additional minor corrections such as language and formatting updates are incorporated throughout the document

Revision C (July 2010)

This revision includes the following updates:

- Updated the WDT Block Diagram (see Figure 9-2)
- Added a new paragraph to **9.3.1 “WDT Operation”**
- Added Table 9-2: Window Bit Options
- Replaced Figure 9-3 and added Figure 9-4 through Figure 9-6
- Additional minor corrections to text and formatting have been incorporated throughout the document

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-60932-368-4

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/05/10