Section 35. Parallel Master Port (PMP)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Parallel Master Port (PMP)"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

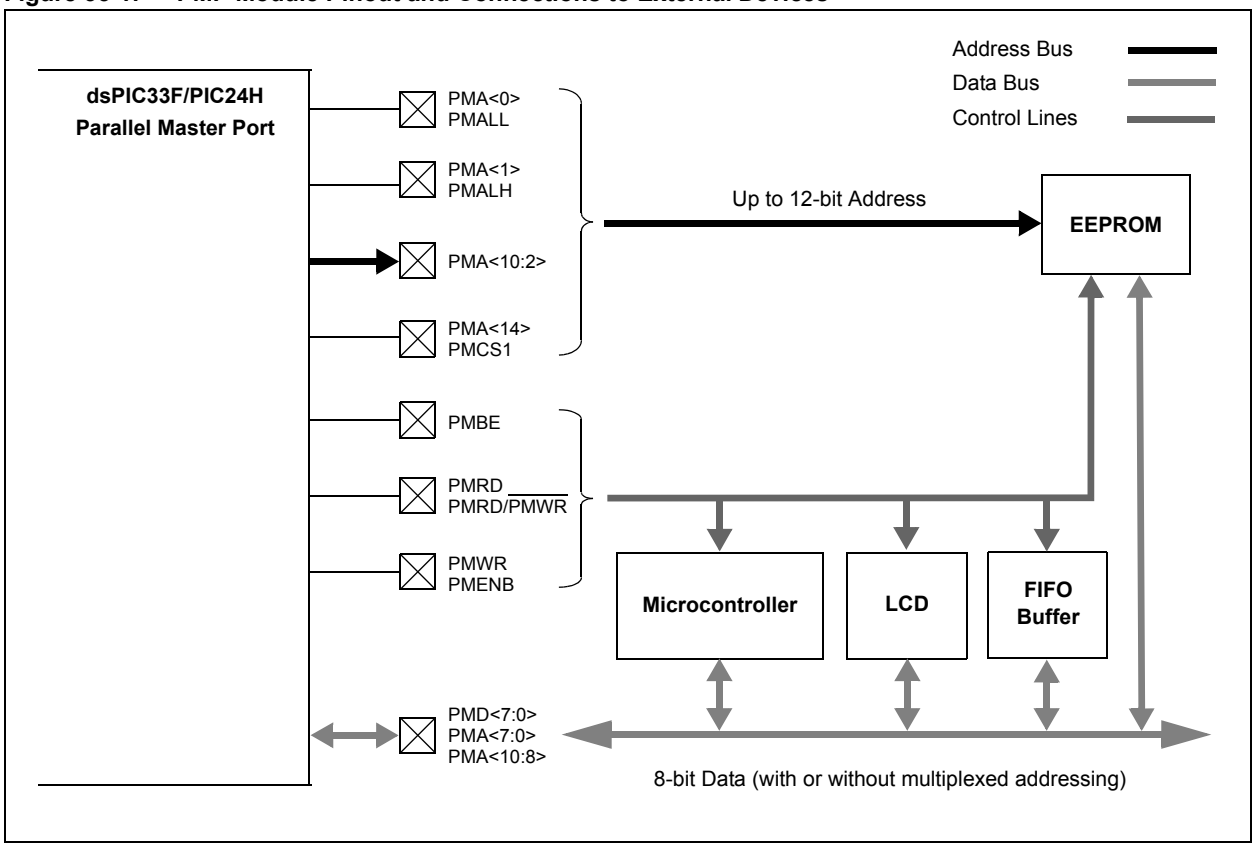
35.1 INTRODUCTION

The Parallel Master Port (PMP) is a parallel 8-bit I/O module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. The PMP module is highly configurable because the interface to parallel peripherals varies significantly.

Key features of the PMP module include:

- Eight Data Lines
- Up to 12 Programmable Address Lines
- Single Chip Select Line
- Programmable Strobe Options:
  - Individual read and write strobes, or
  - Read/Write strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait States

Figure 35-1: PMP Module Pinout and Connections to External Devices



35.2 MODULE REGISTERS

The PMP module uses these Special Function Registers (SFRs):

- **PMCON: Parallel Master Port Control Register**

  The Parallel Master Port Control register contains the bits that control most of the module's basic functionality. A key bit is PMPEN, which is used to reset the module and enable or disable the module. When the module is disabled, all of the associated I/O pins revert to their designated I/O function. In addition, any read or write operations, active or pending, are stopped and the BUSY bit is cleared. The data within the module registers is retained, including PMSTAT. Therefore, the module can be disabled after a reception, and the last received data and status will be available for processing. When the module is enabled, all buffer control logic is reset along with PMSTAT.

  All other bits in the PMCON register control address multiplexing, enable various port control signals, and select control signal polarity. For more information on PMCON bits see **35.4.1 "Parallel Master Port Configuration Options"**.

- **PMMODE: Parallel Master Port Mode Register**

  The Parallel Master Port Mode register contains bits that control the operational modes of the module. The Master/Slave mode selection, and configuration options for both the modes, are set by this register. It also contains the universal status flag, BUSY, used in Master modes to indicate that an operation by the module is in progress.

  For more information on the use of the PMMODE bits to configure PMP operation, see **35.3 "Slave Port Modes"** and **35.4 "Master Port Modes"**.

- **PMADDR: Parallel Master Port Address Register (Master modes only)(1)**

  Depending on the selected mode, this single register can have one of two functions. In Master modes, the register functions as the Parallel Master Port Address register (PMADDR). It contains the address to which outgoing data is to be written to, as well as the Chip Select control bits for addressing parallel slave devices.

  In Slave mode, the register functions as PMDOUT1 and acts as a buffer for outgoing data. Its operation is described in **35.3.2 "Buffered Parallel Slave Port Mode"**.

- **PMAEN: Parallel Master Port Address Enable Register**

  The Parallel Master Port Address Enable register controls the operation of address and Chip Select pins associated with this module. Setting these bits allocates the corresponding microcontroller pins to the PMP module; clearing these bits allocates the pins to port I/O or other peripheral modules associated with the pins.

- **PMSTAT: Parallel Master Port Status Register (Slave mode only)**

  The Parallel Master Port Status register contains status bits associated with buffered operating modes when the port is functioning as a Slave port. This includes the overflow, underflow and full flag bits. For more information on flag bits, see **35.3.2 "Buffered Parallel Slave Port Mode"**.

- **PMDOUT1: Parallel Master Port Data Output 1 Register (Slave mode only)**

  For more information on PMDOUT1, see **PMADDR: Parallel Master Port Address Register (Master modes only)(1)**.

- **PMDOUT2: Parallel Master Port Data Output 2 Register (Slave mode only)**

  The Parallel Master Port Data Output 2 register is only used in Slave mode for buffered output data. It is used in the same way as PMDOUT1.

- **PMDIN1: Parallel Master Port Data Input 1 Register**

  The Parallel Master Port Data Input 1 and Data Input 2 registers are used to buffer incoming data. PMDIN1 is used by the module in Master and Slave modes.

  In Slave mode, this register is used to hold data that is asynchronously clocked in. Its operation is described in **35.3.2 "Buffered Parallel Slave Port Mode"**.

  In Master mode, PMDIN1 is the holding register for both incoming and outgoing data. Its operation in Master mode is described in **35.4.2 "Read Operation"** and **35.4.3 "Write Operation"**.

- **PMDIN2: Parallel Master Port Data Input 2 Register (Buffered Slave mode only)**

  PMDIN2 is only used in Buffered Slave modes for incoming data. In Buffered Slave modes, its operation is similar to that of PMDIN1.

- **PADCFG1: Pad Configuration Control Register**

  In addition to the PMP-specific registers, the PADCFG1 register also affects the configuration of the PMP module. The PMPTTL bit (PADCFG1<0>) allows the user application to select between TTL and Schmitt Trigger (ST) digital input buffers for greater compatibility with external circuits. Setting the PMPTTL bit, selects the TTL input buffers. The default configuration is ST buffers.

Register 35-1: PMCON: Parallel Master Port Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX<1:0>		PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0(1)	U-0	R/W-0(1)	R/W-0	R/W-0	R/W-0
CSF<1:0>		ALP	—	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Reserved
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 8 bits are on PMA<10:8>
00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
1 = PMBE port enabled
0 = PMBE port disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port enabled
0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port enabled
0 = PMRD/$\overline{\text{PMWR}}$ port disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMCS1 functions as Chip Select
0x = PMCS1 functions as address bit 14

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CS1P:** Chip Select 1 Polarity bit(1)
1 = Active-high
0 = Active-low

bit 2 **BEP:** Byte Enable Polarity bit
1 = Byte enable active-high ($\overline{\text{PMBE}}$)
0 = Byte enable active-low ($\overline{\text{PMBE}}$)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 35-1: PMCON: Parallel Master Port Control Register (Continued)

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Read strobe active-high (PMWR)
0 = Read strobe active-low ($\overline{PMWR}$)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{PMENB}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Read strobe active-high (PMRD)
0 = Read strobe active-low ($\overline{PMRD}$)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{PMWR}$)
0 = Read/write strobe active-low ($\overline{PMRD}$/$\overline{PMWR}$)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 35-2: PMMODE: Parallel Master Port Mode Register

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB<1:0>(1)		WAITM<3:0>				WAITE<1:0>(1)	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt generated at the end of the read/write cycle
00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
10 = Decrement ADDR<15,13:0> by 1 every read/write cycle
01 = Increment ADDR<15,13:0> by 1 every read/write cycle
00 = No increment or decrement of address

bit 10 **MODE16:** 8-Bit/16-Bit Mode bit
1 = In 16-bit mode, data register is 16 bits, a read or write to the data register invokes two 8-bit transfers
0 = In 8-bit mode, data register is 8 bits, a read or write to the data register invokes one 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 = Master Mode 1 (PMCSx, PMRD/$\overline{\text{PMWR}}$, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
10 = Master Mode 2 (PMCSx, PMRD, $\overline{\text{PMWR}}$, $\overline{\text{PMBE}}$, PMA<x:0> and PMD<7:0>)
01 = Enhanced PSP, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCSx}}$, PMD<7:0> and PMA<1:0>)
00 = Legacy Parallel Slave Port, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCSx}}$ and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Wait State Configuration bits(1)
11 = Data wait of 4 TCY; multiplexed address phase of 4 TCY
10 = Data wait of 3 TCY; multiplexed address phase of 3 TCY
01 = Data wait of 2 TCY; multiplexed address phase of 2 TCY
00 = Data wait of 1 TCY; multiplexed address phase of 1 TCY

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits
1111 = Wait of additional 15 TCY
•
•
•
0001 = Wait of additional 1 TCY
0000 = No additional Wait cycles (operation forced into one TCY)

Note 1: WAITBx and WAITEx bits are ignored whenever WAITM<3:0> = 0000.

2: WAITM<3:0> and WAITE<1:0> bits are ignored when WAITB<1:0> bits determine the duration of the address latch signal.

Register 35-2: PMMODE: Parallel Master Port Mode Register (Continued)

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits(1)
11 = Wait of 4 TCY
10 = Wait of 3 TCY
01 = Wait of 2 TCY
00 = Wait of 1 TCY

Note 1: WAITBx and WAITEx bits are ignored whenever WAITM<3:0> = 0000.

2: WAITM<3:0> and WAITE<1:0> bits are ignored when WAITB<1:0> bits determine the duration of the address latch signal.

Register 35-3: PMADDR: Parallel Master Port Address Register (Master modes only)(1)

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	CS1(2)	—	—	—	ADDR<10:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **CS1:** Chip Select 1 bit(2)
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive

bit 13-11 **Unimplemented:** Read as '0'

bit 10-0 **ADDR<10:0>:** Destination Address bits 10-0

Note 1: In Enhanced Slave mode, PMADDR functions as PMDOUT1, which is one of the two data buffer registers. For more information, see **35.2 "Module Registers"**.

2: When CSF<1:0> = 0x, CS1 bit functions as ADDR<14>.

Register 35-4: PMAEN: Parallel Master Port Address Enable Register

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	PTEN	—	—	—	PTEN<10:8>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **PTEN<14>:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits
1 = PMA<10:2> function as PMP address lines
0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O

Register 35-5: PMSTAT: Parallel Master Port Status Register (Slave mode only)

R-0	R/W-0 HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0 HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable input buffer registers are full
0 = Some or all the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full input byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBnF:** Input Buffer 'n' Status Full bit
1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable output buffer registers are empty
0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBnE:** Output Buffer 'n' Status Empty bit
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

Register 35-6: PADCFG1: Pad Configuration Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL(1)	PMPTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit(1)
- 1 = RTCC seconds clock is selected for the RTCC pin
- 0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffers

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) bit needs to be set. For more information, refer to **Section 37. "Real-Time Clock and Calendar (RTCC)**" (DS70301)

35.3 SLAVE PORT MODES

In Slave Port mode, the PMP module provides an 8-bit data bus and all the necessary control signals to operate as a slave parallel device. It is also configurable for operation in Legacy, Buffered and Addressable modes. Slave Port mode provides the following options for a flexible interface:

- 8-bit data bus
- Two address lines (Addressable mode only)
- Three control lines (Read, Write and Chip Select)
- Selectable polarity on all control lines

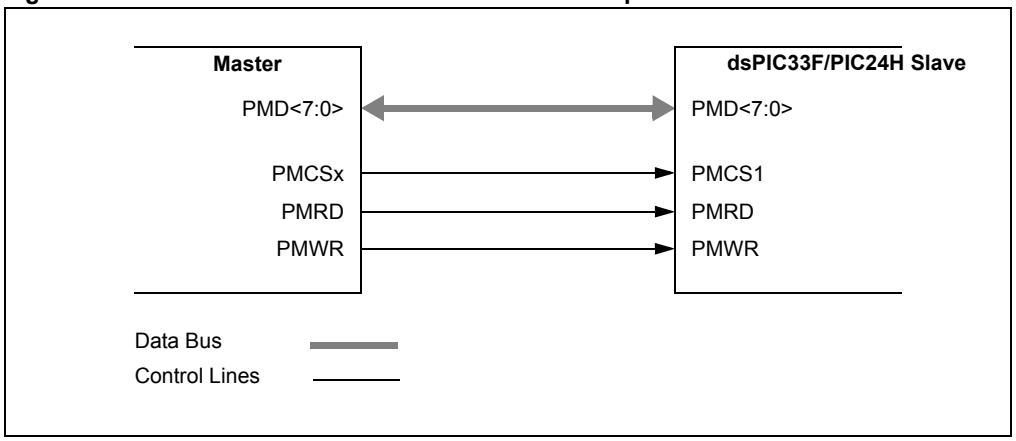
To use the PMP as a slave, the module must be enabled (PMPEN = 1) and the mode must be set to one of the two possible Slave modes (PMMODE<9:8> = 01 or 00).

35.3.1 Legacy Mode

In Legacy mode (PMPEN = 1 and PMMODE<9:8> = 00), the module is configured as a parallel slave port with the associated enable module pins dedicated to the module. In this mode, an external device, such as another microcontroller or microprocessor, can asynchronously read and write data using the 8-bit data bus (PMD<7:0>), the Read (PMRD), Write (PMWR) and Chip Select (PMCS1) inputs.

Note:	PMCS1 is used as the Chip Select input in all slave port modes.

Figure 35-2: Parallel Master/Slave Connection Example

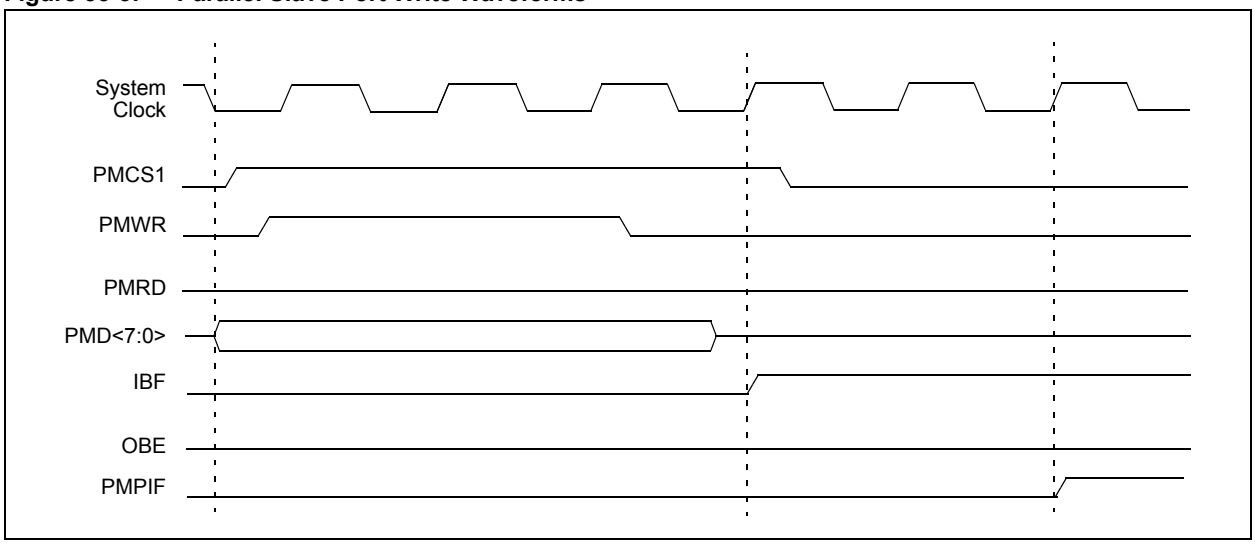


35.3.1.1 WRITE TO SLAVE PORT

When Chip Select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into the lower 8 bits of the PMDIN1 register (PMDIN1<7:0>). The PMPIF and IBF flag bits are set when the write ends.

The timing for the control signals in Write mode is illustrated in Figure 35-3. The polarity of the control signals is configurable.

Figure 35-3: Parallel Slave Port Write Waveforms

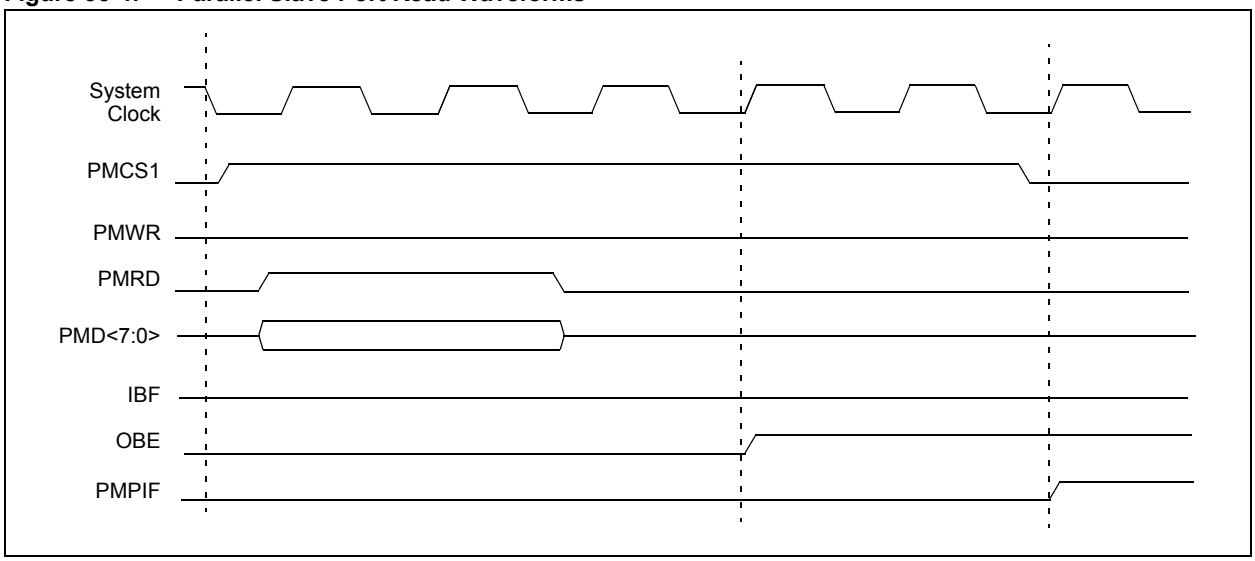


35.3.1.2 READ FROM SLAVE PORT

When Chip Select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from the lower 8 bits of the PMDOUT1 register (PMDOUT1<7:0>) is presented onto PMD<7:0>. The data in PMDIN1<7:0> is read out and the Output Buffer Empty flag (OBE) is set. If the user application writes new data to PMDIN1<7:0>, to clear OBE, the data is immediately read out; however, the OBE is not cleared.

The timing for the control signals in Read mode is illustrated in Figure 35-4.

Figure 35-4: Parallel Slave Port Read Waveforms



35.3.1.3 INTERRUPT OPERATION

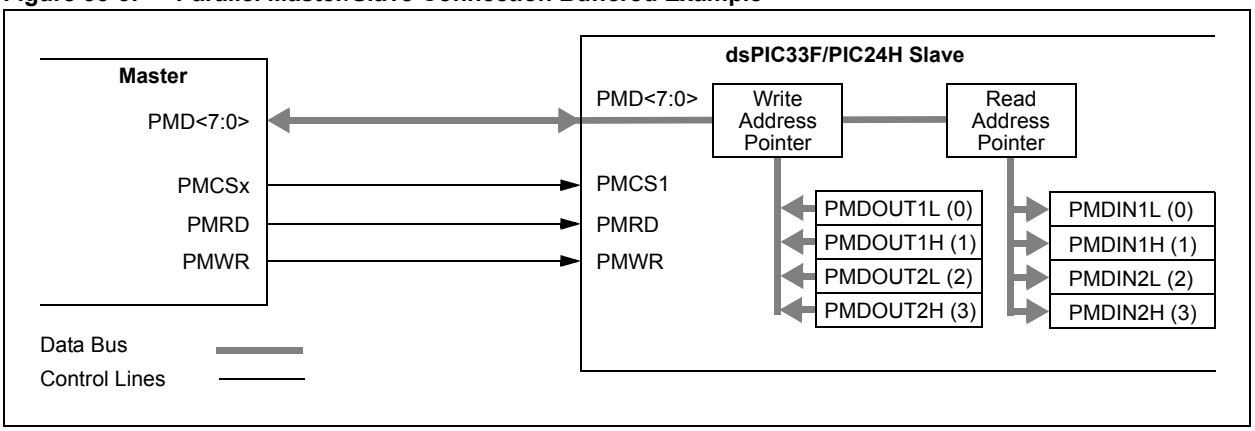
When either the PMCS1 or PMRD lines are detected high, the port pins return to the input state and the PMPIF bit is set. User applications should wait for PMPIF to be set before servicing the module. During this time the IBF and OBE bits can be polled and the appropriate action is carried out.

35.3.2 Buffered Parallel Slave Port Mode

Buffered Parallel Slave Port mode is functionally identical to the Legacy Parallel Slave Port mode with one exception: the implementation of 4-level read and write buffers. Buffered PSP mode is enabled by setting the INCM<1:0> bits (PMMODE<12:11>) to '11'.

When the buffered mode is active, the module uses the PMDIN1 and PMDIN2 registers as write buffers and the PMDOUT1 and PMDOUT2 registers as read buffers. Each register is split into two single byte buffer registers, producing separate read and write buffers that are 4 bytes deep. Buffers are numbered 0 through 3, starting with the lower byte of PMDIN1 or PMDOUT1 and progressing upward through the high byte of PMDIN2 (PMDOUT2).

Figure 35-5: Parallel Master/Slave Connection Buffered Example



35.3.2.1 READ FROM SLAVE PORT

For read operations, the bytes will be sent out sequentially, starting with Buffer 0 (PMDOUT1<7:0>) and ending with Buffer 3 (PMDOUT2<15:8>) for every read strobe. The module maintains an internal pointer to keep track of which buffer is to be read.

Each of the buffers has a corresponding read status bit, OBnE, in the PMSTAT register. This bit is cleared when a buffer contains data that is not written to the bus, and is set when data is written to the bus. If the current buffer location being read from is empty, a buffer underflow is generated, and the Buffer Overflow Flag bit, OBUF (PMSTAT<6>), is set. If all four OBnE status bits are set, the OBE bit will also be set.

35.3.2.2 WRITE TO SLAVE PORT

For write operations, the data is stored sequentially, starting with Buffer 0 (PMDIN1<7:0>) and ending with Buffer 3 (PMDIN2<15:8>). As with read operations, the module maintains an internal pointer to the buffer that is to be written next.

The input buffers have their own write status bits, IBnE. The bit is set when the buffer contains unread incoming data, and cleared when the data is read. The flag bit is set on the write strobe. If a write occurs on a buffer, when its associated IBnE bit is set, the Input Buffer Overflow Flag (IBOV) is set; any incoming data in the buffer will be lost. If all four IBnE flags are set, the Input Buffer Full Flag (IBF) is set.

35.3.2.3 INTERRUPT OPERATION

In Buffered Slave mode, the module can be configured to generate an interrupt on every read or write strobe (IRQM<1:0> = 01). It can also be configured to generate an interrupt on a read from Read Buffer 3 or a write to Write Buffer 3 (IRQM<1:0> = 11), which is essentially an interrupt every fourth read or write strobe. When interrupting every fourth byte for input data, all input buffer registers should be read to clear the IBnF flags. If these flags are not cleared, there is a risk of an overflow condition. The PMSTAT register provides status information on all buffers.

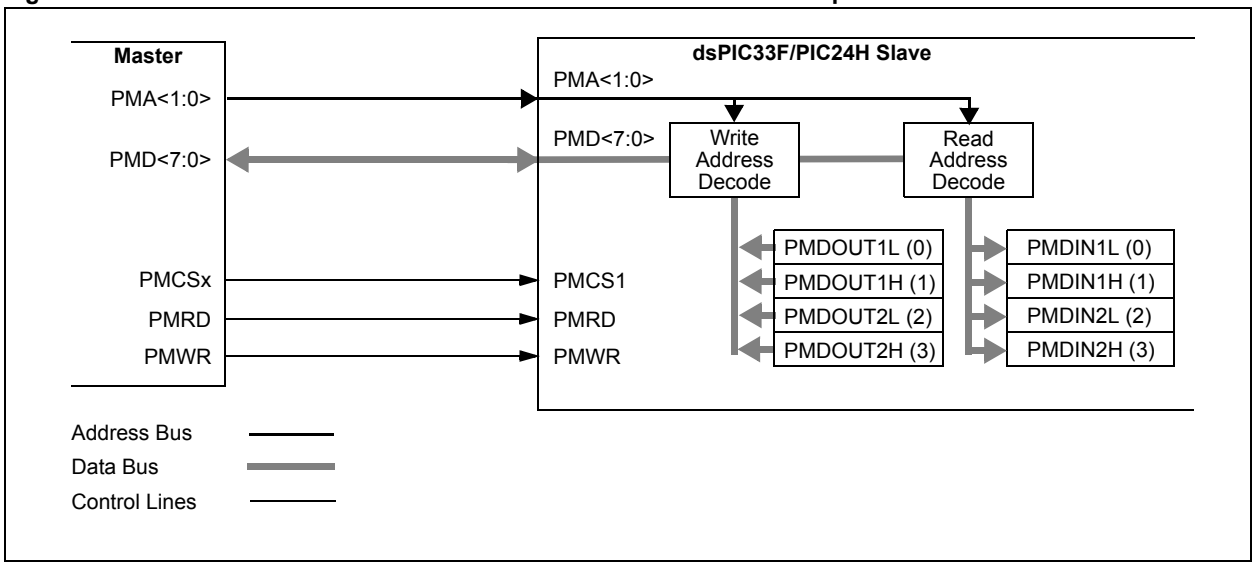
35.3.3 Addressable Parallel Slave Port Mode

In Addressable Parallel Slave Port (PSP) mode, the module is configured with two extra inputs, PMA<1:0>. This makes the 4-byte buffer space directly addressable as fixed pairs of read and write buffers. The Addressable PSP mode is enabled by setting the MODE<1:0> bits (PMMODE<9:8>) to '01'. As with Buffered Legacy mode, data is output from PMDOUT1 and PMDOUT2, and is read in PMDIN1 and PMDIN2. Table 35-1 provides the address resolution for the incoming address to the input and output registers.

Table 35-1: Slave Mode Address Resolution

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1<7:0> (0)	PMDIN1<7:0> (0)
01	PMDOUT1<15:8> (1)	PMDIN1<15:8> (1)
10	PMDOUT2<7:0> (2)	PMDIN2<7:0> (2)
11	PMDOUT2<15:8> (3)	PMDIN2<15:8> (3)

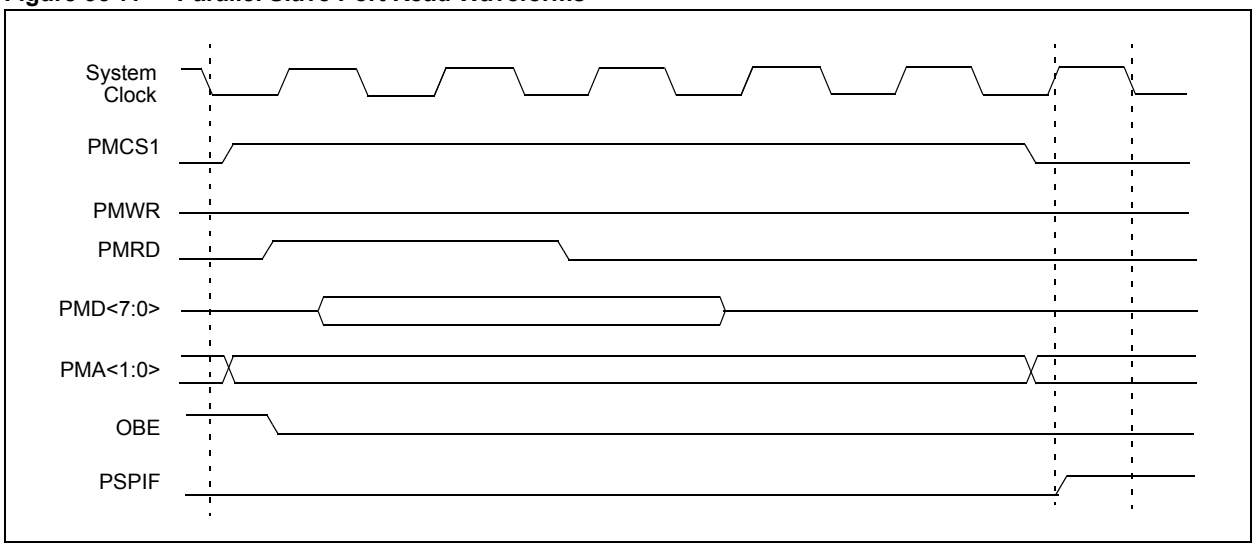
Figure 35-6: Parallel Master/Slave Connection Addressed Buffer Example



35.3.3.1 READ FROM SLAVE PORT

When Chip Select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from one of the four output bytes is presented onto PMD<7:0>. This output byte read depends on the 2-bit address placed on PMA<1:0>. Table 35-1 provides the corresponding output registers and their associated address. When an output buffer is read, the corresponding OBnE bit is set. The OBE flag bit is set when all the buffers are empty. If any buffer is already empty, OBnE = 1, the next read to that buffer will set the OBUF flag (PMSTAT<6>).

Figure 35-7: Parallel Slave Port Read Waveforms

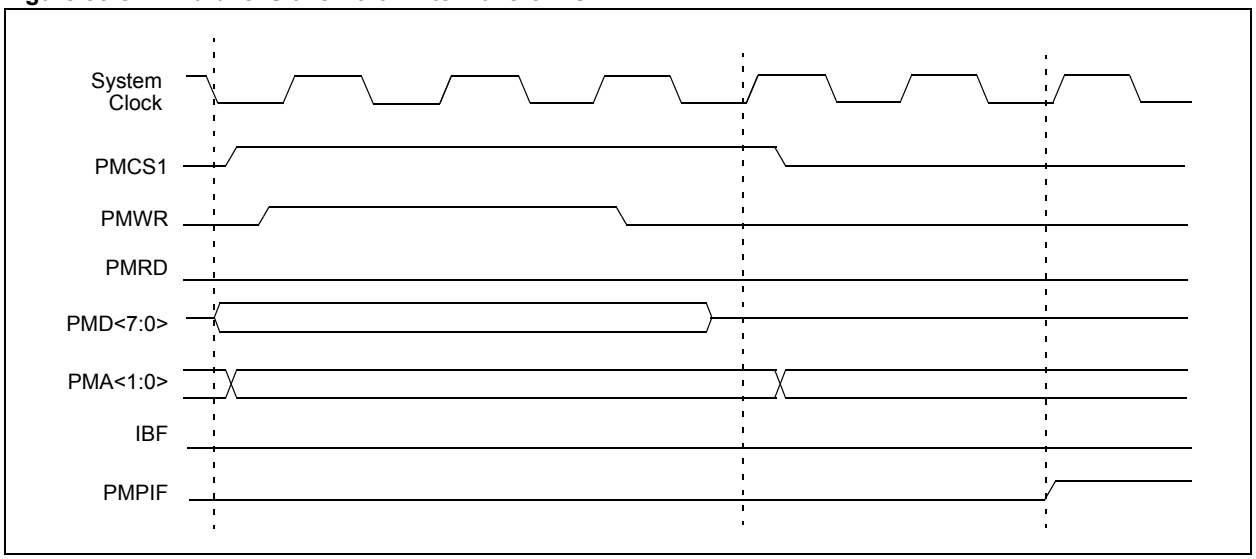


35.3.3.2 WRITE TO SLAVE PORT

When Chip Select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into one of the four input buffer bytes. The byte to be written depends on the 2-bit address placed on PMA<1:0>. Table 35-1 provides the corresponding input registers and their associated address.

When an input buffer is written, the corresponding IBnF bit is set. The IBF flag bit is set when all the buffers are written. If any buffer is already written, IBnF = 1, the next write strobe to that buffer will generate an OBUF event and the byte will be discarded.

Figure 35-8: Parallel Slave Port Write Waveforms



35.3.3.3 INTERRUPT OPERATION

In Addressable PSP mode, the module can be configured to generate an interrupt on every read or write strobe. It can also be configured to generate an interrupt on any read from Read Buffer 3 or write to Write Buffer 3; in other words, an interrupt occurs whenever a read or write occurs when the PMA<1:0> pins are set to '11'.

35.4 MASTER PORT MODES

In the master port modes, the PMP module provides an 8-bit data bus, up to 16 bits of address and all the necessary control signals to operate a variety of external parallel devices, such as memory devices, peripherals and slave microcontrollers. To use the PMP as a master, the module must be enabled (PMPEN = 1), and the mode must be set to one of the two possible Master modes (PMMODE<9:8> = 10 or 11).

the PMP module is designed to be extremely flexible to accommodate a range of configurations, because there are many parallel devices with a variety of control methods. Some of these features include:

- 8-bit and 16-bit Data modes on an 8-bit data bus
- Configurable address/data multiplexing
- Up to 16 selectable address lines
- Address auto-increment and auto-decrement
- Selectable polarity on all control lines
- Configurable Wait states at different stages of the read/write cycle

35.4.1 Parallel Master Port Configuration Options

35.4.1.1 CHIP SELECTS

A single Chip Select line PMCS1 is available for Master mode of PMP module. This Chip Select line is multiplexed with the PMA<14> bit of the address bus. When a pin is configured as a Chip Select, it is not included in any address auto-increment/auto-decrement. The function of the Chip Select signals is configured using the Chip Select Function bits, CSF<1:0> (PMCON <7:6>).

35.4.1.2 PORT PIN CONTROL

Several bits are available to configure the presence or absence of control and address signals in the module. These bits are PTBEEN, PTWREN, PTRDEN and PTEN<14:0>. They can provide conserve pins for other functions and allow flexibility to control the external address. When any one of these bits is set, the associated function is present on its associated pin; when clear, the associated pin reverts to its defined I/O port function.

Setting a PTENx bit will enable the associated pin as an address pin and drive the corresponding data contained in the PMADDR register. Clearing the PTENx bit will force the pin to revert to its original I/O function.

For the pins configured as Chip Select (PMCS1) with the corresponding PTENx bit set, Chip Select pins drive inactive data (configured through the CSxP bits in PMCON) when a read/write operation is not being performed. The PTEN0 and PTEN1 bits also control the PMALL and PMALH signals. When multiplexing is used, the associated address latch signals should be enabled.

35.4.1.3 ADDRESS MULTIPLEXING

In either of the Master modes (MODE<1:0> = 1x), the user application can configure the address bus to be multiplexed together with the data bus. This is accomplished using the ADRMUX<1:0> bits. There are three address multiplexing modes available. Typical pinout configurations for these modes are illustrated in Figure 35-9, Figure 35-10 and Figure 35-11.

In Demultiplexed mode (ADRMUX<1:0> = 00), data and address information are separated. Data bits are presented on PMD<7:0> and address bits are presented on PMA<10:0>.

In Partially Multiplexed mode (ADRMUX<1:0> = 01), the lower eight bits of the address are multiplexed with the data pins on PMD<7:0>. The upper three bits of the address are unaffected and are presented on PMA<10:8>. The PMA<0> pin is used as an address latch, and presents the Address Latch Low enable strobe (PMALL). The read and write sequences are extended by a complete CPU cycle, during which the address is presented on the PMD<7:0> pins.

In Fully Multiplexed mode (ADRMUX<1:0> = 10), the entire 16 bits of the address are multiplexed with the data pins on PMD<7:0>. The PMA<0> and PMA<1> pins are used to present Address Latch Low enable (PMALL) and Address Latch High enable (PMALH) strobes. The read and write sequences are extended by two complete CPU cycles. During the first cycle, the lower 8 bits of the address are presented on the PMD<7:0> pins with the PMALL strobe active. During the second cycle, the upper eight bits of the address are presented on the PMD<7:0> pins with the PMALH strobe active. In the event the upper address bits are configured as Chip Select pins, the corresponding address bits are automatically forced to '0'.

For sample timings of the different multiplexing modes, see **35.4.5 "Master Mode Timing"**.

Figure 35-9: Demultiplexed Addressing Mode (Separate Read and Write Strobes, One Chip Select)

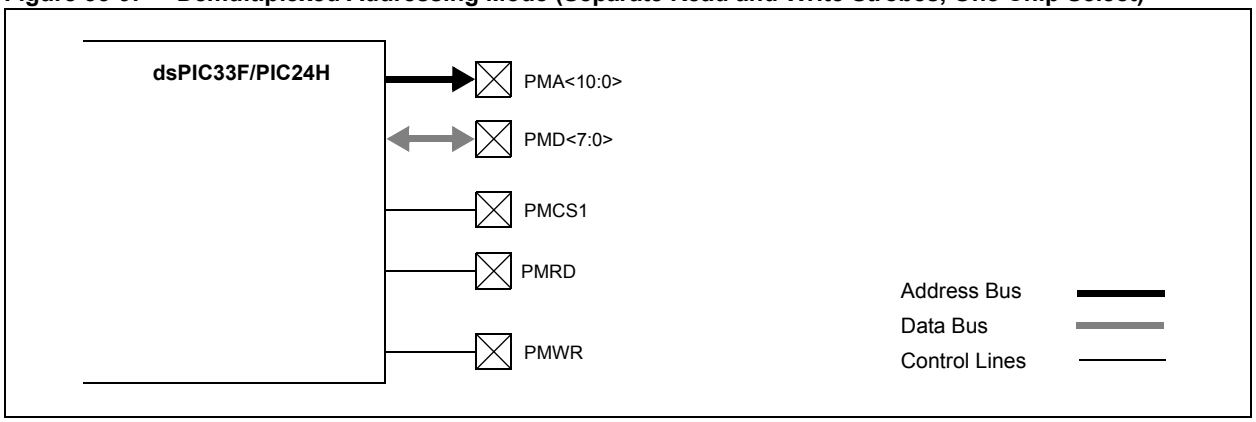


Figure 35-10: Partially Multiplexed Addressing Mode (Separate Read and Write Strobes, One Chip Select)

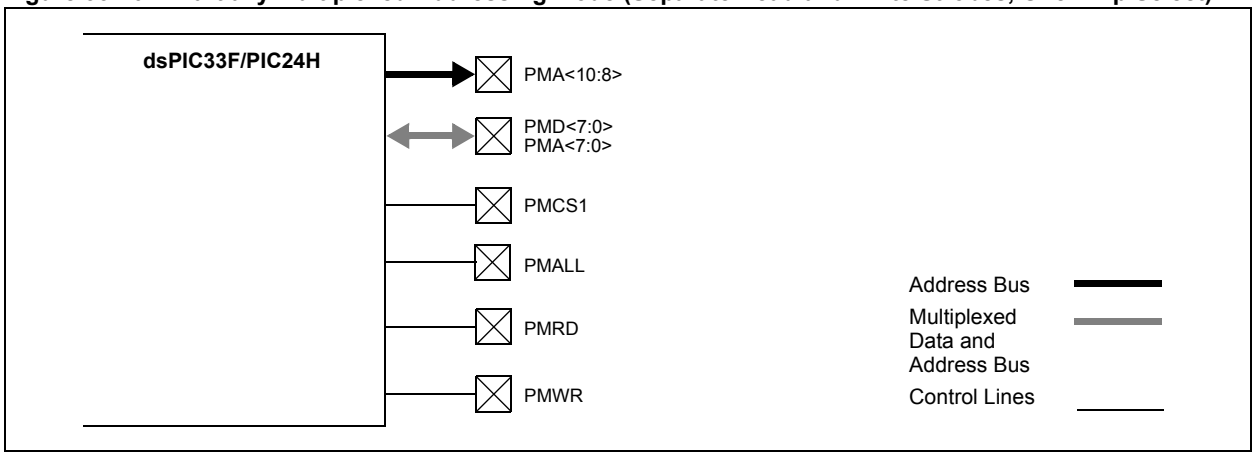


Figure 35-11: Fully Multiplexed Addressing Mode (Separate Read and Write Strobes, One Chip Select)

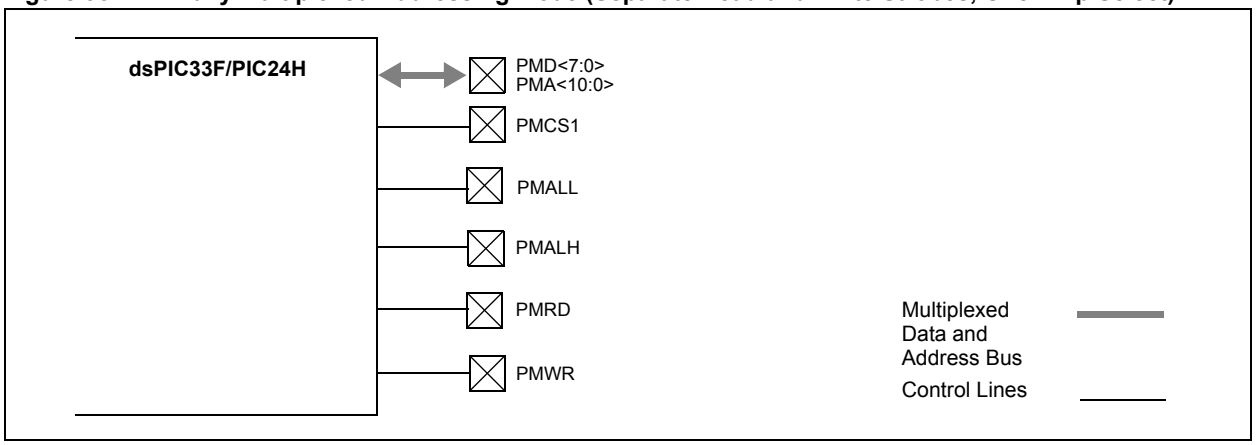
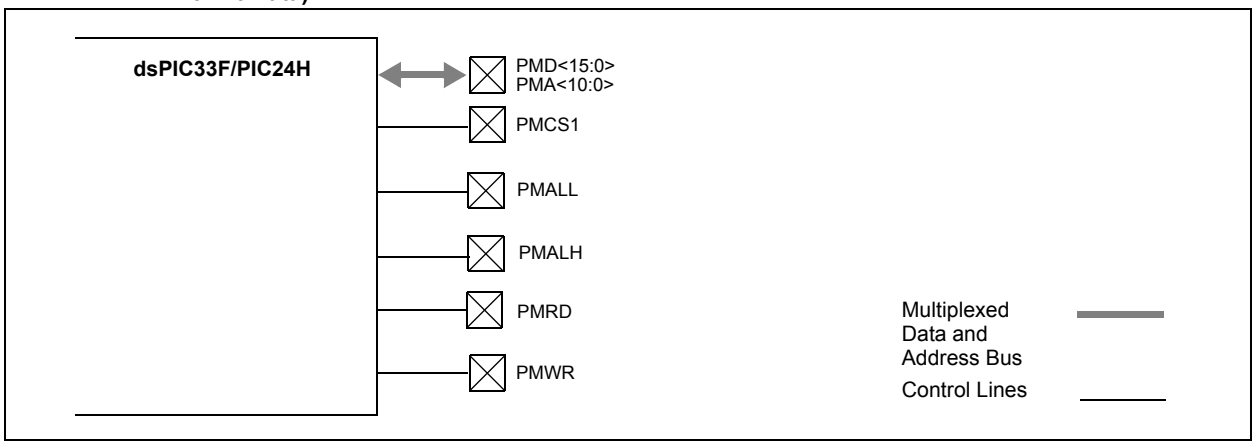


Figure 35-12: Fully Multiplexed Addressing Mode (Separate Read and Write Strobes, One Chip Select and 16-Bit Data)



35.4.1.4 8-BIT AND 16-BIT DATA MODES

The PMP supports data widths of both 8 bits and 16 bits. The data width is selected by the MODE16 bit (PMMODE<10>). Because the data path into and out of the module is only 8 bits wide, 16-bit operations are always handled in a multiplexed fashion, with the Least Significant Byte (LSB) of data being presented first. To differentiate data bytes, the Byte Enable Control Strobe, PMBE, is used to signal when the Most Significant Byte (MSB) of data is being presented on the data lines.

35.4.1.5 READ/WRITE CONTROL

The PMP module supports two distinct read/write signaling methods. In Master mode 1, the read and write strobe are combined into a single control line, PMRD/PMWR; a second control line, PMENB, determines when a read or write action is to be taken. In Master mode 2, separate read and write strobes (PMRD and PMWR) are supplied on separate pins.

35.4.1.6 CONTROL LINE POLARITY

All control signals (PMRD, PMWR, PMBE, PMENB, PMAL and PMCSx) can be individually configured for either positive or negative polarity. The configuration is controlled by separate bits in the PMCON register.

Note:	The polarity of control signals that share the same output pin (for example, PMWR and PMENB) are controlled by the same bit; the configuration depends on which master port mode is being used.

35.4.1.7 AUTO-INCREMENT/AUTO-DECREMENT

While the PMP module is operating in one of the master modes, the INCM bits (PMMODE<12:11>) control the behavior of the address value. The address can be made to automatically increment or decrement after each read and write operation. The address increments after each operation is completed and the BUSY bit goes to '0'. If the Chip Select signals are disabled and configured as address bits, the bits will participate in the increment and decrement operations; otherwise, the CS1 bit value will be unaffected.

35.4.1.8 WAIT STATES

In a master mode, the user has control over the duration of the read, write and address cycles, by configuring the module Wait states as multiples of TCY. Three portions of the cycle, the beginning, middle and end, are configured using the corresponding WAITBx, WAITMx and WAITEx bits in the PMMODE register.

The WAITB<1:0> bits (PMMODE<7:6>) set the number of Wait cycles for the data setup prior to the PMRD/$\overline{\text{PMWT}}$ strobe in Master Mode 2 (MODE <1:0> = 10), or prior to the PMENB strobe in Master Mode 1 (MODE<1:0> = 11).

The WAITM<3:0> bits (PMMODE<5:2>) set the number of Wait cycles for the PMRD/$\overline{\text{PMWT}}$ strobe in Master Mode 2 (MODE <1:0> = 10), or for the PMENB strobe in Master mode 1 (MODE <1:0> = 11). When this Wait state setting is '0', WAITBx and WAITEx have no effect.

The WAITE<1:0> bits (PMMODE<1:0>) set the number of Wait cycles for the data hold time after the PMRD/$\overline{\text{PMWT}}$ strobe in Master mode 2 (MODE <1:0> = 10), or after the PMENB strobe in Master Mode 1 (MODE <1:0> = 11).

35.4.2 Read Operation

To perform a read on the parallel port, the user application reads the low byte of the PMDIN1 register. This causes the PMP to output the desired values on the Chip Select lines and the address bus, and then the read line (PMRD) is strobed. The read data is placed into the low byte of the PMDIN1 register.

If the 16-bit mode is enabled (MODE16 = 1), the read of the low byte of the PMDIN1 register initiates two bus reads. The first read data byte is placed into the lower byte of the PMDIN1 register, and the second read data is placed into the upper byte of PMDIN1.

The read data obtained from the PMDIN1 register is the read value from the previous read operation. Therefore, the first user application read is a dummy read to initiate the first bus read and fill the read register. Also, the requested read value is not ready until after the BUSY bit is observed low. Therefore, in a back-to-back read operation, the data read from the register is the same for both reads. The next read of the register yields the new value.

35.4.3 Write Operation

To perform a write onto the parallel bus, the user application writes to the low byte of the PMDIN1 register. This causes the module to first output the desired values on the Chip Select lines and the address bus. The write data from the low byte of the PMDIN1 register is placed onto the PMD<7:0> data bus. Then, the write line (PMWR) is strobed.

If the 16-bit mode is enabled (MODE16 = 1), the write to the low byte of the PMDIN1 register initiates two bus writes. The first write consists of the data contained in the lower byte of PMDIN1 and the second write contains the upper byte of PMDIN1.

35.4.4 Parallel Master Port Status

35.4.4.1 THE BUSY BIT

In addition to the PMP interrupt, a BUSY bit is provided to indicate the status of the PMP module. This bit is only used in a master mode.

While any read or write operation is in progress, the BUSY bit is set for all but the very last CPU cycle of the operation. In effect, if a single-cycle read or write operation is requested, the BUSY bit will never be active. This allows back-to-back transfers. It is only helpful if Wait states are enabled or multiplexed address/data is selected.

While the BUSY bit is set, any request by the user application to initiate a new operation will be ignored, which means writing or reading the lower byte of the PMDIN1 register will not initiate either a read/write. The user application needs to try again after the BUSY flag is cleared.

35.4.4.2 INTERRUPTS

When the PMP module interrupt is enabled for a master mode, the PMP module will interrupt on every completed read/write cycle. Otherwise, the BUSY bit is available to query the status of the module.

35.4.5 Master Mode Timing

This section contains a number of timing examples that represent the configuration options for the common master mode. These options vary from 8-bit to 16-bit data, fully demultiplexed to fully multiplexed address, as well as Wait states.

Figure 35-13: Read and Write Timing, 8-Bit Data, Demultiplexed Address

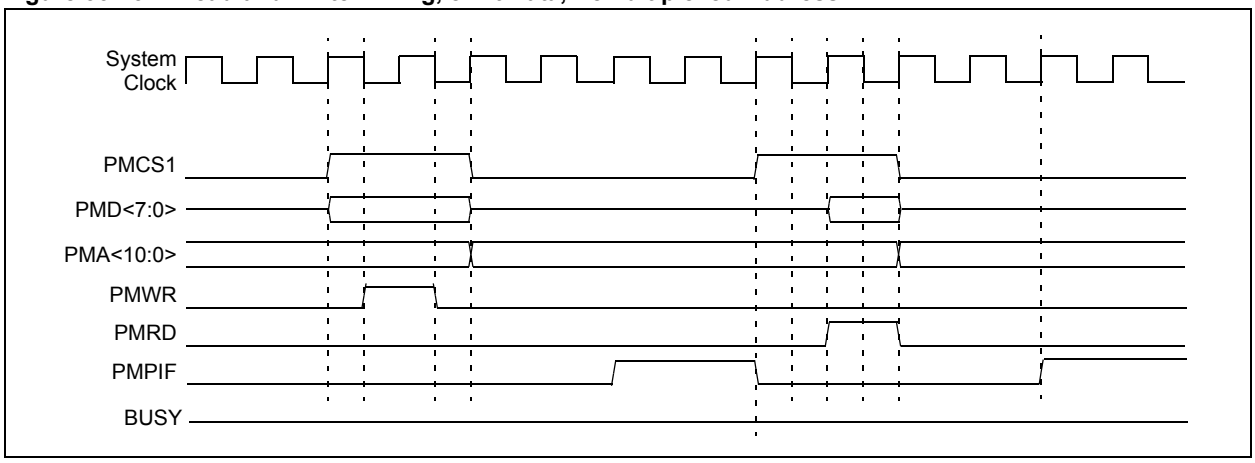


Figure 35-14: Read Timing, 8-Bit Data, Partially Multiplexed Address

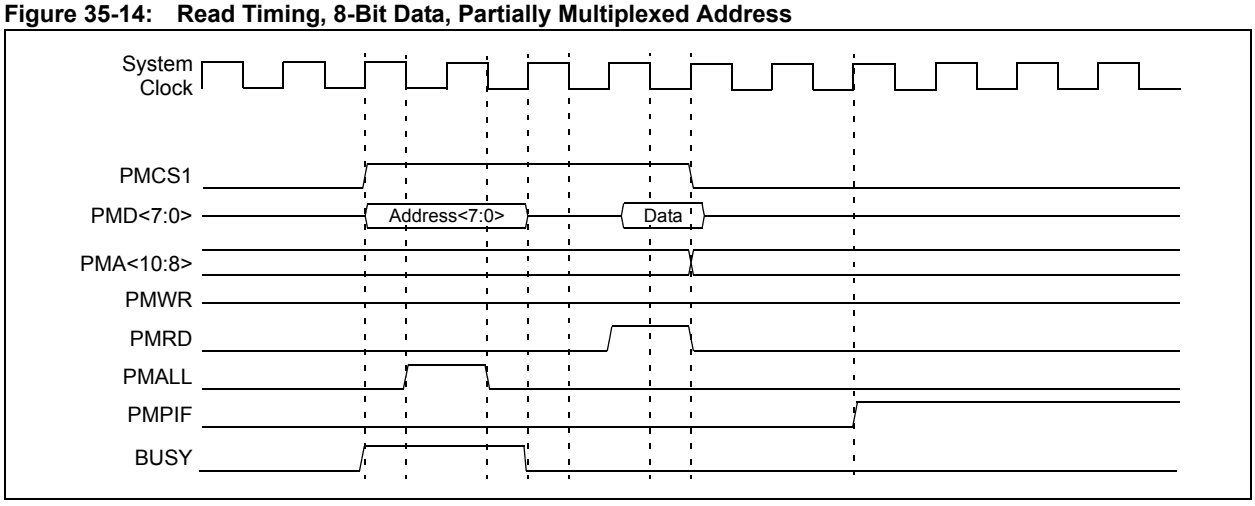


Figure 35-15: Read Timing, 8-Bit Data, Wait States Enabled, Partially Multiplexed Address

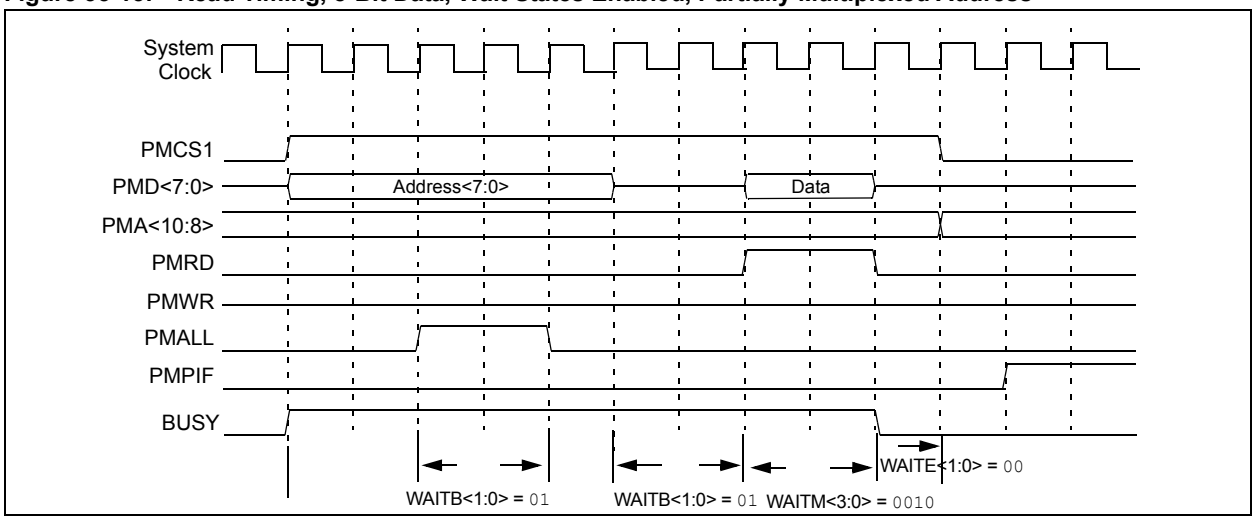


Figure 35-16: Write Timing, 8-Bit Data, Partially Multiplexed Address

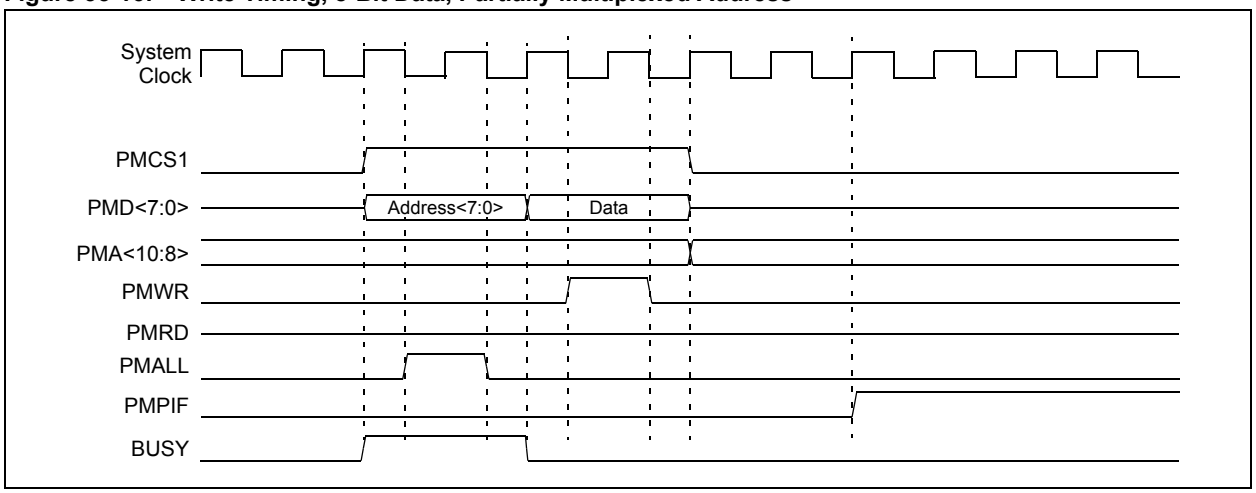


Figure 35-17: Write Timing, 8-Bit Data, Wait States Enabled, Partially Multiplexed Address

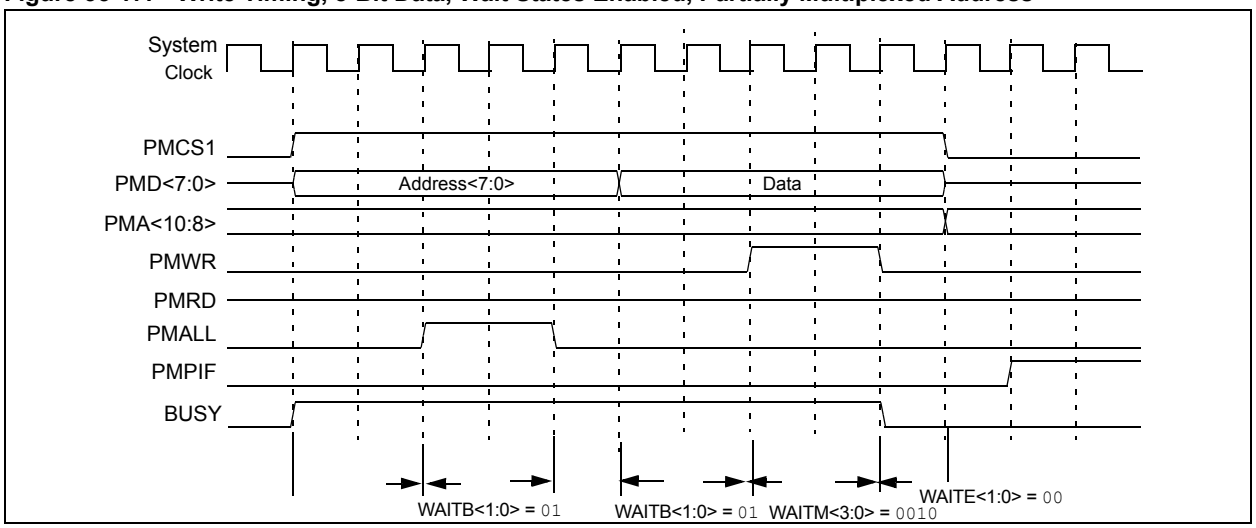


Figure 35-18: Read Timing, 8-Bit Data, Partially Multiplexed Address, Enable Strobe

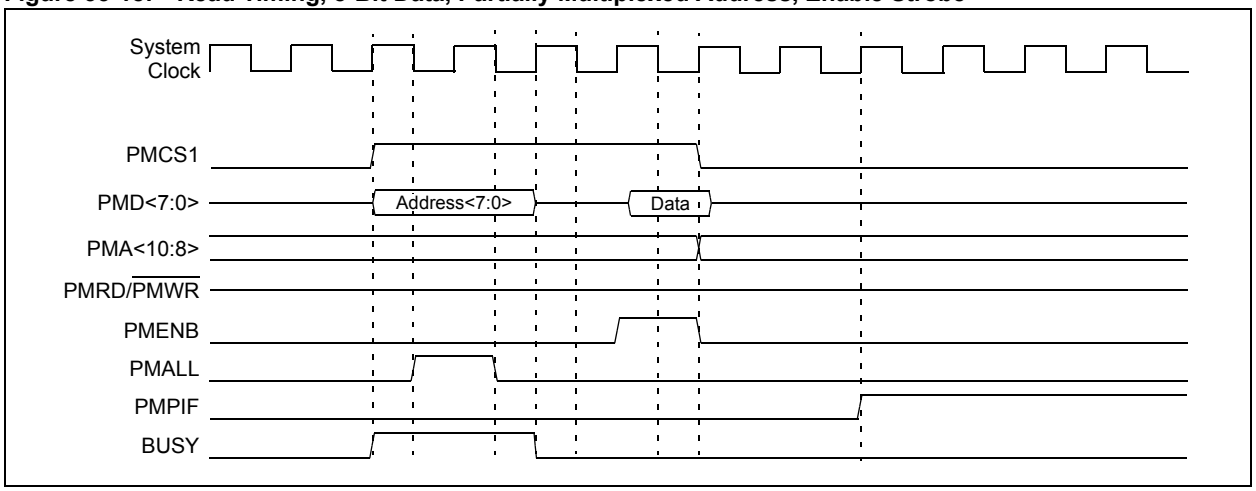


Figure 35-19: Write Timing, 8-Bit Data, Partially Multiplexed Address, Enable Strobe

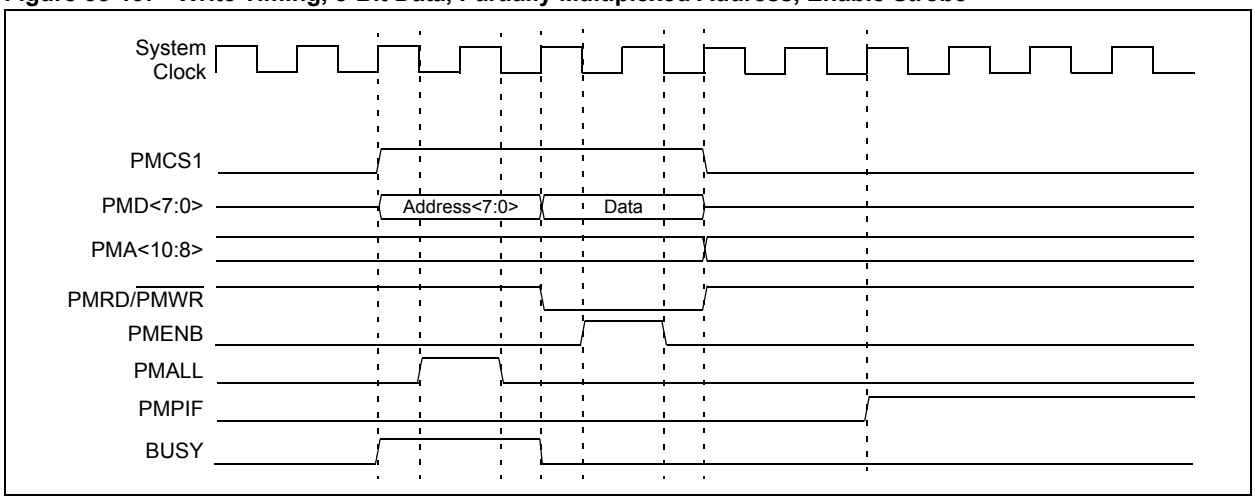


Figure 35-20: Read Timing, 8-Bit Data, Fully Multiplexed 16-Bit Address

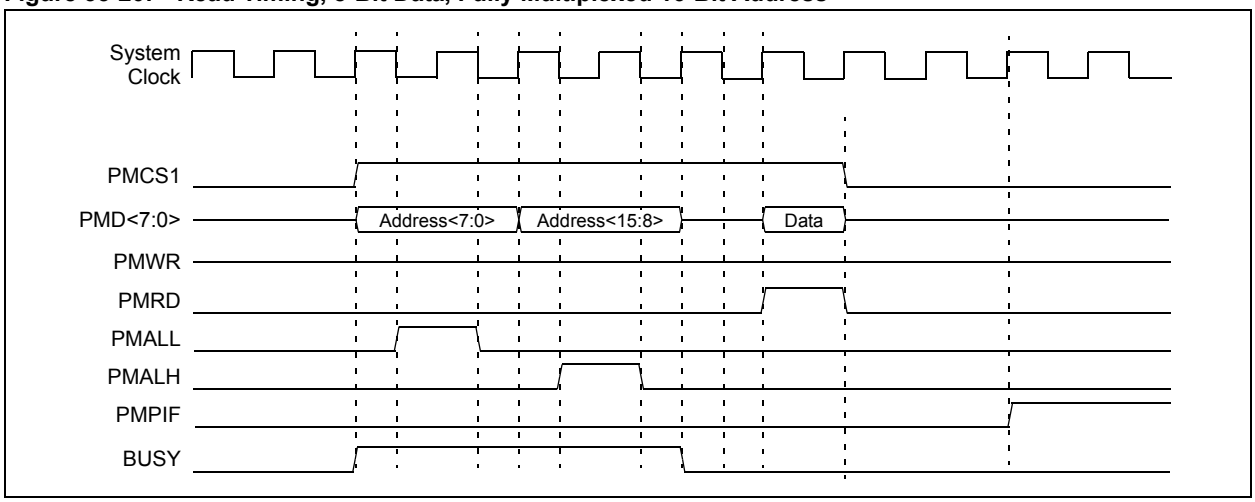


Figure 35-21: Write Timing, 8-Bit Data, Fully Multiplexed 16-Bit Address

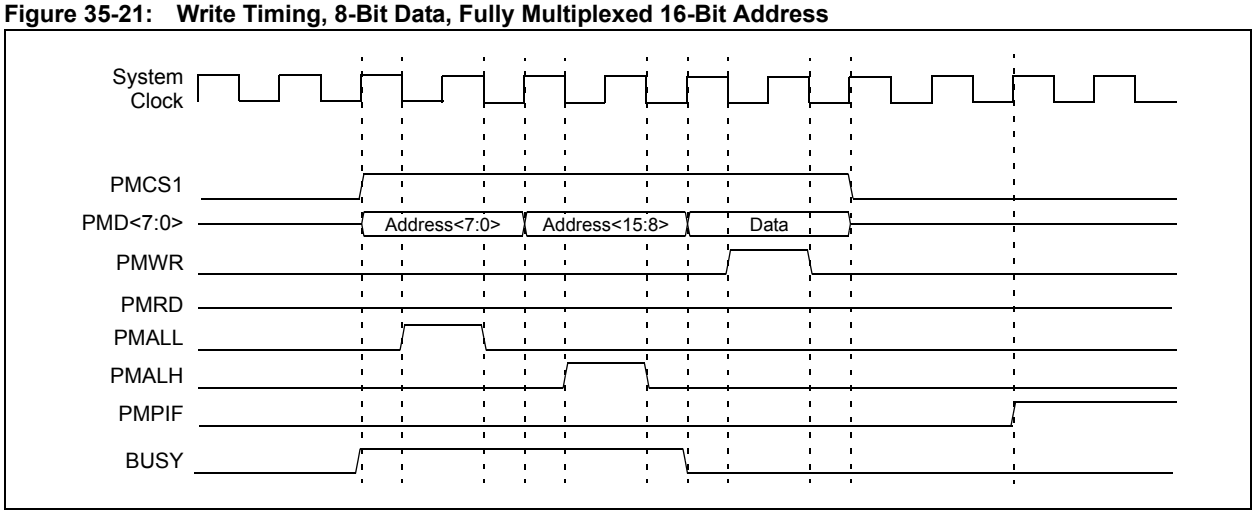


Figure 35-22: Read Timing, 16-Bit Data, Demultiplexed Address

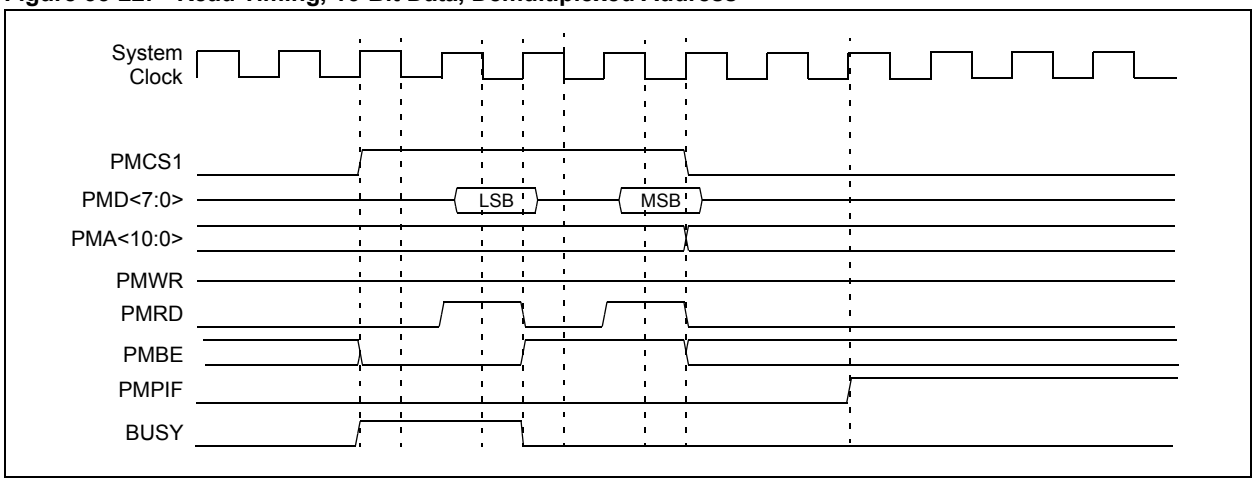


Figure 35-23: Write Timing, 16-Bit Data, Demultiplexed Address

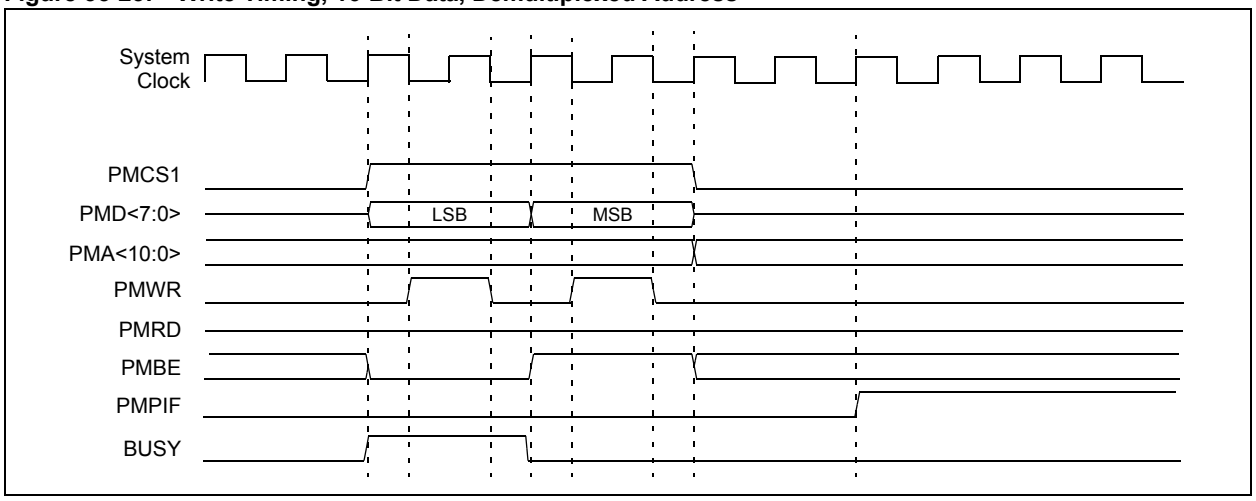


Figure 35-24: Read Timing, 16-Bit Multiplexed Data, Partially Multiplexed Address

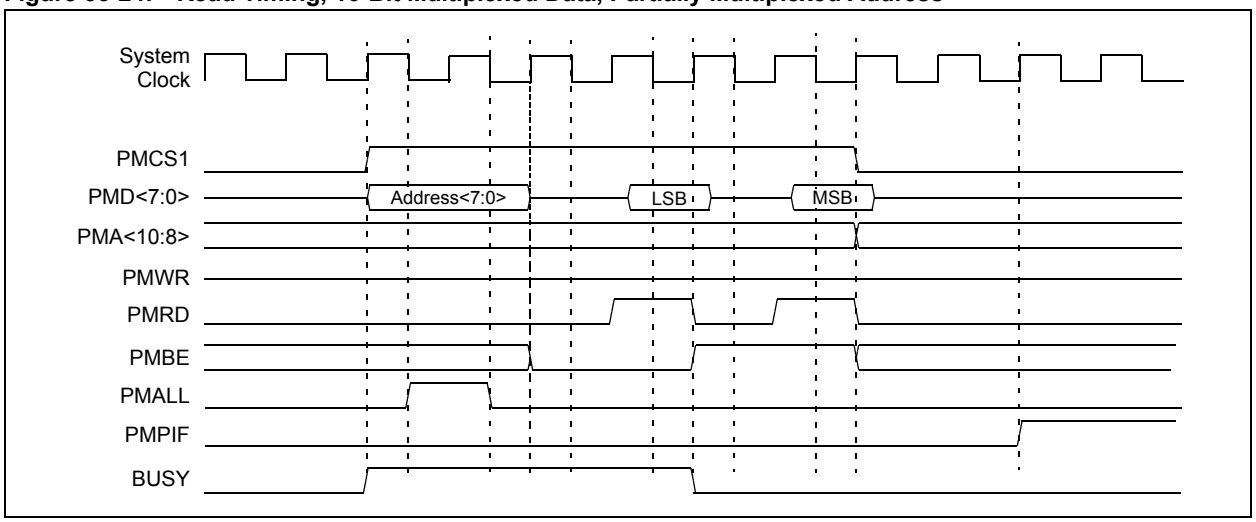


Figure 35-25: Write Timing, 16-Bit Multiplexed Data, Partially Multiplexed Address

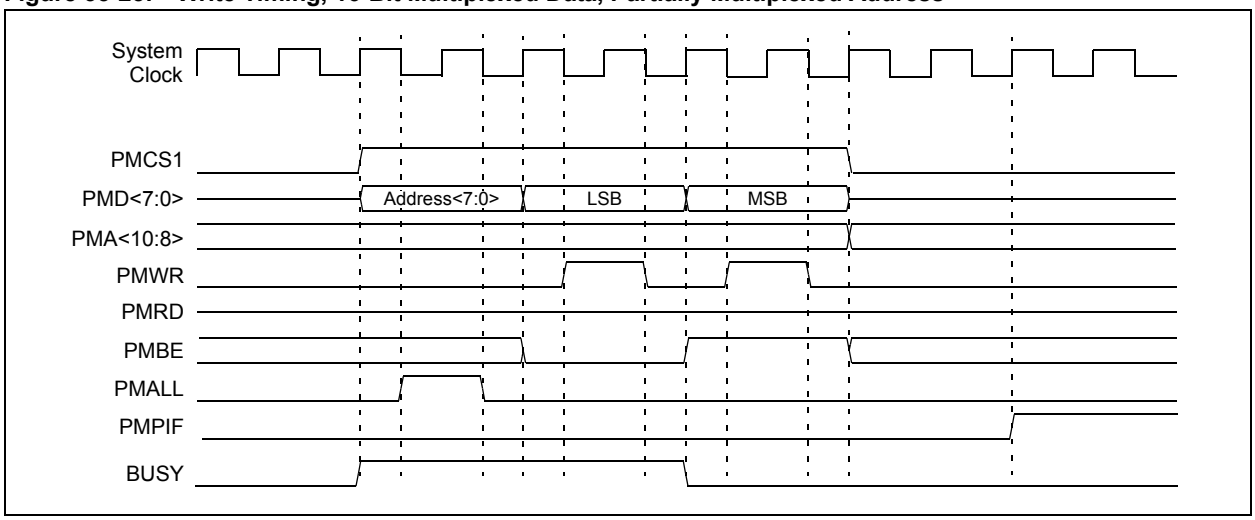


Figure 35-26: Read Timing, 16-Bit Multiplexed Data, Fully Multiplexed 16-Bit Address

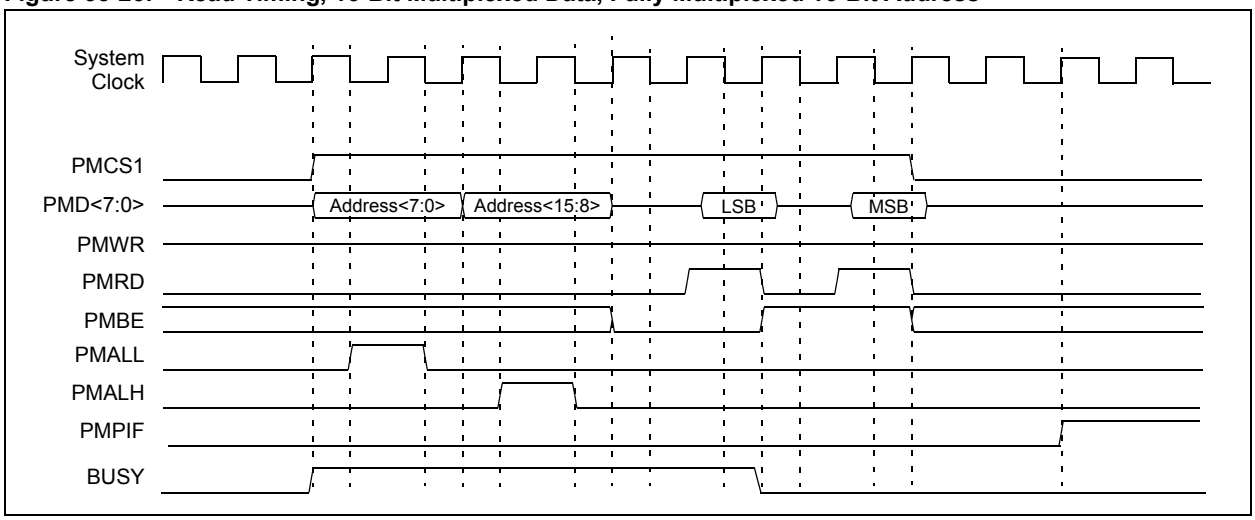
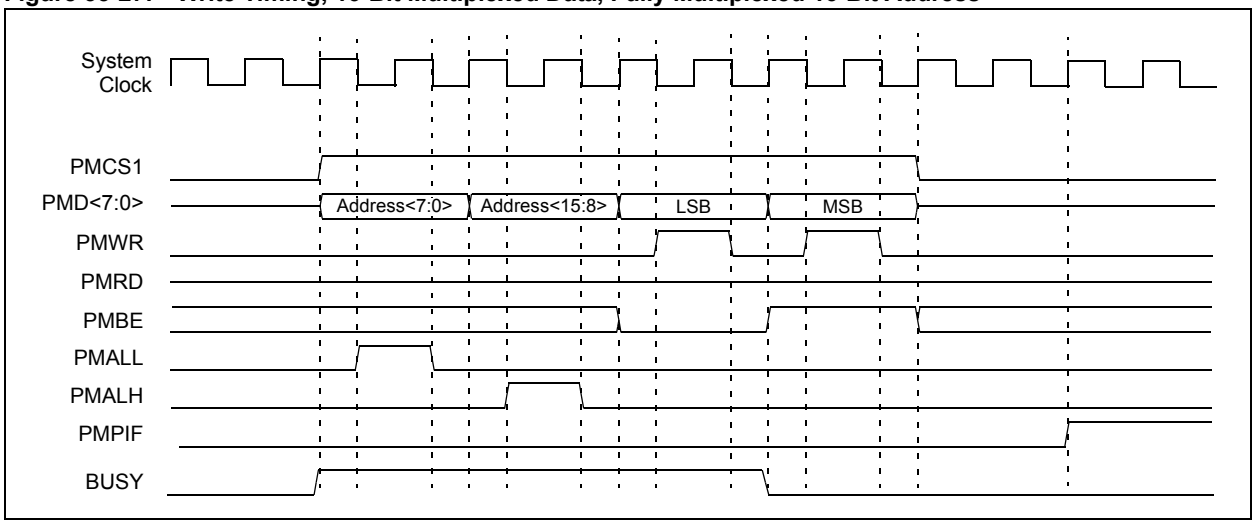


Figure 35-27: Write Timing, 16-Bit Multiplexed Data, Fully Multiplexed 16-Bit Address



35.5 DIRECT MEMORY ACCESS (DMA) SUPPORT

DMA reads from and writes to the PMDIN1 register (DMAxPAD = 0x0608) when the PMP module is configured for a master mode. To use DMA, perform these actions:

- DMAxREQ bits (IRQSEL<6:0>) must be set to 'b0101101'
- PMP module must be configured as a Master (MODE<1:0> = 11 or 10)
- PMP interrupts must be generated on every byte (IRQM<1:0> = 01)

Note: In Slave mode, PMP cannot operate with DMA.

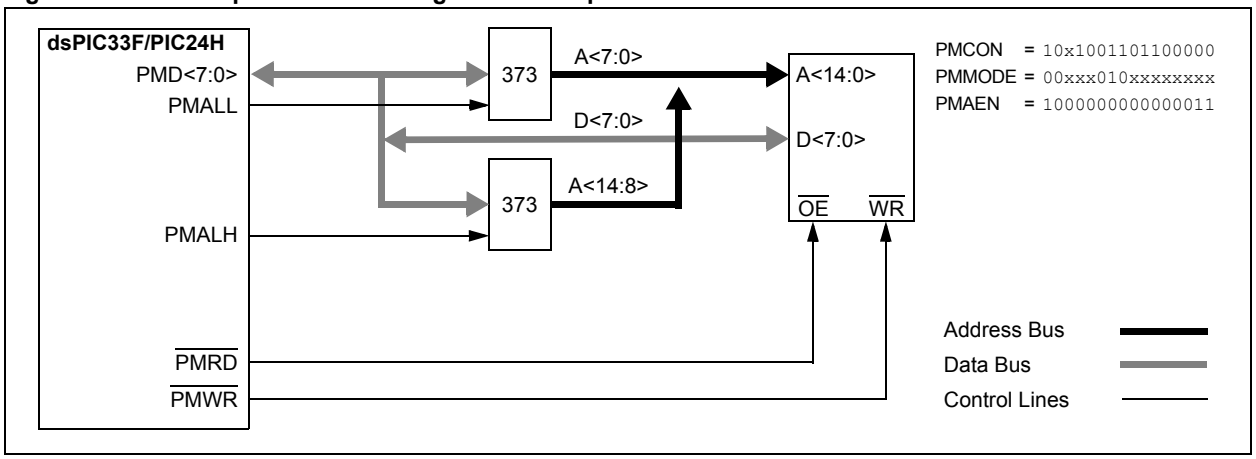
35.6 APPLICATION EXAMPLES

This section introduces some potential applications for the PMP module.

35.6.1 Multiplexed Memory or Peripheral

Figure 35-28 illustrates the hookup of a memory or another addressable peripheral in Full Multiplex mode. Therefore, this mode achieves the best pin savings from the device perspective. However, for this configuration, some external latches are required to maintain the address.

Figure 35-28: Multiplexed Addressing Mode Example



35.6.2 Partially Multiplexed Memory or Peripheral

Partial multiplexing implies using more pins; however, for a few extra pins, some additional performance can be achieved. Figure 35-29 illustrates an example of a memory or peripheral that is partially multiplexed with an external latch. If the peripheral has internal latches, no extra circuitry is required except for the peripheral itself, as illustrated in Figure 35-30.

Figure 35-29: Partially Multiplexed Addressing Mode Example

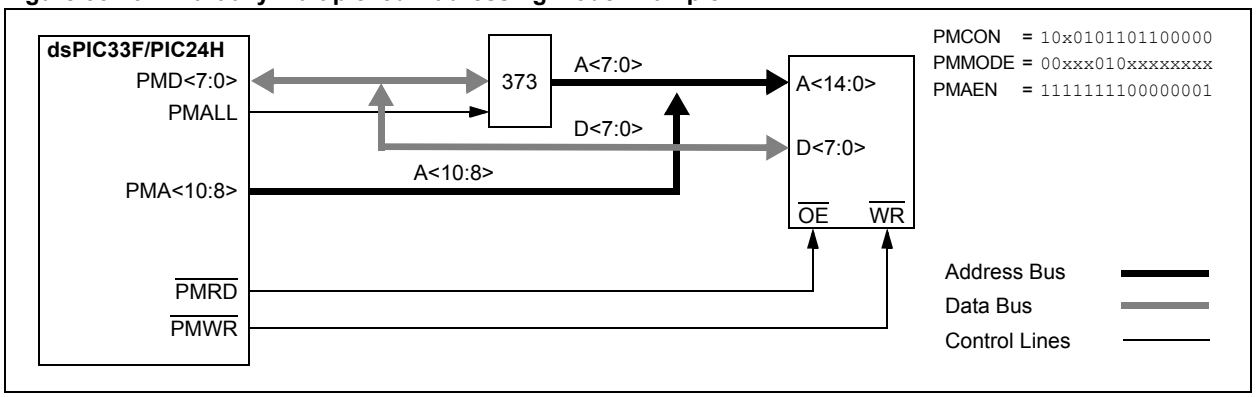
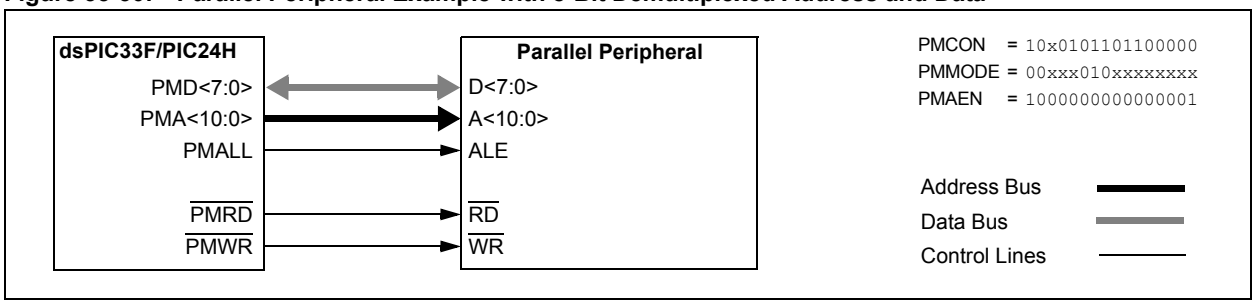


Figure 35-30: Parallel Peripheral Example with 8-Bit Demultiplexed Address and Data



35.6.3 Parallel Flash/EEPROM Examples

Figure 35-31 illustrates an example of connecting parallel Flash/EEPROM to the PMP. Figure 35-32 illustrates a slight variation to this, configuring the connection for 16-bit data from a single byte addressable Flash/EEPROM. Figure 35-33 also demonstrates the interface with a 16-bit device but without using byte select logic.

Figure 35-31: Parallel Flash/EEPROM Example (Up to 11-Bit Address), 8-Bit Data

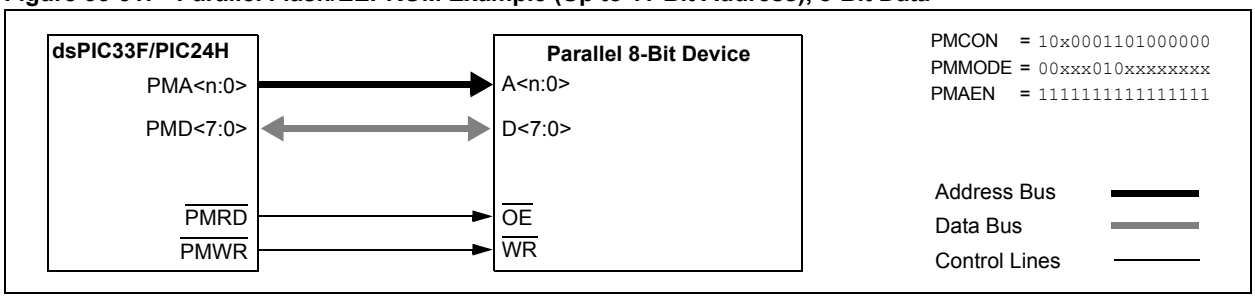


Figure 35-32: Parallel Flash/EEPROM Example (Up to 11-Bit Address), 16-Bit Data (Byte Select Mode)

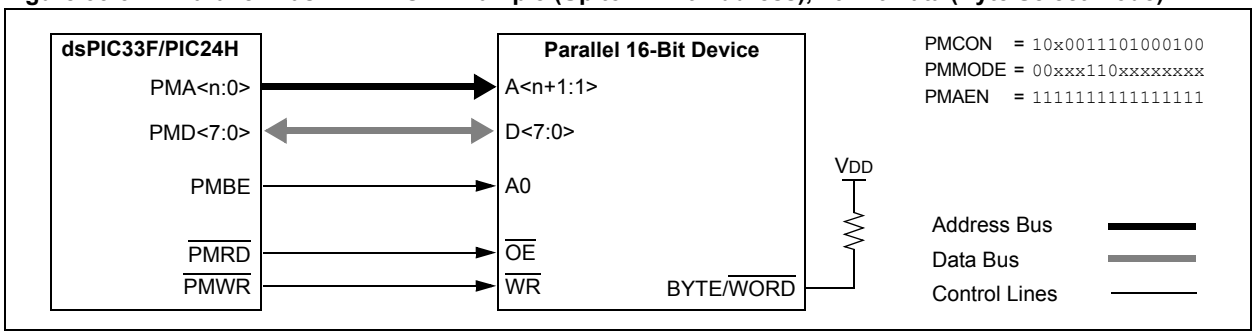
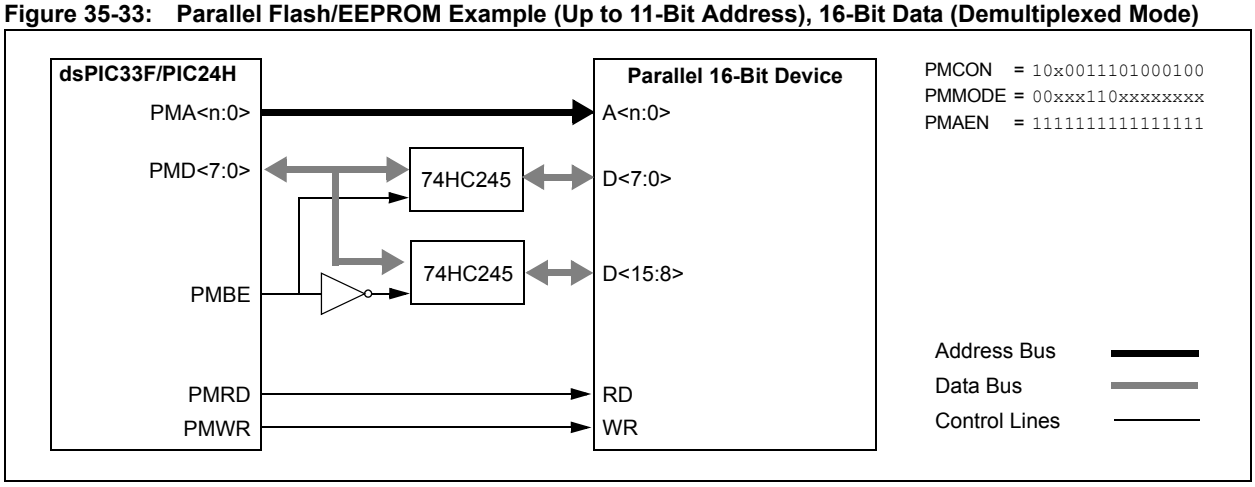


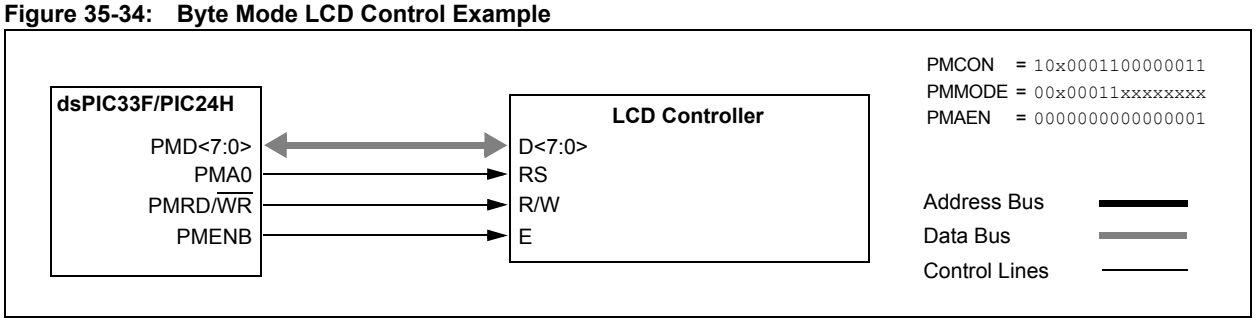
Figure 35-33: Parallel Flash/EEPROM Example (Up to 11-Bit Address), 16-Bit Data (Demultiplexed Mode)



35.6.4 LCD Controller Example

The PMP module can be configured to connect to a typical LCD controller interface, as illustrated in Figure 35-34. In this case, the PMP module is configured for active-high control signals because common LCD displays require active-high control.

Figure 35-34: Byte Mode LCD Control Example



35.7 OPERATION IN POWER-SAVING MODES

The dsPIC33F/PIC24H family of devices has three power modes: the normal operational (Full-Power) mode, and the two power-saving modes (Sleep and Idle), invoked by the PWRSAV instruction. Depending on the mode selected, entering a power-saving mode may also affect the operation of the module.

35.7.1 Sleep Mode

When the device enters Sleep mode, the system clock is disabled. The consequences of Sleep mode depend on which mode the module is configured when Sleep mode is invoked.

35.7.1.1 MASTER MODE OPERATION

If the device enters Sleep mode while the module is operating in a master mode, PMP operation will be suspended in its current state until clock execution resumes. As this might cause unexpected control pin timings, avoid invoking Sleep mode when continuous use of the module is needed.

35.7.1.2 SLAVE MODE OPERATION

While the module is inactive, but enabled for any Slave mode operation, any read or write operations occurring at that time will be able to complete without the use of the device clock. After the operation is completed, the module will issue an interrupt according to the setting of the IRQM bits. This interrupt can wake-up the device from Sleep mode.

35.7.2 Idle Mode

When the device enters Idle mode, the system clock sources remain functional. The PSIDL bit (PMCON<13>) selects whether the module will stop or continue functioning on Idle mode.

- If PSIDL = 1, the module behaves same like in Sleep mode, which means slave reception is still possible even though the module clocks are not available and master modes are suspended.
- If PSIDL = 0 (default), the module will continue operation in Idle mode. The current transaction in master modes and in Slave mode will complete and issue an interrupt.

35.8 REGISTER MAPS

A summary of the registers associated with the PMP module is provided in Table 35-2.

Table 35-2: Parallel Master/Slave Port Register Map(1)

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	CSF1	CSF0	ALP	—	CS1P	BEP	WRSP	RDSP	0000
PMMODE	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000
PMADDR(2)	—	CS1	—	—	—	Parallel Port Address (ADDR<10:0>)											0000
PMAEN	—	PTEN	—	—	—	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMSTAT	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008Fh
PMDIN1	Parallel Port Data In Register 1 (Buffers Level 0 and 1)																0000
PMDIN2	Parallel Port Data In Register 2 (Buffers Level 2 and 3)																0000
PMDOUT1(2)	Parallel Port Data Out Register 1 (Buffers Level 0 and 1)																0000
PMDOUT2	Parallel Port Data Out Register 2 (Buffers Level 2 and 3)																0000
PADCFG1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSECSEL	PMPTTL	0000

Legend: — = unimplemented, read as '0'.

Note 1: Refer to the specific device data sheet for Core register map details.

2: PMADDR and PMDOUT1 are the same physical register, but are defined differently depending on the module's operating mode.

35.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Parallel Master Port (PMP) module are:

Title	Application Note #

Related application notes are not available.

Note: Please visit the Microchip Web site (www.microchip.com) for additional application notes and code examples for the dsPIC33F/PIC24H family of devices.

35.10 REVISION HISTORY

Revision A (October 2007)

This is the initial release of this document.

Revision B (March 2008)

Updated **35.5 "Direct Memory Access (DMA) Support"** to reflect corrected DMAxPAD address of 0x0608 for DMA configuration.

Revision C (September 2010)

This revision includes the following updates:

- Renamed the Family Reference Manual name from dsPIC33F to dsPIC33F/PIC24H.
- All references to dsPIC33F in the document are updated to dsPIC33F/PIC24H.
- Figures:
  - Added PMA<10:0> bits in Figure 35-1
  - Updated PMA<13:0> as PMA<10:0> bits in Figure 35-9
  - Updated PMA<13:8> as PMA<10:8> bits in Figure 35-10
  - Updated PMA<15:0> as PMA<10:0> bits in Figure 35-11and Figure 35-12
  - Updated Figure 35-15 and Figure 35-17
- Notes:
  - Added Note 2 in Register 35-2:

    WAITM<3:0> and WAITE<1:0> bits are ignored when WAITB<1:0> bits determine the duration of the address latch signal
  - Added a shaded note in **35.5 "Direct Memory Access (DMA) Support"**
- Registers:
  - Updated bits 11, 12, 13 and 15 as **Unimplemented** bits in Register 35-3
  - Updated ADDR<13:8> bits as ADDR<10:0> in Register 35-3
- Additional minor corrections such as language and formatting updates are incorporated throughout the document

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ISBN: 978-1-60932-497-1

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