Section 25. Device Configuration

HIGHLIGHTS

This section of the manual contains the following topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.

Please consult the note at the beginning of the **"Special Features"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

25.1 INTRODUCTION

At their highest level of functionality, dsPIC33F/PIC24H devices integrate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

- Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options and changing them if needed during run time.
- Device Identification – Allowing electronic confirmation of a device part number and revision level in the target application.

25.2 DEVICE CONFIGURATION

The basic behavior and operation of dsPIC33F/PIC24H devices are set by the device Configuration bits. These bits allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In all dsPIC33F/PIC24H family devices, device Configuration bits are mapped to the device's program memory space, starting at location 0xF80000.

The method by which the Configuration bits are programmed differs between major device families. The details are discussed in **25.2.1 "Volatile Memory Implementation"** and **25.2.2 "Nonvolatile Memory Implementation"**. See the specific device data sheet for information on which method is implemented for your particular device.

Table 25-1 provides a list of the most common Configuration bit options. Note that this is not a comprehensive list; certain device families will have unique configuration options that are specific to its peripheral set. Each Configuration bit and its operation is described in the relevant section of the *"dsPIC33F/PIC24H Family Reference Manual*". For more information on Configuration bit mapping of a particular device, refer to the specific device data sheet.

Note: All of the bits that are described in Table 25-1 are not present on all the devices. Refer to the specific device data sheet for availability.

Table 25-1: Common dsPIC33F/PIC24H Device Configuration Bits

Configuration Bit	Function
BSS	Enables boot segment and sets security level (3 bits, up to 8 configuration options).
BWRP	Enables boot segment write protection
FNOSC	Selects the initial (default) device oscillator (3 bits, up to 8 configuration options).
FWDTEN	Enables the Watchdog Timer.
GWRP	Enables write/erase protection for program memory.
IESO	Enables Two-Speed Start-up.
IOL1WAY	Selects one-time or unrestricted run-time changes to peripheral mapping.
JTAGEN	Enables dedicated JTAG port and disables corresponding I/O ports on designated pins.
OSCIOFCN	Selects function of OSC2 pin (I/O port or CLKO) in certain external oscillator modes.
POSCMD	Selects primary (external) oscillator configuration (2 bits, 4 configurations).
WINDIS	Selects Windowed Operation mode for the Watchdog Timer.

25.2.1 Volatile Memory Implementation

In Volatile Memory Implementation for dsPIC33F/PIC24H devices, the Configuration bits are implemented as volatile memory; that is, the configuration data must be loaded each time the device is powered up. The actual configuration data is stored in the last several words at the end of the on-chip program memory space, known as the Configuration Words (abbreviated as CW). During all types of device Resets, the configuration data is automatically loaded from the Configuration Words to the proper Configuration registers.

The CWs are 16-bit, packed representations of the actual device Configuration bits; the actual locations of which are distributed among several locations in configuration space. The number of CWs implemented for a particular device family depends on the device's feature set and configuration options. Refer to the specific device data sheet for part-specific implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once. After a bit is initially written during a power cycle or any Reset, it cannot be written to again. Any change of a Configuration bit (not a change to a Flash Configuration Word) causes a Configuration Mismatch (CM) Reset, which then forces a reload of the original values.

25.2.1.1 CONSIDERATIONS WHEN USING FLASH CONFIGURATION WORDS

The upper byte of all the Flash Configuration Words in the program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since the Configuration bits are not implemented in the corresponding locations, writing '1' to these locations has no effect on device operation.

As mentioned previously, changes to the actual device Configuration bits during run time would cause a Configuration Mismatch Reset. This does not prevent changes to Flash Configuration Words during normal operation. This also makes it possible for an application to change its hardware configuration by writing new data to these Flash Configuration Words, and then executing a RESET command, which results in reloading the new values.

25.2.2 Nonvolatile Memory Implementation

With nonvolatile memory implementation, the Configuration bits are implemented as a physically separate block of nonvolatile memory. Once programmed, configuration data is maintained indefinitely. Although they act like fuses, the Configuration bits are freely reprogrammable. Since they lie inside the configuration memory space, the Configuration bits are not directly accessible; they can only be written and read using table read and table write instructions.

Unlike volatile memory implementation devices, the Configuration bits with nonvolatile memory implementation devices are organized into 8-bit registers, always the Least Significant Byte (LSB) of a program memory address. These Configuration registers are symbolically named according to their primary function (i.e., General Segment protection, Oscillator Selection, and so on). Table 25-2 lists the typical names and address of Configuration registers. Note that not all Configuration registers are implemented on all devices and certain devices with extended feature sets may have additional registers. In addition, there may be variations in naming or location of registers in certain devices. Refer to the specific device data sheet for specific information.

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’), to select various configuration options.

The implementation of the Configuration bits in devices using nonvolatile memory implementation makes a Configuration Mismatch (CM) error and Reset during full-speed operation virtually impossible. However, a severe device disturbance (such as an ESD event) during Sleep may disrupt the configuration safety check, resulting in a CM Reset.

Table 25-2: Typical Configuration Registers

Register Name	Primary Function	Address
FBS	Boot Segment Protect	0xF80000
FGS	General Segment Protect	0xF80004
FOSCEL	Oscillator Select	0xF80006
FOSC	Oscillator Configure	0xF80008
FWDT	Watchdog Timer Configure	0xF8000A
FPOR	Reset Configure	0xF8000C
FICD	Debug Configure	0xF8000E

25.3 DEVICE IDENTIFICATION

dsPIC33F/PIC24H devices have two read-only registers that provide device-specific identification information. These are located near the end of the program memory space, starting at 0xFF0000. Like the Flash Configuration Words, the Device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using table read instructions.

The DEVID register at 0xFF0000 (Register 25-1) identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register at 0xFF0002 (Register 25-2) identifies the particular silicon revision for that device in terms of major and minor revision levels (“letter and dot revision” format).

For any given family of dsPIC33F/PIC24H devices, the corresponding Family Silicon Errata and Data Sheet Clarification document provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a silicon revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in the associated Family Silicon Errata and Data Sheet Clarification document.

Register 25-1: DEVID: Device ID Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DEVID<15:0>:** Device ID Value bits

Register 25-2: DEVREV: Device Revision Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV<15:8>							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DEVREV<15:0>:** Device Revision Value bits

25.4 UNIT IDENTIFICATION

Some devices may feature programmable Unit ID registers (FUIDx), which can be programmed by the user with unique device information. Refer to the specific device data sheet for FUIDx availability and memory locations.

25.5 IN-CIRCUIT PROGRAMMING AND DEBUGGING

25.5.1 In-Circuit Serial Programming™ (ICSP™)

The ICSP™ capability is Microchip's proprietary process for microcontroller programming in the target application. The ICSP interface uses two pins as its core. The programming data pin (PGEDx) functions as both an input and an output, allowing programming data to be read in and device information to be read out on command. The programming clock pin (PGECx) clocks in data and controls the overall process.

Serial programming allows customers to manufacture boards with unprogrammed devices and then to program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. For more details on ICSP, refer to the "*dsPIC33F/PIC24H Flash Programming Specification"* (DS70152).

Any of the following three pairs of programming clock/data pins can be used:

- PGEC1/PGED1
- PGEC2/PGED2
- PGEC3/PGED3

During programming, each pin pair is recognized as a valid programming connection. Therefore, no special selection is to be performed by the user to specify which pin pair will be used for programming.

25.5.2 In-Circuit Debugger

When the MPLAB® ICD 3 or MPLAB REAL ICE™ in-circuit emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging when used with MPLAB IDE. The debugging functionality is controlled through the PGECx (emulation/debug clock) and PGEDx (emulation/debug data) pin functions.

Any of the following three pairs of debugging clock/data pins can be used:

- PGEC1/PGED1
- PGEC2/PGED2
- PGEC3/PGED3

The debugging clock and data pins must be selected by programming the ICD Communication Channel Select Enable bits (ICS<1:0>) in the In-Circuit Debugger Configuration register (FICD<1:0>). To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS}, and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

25.6 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Device Configuration include the following:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F/PIC24H family of devices.

25.7 REVISION HISTORY

Revision A (February 2007)

This is the initial release of this section.

Revision B (February 2007)

Minor edits throughout document.

Revision C (January 2008)

This revision includes the following corrections and updates:

- Sections:
  - Added **25.3.6 “JTAG Interface”**
  - Added **25.3.7 “In-Circuit Serial Programming™ (ICSP™)”**
  - Added **25.4.2 “In-Circuit Debugger”**
- Registers:
  - Updated FOSCSEL: Oscillator Source Selection register (see Register 25-4)
  - Updated FPOR: POR Configuration register (see Register 25-7)
  - Added FICD: In-Circuit Debugger Configuration register (see Register 25-8)
- Tables:
  - Updated register map table (see Table 25-1)

Revision D (January 2009)

This revision includes the following corrections and updates:

- Registers:
  - Added the PLLKEN bit to the Watchdog Timer Configuration (FWDT) register (see Register 25-6).
  - Removed the BKBUG and COE bits from the In-Circuit Debugger Configuration (FICD) register (see Register 25-8).
- Updated **25.3.2 “Oscillator Configuration Bits”** to include a reference to the PLLKEN bit
- Additional minor corrections such as language and formatting updates have been incorporated throughout the document.

Revision E (August 2009)

This revision includes the following corrections and updates:

- Note:
  - Added a note in Register 25-7.
- Registers:
  - Updated unimplemented bits to read as ‘0’ in all the registers:
    U = Unimplemented bit, read as '1' is updated as U = Unimplemented bit, read as '0'.
  - Added new bit name and bit descriptions for bit 5 and bit 6 in Register 25-7.
  - Updated the bit name as “r” for bit 6 and bit 7 in Register 25-8.
  - Updated the Legend “r = Reserved” in Register 25-8.
  - Added the **FCMP: Comparator Configuration Register** (see Register 25-9).
- Sections:
  - Updated the **25.3.7 “In-Circuit Serial Programming™ (ICSP™)”** section for selection of programming pins.
  - Changed all instances of PGCx/EMUCx and PGDx/EMUDx (where x = 1, 2, or 3) to PGECx and PGEDx
  - Removed the Register Map section (Section 25.5).
- Additional minor corrections such as language and format updates have been incorporated throughout the document.

Revision F (June 2010)

This revision includes the following changes:

- Updated the entire document for the purpose of maintaining consistency with other Microchip family reference manual sections.
- Changed the document name from dsPIC33F Family Reference Manual to dsPIC33F/PIC24H Family Reference Manual.
- All references to dsPIC33F in the document are updated to dsPIC33F/PIC24H.
- Notes:
  - Added a shaded note at the beginning of the section, which provides information on complimentary documentation.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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