Section 14. Motor Control PWM

HIGHLIGHTS

This section of the manual contains the following topics:

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Motor Control PWM

14.1 INTRODUCTION

This chapter describes the Motor Control Pulse Width Modulator (MCPWM) peripheral in the dsPIC33F family of devices.

14.1.1 Purpose of the MCPWM Peripheral

The MCPWM is used to generate a periodic pulse waveform, which is useful in motor control and power control applications. The MCPWM peripheral acts as a timer to count up to a period count value. The time period and the duty cycle of the pulses are both programmable.

Depending on the device variant, there are up to two MCPWM modules, MCPWM1 and MCPWM2, in the dsPIC33F family of devices. The features of these two modules are listed in sections **14.2 "Features of the MCPWM1 Module"** and **14.3 "Features of the MCPWM2 Module"**.

14.2   FEATURES OF THE MCPWM1 MODULE

The MCPWM1 module is used to generate multiple synchronized pulse width modulated outputs. The following motor and power control applications are supported by the MCPWM1 module:

• Three-Phase AC Induction Motor (ACIM)
• Switched Reluctance Motor
• Brushless DC (BLDC) Motor
• Uninterruptible Power Supply (UPS)

The distinctive features of the MCPWM1 module are summarized below:

• Up to eight PWM outputs with four duty cycle generators
• Dedicated time base that supports $T_{CY}/2$ PWM edge resolution
• On-the-fly PWM frequency changes
• Hardware dead time generators
• Output pin polarity programmed by device configuration bits
• Multiple operating and output modes:
    - Single event mode
    - Edge-aligned mode
    - Center-aligned mode
    - Center-aligned mode with double updates
    - Complementary output mode
    - Independent output mode
• Manual override register for PWM output pins
• Duty cycle updates that can be configured to be immediate or synchronized to the PWM
• Up to 2 hardware fault input pins with programmable function
• Special Event Trigger for synchronizing analog-to-digital conversions
• Output pins associated with the PWM can be individually enabled

> **Note:** Depending on the dsPIC33F device variant, there are different versions of the MCPWM1 module. Refer to the specific device data sheet for further details.

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14.3   FEATURES OF THE MCPWM2 MODULE

The MCPWM2 module provides an additional pair of complementary PWM outputs, which are useful in the following:

- Independent Power Factor Correction (PFC) in a motor system
- Induction cooking systems
- DC motor control systems
- Single-phase inverter control
- Single-phase ACIM control

The distinctive features of the MCPWM2 module are summarized below:

- Two PWM outputs with one duty cycle generator
- Dedicated time base that supports $T_{CY}/2$ PWM edge resolution
- On-the-fly PWM frequency changes
- A hardware dead time generator
- Output pin polarity programmed by device configuration bits
- Multiple output and operating modes:
  - Single Event mode
  - Edge-Aligned mode
  - Center-Aligned mode
  - Center-Aligned mode with double updates
  - Complementary Operating mode
- Manual override register for PWM output pins
- Duty cycle updates that can be configured to be immediate or synchronized to the PWM
- A hardware fault input pin with programmable function
- Special Event Trigger for synchronizing analog-to-digital conversions
- Output pins associated with the PWM that can be individually enabled

> **Note:**   The MCPWM2 module is present only in specific dsPIC33F devices. Refer to the specific device data sheet for further details.

14.4   REGISTER DESCRIPTION

The following registers are used to control the operation of the MCPWM1 and MCPWM2 modules:

> **Note:**   The letter "x" in the register names refers to the MCPWM Module number.

- PxTCON: PWM Time Base Control Register

This register is used for the selection of the time base mode, time base input clock prescaler and time base output postscaler, and for enabling the time base timer.

- PxTMR: PWM Time Base Register

The time base count value and the time base count direction status are obtained in this register.

- PxTPER: PWM Time Base Period Register

The PWM time base value is written into this register, which determines the PWM operating frequency.

- PxSECMP: Special Event Compare Register

This register provides the compare value at which the analog-to-digital conversions are to be synchronized with the PWM time base. Comparison can be either during up-count or down-count in center-aligned mode depending on the setting of the SEVTDIR bit in this register.

- PWMxCON1: PWM Control Register 1

Selection of either Independent or Complementary mode for each PWM I/O pair is performed in this register.

- PWMxCON2: PWM Control Register 2

This register provides the following selections:

  - Selection of a PWM Special Event Trigger output postscaler value
  - Immediate updating of duty cycle registers
  - Selection of output override synchronization with the time base
  - Enabling updates from duty cycle and period buffer registers

- PxDTCON1: Dead Time Control Register 1

The dead time value and clock period prescaler for Dead Time Unit A and Dead Time Unit B can be selected using this register.

- PxDTCON2: Dead Time Control Register 2

Dead time insertions from Dead Time Unit A or Dead Time Unit B for each of the PWM outputs can be selected using this register.

- PxFLTACON: Fault A Control Register

This register provides the following selections:

  - PWM output pin driven on an external fault – active or inactive state
  - Fault mode – Cycle-by-Cycle mode or Latched mode
  - Pin pair to be controlled or not controlled by fault input A

- PxFLTBCON: Fault B Control Register

The following selections can be done using this register:

  - PWM output pin driven on an external fault – active or inactive state
  - Fault mode – Cycle-by-Cycle mode or Latched mode
  - Pin pair to be controlled or not controlled by fault input B

- PxOVDCON: Override Control Register

This register is used for enabling the output override feature and for PWM output pin control selection.

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- PxDC1: PWM Duty Cycle Register 1

  The 16-bit PWM Duty Cycle value for PWM output pair 1 is written into this register.

- PxDC2: PWM Duty Cycle Register 2

  The 16-bit PWM Duty Cycle value for PWM output pair 2 is written into this register.

- PxDC3: PWM Duty Cycle Register 3

  The 16-bit PWM Duty Cycle value for PWM output pair 3 is written into this register.

- PxDC4: PWM Duty Cycle Register 4

  The 16-bit PWM Duty Cycle value for PWM output pair 4 is written into this register.

- FBORPOR: BOR AND POR Device Configuration Register

  In addition to the Special Function Registers (SFRs) associated with the MCPWM module, three device configuration bits can be used to set up the initial Reset states and polarity of the PWM I/O pins. These configuration bits are located in the FBORPOR register.

14.5 SPECIAL FUNCTION REGISTERS

Register 14-1: PxTCON: PWM Time Base Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
PTEN	—	PTSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15 **PTEN:** PWM Time Base Timer Enable bit

1 = PWM time base is on
0 = PWM time base is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit

1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7-4 **PTOPS<3:0>:** PWM Time Base Output Postscale Select bits

1111 = 1:16 postscale

•
•
•

0001 = 1:2 postscale
0000 = 1:1 postscale

bit 3-2 **PTCKPS<1:0>:** PWM Time Base Input Clock Prescale Select bits

11 = PWM time base input clock period is 64 T_{CY} (1:64 prescale)
10 = PWM time base input clock period is 16 T_{CY} (1:16 prescale)
01 = PWM time base input clock period is 4 T_{CY} (1:4 prescale)
00 = PWM time base input clock period is T_{CY} (1:1 prescale)

bit 1-0 **PTMOD<1:0>:** PWM Time Base Mode Select bits

11 = PWM time base operates in a continuous Up/Down mode with interrupts for double PWM updates
10 = PWM time base operates in a continuous Up/Down Counting mode
01 = PWM time base operates in Single Event mode
00 = PWM time base operates in Free Running mode

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Register 14-2:   PxTMR: PWM Time Base Register

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTDIR	PTMR <14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTMR <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **PTDIR:** PWM Time Base Count Direction Status bit (Read Only)

   1 = PWM time base is counting down
   0 = PWM time base is counting up

bit 14-0   **PTMR <14:0>:** PWM Time Base Register Count Value bits

Register 14-3:   PxTPER: PWM Time Base Period Register

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PTPER <14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTPER <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-0   **PTPER<14:0>:** PWM Time Base Period Value bits

Register 14-4: **PxSECMP: Special Event Compare Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTDIR	SEVTCMP <14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **SEVTDIR:** Special Event Trigger Time Base Direction bit[1]

  1 = A Special Event Trigger will occur when the PWM time base is counting down
  0 = A Special Event Trigger will occur when the PWM time base is counting up

bit 14-0   **SEVTCMP <14:0>:** Special Event Compare Value bit[2]

  Note 1: SEVTDIR is compared with PTDIR (PTMR<15>) to generate the Special Event Trigger.
  2: SEVTCMP<14:0> is compared with PTMR<14:0> to generate the Special Event Trigger.

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Register 14-5:   PWMxCON1: PWM Control Register 1

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PMOD4	PMOD3	PMOD2	PMOD1
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **PMOD<4:1>:** PWM I/O Pair Mode bits
1 = PWM I/O pin pair is in the independent output mode
0 = PWM I/O pin pair is in the complementary output mode

bit 7 **PEN4H:** PWMxH4 I/O Enable bits[1,2]

1 = PWMxH4 pin is enabled for PWM output
0 = PWMxH4 pin disabled; I/O pin becomes general purpose I/O

bit 6 **PEN3H:** PWMxH3 I/O Enable bits[1,2]

1 = PWMxH3 pin is enabled for PWM output
0 = PWMxH3 pin disabled; I/O pin becomes general purpose I/O

bit 5 **PEN2H:** PWMxH2 I/O Enable bits[1,2]

1 = PWMxH2 pin is enabled for PWM output
0 = PWMxH2 pin disabled; I/O pin becomes general purpose I/O

bit 4 **PEN1H:** PWMxH1 I/O Enable bits[1,2]

1 = PWMxH1 pin is enabled for PWM output
0 = PWMxH1 pin disabled; I/O pin becomes general purpose I/O

bit 3 **PEN4L:** PWMxL4 I/O Enable bits[1,2]

1 = PWMxL4 pin is enabled for PWM output
0 = PWMxL4 pin disabled; I/O pin becomes general purpose I/O

bit 2 **PEN3L:** PWMxL3 I/O Enable bits[1,2]

1 = PWMxL3 pin is enabled for PWM output
0 = PWMxL3 pin disabled; I/O pin becomes general purpose I/O

bit 1 **PEN2L:** PWMxL2 I/O Enable bits[1,2]

1 = PWMxL2 pin is enabled for PWM output
0 = PWMxL2 pin disabled; I/O pin becomes general purpose I/O

bit 0 **PEN1L:** PWMxL1 I/O Enable bits[1,2]

1 = PWMxL1 pin is enabled for PWM output
0 = PWMxL1 pin disabled; I/O pin becomes general purpose I/O

Note 1: The reset condition of the PENxH and PENxL bits depends on the value of the PWM/PIN device configuration bit in the FBORPOR Device Configuration Register.

2: The letter "x" refers to the MCPWM module number.

Register 14-6: **PWMxCON2: PWM Control Register 2**

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SEVOPS<3:0>			
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IUE	OSYNC	UDIS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SEVOPS<3:0>:** PWM Special Event Trigger Output Postscale Select bits

1111 = 1:16 postscale

•

•

•

0001 = 1:2 postscale

0000 = 1:1 postscale

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **IUE:** Immediate Update Enable bit

1 = Updates to the active PxDCy[1,2] registers are immediate

0 = Updates to the active PxDCy[1,2] registers are synchronized to the PWM time base

bit 1 **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the PxOVDCON[1] register are synchronized to the PWM time base

0 = Output overrides via the PxOVDCON[1] register occur on the next T$_{CY}$ boundary

bit 0 **UDIS:** PWM Update Disable bit

1 = Updates from duty cycle and period buffer registers are disabled

0 = Updates from duty cycle and period buffer registers are enabled

Note 1: The letter "x" refers to the MCPWM module number.

2: The letter "y" refers to the MCPWM Duty Cycle register number.

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Register 14-7: PxDTCON1: Dead Time Control Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTBPS<1:0>		DTB<5:0>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTAPS<1:0>		DTA<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **DTBPS<1:0>:** Dead Time Unit B Prescale Select bits

    11 = Clock period for Dead Time Unit B is 8 T_{CY}
    10 = Clock period for Dead Time Unit B is 4 T_{CY}
    01 = Clock period for Dead Time Unit B is 2 T_{CY}
    00 = Clock period for Dead Time Unit B is T_{CY}

bit 13-8 **DTB<5:0>:** Unsigned 6-bit Dead Time Value bits for Dead Time Unit B

bit 7-6 **DTAPS<1:0>:** Dead Time Unit A Prescale Select bits

    11 = Clock period for Dead Time Unit A is 8 T_{CY}
    10 = Clock period for Dead Time Unit A is 4 T_{CY}
    01 = Clock period for Dead Time Unit A is 2 T_{CY}
    00 = Clock period for Dead Time Unit A is T_{CY}

bit 5-0 **DTA<5:0>:** Unsigned 6-bit Dead Time Value bits for Dead Time Unit A

Register 14-8:   PxDTCON2: Dead Time Control Register 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7   **DTS4A:** Dead Time Select bit for PWM4 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 6   **DTS4I:** Dead Time Select bit for PWM4 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 5   **DTS3A:** Dead Time Select bit for PWM3 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 4   **DTS3I:** Dead Time Select bit for PWM3 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 3   **DTS2A:** Dead Time Select bit for PWM2 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 2   **DTS2I:** Dead Time Select bit for PWM2 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 1   **DTS1A:** Dead Time Select bit for PWM1 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 0   **DTS1I:** Dead Time Select bit for PWM1 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

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Register 14-9:   PxFLTACON: Fault A Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **FAOV4H-FAOV1L:** Fault Input A PWM Override Value bits

> 1 = The PWM output pin is driven Active on an external fault input event
> 0 = The PWM output pin is driven Inactive on an external fault input event

bit 7   **FLTAM:** Fault A Mode bit

> 1 = The Fault A input pin functions in Cycle-by-Cycle mode
> 0 = The Fault A input pin latches all control pins to the programmed states in PxFLTACON<15:8>

bit 6-4   **Unimplemented:** Read as '0'

bit 3   **FAEN4:** Fault Input A Enable bit[1]

> 1 = PWMxH4/PWMxL4 pin pair is controlled by Fault Input A
> 0 = PWMxH4/PWMxL4 pin pair is not controlled by Fault Input A

bit 2   **FAEN3:** Fault Input A Enable bit[1]

> 1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input A
> 0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input A

bit 1   **FAEN2:** Fault Input A Enable bit[1]

> 1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input A
> 0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input A

bit 0   **FAEN1:** Fault Input A Enable bit[1]

> 1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input A
> 0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input A

Note 1:   The letter "x" refers to the MCPWM module number.

Register 14-10: PxFLTBCON: Fault B Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTBM	—	—	—	FBEN4	FBEN3	FBEN2	FBEN1
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-8 **FBOV4H:FBOV1L:** Fault Input B PWM Override Value bits

1 = The PWM output pin is driven Active on an external fault input event
0 = The PWM output pin is driven Inactive on an external fault input event

bit 7 **FLTBM:** Fault B Mode bit

1 = The Fault B input pin functions in Cycle-by-Cycle mode
0 = The Fault B input pin latches all control pins to the programmed states in PxFLTBCON<15:8>

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **FBEN4:** Fault Input B Enable bit[1,2]

1 = PWMxH4/PWMxL4 pin pair is controlled by Fault Input B
0 = PWMxH4/PWMxL4 pin pair is not controlled by Fault Input B

bit 2 **FBEN3:** Fault Input B Enable bit[1,2]

1 = PWMxH3/PWMxL3 pin pair is controlled by Fault Input B
0 = PWMxH3/PWMxL3 pin pair is not controlled by Fault Input B

bit 1 **FBEN2:** Fault Input B Enable bit[1,2]

1 = PWMxH2/PWMxL2 pin pair is controlled by Fault Input B
0 = PWMxH2/PWMxL2 pin pair is not controlled by Fault Input B

bit 0 **FBEN1:** Fault Input B Enable bit[1,2]

1 = PWMxH1/PWMxL1 pin pair is controlled by Fault Input B
0 = PWMxH1/PWMxL1 pin pair is not controlled by Fault Input B

Note 1: Fault pin A has priority over Fault pin B, if enabled.

2: The letter "x" refers to the MCPWM module number.

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Register 14-11: PxOVDCON: Override Control Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **POVD4H-POVD1L:** PWM Output Override bits[1,2]

    1 = Output on PWMxHy/PWMxLy I/O pin is controlled by the PWM generator
    0 = Output on PWMxHy/PWMxLy I/O pin is controlled by the value in the corresponding POUTxx bit

bit 7-0 **POUT4H-POUT1L:** PWM Manual Output bits[1,2]

    1 = PWMxHy/PWMxLy I/O pin is driven Active when the corresponding POVDxx bit is cleared
    0 = PWMxHy/PWMxLy I/O pin is driven Inactive when the corresponding POVDxx bit is cleared

    Note 1: The letter "x" refers to the MCPWM module number.
         2: The letter "y" refers to the MCPWM I/O pin number.

Register 14-12: PxDC1: PWM Duty Cycle Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #1 bits 15-8							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #1 bits 7-0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PxDC1<15:0>:** PWM Duty Cycle #1 Value bits

Register 14-13:   PxDC2: PWM Duty Cycle Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #2 bits 15-8							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #2 bits 7-0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PxDC2<15:0>:** PWM Duty Cycle #2 Value bits

Register 14-14:   PxDC3: PWM Duty Cycle Register 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #3 bits 15-8							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #3 bits 7-0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PxDC3<15:0>:** PWM Duty Cycle #3 Value bits

Register 14-15:   PxDC4: PWM Duty Cycle Register 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #4 bits 15-8							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #4 bits 7-0							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PxDC4<15:0>:** PWM Duty Cycle #4 Value bits

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Register 14-16: FBORPOR: BOR AND POR Device Configuration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	PWMPIN	HPOL	LPOL
bit 15							bit 8

R/P	U-0	R/P	R/P	U-0	U-0	R/P	R/P
BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
P = Programmable configuration bit		

bit 23-11 **Unimplemented**

bit 10 **PWMPIN:** MCPWM Drivers Initialization bit

1 = Pin state at reset is controlled by the I/O Port (PWMCON1<7:0> = 0x00)
0 = Pin state at reset is controlled by the module (PWMCON1<7:0> = 0xFF)

bit 9 **HPOL:** MCPWM High Side Drivers (PWMxH) Polarity bit

1 = Output signal on PWMxH pins has active high polarity
0 = Output signal on PWMxH pins has active low polarity

bit 8 **LPOL:** MCPWM Low Side Drivers (PWMxL) Polarity bit

1 = Output signal on PWMxL pins has active high polarity
0 = Output signal on PWMxL pins has active low polarity

bit 7 **BOREN:** PBOR Enable bit[1]

bit 6 **Unimplemented**

bit 5-4 **BORV:** Brown-out Voltage Select bits[1]

bit 3-2 **Unimplemented**

bit 1-0 **FPWRT:** Power-on Reset Timer Value Selection bits[1]

Note 1: This bit is not used by the MCPWM module. Refer to **Section 25. "Device Configuration"** for information about these configuration bits in this register.

14.6   MCPWM MODULE ARCHITECTURE OVERVIEW

Figure 14-1 provides a block diagram of the MCPWM module for the dsPIC33F devices.

Figure 14-1:   Block Diagram of the MCPWM Module

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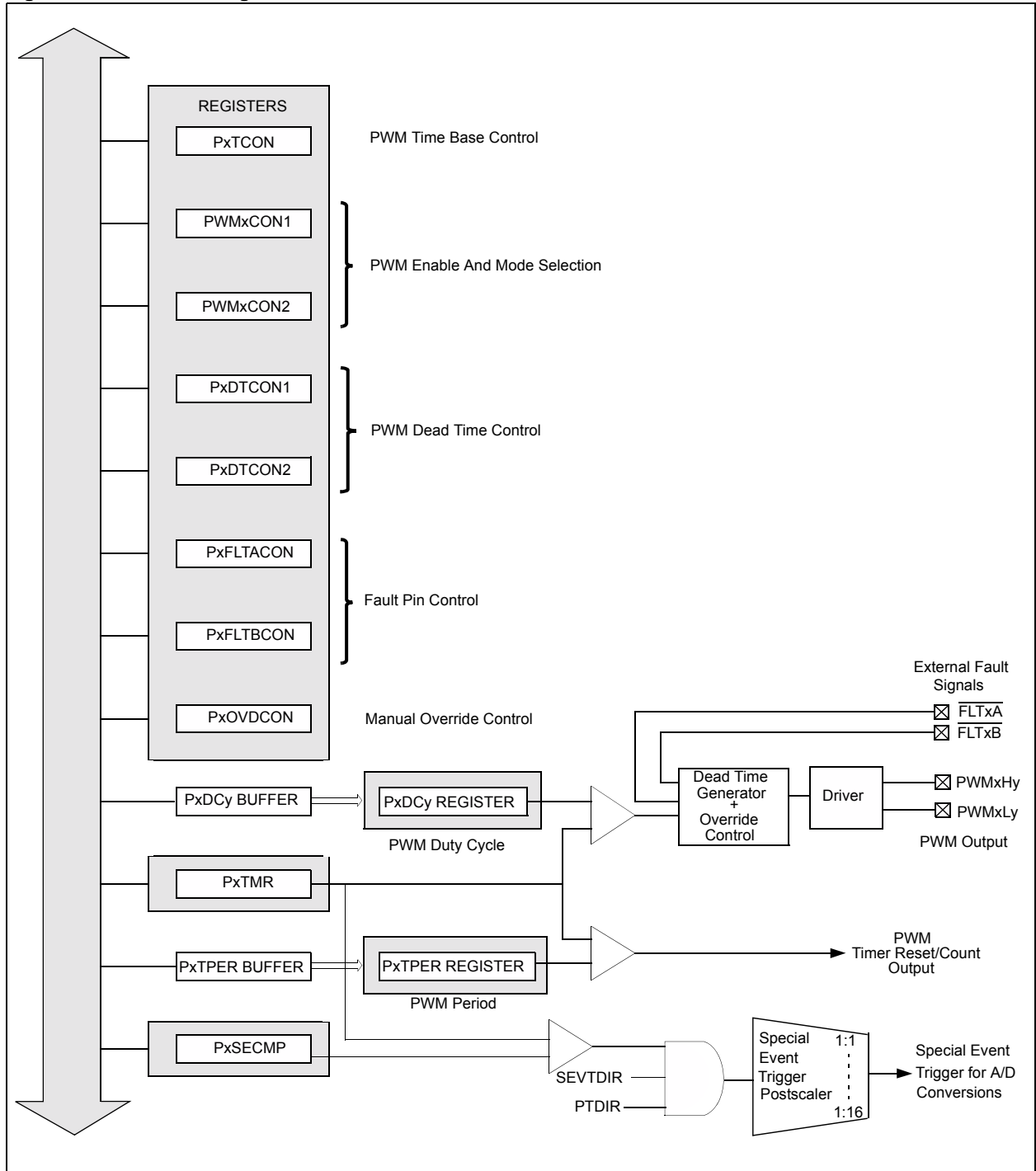
14.6.1 Duty Cycle

The MCPWM module has up to four PWM generators. There are four special function PWM Duty Cycle (PxDCy) registers associated with the module to specify the duty cycle values for the PWM generators. The duty cycle gives the time for which the PWM pulses are active in a given PWM time period.

14.6.2 Dead Time Generation

Dead time generation is automatically enabled when any of the PWM I/O pin pairs are operating in the complementary output mode. Because the power devices cannot switch instantaneously, some amount of time must be provided between the turn-off event of one PWM output in a complementary pair and the turn-on event of the other transistor.

There are two programmable dead time values. To increase user application flexibility, these dead times can be used in either of the two methods described below:

- The PWM output signals can be optimized for different turn-off times in the high-side and low-side transistors. The first dead time is inserted between the turn-off event of the lower transistor of the complementary pair and the turn-on event of the upper transistor. The second dead time is inserted between the turn-off event of the upper transistor and the turn-on event of the lower transistor.
- The two dead times can be assigned to individual PWM I/O pairs. This operating mode allows the PWM module to drive different transistor/load combinations with each complementary PWM I/O pair.

There are up to two dead time generation units (A and B) that can be configured in the Dead Time Control (PxDTCON1 and PxDTCON2) registers.

14.6.3 Output Override Control

The PWM module output override feature allows the user application to manually drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units. The PWM override bits are useful when controlling various types of electrically commutated motors.

The output override feature can be controlled using the PWM Output Override (POVD4H-POVD1L) bits in the Override Control (PxOVDCON<15:8>) register.

14.6.4 Special Event Trigger

The PWM module has a Special Event Trigger that allows analog-to-digital conversions to be synchronized to the PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period. The Special Event Compare (PxSECMP) register specifies the special event compare value for generating the Special Event Trigger to start analog-to-digital conversion.

> **Note:** Detailed descriptions of the PWM timer, PWM time base period, output override feature and Special Event Trigger are given in following sections.

14.7   MCPWM MODULE OPERATING MODES

The MCPWM module can be configured for one of four modes of operation using the PWM Time Base Mode Select (PTMOD) control bits in the PWM Time Base Control (PxTCON<1:0>) register. The four operating modes are described in the following sections.

14.7.1   Free Running Mode (PTMOD <1:0> = 0b00)

In this mode, the PWM Time Base (PxTMR) register will count upward until the value in the PWM Time Base Period (PxTPER) register is matched. The PxTMR register is reset on the following input clock edge. The timer will continue counting upward and resetting as long as the PWM Time Base Timer Enable (PTEN) bit in the PWM Time Base Control (PxTCON<15>) register remains set.

14.7.2   Single Event Mode (PTMOD <1:0> = 0b01)

The PWM timer (PxTMR) will begin counting upward when the PTEN bit is set. When the PxTMR value matches the PxTPER register value, the PxTMR register is reset on the following input clock edge and the PTEN bit is cleared by the hardware to halt the timer.

14.7.3   Continuous Up/Down Count Mode (PTMOD <1:0> = 0b10)

In this mode, the PWM timer (PxTMR) will count upward until the value in the PxTPER register is matched. The timer will begin counting downward on the following clock edge and continue counting down until it reaches zero. The PWM Time Base Count Direction Status (PTDIR) bit in the PWM Time Base (PxTMR<15>) register indicates the counting direction. This bit is set when the timer starts counting downward.

14.7.4   Continuous Up/Down Count Mode with Interrupts for Double Update of Duty Cycle (PTMOD <1:0> = 0b11)

This mode is similar to the Continuous Up/Down Count mode, with the exception that an interrupt event is generated twice per time base: once when the PxTMR register is equal to zero and a second time when a period match occurs.

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14.8   PWM CLOCK CONTROL

The time base for the PWM pulses is provided by the 15-bit timer with prescale and postscale options, as shown in Figure 14-2.

Figure 14-2:   PWM Clock Control
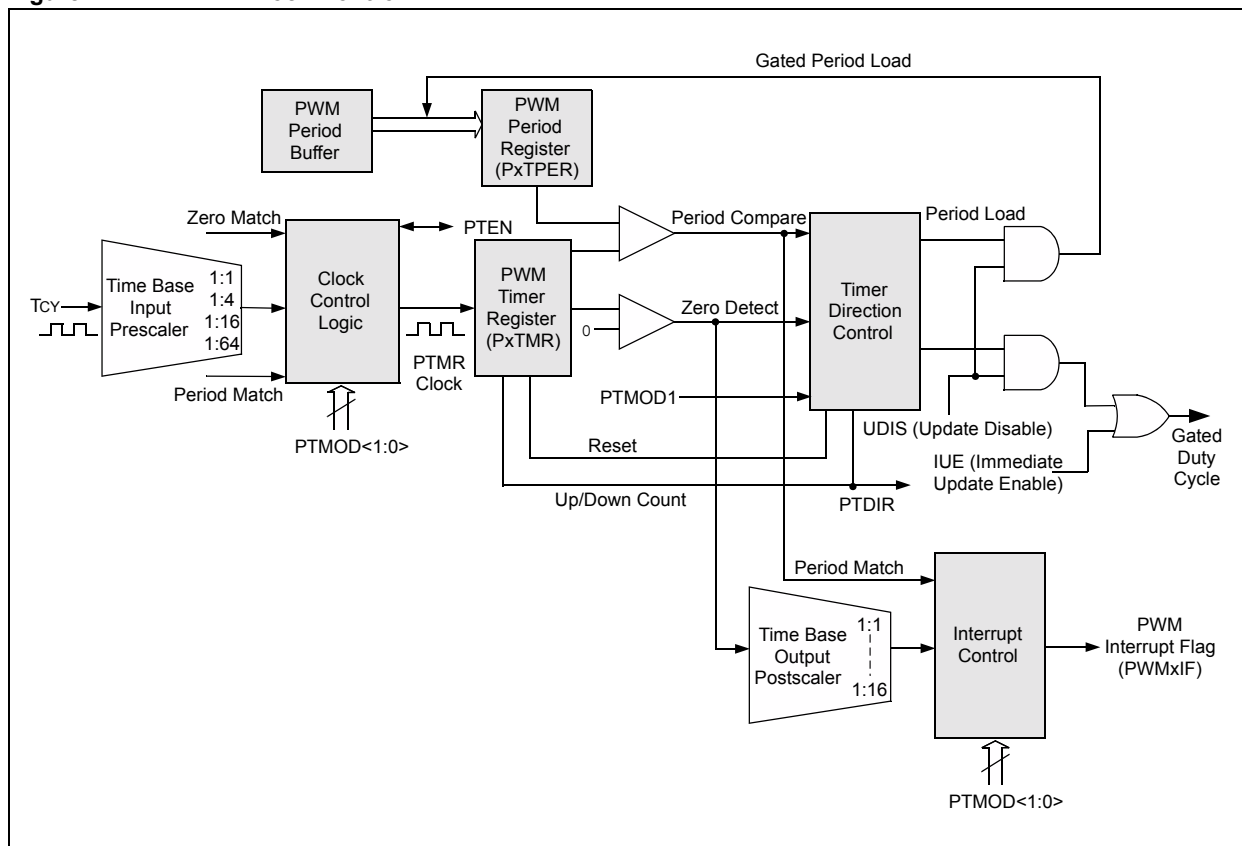
14.8.1   Time Base Input Prescaler

The input clock (T$_{CY}$) derived from the oscillator source can be prescaled to four possible options: 1:1, 1:4, 1:16 and 1:64. These options can be selected by using the PWM Time Base Input Clock Prescale Select (PTCKPS) bits of the PWM Time Base Control (PxTCON<3:2>) register. The prescaled clock is the input to the PWM clock control logic block.

14.8.2   Clock Control Logic and Time Base

This block determines the nature of the PWM timer output, depending on the time period match, zero match and PWM Time Base Mode Select (PTMOD) bits in the PWM Time Base Control (PxTCON<1:0>) register. The time base input prescaler counter is cleared when any of the following occur:

• A write to the PxTMR register
• A write to the PxTCON register
• A device Reset

The PWM Time Base (PxTMR) register is not cleared when PxTCON is written.

The time base value of the PWM Time Base Register Count Value (PTMR) bit in the PWM Time Base (PxTMR<14:0>) register is compared with the contents of the PWM Time Base Period (PxTPER) register. If a match occurs, a period match signal is generated.

If the time base value of the PTMR bits of the PxTMR register is zero, a zero detect signal is generated.

14.8.3 Timer Direction Control

The timer direction control block determines the count direction. The PWM Time Base Count Direction Status (PTDIR) bit in the PWM Time Base (PxTMR<15>) register is a read-only bit that gives the present direction of the count. If the PTDIR bit is cleared, PxTMR is counting upward, and if it is set, PxTMR is counting downward. The time base is enabled or disabled by setting or clearing the PWM Time Base Timer Enable (PTEN) bit in the PWM Time Base Control (PxTMR<15>) register. The PxTMR register is not cleared when the PTEN bit is cleared in software.

14.8.4 Time Base Output Postscaler

The time base output postscaler is used to optionally select one of several possible options (1:1 to 1:16, scaling inclusive) to postscale the timer output. The interrupt control logic decides when to set the PWM Interrupt flag PWMxIF for generating a PWM interrupt, depending on the postscale value. The postscaler is useful when the PWM duty cycles need not be updated every PWM cycle.

The time base output postscaler counter is cleared when any of the following occur:

• A write to the PxTMR register
• A write to the PxTCON register
• A device Reset

The PxTMR register is not cleared when the PxTCON register is written.

14.8.5 PWM Time Period

The PxTPER register determines the counting period for the PxTMR register. The user application must write a 15-bit value into the PWM Time Base Period Value (PxTPER) bits of the PWM Time Base (PxTMR<14:0>) register. When the value of PxTMR<14:0> matches the value of PxTPER<14:0>, the time base will either reset to zero or reverse the count direction on the next clock input edge. The action taken depends on the operating mode of the time base.

The time base period is double buffered to allow run-time changes of the time period of the PWM signal without any glitches. The PxTPER register serves as a buffer to the actual register, which is not accessible by the user application. The PxTPER register contents are loaded into the actual time base period register at the following times:

• Free Running and Single Event modes: when the PxTMR register is reset to zero after a match with the PxTPER register.
• Up/Down Counting modes: when the PxTMR register is zero.

The value held in the PxTPER register is automatically loaded into the PWM Time Base Period (PxTPER) register when the PWM time base is disabled (PTEN = 0). Figure 14-3 and Figure 14-4 indicate the times when the contents of the PxTPER register are loaded into the time base period register.

Figure 14-3:   PWM Period Buffer Updates in Free Running Count Mode
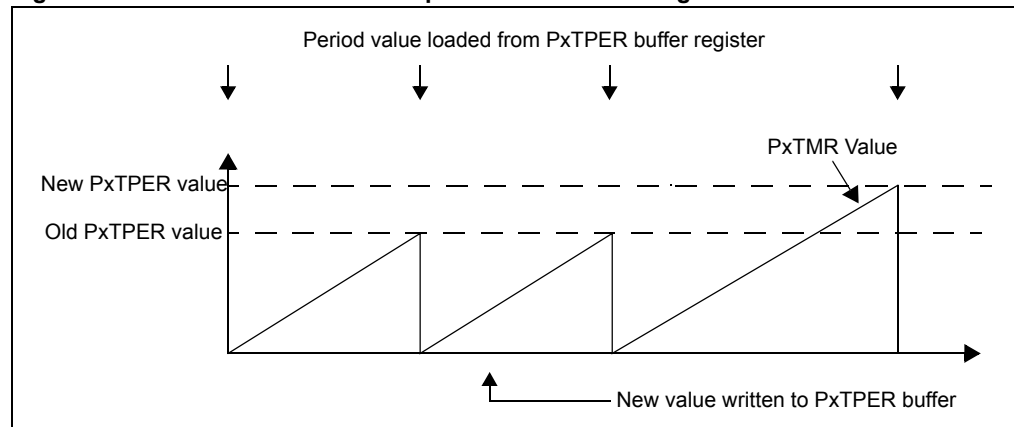
The PWM period can be determined from the formula shown in Equation 14-1:

Equation 14-1:   PWM Period Calculation for Free Running Count Mode (PTMOD = `10` or `11`)

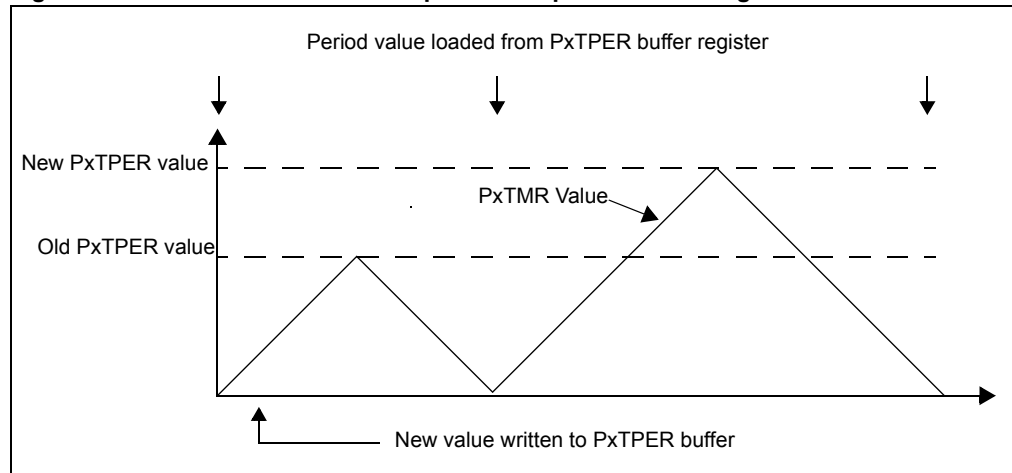$$\text{PxTPER} = \frac{F_{CY}}{F_{PWM} \times (\text{PxTMR Prescaler})} - 1$$

Example:

F_{CY} = 20 MHz
F_{PWM} = 20,000 Hz
PxTMR Prescaler = 1:1

$$\text{PxTPER} = \frac{20,000,000}{20,000 \times 1} - 1$$

$$= 1000 - 1$$
$$= 999$$

Figure 14-4:   PWM Period Buffer Updates in Up/Down Counting Modes

Equation 14-2:   PWM Period Calculation in Up/Down Counting Modes (PTMOD = `00` or `01`)

$$\text{PxTPER} = \frac{F_{CY}}{F_{PWM} \times (\text{PxTMR Prescaler}) \times 2} - 1$$

Example:

F_{CY} = 20 MHz
F_{PWM} = 20,000 Hz
PxTMR Prescaler = 1:1

$$\text{PxTPER} = \frac{20,000,000}{20,000 \times 1 \times 2} - 1$$

$$= 500 - 1$$
$$= 499$$

14.9 TIME BASE INTERRUPTS

The generation of PWM interrupts depends on the mode of operation selected by the PWM Time Base Mode Select (PTMOD) bits of the PWM Time Base Control (PxTCON<1:0>) register and the time base output postscaler selected using the PWM Time Base Output Postscale Select (PTOPS) bits of the PxTCON (PxTCON<7:4>) register.

The interrupt generation for each of the operating modes is described below.

14.9.1 Free Running Mode

An interrupt event is generated when the PWM Time Base (PxTMR) register is reset to '0' due to a match with the PWM Time Base Period (PxTPER) register. The postscaler selection bits can be used in Free Running mode to reduce the frequency of the interrupt events.

14.9.2 Single Event Mode

An interrupt event is generated when the PxTMR register is reset to '0' due to a match with the PxTPER register. The PWM Time Base Timer Enable (PTEN) bit of the PxTCON (PxTCON<15>) register is also cleared to inhibit further PxTMR increments. The postscaler selection bits have no effect in Single Event mode.

14.9.3 Up/Down Counting Mode

An interrupt event is generated each time the value of the PxTMR register is equal to zero and the PWM time base begins to count upward. The postscale selection can be used to reduce the frequency of interrupt events in Up/Down Counting mode.

14.9.4 Up/Down Counting Mode with Double Update of Duty Cycle

An interrupt event is generated each time the PxTMR register is equal to zero and each time a period match occurs. The postscale selection has no effect in Up/Down Counting mode with Double Update of Duty Cycle. This mode allows the control loop bandwidth to be doubled because the PWM duty cycles can be updated twice per period. Every rising and falling edge of the PWM signal can be controlled using the double update mode.

On generation of a PWM interrupt, the PWM Interrupt flag PWMIF is set in the corresponding IFS register.

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14.10   PWM OUTPUT STATE CONTROL

The PWM High and Low I/O Enable (PENxH and PENxL) bits in the PWM Control Register 1 (PWMxCON1<7:0>) enable each PWM output pin for use by the module. When a pin is enabled for PWM output, the PORT and TRIS registers controlling the pin are disabled.

In addition to the PENxH and PENxL control bits, three device configuration bits in the BOR and POR Device Configuration (FBORPOR) register provide PWM output pin control. This register contains the following configuration bits:

• MCPWM High Side Drivers (PWMxH) Polarity bit (HPOL)
• MCPWM Low Side Drivers (PWMxL) Polarity bit (LPOL)
• MCPWM Drivers Initialization bit (PWMPIN)

These three configuration bits work in conjunction with the PWM enable (PENxH and PENxL) bits located in the PWMxCON1 register. These configuration bits ensure that the PWM pins are in the correct states after a device Reset.

14.10.1   Output Polarity Control

The polarity of the PWM I/O pins is set during device programming using the HPOL and LPOL configuration bits in the FBORPOR Device Configuration register. The HPOL configuration bit sets the output polarity for the high-side PWM outputs, PWMxH1-PWMxH4. The LPOL configuration bit sets the output polarity for the low-side PWM outputs PWMxL1-PWMxL4.

If the polarity configuration bit is set to '1', the corresponding PWM I/O pins will have active-high output polarity. If the polarity configuration bit is set to '0', the corresponding PWM pins will have active-low polarity.

14.10.2   PWM Output Pin Reset States

The PWMPIN configuration bit determines the behavior of the PWM output pins on a device Reset and can be used to eliminate external pull-up/pull-down resistors connected to the devices controlled by the PWM module.

If the PWMPIN configuration bit is set to '1', the PENyH and PENyL control bits will be cleared on a device Reset. Consequently, all PWM outputs are tri-stated and controlled by the corresponding PORT and TRIS registers.

If the PWMPIN configuration bit is set to '0', the PENyH and PENyL control bits are set on a device Reset. All PWM pins are enabled for PWM output at the device Reset and are at their inactive states as defined by the HPOL and LPOL configuration bits.

14.11   PWM OUTPUT MODES

This section describes the PWM output modes.

14.11.1   Single Event PWM Operation

The PWM module produces single pulse outputs when the PWM time base is configured for the Single Event mode (PTMOD<1:0> = 01). This mode of operation is useful for driving certain types of electronically commutated motors, such as high-speed switched reluctance motor operation. Only edge-aligned outputs can be produced in Single Event mode.

In Single Event mode, the PWM I/O pin(s) are driven to the active state when the PTEN (PxTCON<15>) bit is set. When a match with a duty cycle register occurs, the PWM I/O pin is driven to the inactive state. When a match with the PxTPER register occurs, the PxTMR register is cleared, all active PWM I/O pins are driven to the inactive state, the PTEN bit is cleared and an interrupt is generated. Operation of the PWM module stops until the PTEN bit is set again in software.

**Figure 14-5:   Single Event PWM Operation**
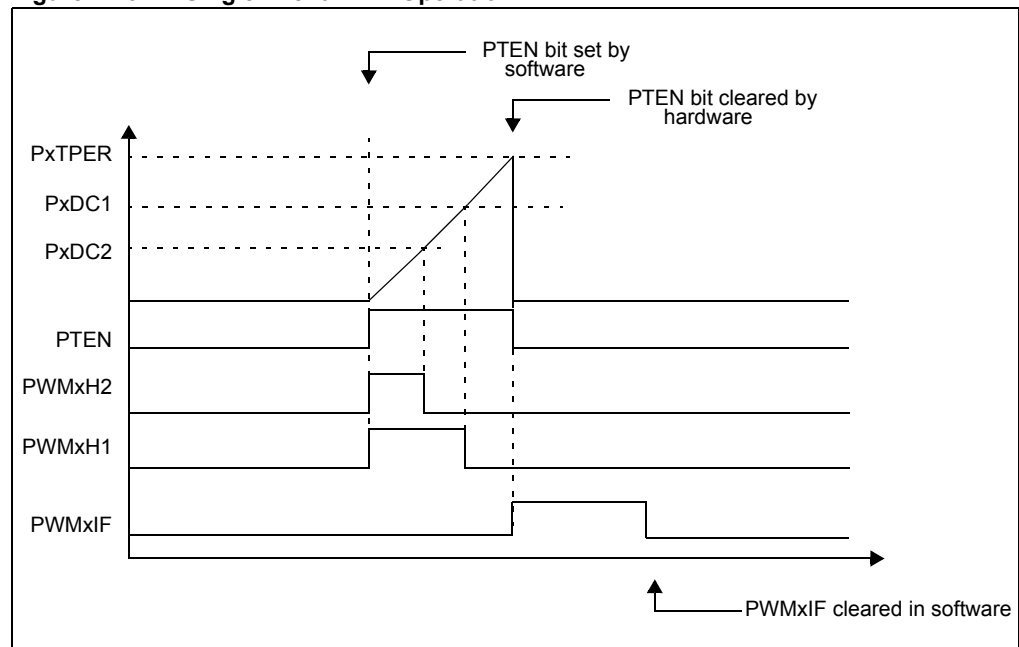
14.11.2   Edge-Aligned PWM

The PWM module produces edge-aligned PWM signals when the PWM time base is operating in Free Running mode. The output signal for a given PWM channel has a period specified by the value loaded in PxTPER and a duty cycle specified by the appropriate PxDCy register (see Figure 14-6). Assuming a non-zero duty cycle and no immediate updates enabled (IUE = 0), the outputs of all enabled PWM generators will be driven active at the beginning of the PWM period (PxTMR = 0). Each PWM output will be driven inactive when the value of PxTMR matches the duty cycle value of the PWM generator.

If the value in the PxDCy register is zero, the output on the corresponding PWM pin is inactive for the entire PWM period. In addition, the output on the PWM pin is active for the entire PWM period if the value in the PxDCy register is greater than the value held in the PxTPER register.

If immediate updates are enabled (IUE = 1), the new duty cycle value will be loaded when the new value is written to any active PxDCy register.

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Figure 14-6:   Edge-Aligned PWM
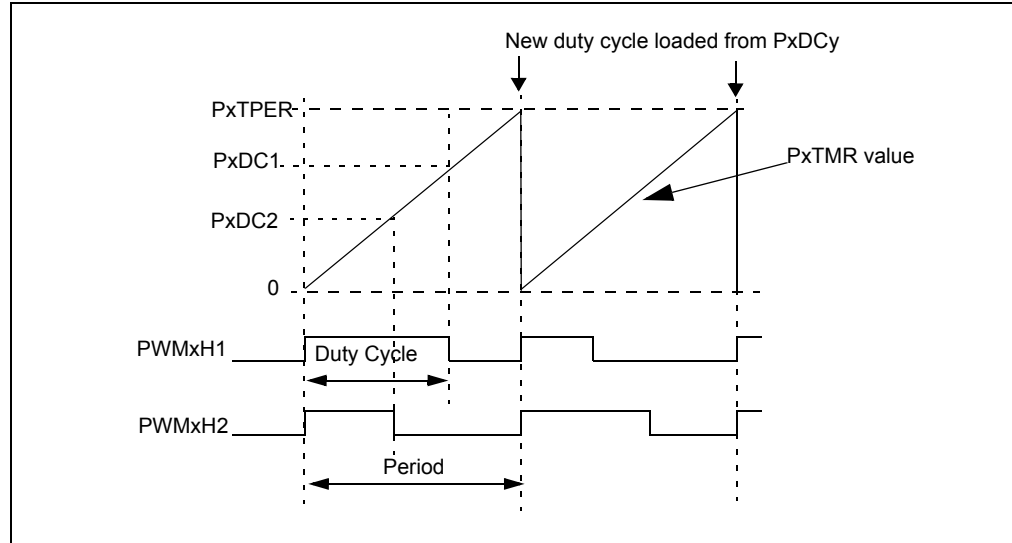
14.11.3   Center-Aligned PWM

The PWM module produces center-aligned PWM signals when the PWM time base is configured in one of the two Up/Down Counting modes (PTMOD<1:0> = 1x).

The PWM compare output is driven to the active state when the value of the duty cycle register matches the value of PTMR and the PWM time base is counting downward (PTDIR = 1). The PWM compare output is driven to the inactive state when the PWM time base is counting upward (PTDIR = 0) and the value in the PxTMR register matches the duty cycle value.

If the value in a particular duty cycle register is zero, the output on the corresponding PWM pin is inactive for the entire PWM period. In addition, the output on the PWM pin is active for the entire PWM period if the value in the duty cycle register is greater than the value in the PxTPER register.

Figure 14-7:   Center-Aligned PWM
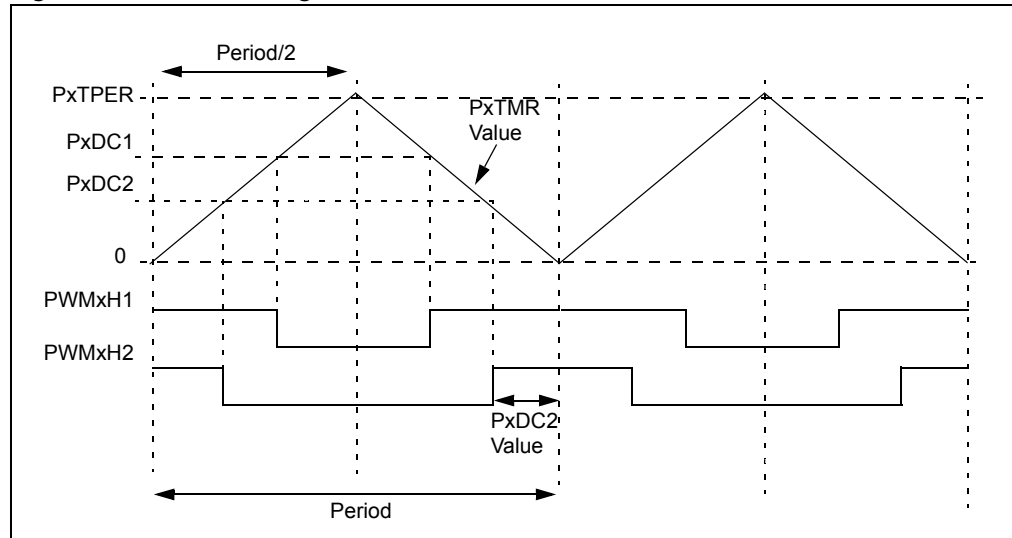
### 14.11.4 Complementary PWM Output Mode

Complementary PWM Output mode is used to drive inverter loads similar to the one shown in Figure 14-8. This inverter topology is typical for ACIM and BLDC applications. In Complementary PWM Output mode, a pair of PWM outputs cannot be active simultaneously. Each PWM channel and output pin pair is internally configured as shown in Figure 14-9. A dead time can be optionally inserted during device switching, making both outputs inactive for a short period. (Refer to **14.16 "Special Features of the MCPWM Module"**.)

Figure 14-8:   Typical Load for Complementary PWM Outputs
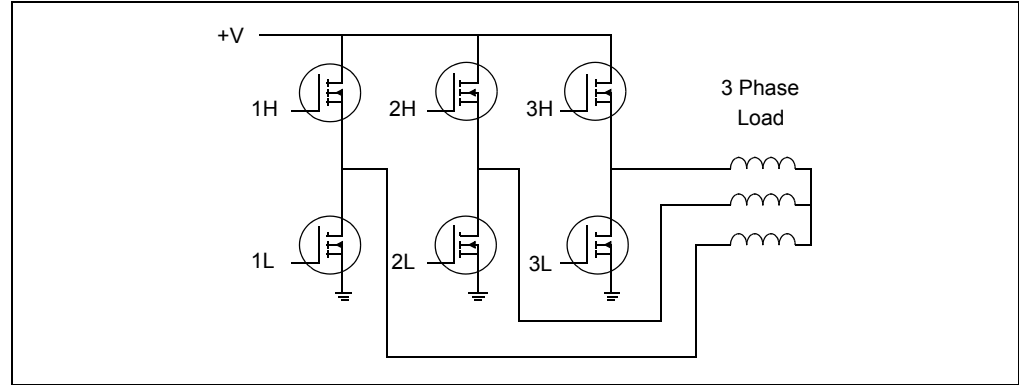
Complementary PWM Output mode is selected for each PWM I/O pin pair by clearing the appropriate PWM I/O Pair Mode (PMOD) bit in PWM Control Register 1 (PWMxCON1<11:8>). The PWM I/O pins are set to Complementary PWM Output mode by default upon a device Reset.

Figure 14-9:   PWM Channel Block Diagram, Complementary PWM Output Mode


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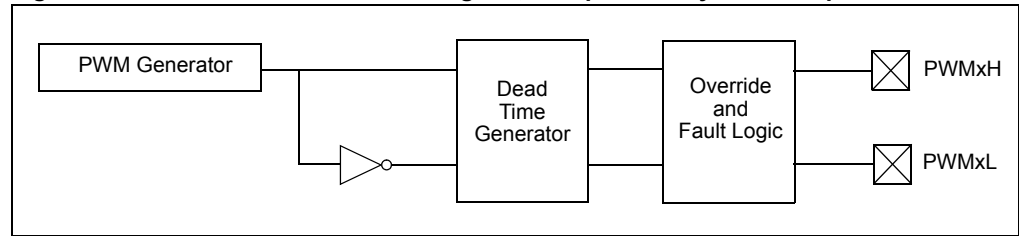
14.11.5 Independent PWM Output Mode

Independent PWM Output mode is useful for driving loads such as the one shown in Figure 14-10. A particular PWM output pair is in Independent PWM Output mode when the corresponding PWM I/O Pair Mode (PMOD) bit in PWM Control Register 1 (PWMxCON1<11:8>) is set. The dead time generators are disabled in Independent PWM Output mode, and there are no restrictions on the state of the pins for a given output pin pair.

Figure 14-10:   Asymmetric Inverter Load Using Independent PWM Output Mode
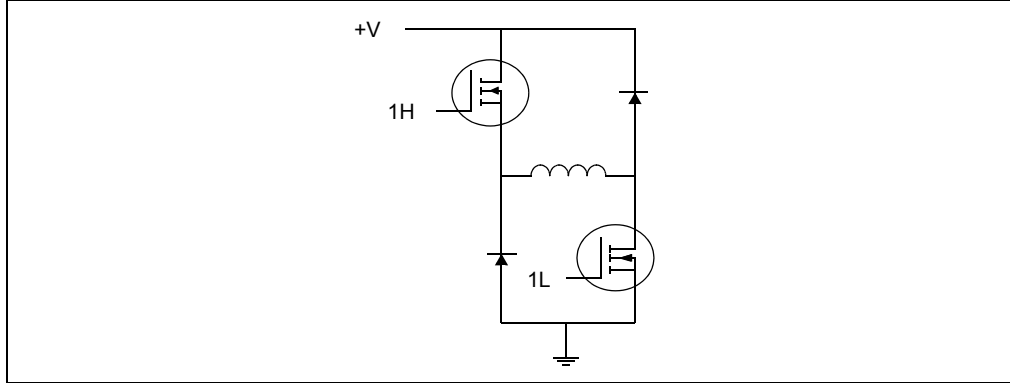
Figure 14-11:   PWM Block Diagram for One Output Pin Pair, Independent PWM Output Mode
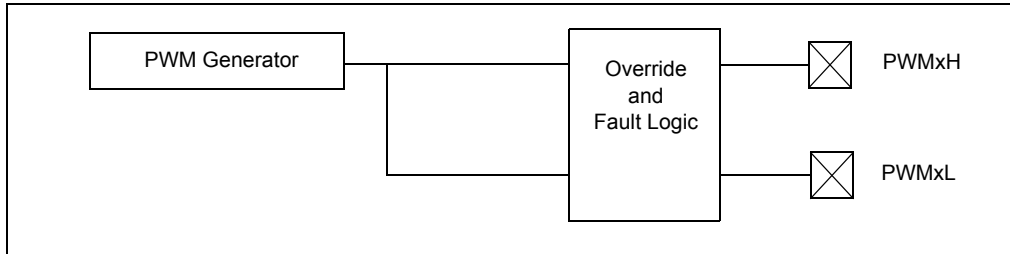
14.12 DUTY CYCLE REGISTER BUFFERING

The four PWM duty cycle registers, PxDC1-PxDC4, are buffered to allow glitchless updates of the PWM outputs. For each generator, there is a PxDCy register (buffer register) that is accessible by the user application and a non-memory mapped Duty Cycle register that holds the actual compare value. The PWM duty cycle is updated with the value in the PxDCy register at specific times in the PWM period to avoid glitches in the PWM output signal.

When the PWM time base is operating in Free Running or Single Event mode (PTMOD<1:0> = 0x), the PWM duty cycle is updated whenever a match with the PxTPER register occurs and PxTMR is reset to '0'.

> **Note:** Any write to the PxDCy registers immediately updates the duty cycle when the PWM time base is disabled (PTEN = 0). This allows a duty cycle change to take effect before PWM signal generation is enabled.

When the PWM time base is operating in Up/Down Counting mode (PTMOD<1:0> = 10), duty cycles are updated when the value of the PxTMR register is zero and the PWM time base begins to count upward. Figure 14-12 indicates the times when the duty cycle updates occur for Up/Down Counting mode.

When the PWM time base is in Up/Down Counting mode with double updates (PTMOD<1:0> = 11), duty cycles are updated when the value of the PxTMR register is zero and when the value of the PxTMR register matches the value in the PxTPER register. Figure 14-12 and Figure 14-13 indicate the times when the duty cycle updates occur for this mode of the PWM time base.

Figure 14-12: Duty Cycle Update Times in Up/Down Counting Mode
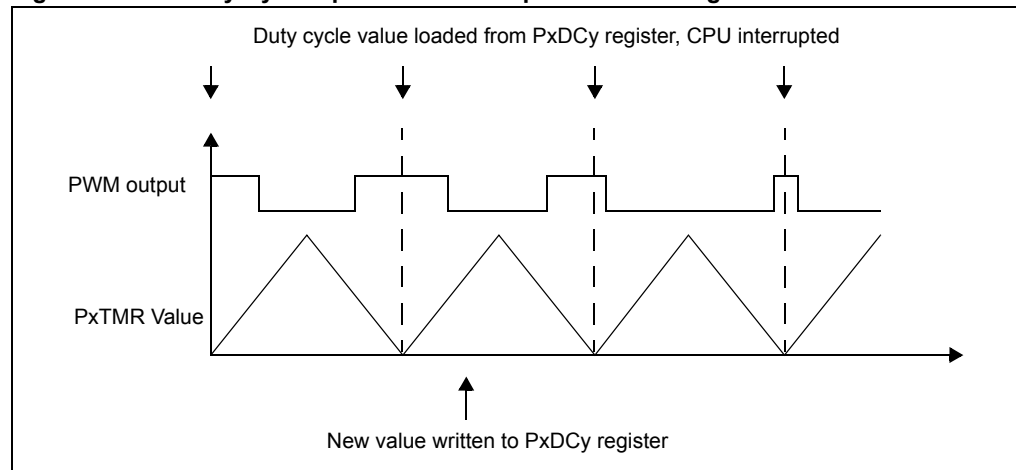
Figure 14-13: Duty Cycle Update Times in Up/Down Counting Mode with Double Updates


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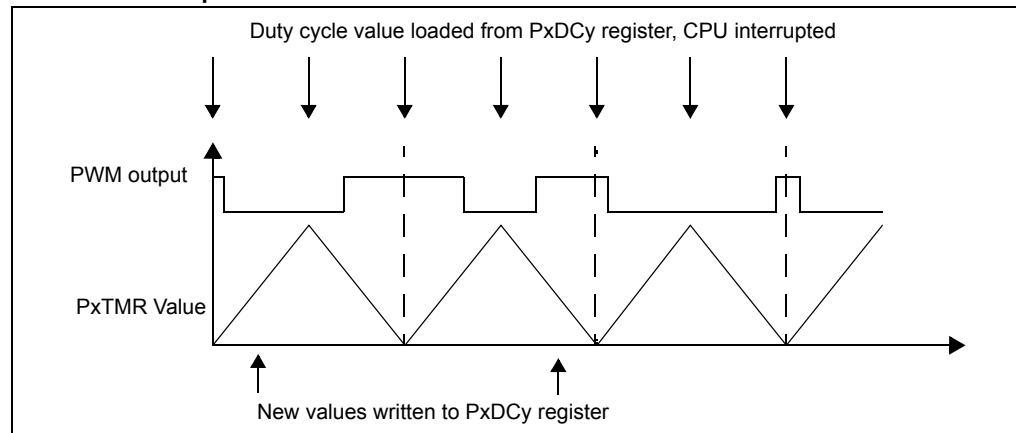
14.12.1 Immediate Update of PWM Duty Cycle

The Immediate Update Enable (IUE) bit in PWM Control Register 2 (PWMxCON2<2>) provides an option for updating the duty cycle values immediately after writing into the duty cycle registers. This feature eliminates waiting for the end of the time base period to update the duty cycle values. If the IUE bit is set, an immediate update of the duty cycle is enabled. If the bit is cleared, immediate update of the duty cycle is disabled. The following three cases are possible when immediate update is enabled:

- **Case 1:** If the PWM output is active at the time the new duty cycle is written and the new duty cycle is greater than the current time base value, the PWM pulse width is lengthened.
- **Case 2:** If the PWM output is active at the time the new duty cycle is written and the new duty cycle is less than the current time base value, the PWM pulse width is shortened.
- **Case 3:** If the PWM output is inactive at the time the new duty cycle is written and the new duty cycle is greater than the current time base value, the PWM output becomes active immediately and remains active for the newly written duty cycle value.

Figure 14-15 shows these cases.

Figure 14-14: Duty Cycle Update Times When Immediate Updates Are Enabled (IUE = 1)
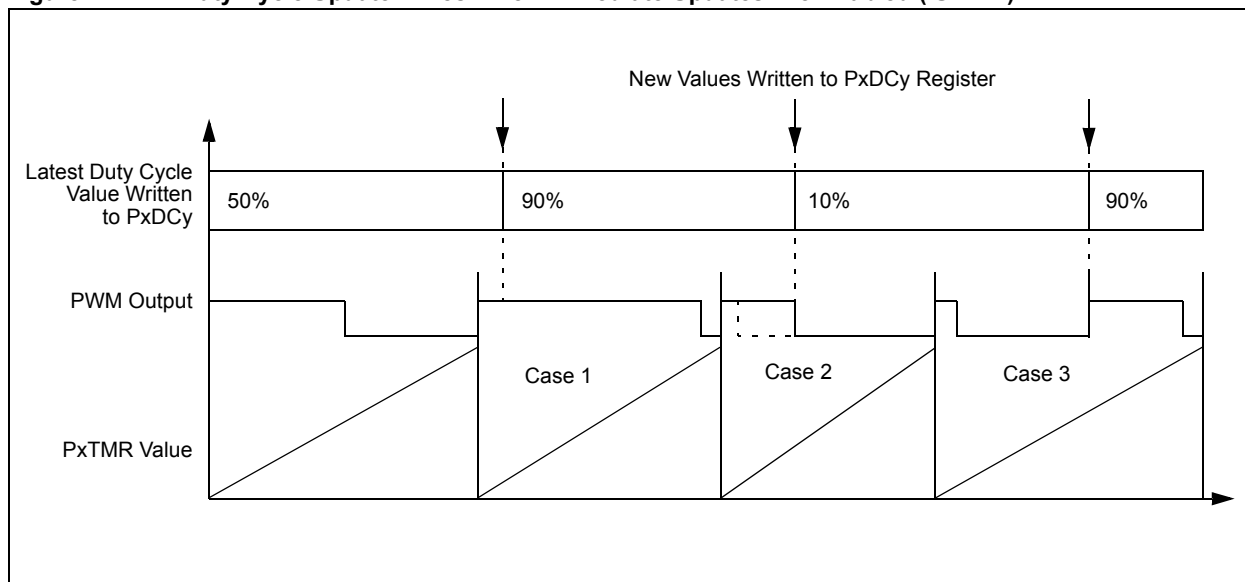
14.13   PWM DUTY CYCLE RESOLUTION

In the MCPWM module, the effective resolution for the generated PWM pulses is a function of the PWM frequency (or period) and the device operating frequency.

The maximum resolution (in bits) for a selected device oscillator and PWM frequency can be determined using the following formula:

Equation 14-3:   PWM Resolution

$$PWMResolution = log_2\left(\frac{2FCY}{FPWM}\right)$$

In Equation 14-3, F_{PWM} is the PWM switching frequency, and F_{CY} is the device operating frequency.

Table 14-1 shows the PWM resolutions and frequencies for a selection of execution speeds and PxTPER values. The PWM frequencies in Table 14-1 are for edge-aligned (Free Running PxTMR) PWM mode. For center-aligned modes (Up/Down PxTMR mode), the PWM frequencies are half the values in Table 14-1, as indicated in Table 14-2.

Table 14-1:   Example PWM Frequencies and Resolutions, 1:1 Prescaler, Edge-Aligned PWM

| T_{CY} (F_{CY})	PxTPER Value	PxDCy Value for 100%	PWM Resolution	PWM Frequency (F_{PWM})
25 ns (40 MHz)	0x7FFF	0xFFFF	16 bits	1.22 kHz
25 ns (40 MHz)	0x3FF	0x7FF	11 bits	39.1 kHz
50 ns (20 MHz)	0x7FFF	0xFFFF	16 bits	610 Hz
50 ns (20 MHz)	0x1FF	0x3FF	10 bits	39.1 kHz
100 ns (10 MHz)	0x7FFF	0xFFFF	16 bits	305 Hz
100 ns (10 MHz)	0xFF	0x1FF	9 bits	39.1 kHz
200 ns (5 MHz)	0x7FFF	0xFFFF	16 bits	153 Hz
200 ns (5 MHz)	0x7F	0xFF	8 bits	39.1 kHz

Table 14-2:   Example PWM Frequencies and Resolutions, 1:1 Prescaler, Center-Aligned PWM

| T_{CY} (F_{CY})	PxTPER Value	PxDCy Value for 100%	PWM Resolution	PWM Frequency
25 ns (40 MHz)	0x7FFF	0xFFFF	16 bits	610 Hz
25 ns (40 MHz)	0x3FFF	0x7FFF	15 bits	1.22 kHz
50 ns (20 MHz)	0x7FFF	0xFFFF	16 bits	305 Hz
50 ns (20 MHz)	0x1FFF	0x3FFF	14 bits	1.22 kHz
100 ns (10 MHz)	0x7FFF	0xFFFF	16 bits	153 Hz
100 ns (10 MHz)	0xFFF	0x1FFF	13 bits	1.22 kHz
200 ns (5 MHz)	0x7FFF	0xFFFF	16 bits	76.3 Hz
200 ns (5 MHz)	0x7FF	0xFFF	12 bits	1.22 kHz

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The MCPWM module can produce PWM signal edges with $T_{CY}/2$ resolution. PxTMR increments every T_{CY} with a 1:1 prescaler. To achieve $T_{CY}/2$ edge resolution, PxDCy<15:1> is compared to PxTMR<14:0> to determine a duty cycle match. The value in PxDCy<0> determines whether the PWM signal edge will occur at the T_{CY} or the $T_{CY}/2$ boundary. When a 1:4, 1:16 or 1:64 prescaler is used with the PWM time base, PxDCy<0> is compared to the Most Significant bit (MSb) of the prescaler counter clock to determine when the PWM edge should occur.

PxTMR and PxDCy resolutions are depicted in Figure 14-15. In this example, PxTMR resolution is T_{CY} and PxDCy resolution is $T_{CY}/2$ for 1:1 prescaler selection.

Figure 14-15: PxTMR and PxDCy Resolution Timing Diagram, Free Running Mode and 1:1 Prescaler Selection
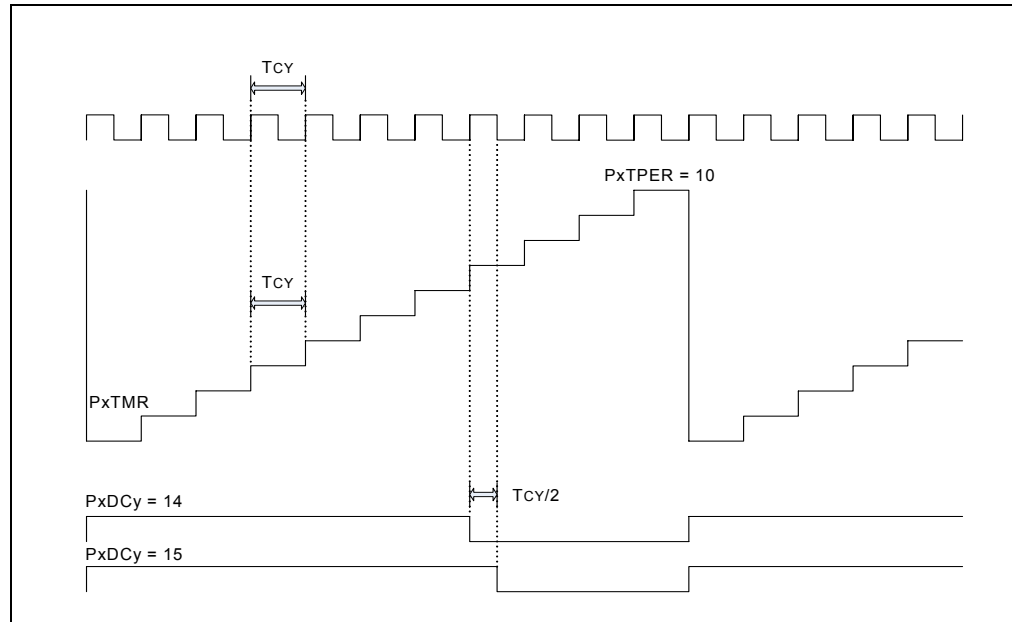
Figure 14-16: Duty Cycle Comparison Logic
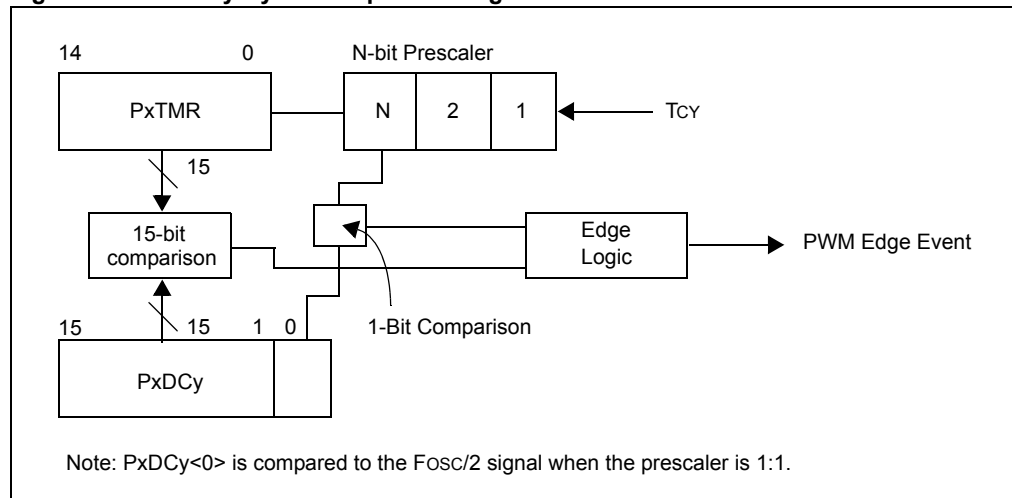
14.14   PWM DEAD TIME CONTROL

Each complementary output pair for the PWM module has a 6-bit down counter that is used to produce the dead time insertion. As shown in Figure 14-17, each dead time unit has a rising and falling edge detector connected to the duty cycle comparison output.

One of the two possible dead times is loaded into the timer on the detected PWM edge event. Depending on whether the edge is rising or falling, one of the transitions on the complementary outputs is delayed until the timer counts down to zero. Figure 14-18 shows a timing diagram indicating the dead time insertion for one pair of PWM outputs. The use of two different dead times for the rising and falling edge events has been exaggerated in the figure for clarity.

Figure 14-17:   Dead Time Unit Block Diagram for One Output Pin Pair
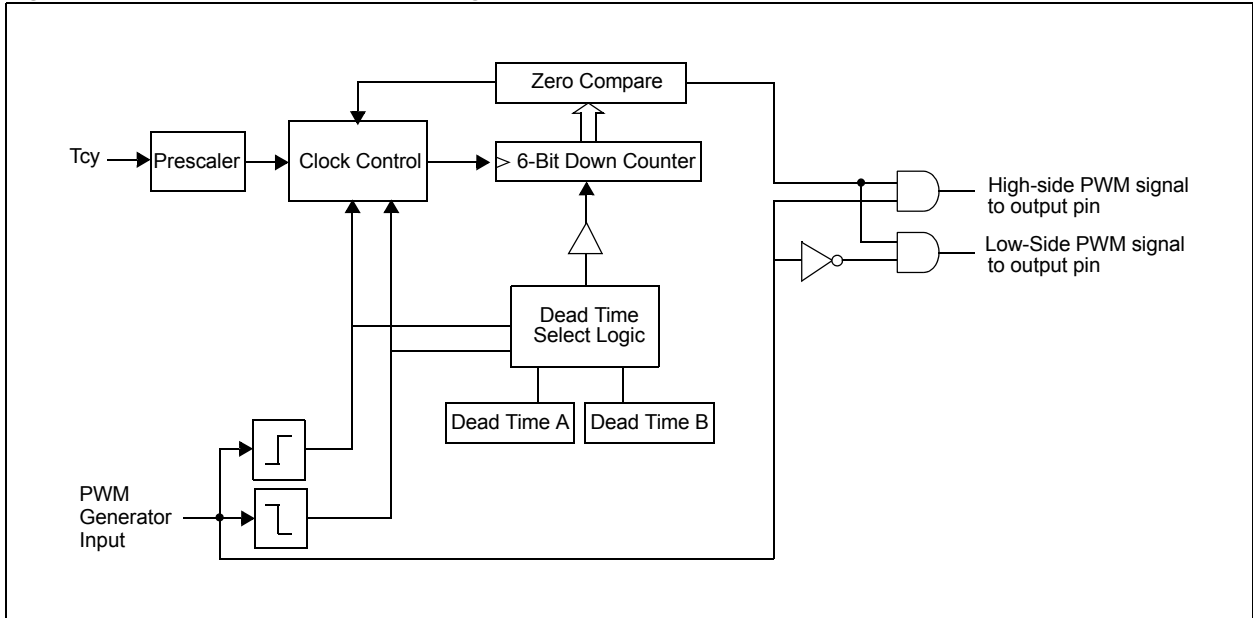
Figure 14-18:   Dead Time Insertion Diagram

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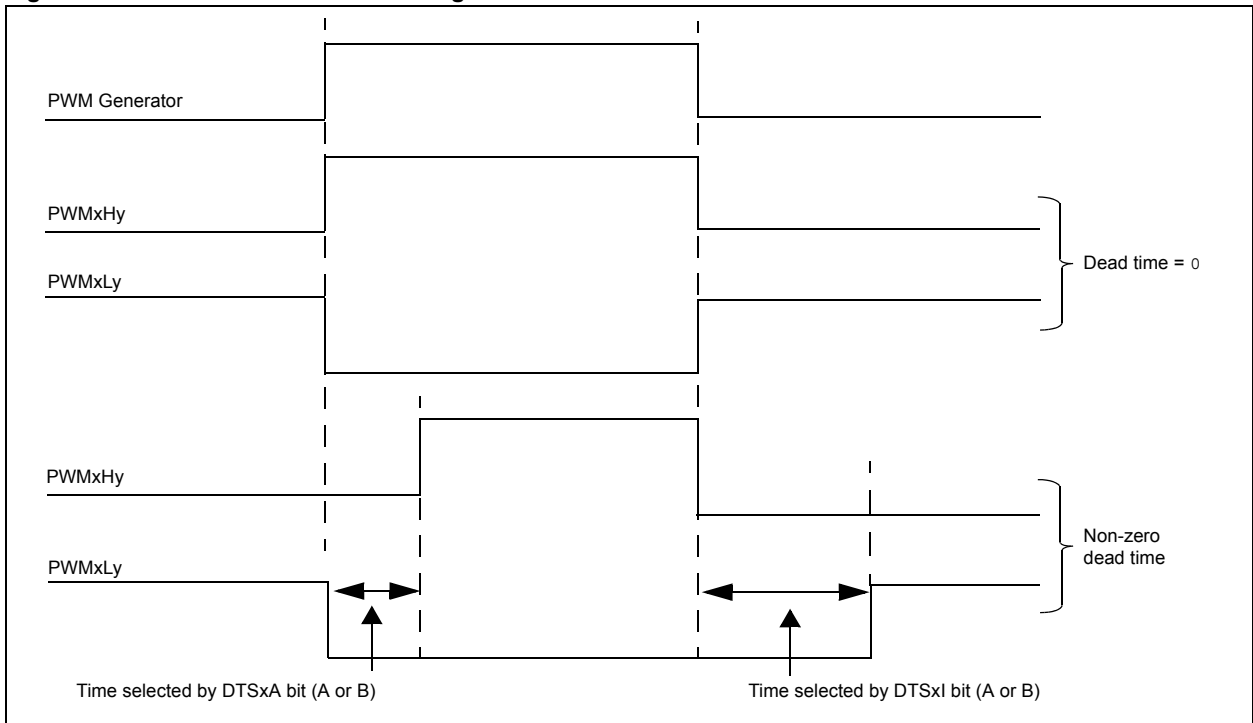
14.14.1 Dead Time Assignment

The Dead Time Control Register 2 (PxDTCON2) contains control bits that allow the two programmable dead times to be assigned to each of the complementary outputs. There are two dead time assignment control bits for each of the complementary outputs. For example, the Dead Time Select bit for PWM1 Signal Going Active (DTS1A) and Dead Time Select bit for PWM1 Signal Going Inactive (DTS1I) control bits select the dead times to be used for the PWMxH1/PWMxL1 complementary output pair. The pair of dead time selection control bits are referred to as the "dead-time-select-active" and "dead-time-select-inactive" control bits, respectively. The function of each bit in a pair is as follows:

- The DTSxA control bit selects the dead time that is to be inserted before the high-side output is driven active.
- The DTSxI control bit selects the dead time that is to be inserted before the low-side PWM output is driven active.

Table 14-3 summarizes the function of each dead time selection control bit.

Table 14-3:   Dead Time Selection Bits

Bit	Function
DTS1A	Selects PWMxH1/PWMxL1 dead time inserted before PWMxH1 is driven active.
DTS1I	Selects PWMxH1/PWMxL1 dead time inserted before PWMxL1 is driven active.
DTS2A	Selects PWMxH2/PWMxL2 dead time inserted before PWMxH2 is driven active.
DTS2I	Selects PWMxH2/PWMxL2 dead time inserted before PWMxL2 is driven active.
DTS3A	Selects PWMxH3/PWMxL3 dead time inserted before PWMxH3 is driven active.
DTS3I	Selects PWMxH3/PWMxL3 dead time inserted before PWMxL3 is driven active.
DTS4A	Selects PWMxH4/PWMxL4 dead time inserted before PWMxH4 is driven active.
DTS4I	Selects PWMxH4/PWMxL4 dead time inserted before PWMxL4 is driven active.

14.14.2 Dead Time Ranges

Dead Time Unit A and Dead Time Unit B are set by selecting an input clock prescaler value and a 6-bit unsigned dead time count value.

Four input clock prescaler selections have been provided to allow a suitable range of dead times based on the device operating frequency. The clock prescaler option can be selected independently for each of the two dead time values. The dead time clock prescaler values are selected using the Dead Time Unit A Prescale Select (DTAPS) bits <1:0> and Dead Time Unit B Prescale Select (DTBPS) bits <1:0> in the Dead Time Control Register 1 (PxDTCON1<15:14> and PxDTCON1<7:6>) SFR. The following clock prescaler options can be selected for each of the dead time values:

- T_{CY}
- 2 T_{CY}
- 4 T_{CY}
- 8 T_{CY}

Equation 14-4:   Dead Time Calculation

$$DT = \frac{Dead\ Time}{Prescale\ Value \bullet T_{CY}}$$

Note: DT (Dead Time) is the DTA<5:0> or DTB<5:0> register value.

Table 14-4 shows example dead time ranges as a function of the input clock prescaler selected and the device operating frequency.

Table 14-4:   Example Dead Time Ranges

Tcy (Fcy)	Prescaler Selection	Resolution	Dead Time Range
25 ns (40 MHz)	1 Tcy	25 ns	25 ns – 1.6 µs
25 ns (40 MHz)	4 Tcy	100 ns	100 ns – 7 µs
50 ns (20 MHz)	4 Tcy	200 ns	200 ns – 12 µs
100 ns (10 MHz)	2 Tcy	200 ns	200 ns – 12 µs
100 ns (10 MHz)	1 Tcy	100 ns	100 ns – 6 µs

14.14.3 Dead Time Distortion

For short PWM duty cycles, the ratio of dead time to the active PWM time can become large. At the extreme case, when the duty cycle is less than or equal to the programmed duty cycle, no PWM pulse will be generated. In these cases, the inserted dead time introduces distortion into waveforms produced by the PWM module.

The user application can minimize dead time distortion by keeping the PWM duty cycle at least three times larger than the dead time. Dead time distortion can also be corrected by other techniques, such as closed loop current control.

A similar effect occurs for duty cycles near 100%. The maximum duty cycle used in the application should be chosen such that the minimum inactive time of the PWM signal is at least three times larger than the dead time.

The following code examples demonstrate how to configure the MCPWM module.

Example 14-1:   MCPWM Module Operating Mode and Time Selection

```
/* Configuration register FBORPOR */
/* High and Low switches set to active high state */

_FPOR(RST_PWMPIN & PWMxH_ACT_HI & PWMxL_ACT_HI)

/* PWM time base operates in a Free Running mode */

P1TCONbits.PTMOD = 0b00;

/* PWM time base input clock period is Tcy (1:1 pre scale) */
/* PWM time base output post scale is 1:1 */

P1TCONbits.PTCKPS = 0b00;
P1TCONbits.PTOPS = 0b00;

/* Choose PWM time period based on input clock selected */
/* Refer to Equation 14-1 */
/* PWM switching frequency is 20KHz */
/* Fcy is 20MHz */

P1TPER = 999;
```

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Example 14-2:   MCPWM Module Output Mode Selection

```
/* PWM I/O pairs 1 to 3 are in complementary mode */
/* PWM pins are enabled for PWM output */

PWM1CON1bits.PMOD1 = 0;
PWM1CON1bits.PMOD2 = 0;
PWM1CON1bits.PMOD3 = 0;
PWM1CON1bits.PEN1H = 1;
PWM1CON1bits.PEN2H = 1;
PWM1CON1bits.PEN3H = 1;
PWM1CON1bits.PEN1L = 1;
PWM1CON1bits.PEN2L = 1;
PWM1CON1bits.PEN3L = 1;


/* Immediate update of PWM enabled */


PWM1CON2bits.IUE = 1;
```

Example 14-3:   Dead Time Insertion (Complementary PWM Output Mode Only)

```
/* Clock period for Dead Time Unit A is Tcy */
/* Clock period for Dead Time Unit B is Tcy */

P1DTCON1bits.DTAPS = 0b00;
P1DTCON1bits.DTBPS = 0b00;

/* Dead time value for Dead Time Unit A */
/* Dead time value for Dead Time Unit B */

P1DTCON1bits.DTA = 10;
P1DTCON1bits.DTB = 20;

/* Dead Time Unit selection for PWM signals */
/* Dead Time Unit A selected for PWM active transitions */
/* Dead Time Unit B selected for PWM inactive transitions */

P1DTCON2bits.DTS3A = 0;
P1DTCON2bits.DTS2A = 0;
P1DTCON2bits.DTS1A = 0;

P1DTCON2bits.DTS3I = 1;
P1DTCON2bits.DTS2I = 1;
P1DTCON2bits.DTS1I = 1;
```

Example 14-4:   MCPWM Module I/O Pin Control

```
/* PWM I/O pin controlled by PWM Generator */

P1OVDCONbits.POVD3H = 1;
P1OVDCONbits.POVD2H = 1;
P1OVDCONbits.POVD1H = 1;
P1OVDCONbits.POVD3L = 1;
P1OVDCONbits.POVD2L = 1;
P1OVDCONbits.POVD1L = 1;
```

Example 14-5:   MCPWM Module Duty Cycle Initialization

```
/* Initialize duty cycle values for PWM1, PWM2 and PWM3 signals */

P1DC1 = 200;
P1DC2 = 200;
P1DC3 = 200;
```

Example 14-6:   Enabling PWM Pulse Generation

```
P1TCONbits.PTEN = 1;
```

14.15   PWM FAULT HANDLING

There are two fault pins, $\overline{\text{FLTxA}}$ and $\overline{\text{FLTxB}}$, associated with the PWM module. When asserted, these pins can optionally drive each of the PWM I/O pins to a defined state. This action takes place without software intervention so fault events can be managed quickly.

These fault pins can have other multiplexed functions depending on the dsPIC33F device variant. When used as a fault input, each fault pin is readable using its corresponding PORT register. The $\overline{\text{FLTxA}}$ and $\overline{\text{FLTxB}}$ pins function as active low inputs so that it is easy to inclusively OR many sources to the same input through an external pull-up resistor. When not used with the PWM module, these pins can be used as general purpose I/O or for another multiplexed function. Each fault pin has its own interrupt vector, Interrupt Flag bit, Interrupt Enable bit and Interrupt Priority bits.

The function of the $\overline{\text{FLTxA}}$ pin is controlled by the Fault A Configuration (PxFLTACON) register, and the function of the $\overline{\text{FLTxB}}$ pin is controlled by the Fault B Configuration (PxFLTBCON) register.

14.15.1   Fault Pin Enable Bits

The PxFLTACON and PxFLTBCON registers each have four Fault Input Enable (FAEN1-FAEN4 and FBEN1-FBEN4) bits that determine whether a particular pair of PWM I/O pins is to be controlled by the fault input pin. To enable a specific PWM I/O pin pair for fault overrides, the corresponding bit should be set in the PxFLTACON or PxFLTBCON register.

If all enable bits are cleared in the PxFLTACON or PxFLTBCON registers, that fault input pin has no effect on the PWM module and no fault interrupts are produced.

14.15.2   Fault States

The PxFLTACON and PxFLTBCON special function registers each have eight bits that determine the state of each PWM I/O pin when the fault input pin becomes active. When these bits are cleared, the PWM I/O pin is driven to the inactive state. If the bit is set, the PWM I/O pin is driven to the active state. The active and inactive states are referenced to the polarity defined for each PWM I/O pin (set by HPOL and LPOL device configuration bits).

A special case exists when a PWM module I/O pair is in Complementary PWM Output mode and both pins are programmed to be active on a Fault condition. The high-side pin will always have priority in Complementary PWM Output mode, so that both I/O pins cannot be driven active simultaneously.

14.15.3   Fault Input Modes

Each of the fault input pins has two modes of operation:

- **Latched Mode:** When the fault pin is driven low, the PWM outputs go to the states defined in the PxFLTACON and PxFLTBCON registers. The PWM outputs remain in this state until the fault pin is driven high and the corresponding interrupt flag (FLTxAIF or FLTxBIF) has been cleared in software. When both of these actions have occurred, the PWM outputs return to normal operation at the beginning of the next PWM period or half-period boundary regardless of the Immediate Update Enable (IUE) bit value. If the interrupt flag is cleared before the fault condition ends, the PWM module waits until the fault pin is no longer asserted to restore the outputs.
- **Cycle-by-Cycle Mode:** When the fault input pin is driven low, the PWM outputs remain in the defined fault states for as long as the fault pin is held low. After the fault pin is driven high, the PWM outputs return to normal operation at the beginning of the following PWM period (or half-period boundary in center-aligned modes) even when immediate updates are enabled.

The operating mode for each fault input pin is selected using the Fault A Mode (FLTAM) bit and Fault B Mode (FLTBM) bit (PxFLTACON<7> and PxFLTBCON<7>).

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14.15.3.1 ENTRY INTO A FAULT CONDITION

When a fault pin is enabled and driven low, the PWM pins are immediately driven to their programmed fault states regardless of the values in the PWM Duty Cycle (PxDCy) and Override Control (PxOVDCON) registers. The fault action has priority over all other PWM control registers.

14.15.3.2 EXIT FROM A FAULT CONDITION

A fault condition must be cleared by the external circuitry driving the fault input pin high and clearing the fault interrupt flag (Latched mode only). After the fault pin condition has been cleared, the PWM module restores the PWM output signals on the next PWM period or half-period boundary. For edge-aligned PWM generation, the PWM outputs are restored when PxTMR = 0. For center-aligned PWM generation, the PWM outputs are restored when PxTMR = 0 or PxTMR = PxTPER, whichever event occurs first.

An exception to these rules occurs when the PWM time base is disabled (PTEN = 0). If the PWM time base is disabled, the PWM module restores the PWM output signals immediately after the Fault condition has been cleared.

14.15.4 Fault Pin Priority

If both fault input pins have been assigned to control a particular pair of PWM pins, the fault states programmed for the $\overline{\text{FLTxA}}$ input pin will take priority over the $\overline{\text{FLTxB}}$ input pin.

One of two actions will take place when the Fault A condition has been cleared. If the $\overline{\text{FLTxB}}$ input is still asserted, the PWM outputs will return to the states programmed in the Fault B Control (PxFLTBCON) register on the next period or half-period boundary. If the $\overline{\text{FLTxB}}$ input is not asserted, the PWM outputs will return to normal operation on the next period or half-period boundary.

> **Note:** When the $\overline{\text{FLTxA}}$ pin is programmed for Latched mode, the PWM outputs will not return to the Fault B states or normal operation until the Fault A interrupt flag has been cleared and the $\overline{\text{FLTxA}}$ pin is de-asserted.

14.15.5 Fault Pin Software Control

Each of the fault pins can be controlled manually in software. Since each fault input is shared with a PORT I/O pin, the PORT pin can be configured as an output by clearing the corresponding TRIS bit. When the PORT bit for the pin is cleared, the fault input is activated.

> **Note:** Caution should be exercised when controlling the fault inputs in software. If the TRIS bit for the fault pin is cleared, the fault input cannot be driven externally.

14.15.6 Fault Timing Examples

The following figures provide examples of PWM fault timing.

Figure 14-19: Example Fault Timing, Cycle-by-Cycle Mode

Note: Arrows indicate the time when normal PWM operation is restored.
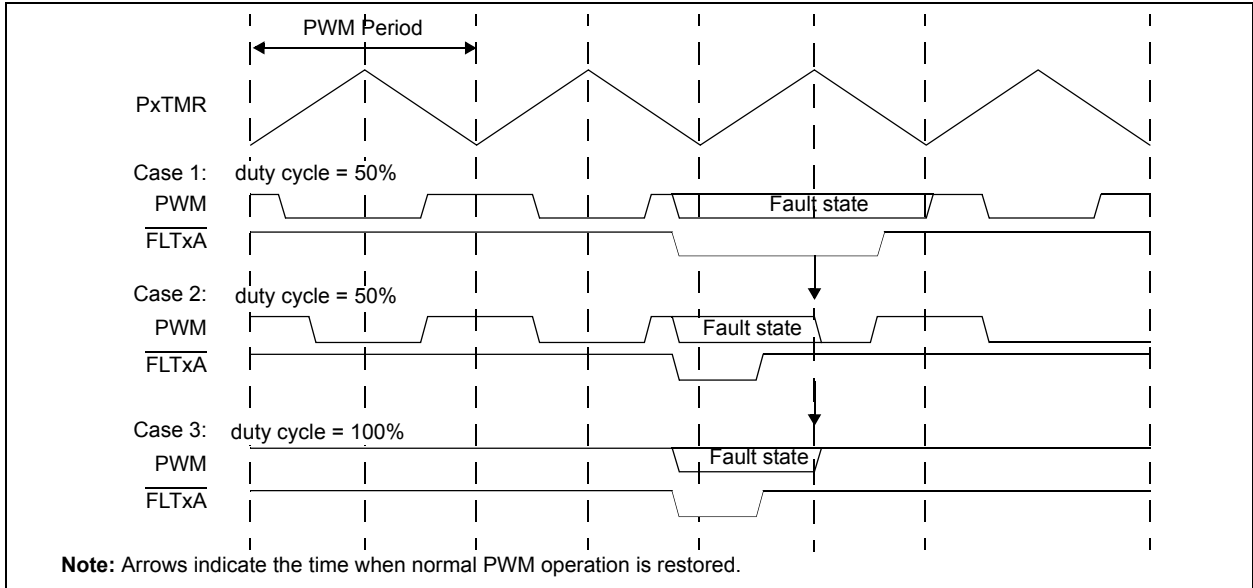
Figure 14-20: Example Fault Timing, Latched Mode

Figure 14-21: Example Fault Timing, Cycle-by-Cycle Mode, Priority Operation

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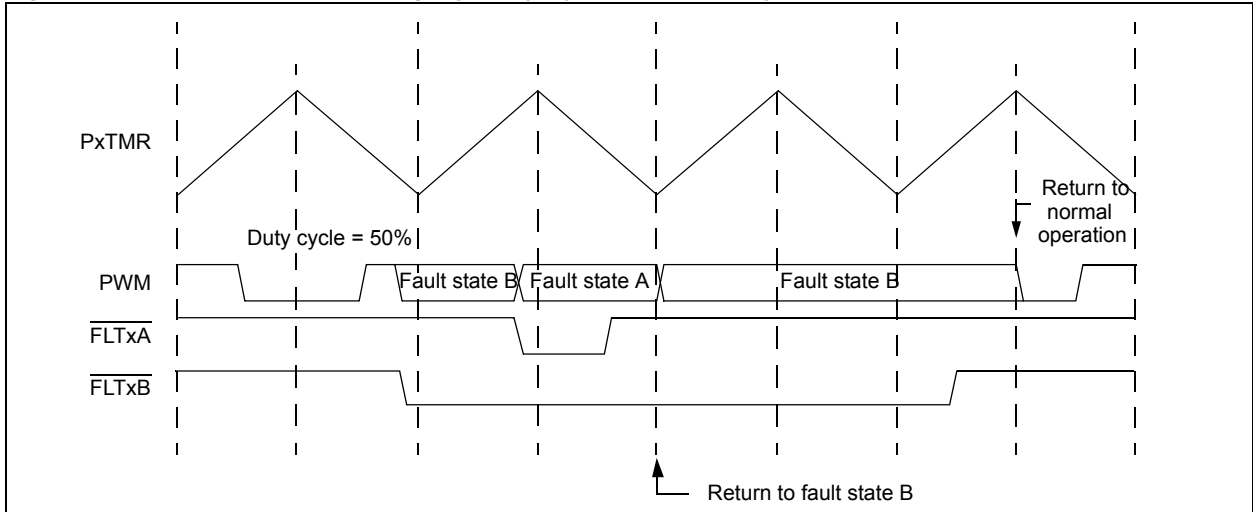
14.16   SPECIAL FEATURES OF THE MCPWM MODULE

The following special features are available in the MCPWM module:

• PWM Output Override
• Special Event Trigger
• PWM Update Lockout
• Device Emulation

14.16.1   PWM Output Override

The PWM output override bits allow the PWM I/O pins to be manually driven to specified logic states independent of the duty cycle comparison units. The PWM override bits are useful when controlling various types of electrically commutated motors.

Figure 14-22 shows a block diagram of the PWM output override control.
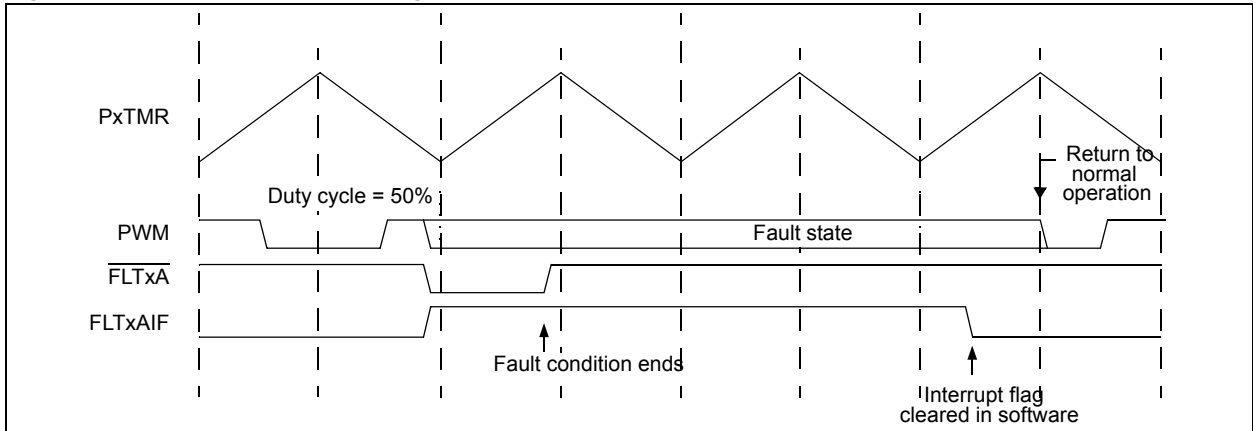
Figure 14-22:   Output Override Control
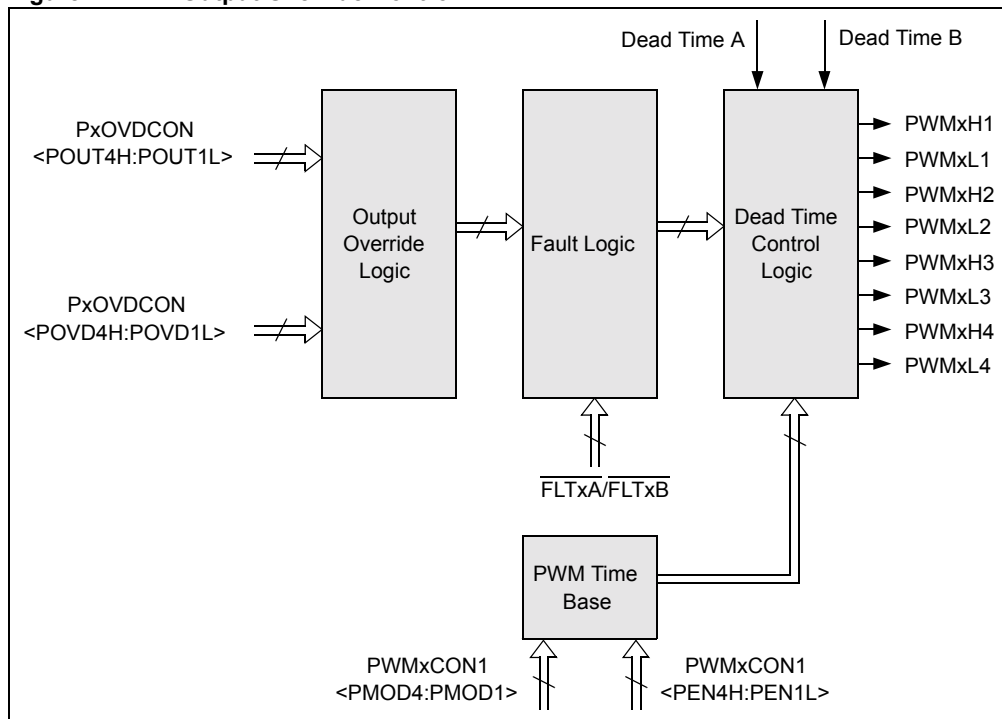
All control bits associated with the PWM output override function are in the Override Control (PxOVDCON) register. The upper half of the PxOVDCON register contains eight PWM Output Override bits (POVDx) that determine which PWM I/O pins will be overridden. The lower half of the PxOVDCON register contains eight PWM Manual Output (POUTx) bits that determine the state of the PWM I/O pin when it is overridden with the POVDx bit.

The POVD bits are active-low control bits. When the POVD bits are set, the corresponding POUTx bit has no effect on the PWM output. When one of the POVD bits is cleared, the output on the corresponding PWM I/O pin is determined by the state of the POUT bit. When a POUT bit is set, the PWM pin is driven to its active state. When the POUT bit is cleared, the PWM pin is driven to its inactive state.

The code shown in Example 14-7 demonstrates the PWM Output Override feature.

Example 14-7:   Code for Using the MCPWM Output Override Feature

```
/* Output Override Synchronization */

/* Output overrides via the P1OVDCON register are synchronized to the PWM
time base by setting the OSYNC bit */

PWM1CON2bits.OSYNC = 1;

/* Override control register configuration */
/* Output on the PWMxHy and PWMxLy I/O pins are controlled by the
corresponding POUTx bits in the PxOVDCON register */

P1OVDCONbits.POVD3H = 0;
P1OVDCONbits.POVD2H = 0;
P1OVDCONbits.POVD1H = 0;
P1OVDCONbits.POVD3L = 0;
P1OVDCONbits.POVD2L = 0;
P1OVDCONbits.POVD1L = 0;

/* PWM I/O pins are driven to active state by setting the corresponding bit */

P1OVDCONbits.POUT3H = 1;
P1OVDCONbits.POUT2H = 1;
P1OVDCONbits.POUT1H = 1;
P1OVDCONbits.POUT3L = 1;
P1OVDCONbits.POUT2L = 1;
P1OVDCONbits.POUT1L = 1;
```

14.16.1.1 OVERRIDE CONTROL FOR COMPLEMENTARY OUTPUT MODE

The PWM module does not allow certain overrides when a pair of PWM I/O pins are operating in Complementary PWM Output mode (PMODx = 0). The module does not allow both pins in the output pair to become active simultaneously. The high-side pin in each output pair always takes priority.

> **Note:**   Dead time insertion is still performed when PWM channels are overridden manually.

14.16.1.2 OVERRIDE SYNCHRONIZATION

If the Output Override Synchronization (OSYNC = 1) bit is set (PWMxCON2<1>), all output overrides performed using the PxOVDCON register will be synchronized to the PWM time base. Synchronous output overrides will occur at the following times:

- Edge-aligned mode when PxTMR is zero
- Center-aligned modes when PxTMR is zero
- When the value of PxTMR matches PxTPER

The override synchronization function, when enabled, can be used to avoid unwanted narrow pulses on the PWM output pins.

14.16.1.3 OUTPUT OVERRIDE EXAMPLES

Figure 14-23 shows an example of a waveform that might be generated using the PWM output override feature. This figure also shows a six-step commutation sequence for a BLDC motor. The motor is driven through a 3-phase inverter, as shown in Figure 14-24. When the appropriate rotor position is detected, the PWM outputs are switched to the next commutation state in the sequence. In this example, the PWM outputs are driven to specific logic states. The PxOVDCON register values used to generate the signals in Figure 14-23 are given in Table 14-5.

The PWM duty cycle registers can be used in conjunction with the PxOVDCON register. The duty cycle registers control the current delivered to the load, and the PxOVDCON register controls the commutation. Such an example is shown in Figure 14-24. The PxOVDCON register values used to generate the signals in Figure 14-24 are given in Table 14-6.

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Table 14-5: PWM Output Override Example #1

State	PxOVDCON<15:8>	PxOVDCON<7:0>
1	00000000b	00100100b
2	00000000b	00100001b
3	00000000b	00001001b
4	00000000b	00011000b
5	00000000b	00010010b
6	00000000b	00000110b

Figure 14-23: PWM Output Override Example #1

Note: Switching times between states 1-6 are controlled by user software. The state switch is controlled by writing a new value to the PxOVDCON register.
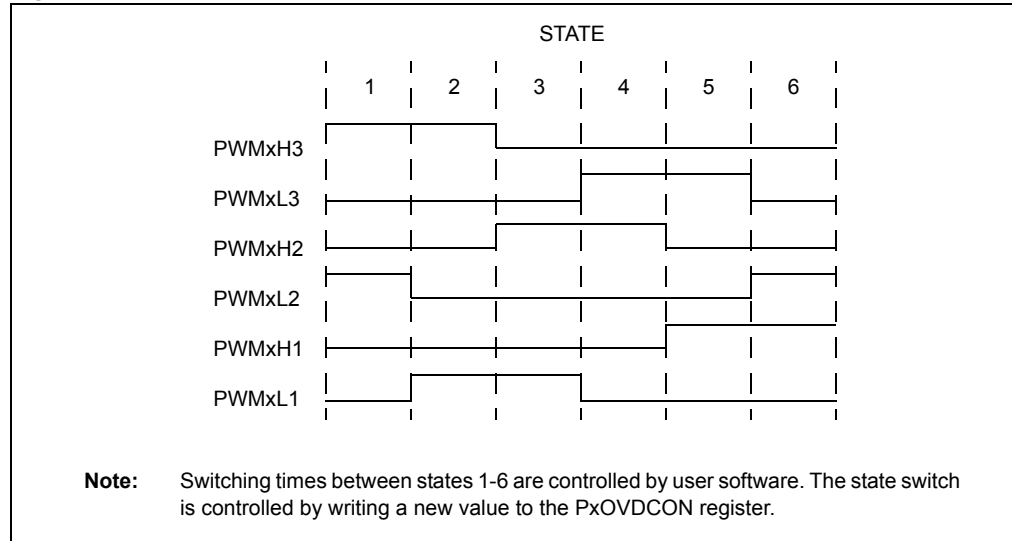
Table 14-6: PWM Output Override Example #2

State	PxOVDCON<15:8>	PxOVDCON<7:0>
1	11000011b	00000000b
2	11110000b	00000000b
3	00111100b	00000000b
4	00001111b	00000000b

Figure 14-24: PWM Output Override Example #2

Note: Switching times between states 1-4 are controlled by user software. The state switch is controlled by writing a new value to PxOVDCON. The PWM outputs are operated in the independent mode for this example.
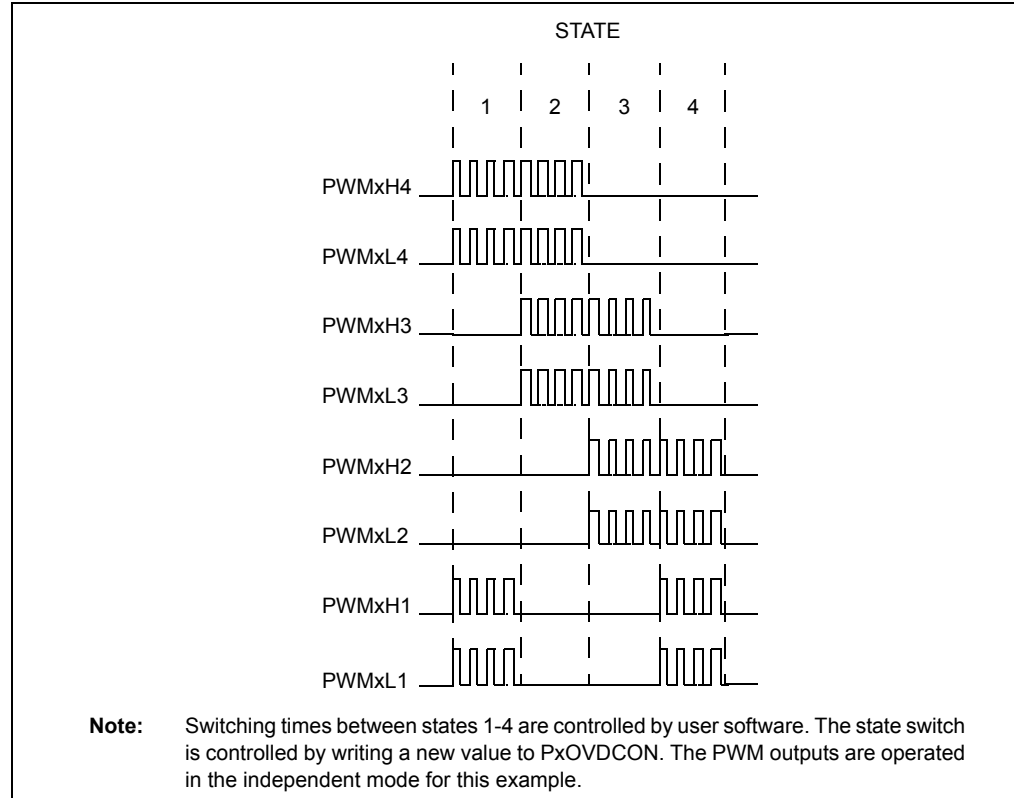
14.16.2 Special Event Trigger

The PWM module has a Special Event Trigger that allows analog-to-digital conversions to be synchronized to the PWM time base. The analog-to-digital sampling and conversion time can be programmed to occur at any point within the PWM period. The Special Event Trigger can minimize the delay between the time the analog-to-digital conversion results are acquired and the time the duty cycle value is updated.

The PWM Special Event Trigger has one SFR (PxSECMP) and four postscaler control bits (SEVOPS<3:0>) to control its operation. The PxTMR value for which a special event trigger should occur is loaded into the Special Event Compare (PxSECMP) register.

When the PWM time base is in Up/Down Counting mode, an additional control bit is required to specify the counting phase for the Special Event Trigger. The count phase is selected using the Special Event Trigger Time Base Direction (SEVTDIR) bit in the MSb of the Special Event Compare (PxSECMP<15>) register. If the SEVTDIR bit is cleared, the Special Event Trigger will occur on the upward counting cycle of the PWM time base. If the SEVTDIR bit is set, the Special Event Trigger will occur on the downward count cycle of the PWM time base. The SEVTDIR control bit has no effect unless the PWM time base is configured for Up/Down Counting mode.

The code in Example 14-8 demonstrates how to trigger an analog-to-digital conversion based on MCPWM special event generation.

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Example 14-8:   Triggering ADC Based on MCPWM Special Event Generation

```
/* Select Special Event time base direction such that trigger will occur */
/* when PWM time base is counting downwards */

P1SECMPbits.SEVTDIR = 1;

/* Select PWM Special Event Trigger Output Post scale value to 1:1 */

PWM1CON2bits.SEVOPS = 0b0000;

/* Assign special event compare value */

P1SECMPbits.SEVTCMP = 100;

/* Choose ADC1 trigger source such that MCPWM1 module stops sampling and */
/* starts conversion */

AD1CON1bits.SSRC = 0b011;
```

14.16.2.1 SPECIAL EVENT TRIGGER ENABLE

The PWM module always produces the Special Event Trigger signal. This signal may option-ally be used by the analog-to-digital module. Refer to **Section 16. "10/12-bit ADC with DMA"** for more information on using the Special Event Trigger.

14.16.2.2 SPECIAL EVENT TRIGGER POSTSCALER

The PWM Special Event Trigger has a postscaler that allows a 1:1 to 1:16 postscale ratio. The postscaler is useful when synchronized A/D conversions do not need to be performed during every PWM cycle. The postscaler is configured by writing the PWM Special Event Trigger Output Postscale Select (SEVOPS) control bits in the PWM Control Register 2 (PWMxCON2<11:8>) SFR.

The special event output postscaler is cleared on the following events:

• Any write to the Special Event Compare (PxSECMP) register
• Any device Reset

14.16.3   PWM Update Lockout

In some applications, it is important that all duty cycle and period registers be written before the new values take effect. The update disable feature allows the user application to specify when new duty cycle and period values can be used by the module. The PWM update lockout feature is enabled by setting the PWM Update Disable (UDIS) bit in the PWM Control Register 2 (PWMxCON2<0>) SFR.

The UDIS bit affects all duty cycle registers, PxDC1-PxDC4, and the PWM time base period buffer, PxTPER. To execute an update lockout, perform the following steps:

• Set the UDIS bit
• Write all duty cycle registers and PxTPER, if applicable
• Clear the UDIS bit to re-enable updates

Note:	Immediate updates must be disabled (IUE = 0) to use the PWM update lockout feature.

14.16.4   Device Emulation

The PWM module has a special feature to support the debugging environment. All enabled PWM pins can be optionally tri-stated when the hardware emulator or debugger device is halted to examine memory contents. Install pull-up and pull-down resistors to ensure that the PWM outputs are driven to the correct state when device execution is halted.

The function of the PWM output pins at a device Reset and the output pin polarity is determined by three device configuration bits (see **14.10 "PWM Output State Control"**). Use a hardware debugger or emulation tool to change the values of these configuration bits. Please refer to the tool's technical documentation for more information.

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Motor Control PWM

14.17   OPERATION IN POWER SAVE MODES

14.17.1   PWM Operation in Sleep mode

When the device enters Sleep mode, the system clock is disabled. Since the clock for the PWM time base is derived from the system clock source (T_{CY}), that clock will also be disabled. All enabled PWM output pins will be frozen in the output states that were in effect prior to entering Sleep mode.

If the PWM module is used to control a load in a power application, the PWM module outputs must be placed into a safe state before executing the PWRSAV instruction. Depending on the application, the load may begin to consume excessive current when the PWM outputs are frozen in a particular output state. For example, the PxOVDCON register can be used to manually turn off the PWM output pins, as shown in Example 14-9.

Example 14-9:   Manually Placing PWM Pins Into An Inactive State

```
; This code example drives all PWM1 pins to the inactive state
; before executing the PWRSAV instruction.

    CLR         P1OVDCON        ; Force all PWM outputs inactive
    PWRSAV      #0              ; Put the device in Sleep mode
    SETM.B      P1OVDCONH       ; Set POVD bits when device wakes.
```

The Fault A and Fault B input pins, if enabled to control the PWM pins via the PxFLTACON and PxFLTBCON registers, continue to function normally when the device is in Sleep mode. If one of the fault pins is driven low while the device is in Sleep mode, the PWM outputs are driven to the programmed Fault states in the PxFLTACON and PxFLTBCON registers.

The fault input pins can also wake the CPU from Sleep mode. If the fault interrupt enable bit is set (FLTxAIE = 1 or FLTxBIE = 1), the device will wake from Sleep mode when the fault pin is driven low. If the fault pin interrupt priority is greater than the current CPU priority, program execution starts at the fault pin interrupt vector location upon wake-up. Otherwise, execution continues from the next instruction following the PWRSAV instruction.

14.17.2   PWM Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The PWM module can optionally continue to operate in Idle mode. The PWM Time Base Stop in Idle Mode (PTSIDL) bit in the PWM Time Base Control (PxTCON<13>) register determines whether the PWM module stops in Idle mode or continues to operate normally.

If PTSIDL = 0, the module operates normally when the device enters Idle mode. The PWM time base interrupt, if enabled, can be used to wake the device from Idle mode. If the PWM Time Base Interrupt Enable (PTIE) bit is set (PTIE = 1), the device will wake from Idle mode when the PWM time base interrupt is generated. If the PWM time base interrupt priority is greater than the current CPU priority, program execution starts at the PWM interrupt vector location upon wake-up. Otherwise, execution will continue from the next instruction following the PWRSAV instruction.

If PTSIDL = 1, the module stops in Idle mode. If the PWM module is programmed to stop in Idle mode, the operation of the PWM outputs and fault input pins is the same as the operation in Sleep mode. (See **14.17.1 "PWM Operation in Sleep mode"** for details.)

Table 14-7: **Registers Associated with 8-Output PWM1 Module**

Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset
IFS3	008A	FLT1AIF	—	—	—	—	—	PWM1IF	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IFS4	008C	—	—	—	FLT2BIF	—	FLT2AIF	PWM2IF	—	—	—	—	—	—	—	—	FLT1BIF	0000 0000 0000 0000
IEC3	009A	FLT1AIE	—	—	—	—	—	PWM1IE	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IEC4	009C	—	—	—	FLT2BIE	—	FLT2AIE	PWM2IE	—	—	—	—	—	—	—	—	FLT1BIE	0000 0000 0000 0000
IPC14	00C0	—	—	—	—	—	—	—	—	—	PWM1IP<2:0>			—	—	—	—	0000 0000 0000 0000
IPC15	00C2	—	FLT1AIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IPC16	00C4	—	—	—	—	—	—	—	—	—	—	—	—	—	FLT1BIP<2:0>			0000 0000 0000 0000
P1TCON	01C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
P1TMR	01C2	PTDIR	PWM Time Base register															0000 0000 0000 0000
P1TPER	01C4	—	PWM Time Base Period register															0111 1111 1111 1111
P1SECMP	01C6	SEVTDIR	PWM Special Event Compare register															0000 0000 0000 0000
PWM1CON1	01C8	—	—	—	—	PMOD4	PMOD3	PMOD2	PMOD1	PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L	0000 0000 0000 0000
PWM1CON2	01CA	—	—	—	—	SEVOPS<3:0>				—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
P1DTCON1	01CC	DTBPS<1:0>		Dead Time B Value register						DTAPS<1:0>		Dead Time A Value register						0000 0000 0000 0000
P1DTCON2	01CE	—	—	—	—	—	—	—	—	DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
P1FLTACON	01D0	FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1	0000 00-0 0000 0000
P1FLTBCON	01D2	FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	—	—	—	FBEN4	FBEN3	FBEN2	FBEN1	0000 00-0 0000 0000
P1OVDCON	01D4	POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	1111 1111 0000 0000
P1DC1	01D6	PWM Duty Cycle #1 register																0000 0000 0000 0000
P1DC2	01D8	PWM Duty Cycle #2 register																0000 0000 0000 0000
P1DC3	01DA	PWM Duty Cycle #3 register																0000 0000 0000 0000
P1DC4	01DC	PWM Duty Cycle #4 register																0000 0000 0000 0000

Legend: u = uninitialized bit, — = unimplemented, read as '0'
Note 1: Shaded register and bit locations are not implemented for the 8-output PWM1 module.

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Table 14-8: **Registers Associated with 2-Output PWM2 Module**

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
IFS3	008A	FLT1AIF	—	—	—	—	—	PWM1IF	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IFS4	008C	—	—	—	FLT2BIF	—	FLT2AIF	PWM2IF	—	—	—	—	—	—	—	—	FLT1BIF	0000 0000 0000 0000
IEC3	009A	FLT1AIE	—	—	—	—	—	PWM1IE	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IEC4	009C	—	—	—	FLT2BIE	—	FLT2AIE	PWM2IE	—	—	—	—	—	—	—	—	FLT1BIE	0000 0000 0000 0000
IPC18	00C8	—	—	—	—	—	FLT2AIP<2:0>			—	PWM2IP<2:0>			—	—	—	—	0000 0000 0000 0000
IPC19	00CA	—	—	—	—	—	—	—	—	—	—	—	—	—	FLT2BIP<2:0>			0000 0000 0000 0000
P2TCON	05C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
P2TMR	05C2	PTDIR	PWM Timer Count Value Register															0000 0000 0000 0000
P2TPER	05C4	—	PWM Time Base Period Register															0000 0000 0000 0000
P2SECMP	05C6	SEVTDIR	PWM Special Event Compare Register															0000 0000 0000 0000
PWM2CON1	05C8	—	—	—	—	—	—	—	PMOD1	—	—	—	PEN1H	—	—	—	PEN1L	0000 0000 1111 1111
PWM2CON2	05CA	—	—	—	—	SEVOPS<3:0>				—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
P2DTCON1	05CC	DTBPS<1:0>		DTB<5:0>						DTAPS<1:0>		DTA<5:0>						0000 0000 0000 0000
P2DTCON2	05CE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTS1A	DTS1I	0000 0000 0000 0000
P2FLTACON	05D0	—	—	—	—	—	—	FAOV1H	FAOV1L	FLTAM	—	—	—	—	—	—	FAEN1	0000 0000 0000 0000
P2OVDCON	05D4	—	—	—	—	—	—	POVD1H	POVD1L	—	—	—	—	—	—	POUT1H	POUT1L	1111 1111 0000 0000
P2DC1	05D6	PWM Duty Cycle #1 Register																0000 0000 0000 0000

Legend: u = uninitialized bit, — = unimplemented, read as '0'
Note 1: Shaded register and bit locations are not implemented for the 2-output PWM2 module.

14.18   RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the MCPWM module include the following:

Title	Application Note #
PIC18CXXX/PIC16CXXX Servomotor	AN696
Using the dsPIC30F for Sensorless BLDC Control	AN901
Using the dsPIC30F for Vector Control of an ACIM	AN908
Sensored BLDC Motor Control Using dsPIC30F2010	AN957
An Introduction to AC Induction Motor Control Using the dsPIC30F MCU	AN984
Sinusoidal Control of PMSM Motors with dsPIC30F DSC	AN1017
Getting started with the BLDC Motors and dsPIC30F Devices	GS001
Measuring speed and position with the QEI Module	GS002
Driving ACIM with the dsPIC DSC MCPWM Module	GS004
Using the dsPIC30F Sensorless Motor Tuning Interface	GS005

> **Note:**   Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F family of devices.

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Motor Control PWM

14.19   REVISION HISTORY

Revision A (February 2007)

This is the initial released revision of this document.

Revision B (February 2007)

Minor edits throughout document.