Section 8. Reset

HIGHLIGHTS

This section of the manual contains the following major topics:

8.1 INTRODUCTION

The Reset module combines all reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Reset
- CM: Configuration Mismatch Reset (This reset source is not available on all devices. Refer to the specific device data sheet for details.)
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

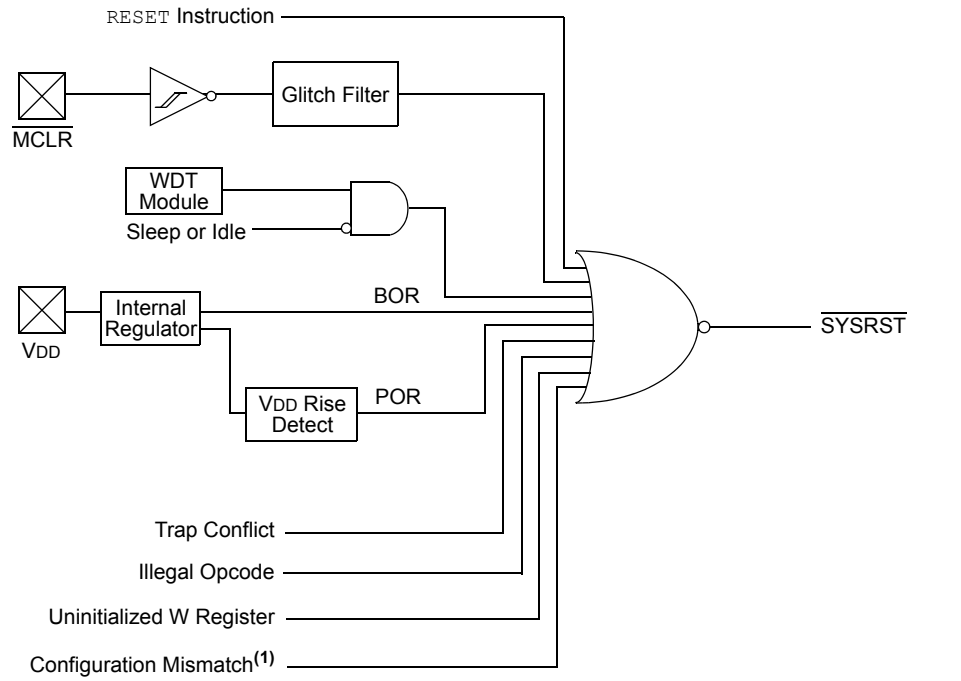
A simplified block diagram of the Reset module is shown in Figure 8-1. Any active source of reset will make the SYSRST signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known reset state, while some are unaffected.

Note:	Refer to the specific peripheral section or **Section 2. "CPU"** in the "*dsPIC33F Family Reference Manual*" for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of reset (see Register 8-1). A POR clears all bits except for the POR and BOR bits (RCON<1:0>), which are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset.

The RCON register also contains bits associated with the Watchdog Timer and device power saving states. For more information, refer to **Section 9. "WDT and Power Saving Modes"**.

Figure 8-1: Reset System Block Diagram



Note 1: The configuration mismatch is not available on all devices. Refer to the specific device data sheet for details.

Register 8-1: RCON: Reset Control Register(1)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM(2)	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(3)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or an uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W register Reset has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit(2)
1 = A configuration mismatch Reset has occurred
0 = A configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(3)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: The configuration mismatch reset flag is not available on all devices. (Refer to the specific device data sheet.)

3: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

Register 8-1: RCON: Reset Control Register(1) (Continued)

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-up Reset has occurred
0 = A Power-up Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: The configuration mismatch reset flag is not available on all devices. (Refer to the specific device data sheet.)

3: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

8.2 SYSTEM RESET

The dsPIC33F family of devices have two types of Reset:

- Cold Reset
- Warm Reset

A cold Reset is the result a of Power-on Reset (POR) or Brown-out Reset (BOR). On a cold Reset, the FNOSC configuration bits in the FOSC device configuration register select the device clock source.

A warm Reset is the result of all other reset sources, including the RESET instruction. On a warm Reset, the device will continue to operate from the current clock source as indicated by the Current Oscillator Selection (COSC<2:0>) bits in the Oscillator Control (OSCCON<14:12>) register.

The device is kept in a reset state until the system power supplies have stabilized at appropriate levels and the oscillator clock is ready. The sequence in which this occurs is detailed below and shown in Figure 8-2.

1. **POR Reset:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay TPOR has elapsed.
2. **BOR Reset:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay TBOR has elapsed. The delay TBOR ensures the voltage regulator output becomes stable.
3. **PWRT Timer:** The programmable power-up timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay TPWRT ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay TPWRT has elapsed, the $\overline{\text{SYSRST}}$ becomes inactive, which in turn enables the selected oscillator to start generating clock cycles.
4. **Oscillator Delay:** The total delay for the clock to be ready for various clock source selections is given in Table 8-1. Refer to **Section 7. "Oscillator"** for more information.
5. When the oscillator clock is ready, the processor begins execution from location 0x000000. The user application programs a GOTO instruction at the reset address which redirects program execution to the appropriate start-up routine.
6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay TFSCM has elapsed.

Table 8-1: Oscillator Delay

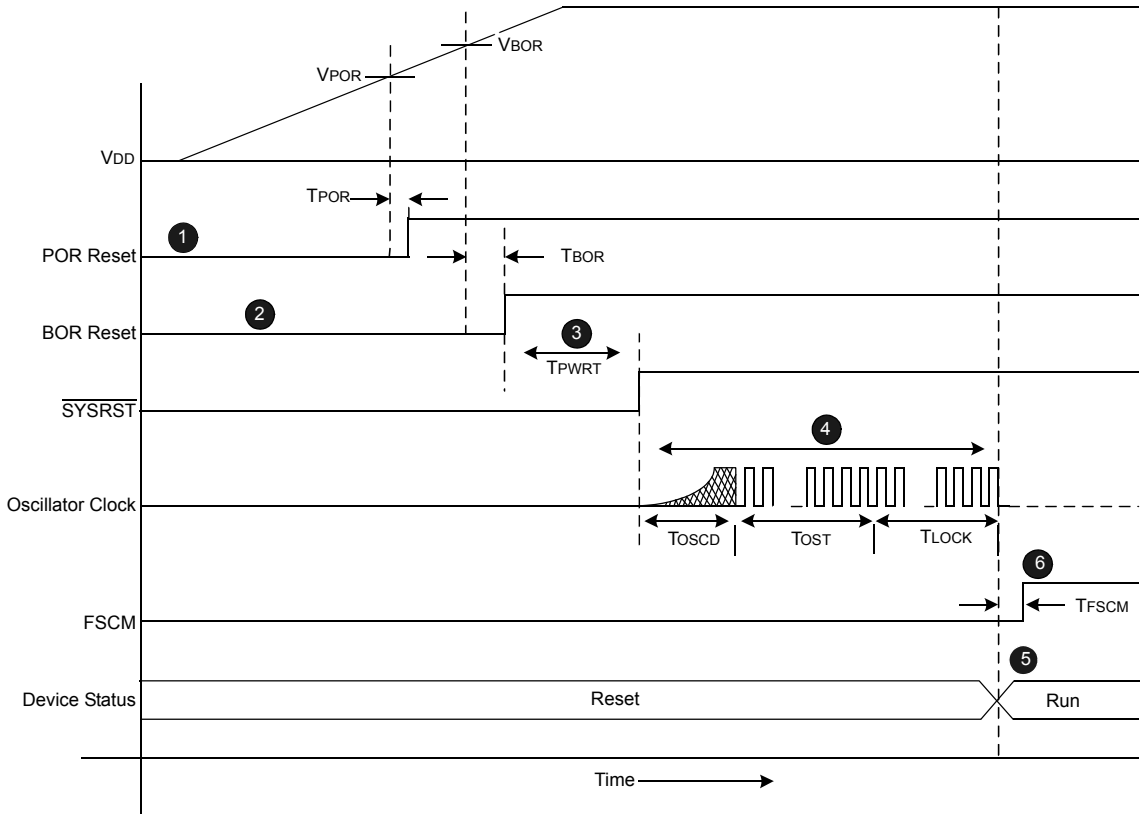
Oscillator Mode	Oscillator Startup Delay	Oscillator Startup Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	TOSCD	—	—	TOSCD
FRCPLL	TOSCD	—	TLOCK	TOSCD + TLOCK
XT	TOSCD	TOST	—	TOSCD + TOST
HS	TOSCD	TOST	—	TOSCD + TOST
EC	—	—	—	—
XTPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
HSPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
ECPLL	—	—	TLOCK	TLOCK
SOSC	TOSCD	TOST	—	TOSCD + TOST
LPRC	TOSCD	—	—	TOSCD

Note 1: TOSCD = Oscillator Start-up Delay (1.1 μs max for FRC, 70 μs max for LPRC). Crystal Oscillator start-up times vary with crystal characteristics, load capacitance, etc.

2: TOST = Oscillator Start-up Timer Delay (1024 oscillator clock periods). For example, TOST = 102.4 μs for a 10 MHz crystal and TOST = 32 ms for a 32 kHz crystal.

3: TLOCK = PLL lock time (1.5 ms nominal), if the PLL is enabled.

Figure 8-2: System Reset Timing



1. **POR Reset:** A POR circuit holds the device in Reset when the power supply is turned on. The POR circuit is active until VDD crosses the VPOR threshold and the delay Tpor has elapsed.
2. **BOR Reset:** The on-chip voltage regulator has a BOR circuit that keeps the device in Reset until VDD crosses the VBOR threshold and the delay TBOR has elapsed. The delay TBOR ensures the voltage regulator output becomes stable.
3. **PWRT Timer:** The programmable power-up timer continues to hold the processor in Reset for a specific period of time (TPWRT) after a BOR. The delay TPWRT ensures that the system power supplies have stabilized at the appropriate level for full-speed operation. After the delay TPWRT has elapsed, the SYSRST becomes inactive, which in turn enables the selected oscillator to start generating clock cycles.
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6. The Fail-Safe Clock Monitor (FSCM), if enabled, begins to monitor the system clock when the system clock is ready and the delay TFSCM has elapsed.

Table 8-2: Reset Characteristics

Symbol	Parameter	Value
VPOR	POR threshold	1.8V nominal
TPOR	POR extension time	30 μs maximum
VBOR	BOR threshold	2.5V nominal
TBOR	BOR extension time	100 μs maximum
TPWRT	Programmable power-up time delay	0-128 ms nominal
TFSCM	Fail-safe Clock Monitor delay	900 μs maximum

Note: When the device exits the reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges, otherwise the device may not function correctly. The user application must ensure that the delay between the time at which power is first applied and the time the SYSRST becomes inactive is long enough to get all operating parameters within specification.

8.2.1 Power-on Reset (POR)

A Power-on Reset (POR) circuit ensures the device is reset from power-on. The POR circuit is active until VDD crosses the VPOR threshold and the delay TPOR has elapsed. The delay TPOR ensures the internal device bias circuits become stable.

The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR. Refer to the “Electrical Characteristics” section of the specific device data sheet for details.

The POR status (POR) bit in the Reset Control (RCON<0>) register is set to indicate the Power-on Reset.

8.2.2 Brown-out Reset (BOR) and Power-up Timer (PWRT)

The on-chip regulator has a Brown-out Reset (BOR) circuit that resets the device when the VDD is too low (VDD < VBOR) for proper device operation. The BOR circuit keeps the device in Reset until VDD crosses the VBOR threshold and the delay TBOR has elapsed. The delay TBOR ensures the voltage regulator output becomes stable.

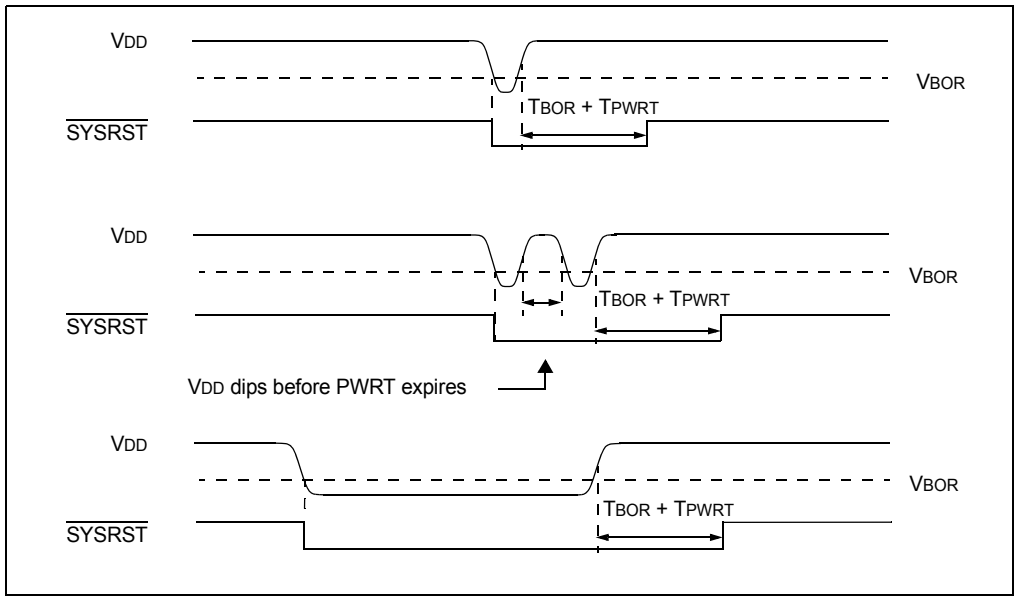
The BOR status (BOR) bit in the Reset Control (RCON<1>) register is set to indicate the Brown-out Reset.

The device will not run at full speed after a BOR as the VDD must rise to acceptable levels for full-speed operation. The PWRT provides a power-up time delay (TPWRT) to ensure that the system power supplies have stabilized at the appropriate levels for full-speed operation before the $\overline{\text{SYSRST}}$ is released.

The power-up timer delay (TPWRT) is programmed by the Power-on Reset Timer Value Select (FPWRT<2:0>) bits in the POR Configuration (FPOR<2:0>) register, which provide eight settings (from 0 ms to 128 ms). Refer to **Section 25. “Device Configuration”** for further details.

Figure 8-3 shows the typical brown-out scenarios. The reset delay (TBOR + TPWRT) is initiated each time VDD rises above the VBOR trip point.

Figure 8-3: Brown-out Situations



8.2.3 External Reset (EXTR)

The external reset is generated by driving the MCLR pin low. The MCLR pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to the “Electrical Characteristics” section of the specific device data sheet for minimum pulse width specifications. The External Reset (MCLR) Pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the MCLR Reset.

8.2.3.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate reset signals to Reset multiple devices in the system. This external Reset signal can be directly connected to the MCLR pin to Reset the device when the rest of the system is Reset.

8.2.3.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to Reset the device, the external reset pin (MCLR) should be tied directly or resistively to VDD. In this case, the MCLR pin will not be used to generate a Reset. The external reset pin (MCLR) does not have an internal pull-up and must not be left unconnected.

8.2.4 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert SYSRST, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will remain in effect. SYSRST is released at the next instruction cycle, and the reset vector fetch will commence.

The Software Reset (Instruction) Flag (SWR) bit in the Reset Control (RCON<6>) register is set to indicate the software Reset.

8.2.5 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog time-out occurs, the device will asynchronously assert SYSRST. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out Flag (WDTO) bit in the Reset Control (RCON<4>) register is set to indicate the Watchdog Reset. Refer to **Section 9. “Watchdog Timer and Power Saving Modes”** for more information on Watchdog Reset.

8.2.6 Trap Conflict Reset

If a lower-priority hard trap occurs while a higher-priority trap is being processed, a hard trap conflict Reset occurs. The hard traps include exceptions of priority level 13 through level 15, inclusive. The address error (level 13) and oscillator error (level 14) traps fall into this category.

The Trap Reset Flag (TRAPR) bit in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 6. “Interrupts”** for more information on trap conflict Resets.

8.2.7 Configuration Mismatch Reset

To maintain the integrity of the peripheral pin select control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change occurs in any of the registers (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset occurs.

The Configuration Mismatch Flag (CM) bit in the Reset Control (RCON<9>) register is set to indicate the configuration mismatch Reset. Refer to **Section 30. “I/O Ports with Peripheral Pin Select”** for more information on the configuration mismatch Reset.

Note:	The configuration mismatch feature and associated reset flag are not available on all devices. (Refer to the specific device data sheet.)

8.2.8 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag (IOPUWR) bit in the Reset Control (RCON<14>) register is set to indicate the illegal condition device Reset.

8.2.8.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The illegal opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the illegal opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

8.2.8.2 UNINITIALIZED W REGISTER RESET

Any attempts to use the uninitialized W register as an address pointer will Reset the device. The W register array (with the exception of W15) is cleared during all resets and is considered uninitialized until written to.

8.2.8.3 SECURITY RESET

If a Program Flow Change (PFC) or Vector Flow Change (VFC) targets a restricted location in a protected segment (Boot and Secure Segment), that operation will cause a security Reset.

The PFC occurs when the Program Counter is reloaded as a result of a Call, Jump, Computed Jump, Return, Return from Subroutine, or other form of branch instruction.

The VFC occurs when the Program Counter is reloaded with an Interrupt or Trap vector.

Refer to **Section 23. "CodeGuard™ Security"** for more information on Security Reset.

8.3 USING THE RCON STATUS BITS

The user application can read the Reset Control (RCON) register after any device Reset to determine the cause of the reset.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 8-3 provides a summary of the reset flag bit operation.

Table 8-3: Reset Flag Bit Operation

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR, BOR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access or Security Reset	POR, BOR
CM (RCON<9>)	Configuration Mismatch	POR, BOR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	`RESET` instruction	POR, BOR
WDTO (RCON<4>)	WDT time-out	`PWRSAV` instruction, `CLRWDT` instruction, POR, BOR
SLEEP (RCON<3>)	`PWRSAV #SLEEP` instruction	POR, BOR
IDLE (RCON<2>)	`PWRSAV #IDLE` instruction	POR, BOR
BOR (RCON<1>)	POR, BOR	
POR (RCON<0>)	POR	

Note: All Reset flag bits can be set or cleared by the user software.

8.4 DEVICE START-UP TIME LINES

Figure 8-4 shows the device start-up time line when a crystal oscillator is used as the system clock.

The power-up timer (PWRT) keeps the device in the Reset state for the user application-selected power-up time delay (TPWRT) after a Brown-out Reset to ensure that VDD rises to an acceptable level.

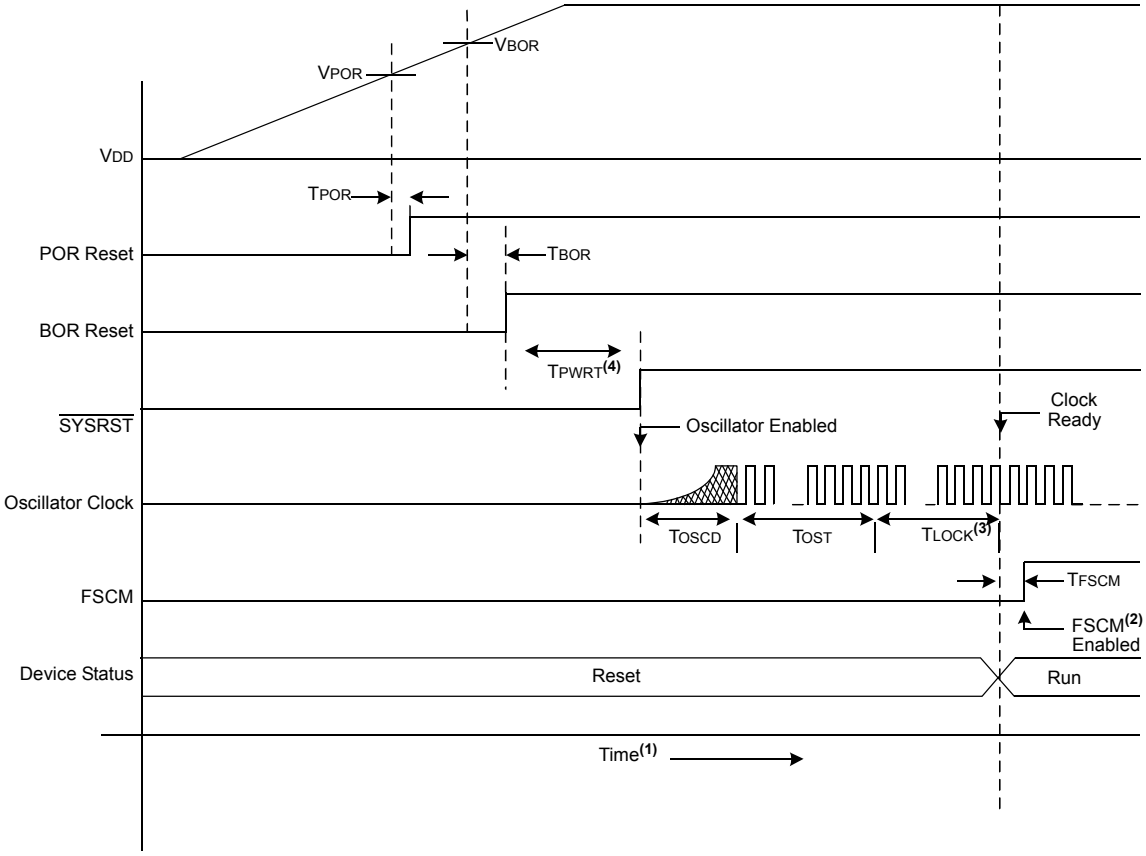
The crystal oscillator is enabled after $\overline{\text{SYSRST}}$ is released. Once enabled, the crystal oscillator takes a finite amount of time to start oscillating. This delay is denoted as TOSCD.

To ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, a simple 10-bit counter counts 1024 oscillator clock cycles before releasing the oscillator clock. This time period is denoted as TOST. For example, TOST is 102.4 μs for a 10 MHz crystal.

If the primary oscillator is used with the PLL, an additional delay is required for PLL locking. The device begins to execute after the clock is ready.

The Fail-safe clock monitor (FSCM), if enabled, begins to monitor the system clock for activity when the system clock is ready and the delay TFSCM has elapsed.

Figure 8-4: Device Start-up Timing for Crystal Oscillator



Note 1: Delay times shown are not drawn to scale.

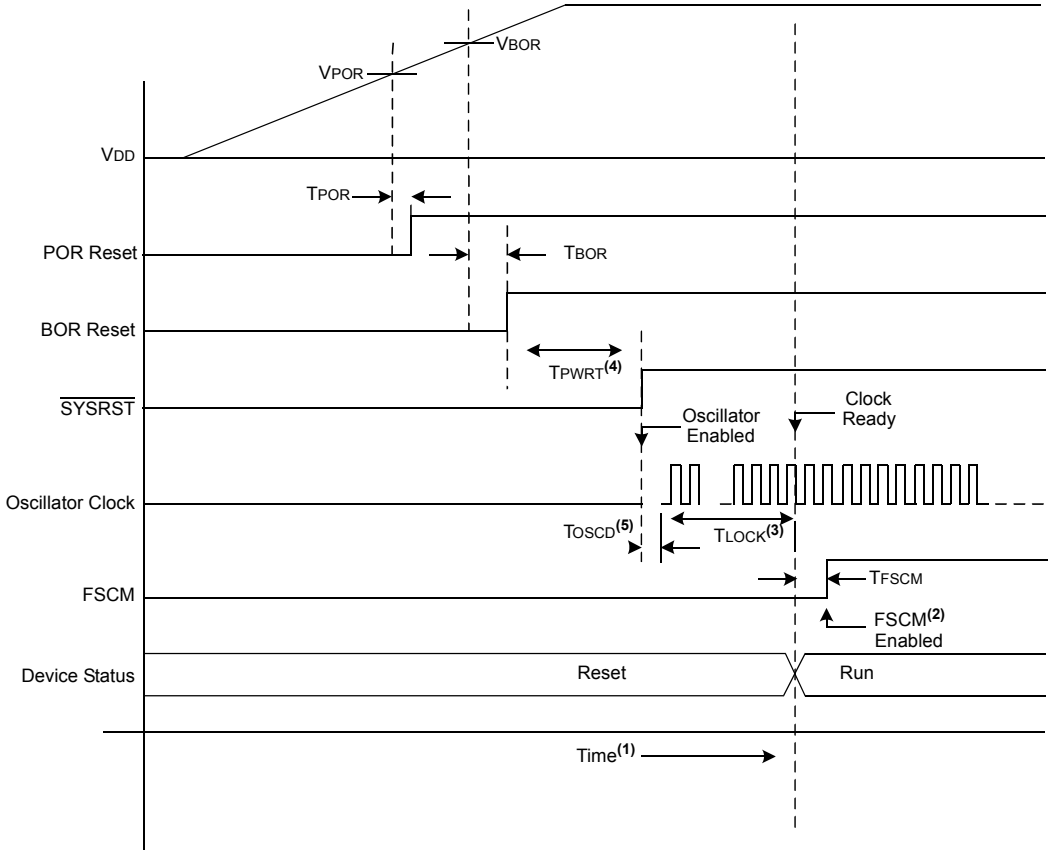
2: FSCM, if enabled, monitors the system clock at the expiration of the TFSCM delay after the device starts running.

3: TLOCK is not inserted when the PLL is disabled.

4: TPWRT is not inserted when the PWRT delay is not enabled.

Figure 8-5 shows the device start-up time line when the FRC oscillator is used as the system clock. The FRC oscillator exhibits little start-up delay (TOSCD), so the oscillator start-up time (TOST) is not required.

Figure 8-5: Device Start-up Timing for FRC Oscillator



Note 1: Delay times shown are not drawn to scale.

2: FSCM, if enabled, monitors the system clock at the expiration of the TFSCM delay after the device starts running.

3: TLOCK is not inserted when the PLL is disabled.

4: TPWRT is not inserted when the PWRT delay is not enabled.

5: TOSCD for the FRC is 1.1 µs.

8.5 SPECIAL FUNCTION REGISTER RESET STATES

Most of the special function registers (SFRs) associated with the dsPIC33F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their reset values are specified in the appropriate sections of this manual.

The reset value for each SFR does not depend on the type of reset, with the exception of two registers. The reset value for the Reset Control register, RCON, will depend on the type of device Reset. The reset value for the Oscillator Control register, OSCCON, will depend on the type of reset and the programmed values of the oscillator configuration bits in the FOSC Device Configuration register.

8.6 DESIGN TIPS

Question 1: ***How do I use the RCON register?***

Answer: The initialization code after a device Reset should examine the RCON register and confirm the source of the reset. In certain applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All reset status bits in the RCON register should be cleared after reading them to ensure the RCON value will provide meaningful results after the next device Reset.

Question 2: ***The BOR module does not have the programmable trip points that my application needs. How can I work around this?***

Answer: The BOR circuitry is used to avoid violation of the V/F specification of the device. In many devices, the minimum voltage for full-speed operation is much higher than in dsPIC33F devices. Therefore, in such devices, a programmable BOR circuit is needed to provide the multiple speed option. The dsPIC33F devices, however, support full-speed operation at a much lower voltage, so the simple BOR module is enough. If the device operating voltage drops to a value where full-speed operation isn't possible, then BOR is asserted. If the device is in a non-BOR state, then full-speed operation is valid.

Question 3: ***I initialized a W register with a 16-bit address, but the device appears to reset when I attempt to use the register as an address.***

Answer: Because all data addresses are 16-bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two-byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an address pointer in an operation.

8.7 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Reset module include the following:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F Family of devices.

8.8 REVISION HISTORY

Revision A (February 2007)

This is the initial released revision of this document.

Revision B (February 2007)

Minor edits throughout document.