Section 36. Programmable Cyclic Redundancy Check (CRC)

HIGHLIGHTS

This section of the manual contains the following major topics:

36.1 INTRODUCTION

The programmable Cyclic Redundancy Check (CRC) module in dsPIC33F devices is a software configurable CRC checksum generator. The checksum is a unique number associated with a message or a particular block of data containing several bytes. Whether it is a data packet for communication, or a block of data stored in memory, a piece of information like the checksum helps to validate it before processing.

The simplest way to calculate a checksum is to add together all the data bytes present in the message. However, this method of checksum calculation fails when the message is modified by inverting or swapping groups of bytes. Also, it fails when null bytes are added anywhere in the message.

The CRC is a more complicated, but robust, error checking algorithm. The main idea behind the CRC algorithm is to treat a message as a binary bit stream and divide it by a fixed binary number. The remainder from this division is considered as the checksum. Like in division, the CRC calculation is also an iterative process. The only difference is that these operations are done on modulo arithmetic based on mod2. For example, division is replaced with the XOR operation (i.e., subtraction without carry). The CRC algorithm uses the term polynomial to perform all of its calculations. The divisor, dividend and remainder that are represented by numbers, are termed as polynomials with binary coefficients. For example, as shown in Equation 36-1, the number 19h (`11001`) is represented as:

Equation 36-1:

$$(1 \bullet x^4) + (1 \bullet x^3) + (0 \bullet x^2) + (0 \bullet x^1) + (1 \bullet x^0)$$

or, in simpler terms:

$$x^4 + x^3 + x^0$$

To perform the CRC calculation, a suitable divisor is first selected. This divisor is called the generator polynomial. Since the CRC is used to detect errors, a suitable generator polynomial of suitable length needs to be chosen for a given application, as each polynomial has different error detection capabilities. Some polynomials are widely used for many applications; however, a discussion of the error detecting capabilities of any particular polynomial is beyond the scope of this reference section.

The CRC calculation is an iterative process and consumes considerable CPU bandwidth when implemented in a software. The software configurable CRC hardware module in dsPIC33F devices facilitates a fast CRC checksum calculation with minimal software overhead.

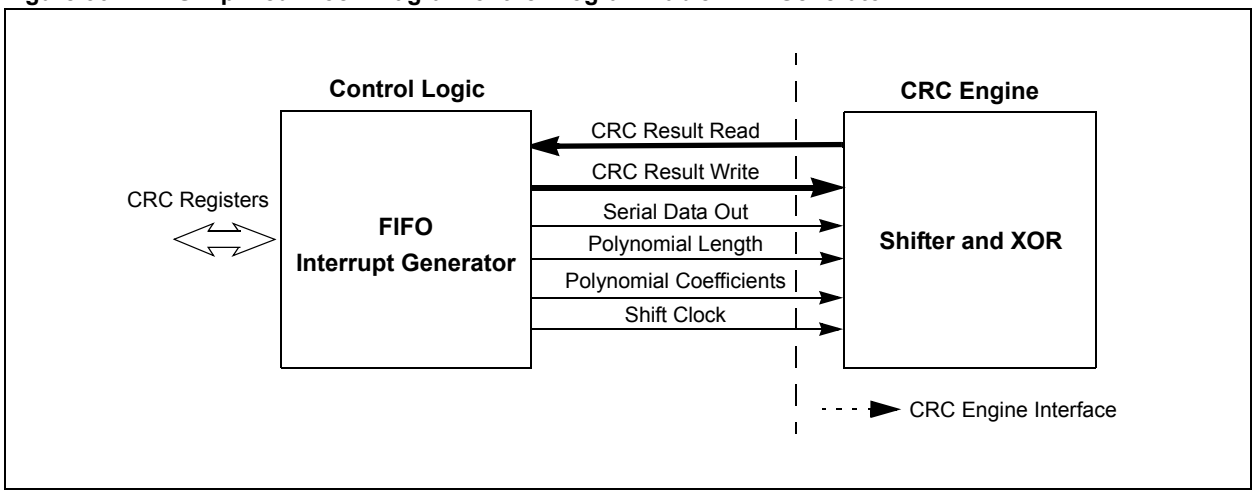
The primary features of the programmable CRC module are:

- Programmable bit length for the CRC generator polynomial (up to 16-bit length)
- Programmable CRC generator polynomial
- Interrupt output
- 8-deep, 16-bit or 16-deep, 8-bit FIFO for data input

36.2 MODULE OVERVIEW

The programmable CRC module in dsPIC33F devices is organized into two logical blocks: the Control Logic and the CRC Engine. The control logic incorporates a register interface, a FIFO, an interrupt generator and a CRC engine interface. The CRC engine incorporates a CRC calculator, which is implemented using a serial shifter with an XOR function. A simplified block diagram of the CRC module is shown in Figure 36-1.

Figure 36-1: Simplified Block Diagram of the Programmable CRC Generator



36.3 CRC REGISTERS

This section describes the registers associated with the CRC module. These registers are mapped onto the data RAM space as Special Function Registers (SFRs) in dsPIC33F devices:

- **CRCCON: CRC Control Register**
- **CRCXOR: CRC XOR Register**
- **CRCDAT: CRC Data Register**
- **CRCWDAT: Write CRC Shift Register**

The CRCCON register (Register 36-1) is the primary control and status register for the module. The CRCXOR register (Register 36-2) is used to define the generator polynomial by selecting the terms to be used. The CRCDAT and CRCWDAT registers are buffers for data input and result output, respectively.

Register 36-1: CRCCON: CRC Control Register

U-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
—	—	CSIDL	VWORD<4:0>				
bit 15							bit 8

R-0	R-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CRCFUL	CRCMPT	—	CRCGO	PLEN<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-8 **VWORD<4:0>:** FIFO Pointer Value bits
Indicates the number of valid words or bytes in the FIFO. Has a maximum value of 8 when PLEN<3:0> is greater than 7, or a value of 16 when PLEN<3:0> is less than or equal to 7.

bit 7 **CRCFUL:** FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **Unimplemented:** Read as '0'

bit 4 **CRCGO:** Start CRC bit
1 = Start CRC serial shifter
0 = CRC serial shifter turned off

bit 3-0 **PLEN<3:0>:** Polynomial Length bits
Generator Polynomial Length = Value of PLEN<3:0> plus 1

Register 36-2: CRCXOR: CRC XOR Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **X<15:1>:** XOR of Polynomial Term n Enable bits
1 = Include (XOR) the n^{th} term (x^n) in the polynomial
0 = Do not include x^n in the polynomial

bit 0 **Unimplemented:** Read as '0'

36.4 CRC ENGINE

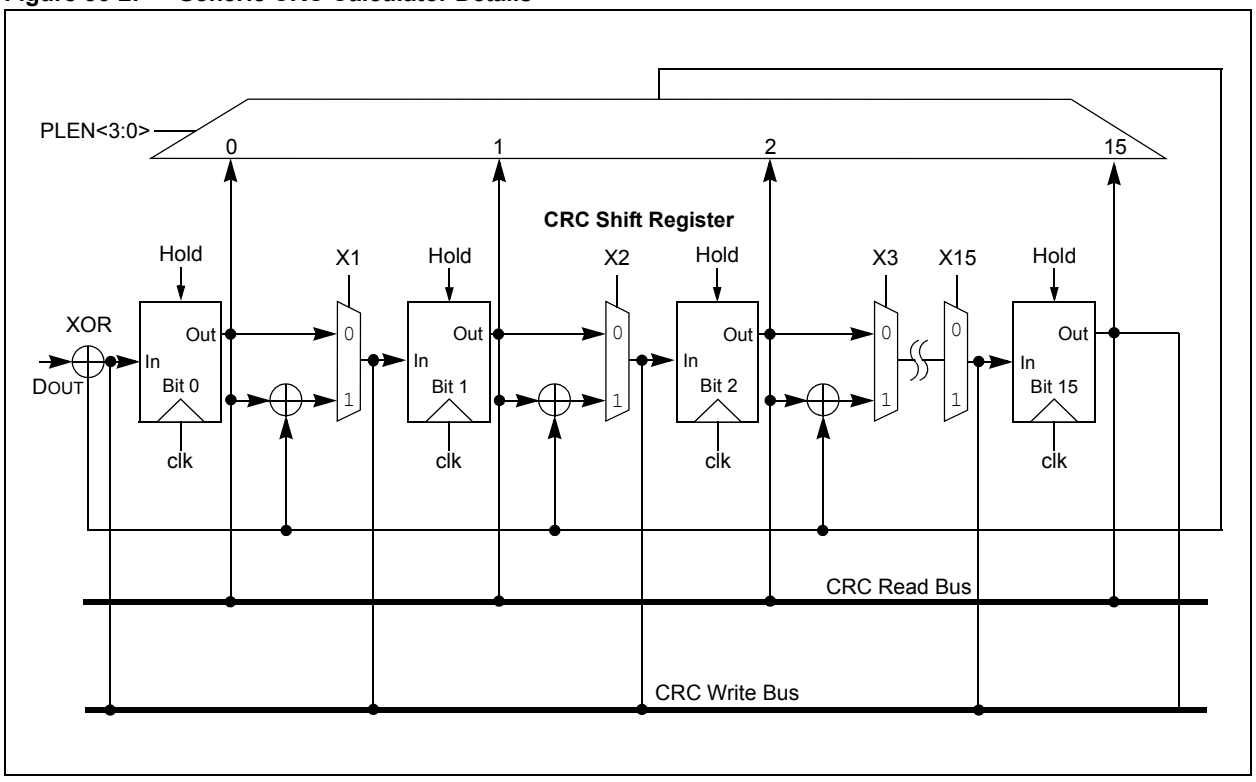
36.4.1 Generic CRC Engine

The CRC engine is a serial shifting CRC calculator with feedforward and feedback points, and is configurable through multiplexor settings. The topology of a generic CRC calculator is shown in Figure 36-2.

The CRC algorithm uses a simplified form of arithmetic process, using the XOR boolean operation instead of binary division. The coefficients of the generator polynomial are programmed with the CRCXOR<15:1> bits. Writing a '1' into a location enables an XOR of that element in the polynomial. The length of the polynomial is programmed using the Polynomial Length (PLEN<3:0>) bits in the CRC Control register (CRCCON<3:0>). The PLEN<3:0> value signals the length of the polynomial, and switches a multiplexor to indicate the tap from which the feedback originated.

The result of the CRC calculation is obtained by reading the holding registers through the CRC read bus. A direct write path to the CRC Shift registers is also provided through the CRC write bus. This path is accessed by the CPU through the Write CRC Shift Register (CRCWDAT) register.

Figure 36-2: Generic CRC Calculator Details



36.4.2 Software Configuration of the CRC Engine

The CRC engine needs to be properly configured in software for a given generator polynomial. The generator polynomial is a hexadecimal number with 'n' bits. The Most Significant bit (MSb) is represented as x^n and the Least Significant bit (LSb) is represented as x^1. The MSb is always assumed to be '1'. The x^0 coefficient is omitted and understood to be '1'. Therefore, only the coefficients of x^{n-1} to x^1 need to be programmed in the CRCXOR register.

Consider a specific CRC polynomial as an example:

Equation 36-2:

$$x^{16} + x^{12} + x^5 + 1$$

The length of the polynomial is represented by the order of the highest power of the polynomial. Therefore, the above polynomial is of a 16-bit length. Some of its coefficients are zeros and some are ones.

To program this polynomial into a CRC generator, the PLEN bits (CRCCON<3:0>) and CRCXOR<15:1> bits should be programmed as shown in Table 36-1.

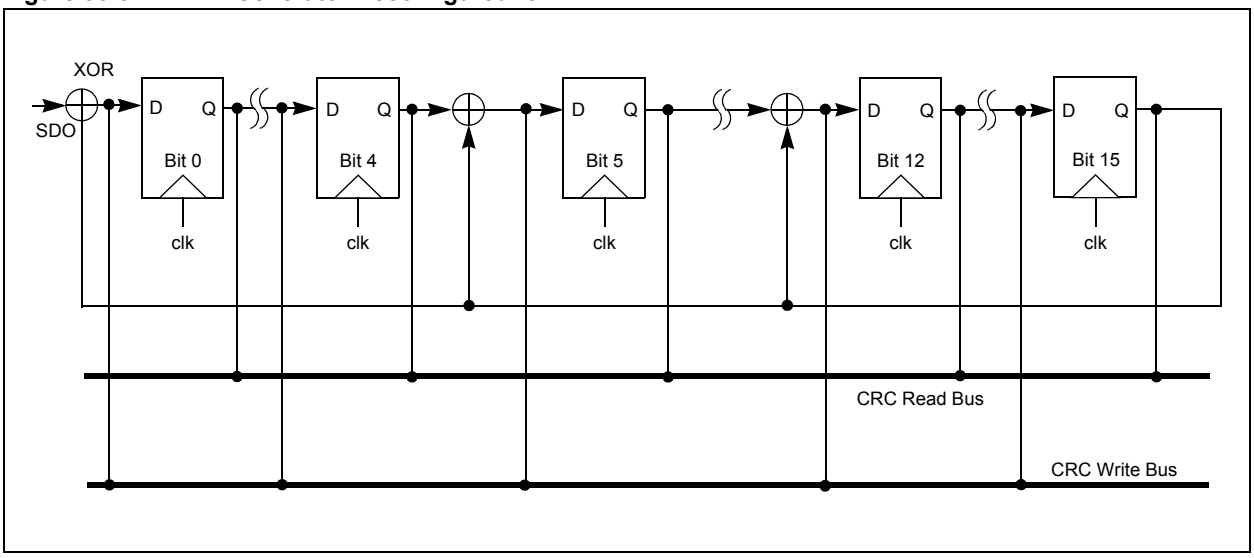
Table 36-1: Example CRC Setup

Register Names	Bit Names	Bit Values
CRCCON	PLEN<3:0>	0Fh
CRCXOR	X<15:1>	1020h

The polynomial length in this case is 16 (PLEN<3:0> + 1). Note that for the value of X<15:1>, as programmed in Table 36-1, the 12 and 5 bits are set to '1' as required by the generator polynomial. Bit 0 is always XORed. For a 16-bit polynomial, the 16th bit is always assumed to be XORed; therefore, there is no CRCXOR bit for either bit 0 or bit 16.

The topology of the CRC generator configured for the example polynomial is shown in Figure 36-3.

Figure 36-3: CRC Generator Reconfigured for $x^{16} + x^{12} + x^5 + 1$



Note: The x^0 bit in the CRCXOR register is omitted and is always assumed to be '1'. Therefore, a polynomial with a LSb of '0' or '1' (e.g., 1020h or 1021h) has the same effect on the CRC calculation.

36.5 CONTROL LOGIC

36.5.1 FIFO

The FIFO is physically implemented as an 8-deep, 16-bit wide storage element. The logic associated with the FIFO contains a 5-bit counter, named VWORD (VWORD<4:0> or CRCCON<12:8>). The value in the VWORD<4:0> bits indicates the number of new data elements in the FIFO.

The FIFO behaves as an 8-deep, 16-bit wide array when PLEN<3:0> is greater than 7, and a 16-deep, 8-bit wide array otherwise. The data for which the CRC is to be calculated must first be written into the FIFO by the CPU using the CRC Data (CRCDAT) register. Data must always be written into the CRCDAT register. Reading of the CRCDAT register is not allowed and always returns zero.

The smallest data element that can be written into the FIFO is one byte. When PLEN<3:0> is less than or equal to 7, every byte write into the FIFO increments VWORD by one, or by two, for every word write operation.

If PLEN<3:0> is greater than 7, a word write into the FIFO increments the value of VWORD by one. A single byte write to the CRCDAT register does not increment the value of VWORD; instead, VWORD increments by one only after an even number of bytes (integer multiple of words) are written into the CRCDAT register.

The FIFO Full (CRCFUL) bit is set (indicating the FIFO is full) when the value of VWORD reaches 8 (for the 8-deep, 16-bit FIFO configuration) or 16 (for the 16-deep, 8-bit FIFO configuration). The user application needs to ensure that the FIFO is not full while writing a new value to the CRCDAT register.

While processing a block of data, the application must ensure that the last word of the data block has been shifted out of the CRC register to produce the correct CRC checksum result. This can be achieved by writing 0x0000 to the CRCDAT register after the last word of the data block has been written to the CRCDAT register. Additionally, the application must ensure that the FIFO is not full (CRCFUL = 0) while writing this word to the CRCDAT register.

36.5.2 CRC Engine Interface

36.5.2.1 FIFO TO CRC CALCULATOR

To start serial shifting from the FIFO to the CRC calculator, the Start CRC (CRCGO) bit must be set (CRCCON<4> = 1). The serial shifter starts shifting data, starting from the MSb first, into the CRC engine only when CRCGO = 1 and the value of VWORD is greater than zero. If the CRCFUL bit was set earlier, it is cleared when VWORD decrements by one. VWORD decrements by one when a FIFO location gets shifted completely to the CRC calculator. The serial shifter continues shifting until VWORD reaches zero, at which point, the FIFO Empty (CRCMPT) bit becomes set to indicate that the FIFO is empty.

The frequency of the CRC shift clock is twice that of the dsPIC33F instruction clock cycle, which makes this hardware shifting process faster than a software shifter. The user application can write into the FIFO while the shift operation is in progress. For a continuous data feed into the CRC engine, the recommended mode of operation is to initially “prime” the FIFO with a sufficient number of words or bytes. Once this is completely done, the user application can start the CRC by setting the CRCGO bit to ‘1’. From this point forward, either VWORD or the CRCFUL bit should be monitored. If the CRCFUL bit is not set, or the VWORD reads less than 8 or 16, another word can be written onto the FIFO. At least one instruction cycle must pass after a write to the CRCDAT register before a read of the VWORD bits is done.

To empty words already written into a FIFO, the CRCGO bit must be set to ‘1’ and the CRC shifter must be allowed to run until the CRCMPT bit is set.

Note:	When PLEN<3:0> is greater than 7, an integer multiple of words should be loaded into the FIFO before the application software sets the CRCGO bit. If the CRCGO bit is set after loading an odd number of bytes into the FIFO, the last odd byte is never shifted out, and the CRCMPT bit always remains at ‘0’, indicating that the FIFO is not empty.

36.5.2.2 NUMBER OF DATA BITS SHIFTED FROM FIFO

The number of data bits to be shifted depends upon the length of the polynomial selected. For example, if PLEN<3:0> = 5, the length of the generator polynomial and the size of one data is 6 bits (PLEN<3:0> + 1). In this case, a full byte of a FIFO location is not shifted out, even though the CPU can write only one byte. Only 6 bits of a byte are shifted out, starting from the 6th bit (i.e., the MSb in this case). The two MSbs of each byte are don't care bits. Therefore, for a given value of PLEN<3:0>, it will take ((PLEN<3:0> + 1) • VWORD) number of shift clock cycles to complete the CRC calculations. Similarly, for a 12-bit polynomial selection, the shifting starts from the 12th bit of the word, which is the MSb for this selection. The Most Significant 4 bits of each word are ignored.

Note:	For 'n' bit polynomial selection, the CRC calculation is done with integer multiple of 'n' bit of data. For example, for a 16 bit polynomial, the CRC calculation is done with integer multiple of words.

36.5.2.3 CRC RESULT

When the CPU reads the CRCWDAT register, the CRC result is read directly out of the shift register through the CRC read bus. To get the correct CRC reading, it is necessary to wait for the CRCMPT bit to go high before reading the CRCWDAT register.

A direct write path to the CRC Shift registers is also provided through the CRC write bus. This path is accessed by the CPU through the CRCWDAT register. The CRCWDAT register can be loaded with a desired value prior to the start of the shift process.

Note:	When the CPU writes to the shift registers directly through the CRCWDAT register, the CRCGO bit must be '0'.

36.5.3 Interrupt Operation

Serial shifting of the FIFO data to the CRC engine begins when the CRCGO bit is set and the VWORD<4:0> bits are greater than zero. During this process, if the CRCMPT bit makes a transition from '0' (not empty) to '1' (empty), or when the VWORD<4:0> bits make a transition from any value greater than zero to zero, the CRCIF interrupt flag becomes set. If the CRC interrupt is enabled by setting the CRCIE bit, and the CRCIF bit becomes set, an interrupt is generated.

Table 36-2 in **36.9 "Register Maps"** details the interrupt register associated with the CRC module. For more details on interrupts and interrupt priority settings, refer to **Section 8. "Interrupts"**.

Note:	If new data is written into the CRCDAT register when the CRCFUL bit is set, the VWORD Pointer rolls over through '0'. However, the CRC Interrupt Flag, CRCIF is not set in this condition. Here, the CRCFUL bit gets reset, all previous data written into the FIFO is lost and the new data is written into the first location of the FIFO. Remaining locations of the FIFO are empty and new data can be written into the empty locations.

36.5.4 CRC Module Operation Example

Consider the following CRC module configuration example, where the CRC generator polynomial length is selected as 16 (PLEN<3:0> = 0xF) and the CRC generator polynomial is as shown in Equation 36-3. The CRCXOR register has a value of 0x0800E to obtain this polynomial. Since the value of PLEN is configured so that 16 bits are shifted through the CRC Shift register, the FIFO becomes a 16-bit and 8-deep FIFO.

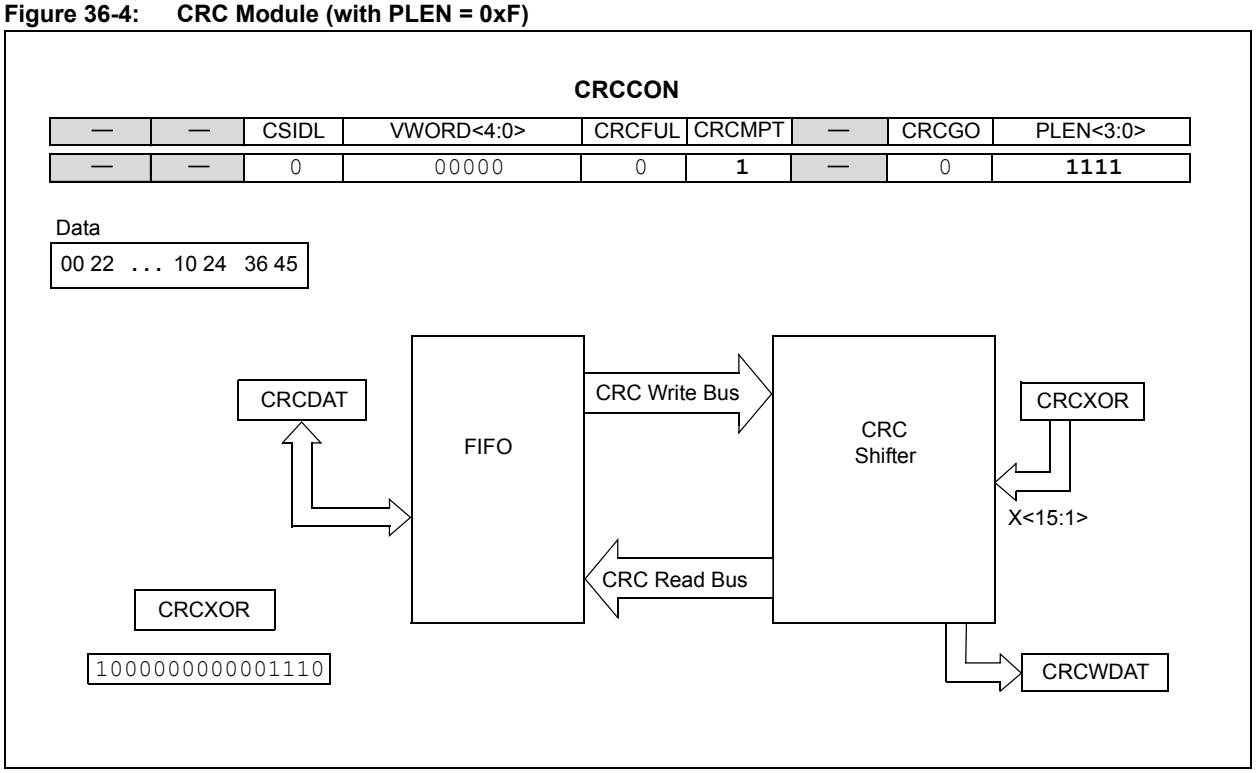
Equation 36-3: Generator Polynomial

$$x^{16} + x^{15} + x^3 + x^2 + x^1 + 1$$

The following process and corresponding figures describe the operation of the CRC module:

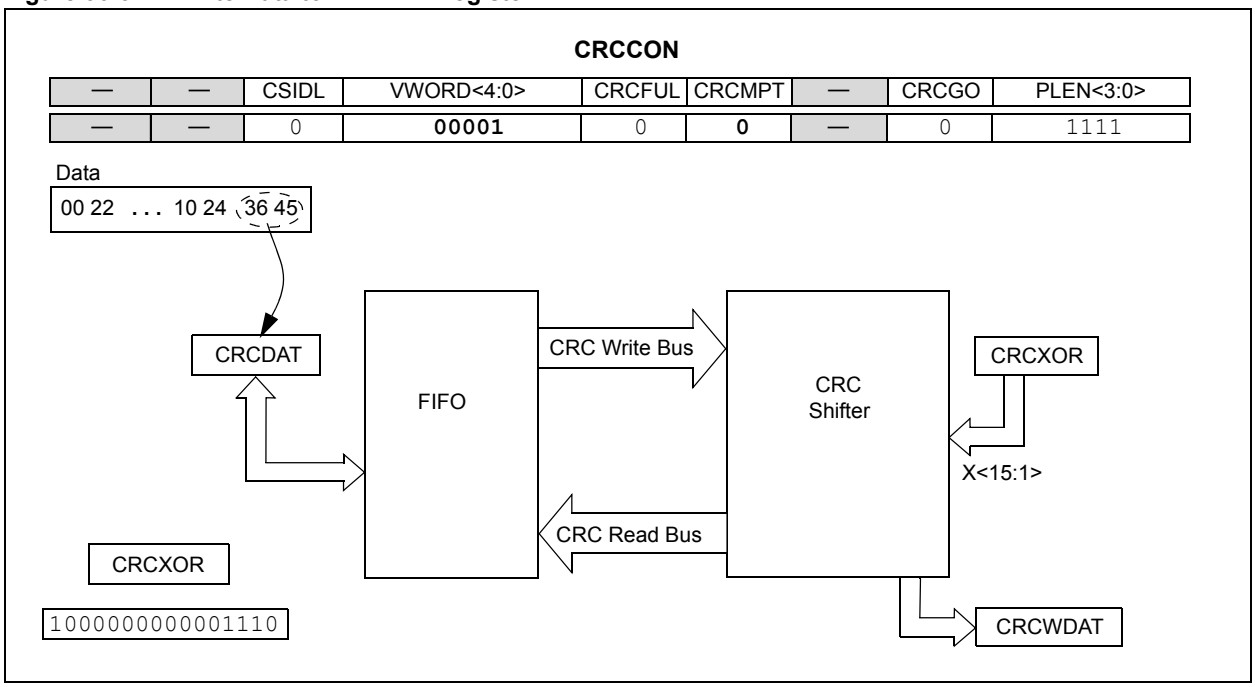
1. The CRC module is configured for a 16-bit CRC generator polynomial. The CRCMPT bit value is '1' indicating that the CRC FIFO is empty.

Figure 36-4: CRC Module (with PLEN = 0xF)



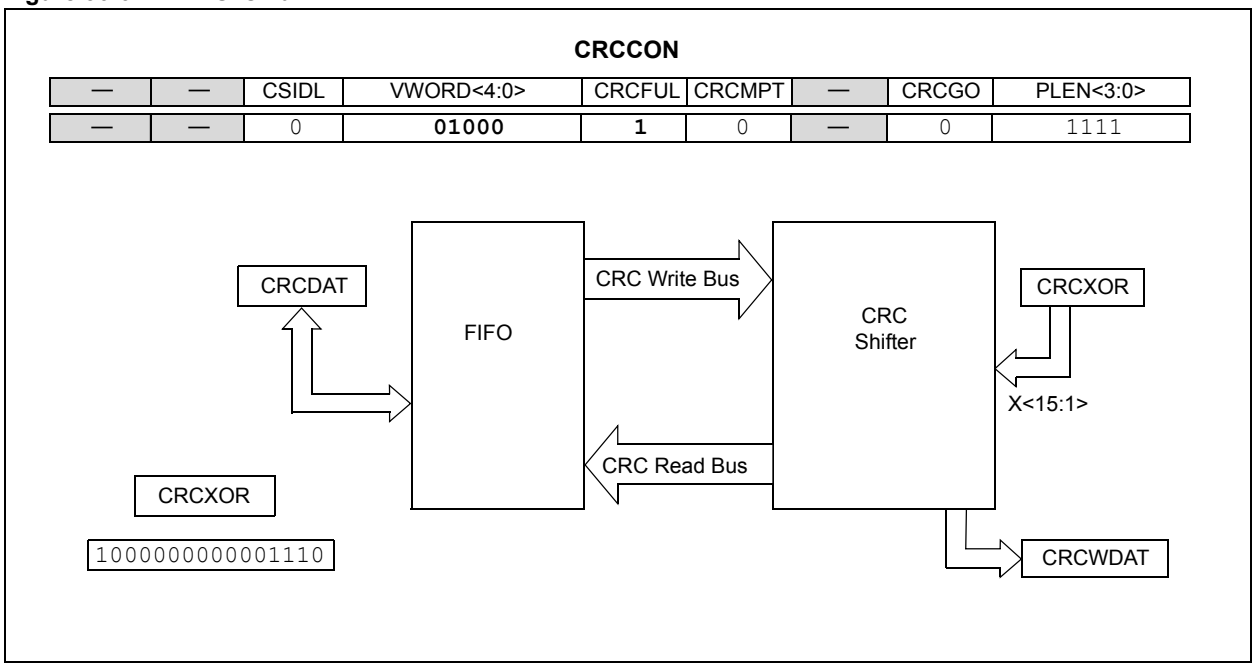
2. The application starts writing data to the CRCDAT register. The VWORD bits increment and indicate the number of words written to the CRCDAT register. The CRCMPT bit is cleared indicating the CRC FIFO is not empty.

Figure 36-5: Write Data to CRCDAT Register



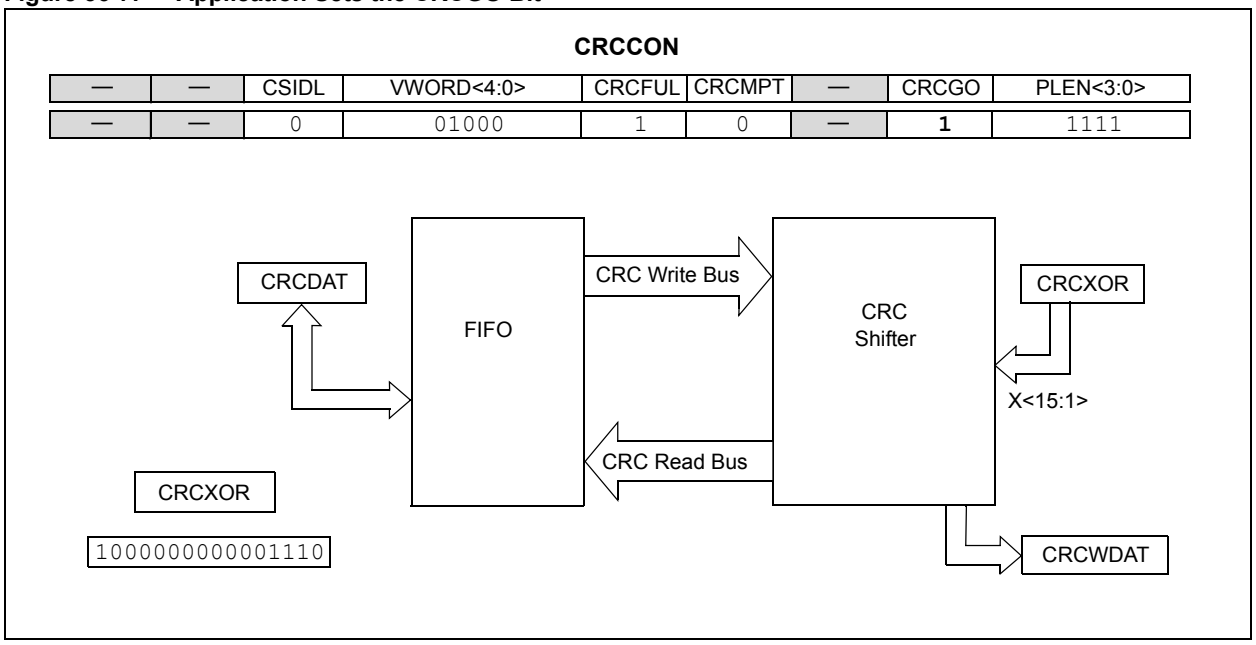
3. When eight words have been written to the FIFO, the VWORD bit is read as 0x8 and the CRCFUL bit is set. The CRC module is now ready to process a data block of eight words.

Figure 36-6: FIFO is Full



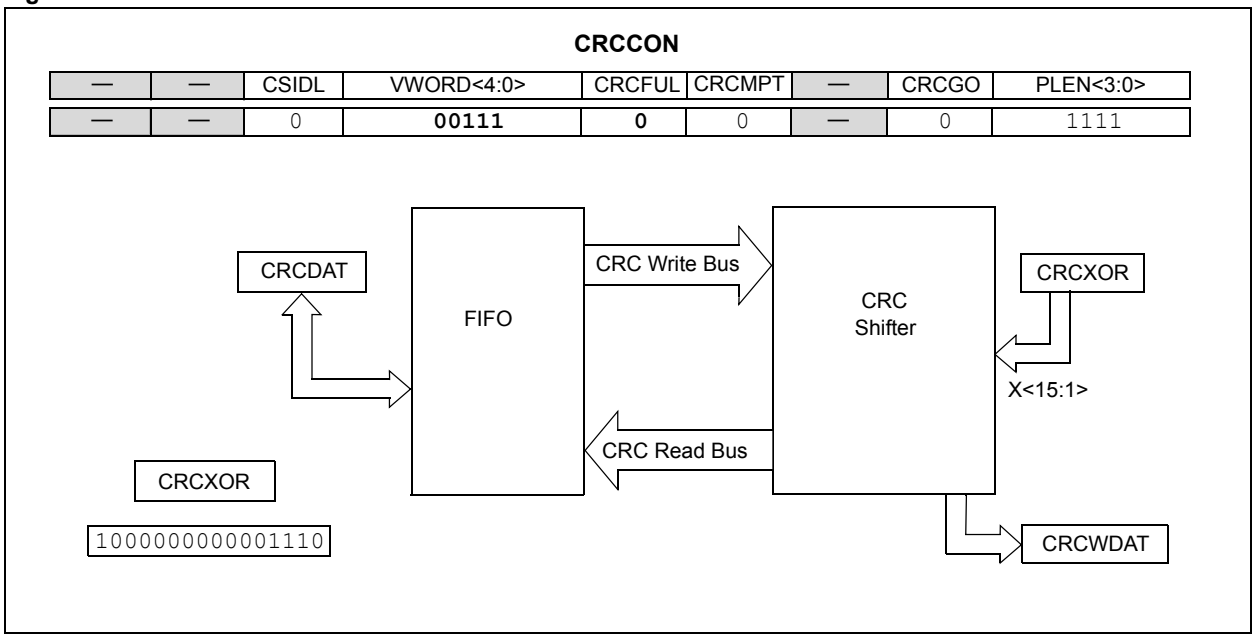
4. The application sets the CRCGO bit, which instructs the CRC module to start shifting words though the CRC shift register.

Figure 36-7: Application Sets the CRCGO Bit



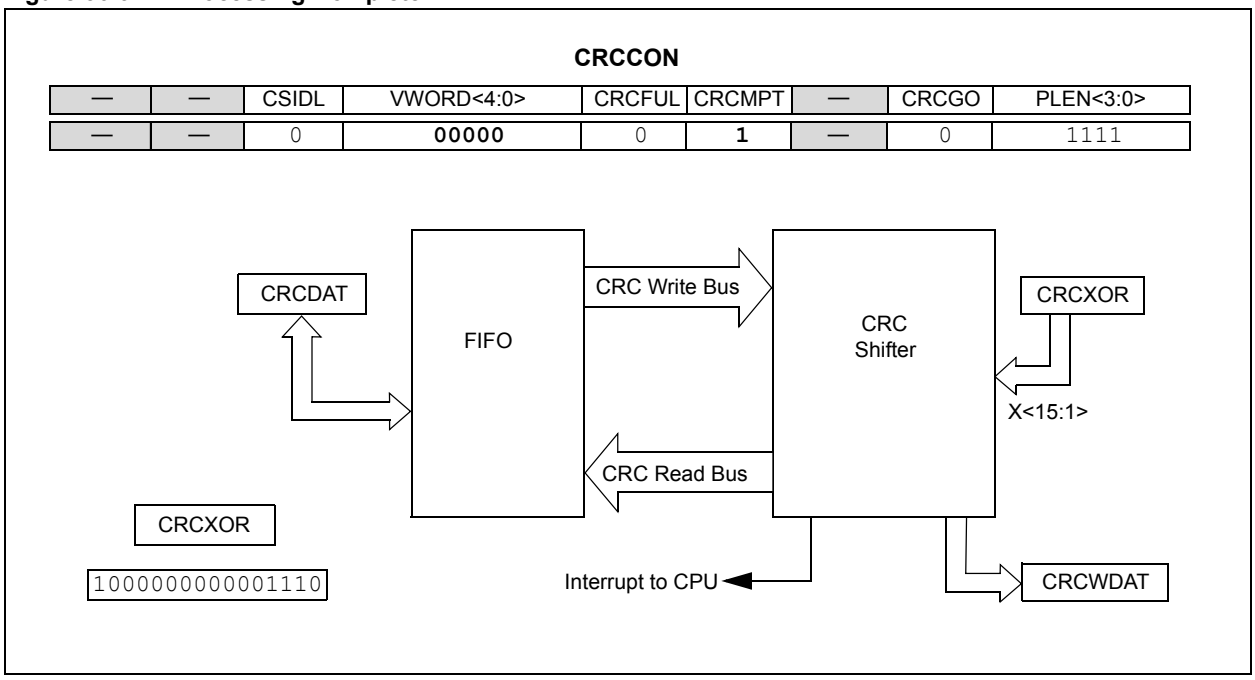
5. The CRC shift register starts shifting the word from the FIFO. The VWORD bits decrement and indicate the number of words that have been processed. When the CRC module starts transferring data from the FIFO to the CRC shift register, the CRCFUL bit is cleared.

Figure 36-8: CRC Module Processes Data from the FIFO



6. The CRC module completes processing eight words of data and causes an Interrupt. Next, the CRC Checksum result is stored in the CRCWDAT register. Finally, the CRCMPT bit indicates that the CRC FIFO is empty.

Figure 36-9: Processing Complete



36.6 ADVANTAGES OF PROGRAMMABLE CRC MODULE

The CRC algorithm is straightforward to implement in software. However, it requires considerable CPU bandwidth to implement the basic requirements, such as shift, bit test and XOR. Moreover, CRC calculation is an iterative process and additional software overhead for data transfer instructions puts enormous burden on the MIPS requirement of a device.

The CRC engine in dsPIC33F devices calculates the CRC checksum without CPU intervention. Moreover, it is much faster than the software implementation; the CRC engine consumes only half of an instruction cycle per bit for its calculation as the frequency of the CRC shift clock is twice that of the dsPIC33F instruction clock cycle. For example, the CRC hardware engine takes only 64 instruction cycles to calculate a CRC checksum on a message that is 128 bits (16x8) long. The same calculation, if implemented in software, will consume more than a thousand instruction cycles even for a well optimized piece of code.

36.7 APPLICATION OF CRC MODULE

Calculating a CRC is a robust error checking algorithm in digital communication for messages containing several bytes or words. After calculation, the checksum is appended to the message and transmitted to the receiving station. The receiver calculates the checksum with the received message to verify the data integrity.

36.7.1 Variations

The CRC module of dsPIC33F devices shifts out the MSb first. This is a popular implementation as employed in XMODEM protocol. In one of the variations (CCITT protocol) for CRC calculation, the LSb is shifted out first. This requires bit reversal of the message polynomial in the software before feeding the message to the dsPIC33F CRC hardware module, and this also adds considerable software overhead. Discussions on all the variations are beyond the scope of this document, but several variations of CRC can be implemented using the programmable CRC module in dsPIC33F devices with minimal software overhead.

The choice of the polynomial length, and the polynomial itself, are application dependent. Polynomial lengths of 5, 7, 8, 10, 12 and 16 are normally used in various standard implementations. The CRC module in dsPIC33F devices can be configured for different polynomial lengths and for different equations. If a polynomial of ‘n’ bits is selected for calculation, normally ‘n’ zeros are appended to the message stream, though there are variations in this process as well. The following sections explain the recommended step-by-step procedure for CRC calculation, where ‘n’ zeros are appended to the message stream for an ‘n’ bit polynomial. Users can decide whether zeros, or any other values, need to be appended to the message stream. Depending on the application, the designer may decide whether any value needs to be appended at all.

36.7.2 8-Bit Polynomial

The recommended procedure to calculate a CRC with an 8-bit polynomial is as follows:

1. Program PLEN<3:0> bits (CRCCON<3:0>) = 07h.
2. Program a value to CRCXOR (e.g., CRCXOR = 31h).
3. Program a value in CRCWDAT:
   - 0000h (for the start of a new calculation), or
   - the previously calculated partial result (for part of the whole message stream).
4. If the CRCFUL bit is not set, and if all the data bytes of the message stream are not written into the FIFO, then write a data byte to the CRCDAT register.
5. If the CRCFUL bit is not set, and if all the data bytes of the message stream have already been written into the FIFO, then write a byte of 00h in the CRCDAT register and set a software flag bit in the application using the CRC (i.e., `FINAL_CALCULATION`).
6. If the CRCFUL bit or the software `FINAL_CALCULATION` flag is set, then start CRC by setting the CRCGO bit.
7. When CRCMPT is set, clear the CRCGO bit and read the result byte from the CRCWDAT register.
8. For a partial result (CRC calculation is done but the `FINAL_CALCULATION` flag is not set), pass the partial result to the next calculation process.

36.7.3 5-Bit or 7-Bit Polynomials

For 5-bit or 7-bit polynomials, the CRC module will calculate the checksum taking into account the 5 or 7 Least Significant bits of a byte, respectively. In the case of 5 bits of data, a byte should contain the 5 bits of data in its 5 Least Significant bits; the Most Significant 3 bits of the byte may be programmed as zeros. In case of a 7-bit calculation, a byte should contain the 7 bits of data in its 7 Least Significant bits; the Most Significant bit of a byte may be programmed as zero. Refer to **Section 36.5.2.1 "FIFO to CRC Calculator"** for more details.

After forming the bytes from a message stream, the same steps as explained in **36.7.2 "8-Bit Polynomial"** can be applied. For the polynomial length (PLEN<3:0>), use values of 04h or 06h for 5-bit and 7-bit polynomials, respectively. A suitable 5-bit or 7-bit generator polynomial may be programmed in the CRCXOR register.

36.7.4 16-Bit Polynomials

The recommended procedure to calculate a CRC with a 16-bit polynomial is as follows:

1. Program PLEN<3:0> bits (CRCCON<3:0>) = 0Fh.
2. Program a value to CRCXOR (e.g., CRCXOR = 8005h).
3. Program a value in CRCWDAT:
   - 0000h (for the start of a new calculation), or
   - the previously calculated partial result (for part of the whole message stream).
4. If the CRCFUL bit is not set, and if all the data words of the message stream are not written into the FIFO, then write a data word to the CRCDAT register.
5. If the CRCFUL bit is not set, and if all the data words of the message stream are already written into the FIFO, then write a word of 0000h in CRCDAT and set a software flag in the application using the CRC (i.e., `FINAL_CALCULATION`).
6. If the CRCFUL bit or the software `FINAL_CALCULATION` flag is set, then start CRC by setting the CRCGO bit.
7. When CRCMPT is set, then clear the CRCGO bit and read the result byte from the CRCWDAT register.
8. For a partial result (CRC calculation is done but the `FINAL_CALCULATION` flag is not set), pass the partial result to the next calculation process.

Note:	If the length of the polynomial is 16 bits, the CRC module expects an integer multiple of 16 bits in the FIFO.

A word write is a simple process for a 16-bit polynomial. However, in some applications, byte write operations may be used with 16-bit polynomials (e.g., in UART transmission/reception). In these applications, an odd number of bytes may need to be padded up with an extra dummy byte. A dummy byte should not be added if the message stream contains an even number of bytes. In this case, the procedure explained above for 16-bit polynomials may need to be modified as follows:

1. Program PLEN<3:0> bits (CRCCON<3:0>) = 0Fh.
2. Program a value to CRCXOR (e.g., CRCXOR = 8005h).
3. Program a value in CRCWDAT:
   - 0000h (for the start of a new calculation), or
   - The previously calculated partial result (for part of the whole message stream).
4. If the CRCFUL bit is not set, and if all the data bytes of the message stream are not written into the FIFO, then write a data byte to the CRCDAT register and increment a counter to keep track of the number of bytes written to the FIFO.
5. If the CRCFUL bit is not set, and if all the data bytes of the message stream are already written into the FIFO which are odd, then write a byte of 00h (dummy byte) to CRCDAT and set a software flag in the software application (i.e., `MESSAGE_OVER`).
6. If the CRCFUL bit is not set, and if all the data bytes of the message stream are already written into the FIFO which are even, then set a software flag (`MESSAGE_OVER`).
7. If the CRCFUL bit is not set, and if the `MESSAGE_OVER` flag is set, write a word of 0000h to CRCDAT and set a software flag (i.e., `FINAL_CALCULATION`).

8. If the CRCFUL bit or the FINAL_CALCULATION flag is set, start CRC by setting the CRCGO bit.
9. When CRCMPT is set, clear the CRCGO bit and read the result byte from the CRCWDAT register.
10. For a partial result (CRC calculation is done but the FINAL_CALCULATION flag is not set), pass the partial result to the next calculation process.

36.7.4.1 CODE EXAMPLE

Example 36-1 shows an example of application code for configuring the CRC module to use a 16-bit polynomial and process a block of data that is eight words in size. The application code can either poll the CRCIF flag or create and use the CRC Interrupt ISR to check when the CRC module has completed processing.

Note that the code example processes a block of data whose size is larger than the FIFO. The data is written to the FIFO when the FIFO is not full. This process takes place even when the CRC shift register is processing the data words from the FIFO. When the last word of the data block is written to the FIFO, a value of 0x0000 is written to shift out the last word of data from the CRC shift register.

Example 36-1: Code Example

```
int src[20];       /* The data block to be processed */
int i;

CRCCON  = 0x0F;            /* Configure the polynomial length (PLEN) */
CRCXOR  = 0x8004;          /* In CRCXOR, configure for the polynomial x^16 + x^15 + x^2 + 1 */
CRCWDAT = 0x00;            /* Clear CRCWDAT*/


for(i = 0;i < 20;i ++)
{
    CRCDAT=Src[i];             /* Populate the FIFO */
    if(CRCCONbits.CRCFUL)
    {
        CRCCONbits.CRCGO = 1;  /* CRC calculation start */
    }
    while(CRCCONbits.CRCFUL); /* Wait for available FIFO register */
}

CRCDAT = 0x0000;/* Do this to shift the last word out of the CRC shift register */


while (!IFS4bits.CRCIF);  /* Check for interrupt flag bit */
IFS4bits.CRCIF = 0;

while(!CRCCONbits.CRCMPT);/* Wait for CRC shifter to clear FIFO */
CRCResult = CRCWDAT;       /* Output result */
CRCWDAT = 0;
```

36.7.5 10-Bit or 12-Bit Polynomial

For 10-bit or 12-bit polynomials, the CRC module calculates the checksums by taking into account the 10 or 12 Least Significant bits of a word, respectively. For 10 bits of data, the Most Significant 6 bits of a word may be programmed as zero. For 12-bit calculation, the Most Significant 4 bits of a word may be programmed as zero. Refer to **36.5.2.1 “FIFO to CRC Calculator”** for more details.

After forming the words with 10 or 12 bits of actual data and the rest as “don’t care” bits, the same steps as explained in **36.7.4 “16-Bit Polynomials”** can be applied. For the PLEN<3:0> bits, use a value of 09h or 0Bh for 10-bit or 12-bit polynomials, respectively. A suitable generator polynomial of the same length may be programmed in the CRCXOR register.

36.8 OPERATION IN POWER SAVE MODES

36.8.1 Sleep Mode

If Sleep mode is entered while the module is operating, the module is suspended in its current state until clock execution resumes.

36.8.2 Idle Mode

To continue full module operation in Idle mode, the CSIDL bit must be cleared prior to entry into the mode.

If CSIDL = 1, the module behaves the same way as it does in Sleep mode; pending interrupt events will be passed on, even though the module clocks are not available.

36.9 REGISTER MAPS

A summary of the Special Function Registers associated with the dsPIC33F Programmable Cyclic Redundancy Check (CRC) module is provided in Table 36-2.

Table 36-2: Special Function Registers Associated with the Programmable CRC Module(1)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON	0640	—	—	CSIDL	VWORD<4:0>					CRCFUL	CRCMPT	—	CRCGO	PLEN<3:0>				0040
CRCXOR	0642	X<15:1>															—	0000
CRCDAT	0644	CRC Data Input Register																0000
CRCWDAT	0646	CRC Result Register																0000

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

Note 1: Please refer to the device data sheet for specific memory map details.

36.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Programmable Cyclic Redundancy Check (CRC) module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip website (www.microchip.com) for additional application notes and code examples for the dsPIC33F family of devices.

36.11 REVISION HISTORY

Revision A (October 2007)

This is the initial release of this document.