Section 34. Comparator

HIGHLIGHTS

This section of the manual contains the following major topics:

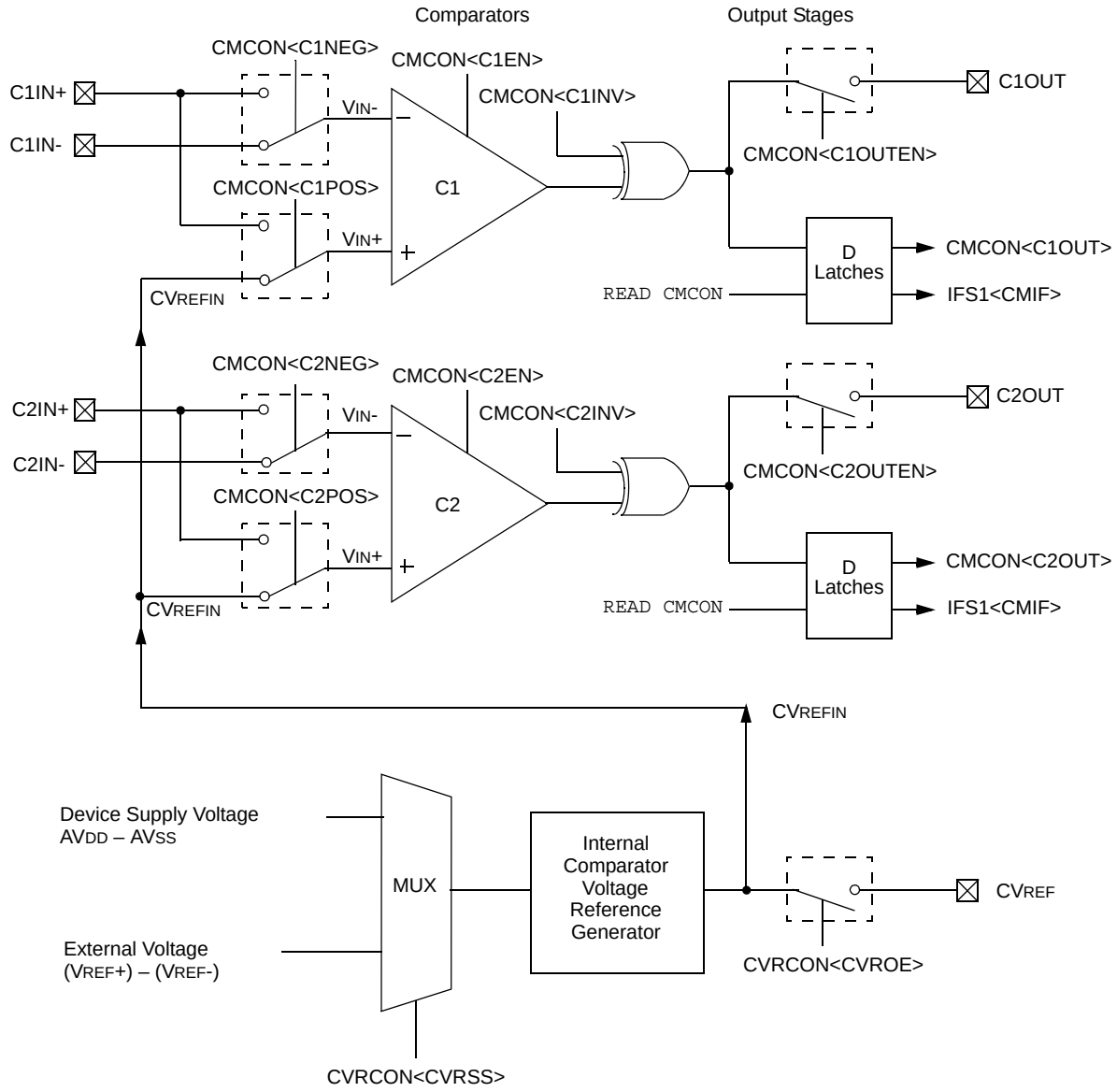
34.1 INTRODUCTION

The dsPIC33F Comparator module provides two comparators that can be configured in a variety of ways. As shown in Figure 34-1, individual comparator options are specified by Configuration bits in the Comparator Control (CMCON) register to do the following:

- Enable the comparator
- Select input combinations
- Enable output inversion
- Enable output on an I/O pin

The comparator operating mode is determined by the input selections (i.e., whether the input voltage is compared to a second input voltage or to an internal reference voltage). The internal reference voltage is generated by a resistor ladder network that is configured by the Comparator Voltage Reference Control (CVRCON) register.

Figure 34-1: Comparator I/O Operating Modes



Note: The quantity (VREF+) - (VREF-) and (AVDD - AVSS) is generally represented as CVRSRC in subsequent sections.

34.2 COMPARATOR REGISTERS

The Comparator module uses these registers:

- **CMCON: Comparator Control Register**

  This register allows the application program to enable, configure and interact with the individual comparators.

- **CVRCON: Comparator Voltage Reference Control Register**

  This register allows the application program to enable, configure and interact with the comparator internal voltage reference generator (see **34.6 "Comparator Voltage Reference Generator"** for details).

Register 34-1: CMCON: Comparator Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIDL	—	C2EVT	C1EVT	C2EN	C1EN	C2OUTEN	C1OUTEN
bit 15							bit 8

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	C2NEG	C2POS	C1NEG	C1POS
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL:** Stop in Idle Mode bit
1 = When device enters Idle mode, module does not generate interrupts. Module is still enabled
0 = Continue normal module operation in Idle mode

bit 14 **Unimplemented:** Read as '0'

bit 13 **C2EVT:** Comparator 2 Event bit
1 = Comparator output changed states
0 = Comparator output did not change states

bit 12 **C1EVT:** Comparator 1 Event bit
1 = Comparator output changed states
0 = Comparator output did not change states

bit 11 **C2EN:** Comparator 2 Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 10 **C1EN:** Comparator 1 Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 9 **C2OUTEN:** Comparator 2 Output Enable bit
1 = Comparator output is driven on the output pad
0 = Comparator output is not driven on the output pad

bit 8 **C1OUTEN:** Comparator 1 Output Enable bit
1 = Comparator output is driven on the output pad
0 = Comparator output is not driven on the output pad

Register 34-1: CMCON: Comparator Control Register (Continued)

bit 7 **C2OUT:** Comparator 2 Output bit
When C2INV = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When C2INV = 1:
0 = VIN+ > VIN-
1 = VIN+ < VIN-

bit 6 **C1OUT:** Comparator 1 Output bit
When C1INV = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When C1INV = 1:
0 = VIN+ > VIN-
1 = VIN+ < VIN-

bit 5 **C2INV:** Comparator 2 Output Inversion bit
1 = C2 output inverted
0 = C2 output not inverted

bit 4 **C1INV:** Comparator 1 Output Inversion bit
1 = C1 output inverted
0 = C1 output not inverted

bit 3 **C2NEG:** Comparator 2 Negative Input Configure bit
1 = Input is connected to C2IN+
0 = Input is connected to C2IN-
See Figure 34-1 for the Comparator modes.

bit 2 **C2POS:** Comparator 2 Positive Input Configure bit
1 = Input is connected to C2IN+
0 = Input is connected to CVREFIN
See Figure 34-1 for the Comparator modes.

bit 1 **C1NEG:** Comparator 1 Negative Input Configure bit
1 = Input is connected to C1IN+
0 = Input is connected to C1IN-
See Figure 34-1 for the Comparator modes.

bit 0 **C1POS:** Comparator 1 Positive Input Configure bit
1 = Input is connected to C1IN+
0 = Input is connected to CVREFIN
See Figure 34-1 for the Comparator modes.

Register 34-2: CVRCON: Comparator Voltage Reference Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE(1)	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit powered on
0 = Comparator voltage reference circuit powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable bit(1)
1 = Voltage level is output on CV_{REF} pin
0 = Voltage level is disconnected from CV_{REF} pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = 0 CV_{RSRC} to 0.67 CV_{RSRC}, with CV_{RSRC}/24 step size
0 = 0.25 CV_{RSRC} to 0.75 CV_{RSRC}, with CV_{RSRC}/32 step size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = (V_{REF+}) – (V_{REF-})$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \le CVR<3:0> \le 15$ bits
When CVRR = 1:
$CV_{REFIN} = (CVR<3:0>/24) \times (CV_{RSRC})$
When CVRR = 0:
$CV_{REFIN} = 1/4 \times (CV_{RSRC}) + (CVR<3:0>/32) \times (CV_{RSRC})$

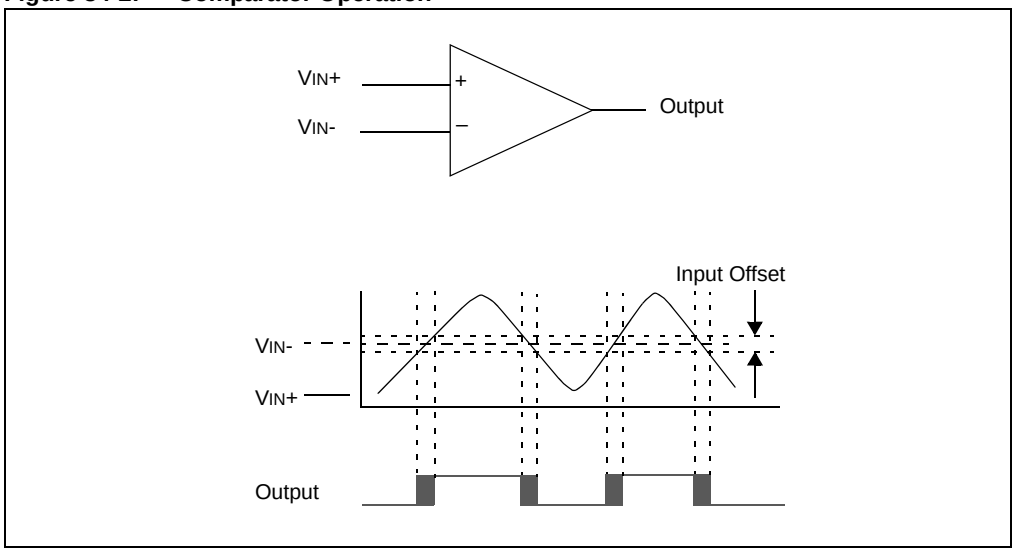
Note 1: CVROE overrides the TRIS bit setting.

34.3 COMPARATOR OPERATION

The operation of a typical comparator is shown in Figure 34-2, along with the relationship between the analog input levels and the digital output. Depending on the comparator operating mode, the monitored analog signal is compared to either an external or internal voltage reference. Each of the two comparators can be configured to use the same, or different reference sources. For example, one comparator can use an external reference while the other uses the internal reference. However, if both comparators use an internal reference, they must use the same reference voltage value (CVREFIN). For further details on comparator operation, see **34.6 "Comparator Voltage Reference Generator"**.

In Figure 34-2, the external reference VIN-, is a fixed external voltage. The analog signal present at VIN+ is compared to the reference signal at VIN-, and the digital output of the comparator is created when the difference is great enough. When VIN+ is less than VIN-, the output of the comparator is a digital low level. When VIN+ is greater than VIN-, the output of the comparator is a digital high level. The shaded areas of the output represent the area of uncertainty due to input offsets and response time.

Figure 34-2: Comparator Operation



Input offset represents the range of voltage levels within which the comparator trip point can occur. The output can switch at any point in this offset range. Response time is the minimum time required for the comparator to recognize a change in input levels.

34.4 COMPARATOR CONFIGURATION

Each of the two comparators in the Comparator module is configured independently by Configuration bits in the Comparator Control (CMCON) register (Register 34-1). This register enables the application program to interact with the Comparator module to control:

- Input signal source (CxPOS and CxNEG bits)
- Output signal polarity (CxINV bits)
- Output signal path (CxOUT bits)

34.4.1 Input Signal Source

The input signals can be connected to either of the positive (V_{IN+}) or the negative (V_{IN-}) comparator terminals. The connections are defined by these Configuration bits:

- **C1POS** – Comparator 1 Positive Input Configure bit (CMCON<0>)
- **C1NEG** – Comparator 1 Negative Input Configure bit (CMCON<1>)
- **C2POS** – Comparator 2 Positive Input Configure bit (CMCON<2>)
- **C2NEG** – Comparator 2 Negative Input Configure bit (CMCON<3>)

Table 34-1 outlines the possible input signal configurations and the Configuration bit settings for each.

Table 34-1: Input Signal Configurations

Comparator Input Terminal		CxPOS	CxNEG
Positive (V_{IN+})	Negative (V_{IN-})		
CV_{REFIN}	C1IN-	0	0
CV_{REFIN}	C1IN+	0	1
C1IN+	C1IN-	1	0

Note: The reference voltage CV_{REFIN} can be generated either from the device supply voltage (AV_{DD} - AV_{SS}) or from an external voltage (V_{REF+}) - (V_{REF-}). This selection is done using the CVRCON<CVRSS> bits.

34.4.2 Output Signal Polarity

The polarity of the output signal is determined by these Configuration bits:

- **C1INV** – Comparator 1 Output Inversion bit (CMCON<4>)
- **C2INV** – Comparator 2 Output Inversion bit (CMCON<5>)

The configuration of these bits specifies how the state of the corresponding Comparator Output bit is achieved.

34.4.3 Output Signal Paths

The Comparator module provides two output signal paths as reflected in Figure 34-3. The first path is through these CMCON register bits:

- **C1OUT** – Comparator 1 Output (CMCON<6>)
- **C2OUT** – Comparator 2 Output (CMCON<7>)

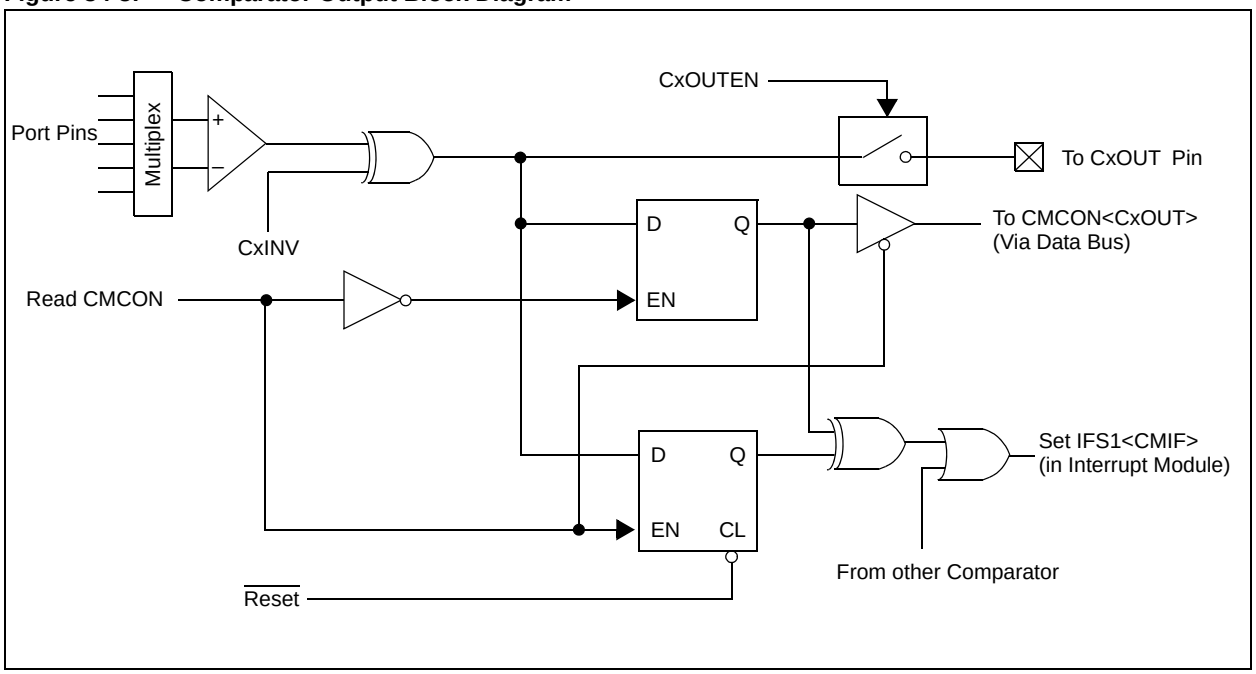
These bits are read-only. Their state is determined by the relationship of the input signals as defined by the signal source and signal polarity configurations at the time of a Read operation.

The second output path is through the C1OUT and C2OUT I/O pins. The real-time output of the comparator can be gated directly to the C1OUT and C2OUT I/O pins by these Configuration bits:

- **C1OUTEN** – Comparator 1 Output Enable (CMCON<8>)
- **C2OUTEN** – Comparator 2 Output Enable (CMCON<9>)

The associated TRIS bits still function as an output enable/disable for the I/O pins while this output signal path is in use.

Figure 34-3: Comparator Output Block Diagram



34.5 COMPARATOR INTERRUPTS

The Comparator Interrupt Flag, CMIF (IFS1<2>), is set when the synchronized output value of either comparator changes with respect to the last read value. These status bits reflect the output change:

- **C1EVT** – Comparator 1 Event (CMCON<12>)
- **C2EVT** – Comparator 2 Event (CMCON<13>)

Software can read C1EVT and C2EVT to determine the actual change that occurred. Since it is also possible to write a '1' to this register, a simulated interrupt can be software initiated. Both the CMIF and CxEVT bits must be reset by clearing them in software. These bits can be cleared in the Interrupt Service Routine (ISR). Refer to **Section 6. "Interrupts"** (DS70184), for more information.

Note:	The comparison required for generating interrupts is based on the current comparator state and the last read value of the comparator outputs. Reading the C1OUT and C2OUT bits in the CMCON register will update the values used for the interrupt generation.

34.5.1 Interrupt Operation During Sleep

If a comparator is enabled, and the dsPIC33F device is placed in Sleep mode, the comparator remains active. If the comparator interrupt is enabled in the Interrupt module, it also remains functional. Under these conditions, a comparator interrupt event will wake the device from Sleep mode.

Each operational comparator consumes additional current. To minimize power consumption in Sleep mode, turn off the comparators before entering Sleep by disabling the C1EN and C2EN bits (CMCON<11:10>). If the device wakes up from Sleep, the contents of the CMCON register are not affected. Refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196), for more information on Sleep mode.

34.5.2 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator modules to be turned off (CxEN = 0). However, the input pins multiplexed with analog input sources are configured as analog inputs by default on device Reset. The I/O configuration for these pins is determined by the setting of the ADxPCFG register. Therefore, device current is minimized when analog inputs are present at Reset time.

34.5.3 Analog Input Connection Considerations

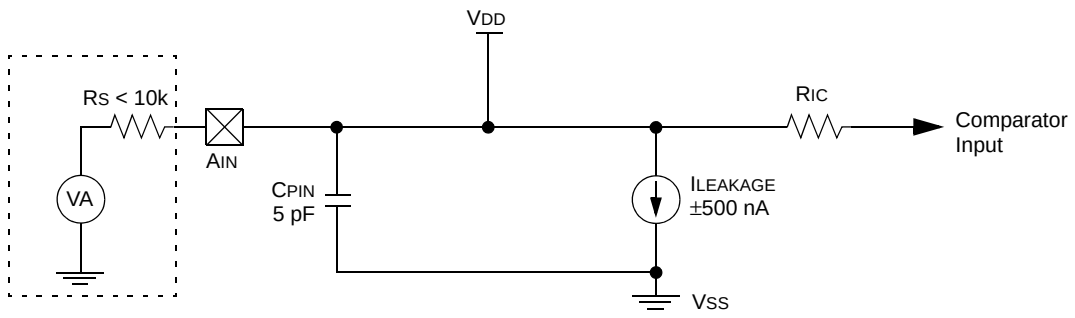
A simplified circuit for an analog input is shown in Figure 34-4. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or Zener diode, should have very little leakage current.

34.5.4 Interrupt Operation During Idle

Comparator interrupt operation during idle is controlled by the Stop in Idle Mode (CMIDL) bit (CMCON<15>). If CMIDL = 0, normal interrupt operation continues. If CMIDL = 1, the comparator continues to operate, but it does not generate interrupts. The comparator remains active in Idle mode.

Refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196), for more information on Idle mode.

Figure 34-4: Comparator Analog Input Model



Legend:

CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage

34.6 COMPARATOR VOLTAGE REFERENCE GENERATOR

The internal comparator voltage reference is derived from a 16-tap resistor ladder network that provides a selectable voltage level, as shown in Figure 34-5. This resistor network generates the internal voltage reference for the analog comparators.

This voltage generator network is managed by the Comparator Voltage Reference Control (CVRCON) register (see Register 34-2) via these control bits:

- **CVREN** – Comparator Voltage Reference Enable (CVRCON<7>)

  This control bit enables the voltage reference circuit.

- **CVROE –** Comparator Voltage Reference Output Enable (CVRCON<6>)

  This control bit enables the reference voltage to be placed on the CVREF pin. When enabled, this bit overrides the corresponding TRIS bit setting.

- **CVRSS** – Comparator Voltage Reference Source Selection (CVRCON<4>)

  This control bit specifies that the source (CVRSS) for the voltage reference circuit is either the device voltage supply (AVDD and AVSS) or an external reference (VREF+ and VREF-).

- **CVRR** – Comparator Voltage Reference Range Selection (CVRCON<5>)

  This control bit selects one of two voltage ranges covered by the 16-tap resistor-ladder network:

  - 0 CVRSRC through 0.67 CVRSRC
  - 0.25 CVRSRC through 0.75 CVRSRC

  The range selected also determines the voltage increment available from the resistor-ladder taps (see **34.6.1 "Configuring the Comparator Voltage Reference"**).

- **CVR<3:0>** – Comparator Voltage Reference Value Selection (CVRCOM<3:0>)

  These bits designate the resistor-ladder tap position.

Table 34-2 lists the voltage at each tap for both ranges with CVRSRC = 3.3V.

Figure 34-5: Comparator Voltage Reference Block Diagram

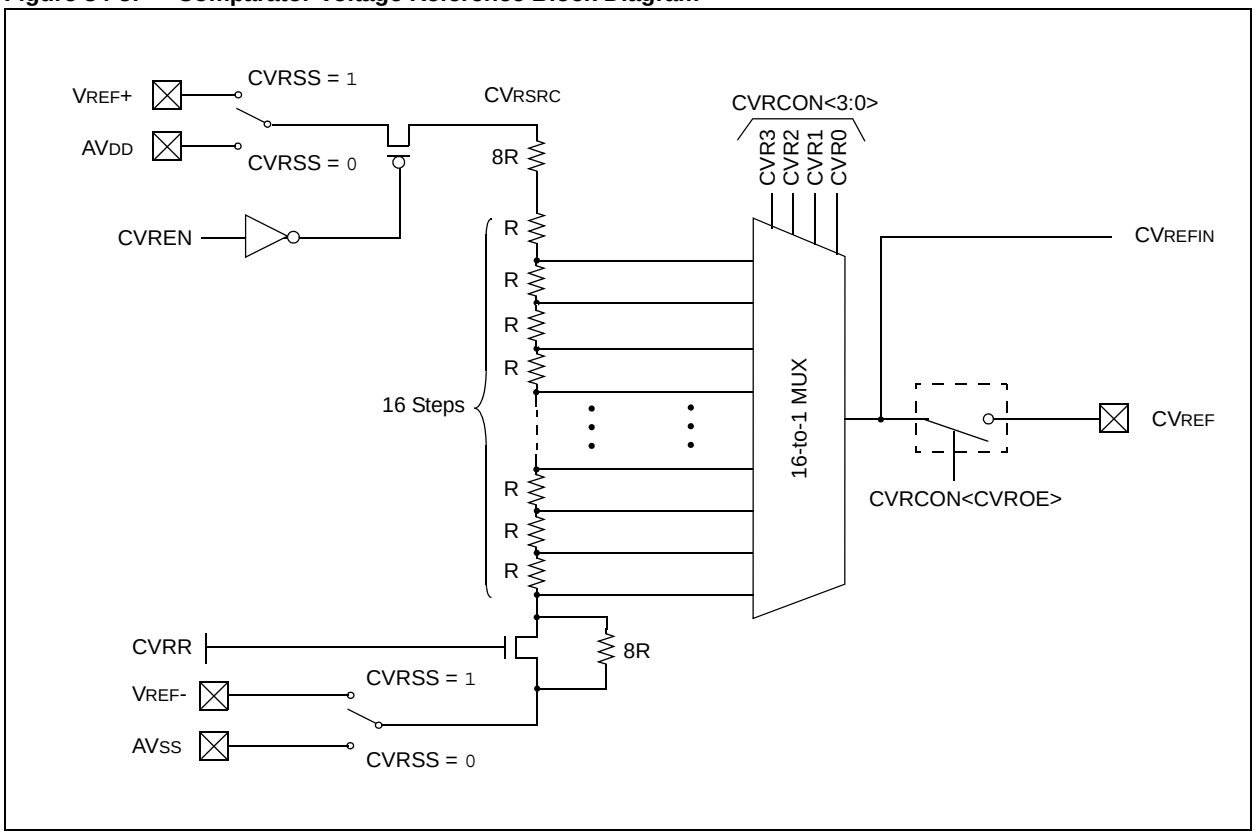


Table 34-2: Typical Voltage Reference with CVRSRC = 3.3V

CVR<3:0>	Tap	Voltage Reference	
		CVRR = 0	CVRR = 1
0000	0	0.83V	0.00V
0001	1	0.93V	0.14V
0010	2	1.03V	0.28V
0011	3	1.13V	0.41V
0100	4	1.24V	0.55V
0101	5	1.34V	0.69V
0110	6	1.44V	0.83V
0111	7	1.55V	0.96V
1000	8	1.65V	1.10V
1001	9	1.75V	1.24V
1010	10	1.86V	1.38V
1011	11	1.96V	1.51V
1100	12	2.06V	1.65V
1101	13	2.17V	1.79V
1110	14	2.27V	1.93V
1111	15	2.37V	2.06V

34.6.1 Configuring the Comparator Voltage Reference

The voltage range selected by the CVRR bit also determines the size of the steps selected by the CVR<3:0> bits. One range (CVRR = 0) provides finer resolution by offering smaller voltage increments for each step. The equations used to calculate the comparator voltage reference are as follows:

- If CVRR = 1:
  Voltage Reference = ((CVR<3:0>)/24) x (CVRSRC)
- If CVRR = 0:
  Voltage Reference = (CVRSRC/4) + ((CVR<3:0>)/32) x (CVRSRC)

34.6.2 Voltage Reference Accuracy/Error

The full voltage reference range cannot be realized because the transistors on the top and bottom of the resistor ladder network (Figure 34-5) keep the voltage reference from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the voltage reference output changes with fluctuations in that source. Check the Electrical Characteristics of the device you are using for reference voltage accuracy.

34.6.3 Operation During Sleep

When the device wakes up from Sleep through an interrupt or Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

34.6.4 Effects of a Reset

A device Reset has these effects:

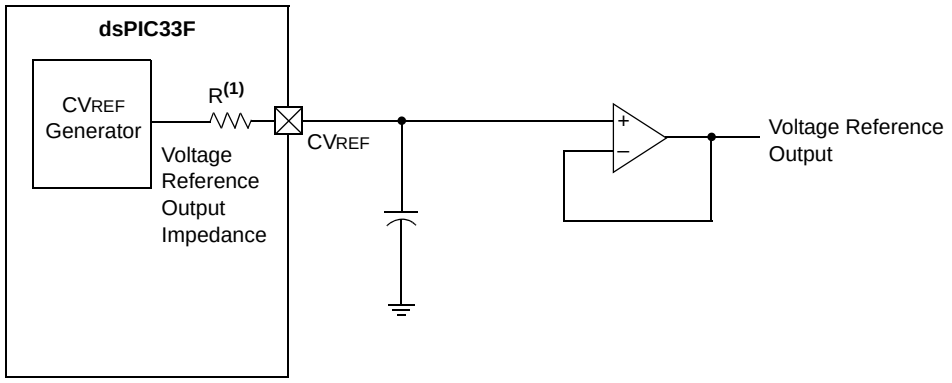
- Disables the voltage reference by clearing the CVREN bit (CVRCON<7>)
- Disconnects the reference from the CVREF pin by clearing the CVROE bit (CVRCON<6>)
- Selects the high-voltage range by clearing the CVRR bit (CVRCON<5>)
- Clears the CVR value bits (CVRCON<3:0>)

34.6.5 Connection Considerations

The voltage reference generator operates independently of the Comparator module. The output of the reference generator is connected to the CVREF pin, if the CVROE bit (CVRCON<6>) is set. Enabling the voltage reference output onto the I/O when it is configured as a digital input will increase current consumption. Configuring the port associated with CVREF as a digital output, with CVRSS enabled, will also increase current consumption.

The CVREF output pin can be used as a simple D/A output with limited drive capability. Due to this limited current drive capability, a buffer must be used on the voltage reference output for external connections to CVREF. Figure 34-6 shows a buffering technique example.

Figure 34-6: Comparator Voltage Reference Output Buffer Example



Note 1: R is dependent upon the comparator voltage reference control CVRR bits (CVRCON<5>) and CVR<3:0> value bits (CVRCON<3:0>).

34.7 INITIALIZATION

The initialization sequence shown in Example 34-1 configures the Comparator module as two independent comparators with outputs enabled and Comparator 1 output inverted. The Comparator Voltage Reference module is configured for output enabled and set for 0.25 * VDD. The delay used in this example is based on an 8 MHz oscillator.

Example 34-1: Comparator and Voltage Reference Configuration

```
CMCON = 0x0F10;      //Initialize Comparator Module

CVRCON= 0x00C0;      //Initialize Voltage Reference Module

CMCONbits.C1EVT= 0;  //Clear Comparator 1 Event
CMCONbits.C2EVT= 0;  //Clear Comparator 2 Event

asm volatile("repeat #40"); //Delay 10 µs
Nop();
```

34.8 REGISTER MAP

A summary of the registers associated with the Comparator module is provided in Table 34-3.

Table 34-3: Comparator Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMCON	CMIDL	—	C2EVT	C1EVT	C2EN	C1EN	C2OUTEN	C1OUTEN	C2OUT	C1OUT	C2INV	C1INV	C2NEG	C2POS	C1NEG	C1POS	0000
CVRCON	—	—	—	—	—	—	—	—	CVREN	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

34.9 DESIGN TIPS

Question 1: ***Why is not my voltage reference what I expect?***

Answer: Any variation of the voltage reference source will translate directly onto the CVREF pin. Also, ensure that you have correctly calculated (specified) the voltage divider which generates the voltage reference.

Question 2: ***Why is not my voltage reference at the expected level when I connect CVREF into a low-impedance circuit?***

Answer: The Voltage Reference module is not intended to drive large loads. A buffer must be used between the dsPIC® DSC device's CVREF pin and the load (see Figure 34-6).

34.10 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator module include the following:

Title	Application Note #
Make a Delta-Sigma Converter Using a Microcontroller's Analog Comparator Module	AN700
A Comparator Based Slope ADC	AN863

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F Family of devices.

34.11 REVISION HISTORY

Revision A (October 2007)

This is the initial release of this document.

Revision B (January 2009)

This revision includes the following updates:

- Figures:
  - Updated the inputs to the comparator in Figure 34-1.
- Note:
  - Added a note on CVRSRC in Figure 34-1.
  - Added a note on reference voltage CVREFIN in **34.4.1 “Input Signal Source”**.
- Sections:
  - Updated the incorrect description for Input offset in **34.3 “Comparator Operation”**.
  - Removed the incorrect description in **34.6.1 “Configuring the Comparator Voltage Reference”**.
- Tables:
  - Updated the incorrect table values in Table 34-1.
- Additional minor corrections such as language and formatting updates are incorporated throughout the document.