Section 30. Device Configuration

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33E/PIC24E devices.

Please consult the note at the beginning of the **"Special Features"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

30.1 INTRODUCTION

At their highest level of functionality, dsPIC33E/PIC24E devices integrate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

- Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options and changing them if needed during run time
- Device Identification – Allowing electronic confirmation of a device part number and revision level in the target application

30.2 DEVICE CONFIGURATION

The basic behavior and operation of dsPIC33E/PIC24E devices are set by the device Configuration bits. These bits allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In all dsPIC33E/PIC24E family devices, device Configuration bits are mapped to the device's program memory space, starting at location 0xF80000.

The method by which the Configuration bits are programmed differs between major device families. The details are discussed in **30.2.1 "Volatile Memory Implementation"** and **30.2.2 "Nonvolatile Memory Implementation"**. Refer the specific device data sheet for information on which method is implemented for your particular device.

Table 30-1 provides a list of the most common Configuration bit options. Note that this is not a comprehensive list; certain device families will have unique configuration options that are specific to its peripheral set. Each Configuration bit and its operation is described in the relevant section of the *"dsPIC33E/PIC24E Family Reference Manual"*. For more information on the Configuration bit mapping of a particular device, refer to the specific device data sheet.

Note: All of the bits that are described in Table 30-1 are not present on all the devices. Refer to the specific device data sheet for availability.

Table 30-1: Common dsPIC33E/PIC24E Device Configuration Bits

Configuration Bit	Function
GSS	Enables General Segment code protection.
GWRP	Enables write/erase protection for program memory.
FNOSC	Selects the initial (default) device oscillator (three bits, up to eight configuration options).
FWDTEN	Enables the Watchdog Timer.
IESO	Enables Two-Speed Start-up.
IOL1WAY	Selects one-time or unrestricted run-time changes to peripheral mapping.
JTAGEN	Enables dedicated JTAG port and disables corresponding I/O ports on designated pins.
OSCIOFNC	Selects function of OSC2 pin (I/O port or CLKO) in certain external oscillator modes.
POSCMD	Selects Primary (external) Oscillator configuration (two bits, four configurations).
WINDIS	Selects Windowed Operation mode for the Watchdog Timer.

30.2.1 Volatile Memory Implementation

In certain dsPIC33E/PIC24E devices, the Configuration bits are implemented as volatile memory; that is, the configuration data must be loaded each time the device is powered up. The actual configuration data is stored in the last several words at the end of the on-chip program memory space, known as the Configuration Bytes. During all types of device resets, the configuration data is automatically loaded from the Configuration Bytes to the proper Configuration registers. Refer to the specific device data sheet for implementation details.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once. After a bit is initially written, it cannot be written to again.

30.2.1.1 CONSIDERATIONS WHEN USING FLASH CONFIGURATION WORDS

The upper bytes of all the Flash Configuration Bytes in the program memory should always be '1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since the Configuration bits are not implemented in the corresponding locations, writing '1' to these locations has no effect on device operation.

Erasing the last page of program memory will automatically enable code protection, which prevents further reads or writes to program memory. As a result, it is not recommended to perform a page erase on the last page of memory where the Configuration bits are stored.

30.2.2 Nonvolatile Memory Implementation

With nonvolatile memory implementation, the Configuration bits are implemented as a physically separate block of nonvolatile memory. Once programmed, configuration data is maintained indefinitely. Although they act like fuses, the Configuration bits are freely reprogrammable. Since they lie inside the configuration memory space, the Configuration bits are not directly accessible; they can only be written and read using table read and table write instructions.

Unlike volatile memory implementation devices, the Configuration bits with nonvolatile memory implementation devices are organized into 8-bit registers, always the Least Significant Byte (LSB) of a program memory address. These Configuration registers are symbolically named according to their primary function (i.e., General Segment protection, Oscillator Selection, and so on). Table 30-2 lists the typical names and address of Configuration registers. Note that not all Configuration registers are implemented on all devices and certain devices with extended feature sets may have additional registers. In addition, there may be variations in naming or location of registers in certain devices. Refer to the specific device data sheet for more information.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options.

The implementation of the Configuration bits in devices using nonvolatile memory implementation makes a Configuration Mismatch (CM) error and Reset during full-speed operation virtually impossible. However, a severe device disturbance (such as an ESD event) during Sleep may disrupt the configuration safety check, resulting in a CM Reset.

Table 30-2: Typical Configuration Registers

Register Name	Primary Function	Address
FGS	General Segment Protect	0xF80004
FOSCEL	Oscillator Select	0xF80006
FOSC	Oscillator Configure	0xF80008
FWDT	Watchdog Timer Configure	0xF8000A
FPOR	Reset Configure	0xF8000C
FICD	Debug Configure	0xF8000E

30.3 DEVICE IDENTIFICATION

dsPIC33E/PIC24E devices have two read-only registers that provide device-specific identification information. These are located near the end of the program memory space, starting at 0xFF0000. Like the Flash Configuration Words, the Device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using table read instructions.

The DEVID register at 0xFF0000 (Register 30-1) identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register at 0xFF0002 (Register 30-2) identifies the particular silicon revision for that device in terms of major and minor revision levels (“letter and dot revision” format).

For any given family of dsPIC33E/PIC24E devices, the corresponding Family Silicon Errata and Data Sheet Clarification document provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a silicon revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in the associated Family Silicon Errata and Data Sheet Clarification document.

Register 30-1: DEVID: Device ID Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’
bit 15-0 **DEVID<15:0>:** Device ID Value bits

Register 30-2: DEVREV: Device Revision Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV<15:8>							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’
bit 15-0 **DEVREV<15:0>:** Device Revision Value bits

30.4 UNIT IDENTIFICATION

Some devices may feature programmable Unit ID registers (FUIDx), which can be programmed by the user with unique device information. Refer to the specific device data sheet for FUIDx availability and memory locations.

30.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33E/PIC24E product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Device Configuration include the following:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33E/PIC24E family of devices.

30.6 REVISION HISTORY

Revision A (November 2009)

This is the initial released version of this document.

Revision B (July 2010)

This revision includes major updates that have been incorporated throughout the document.

Revision C (June 2011)

This revision includes the following updates:

- Updated all paragraphs of **30.2.1 "Volatile Memory Implementation"** and replaced references to Configuration Words with Configuration Bytes
- Removed section 30.5 "In-Circuit Programming and Debugging"
- Changes to formatting and minor text updates were incorporated throughout the document

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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