Section 7. Reset

HIGHLIGHTS

This section of the manual contains the following topics:

7.1 INTRODUCTION

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Pin Reset
- SWR: RESET Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode/Uninitialized W Register Reset

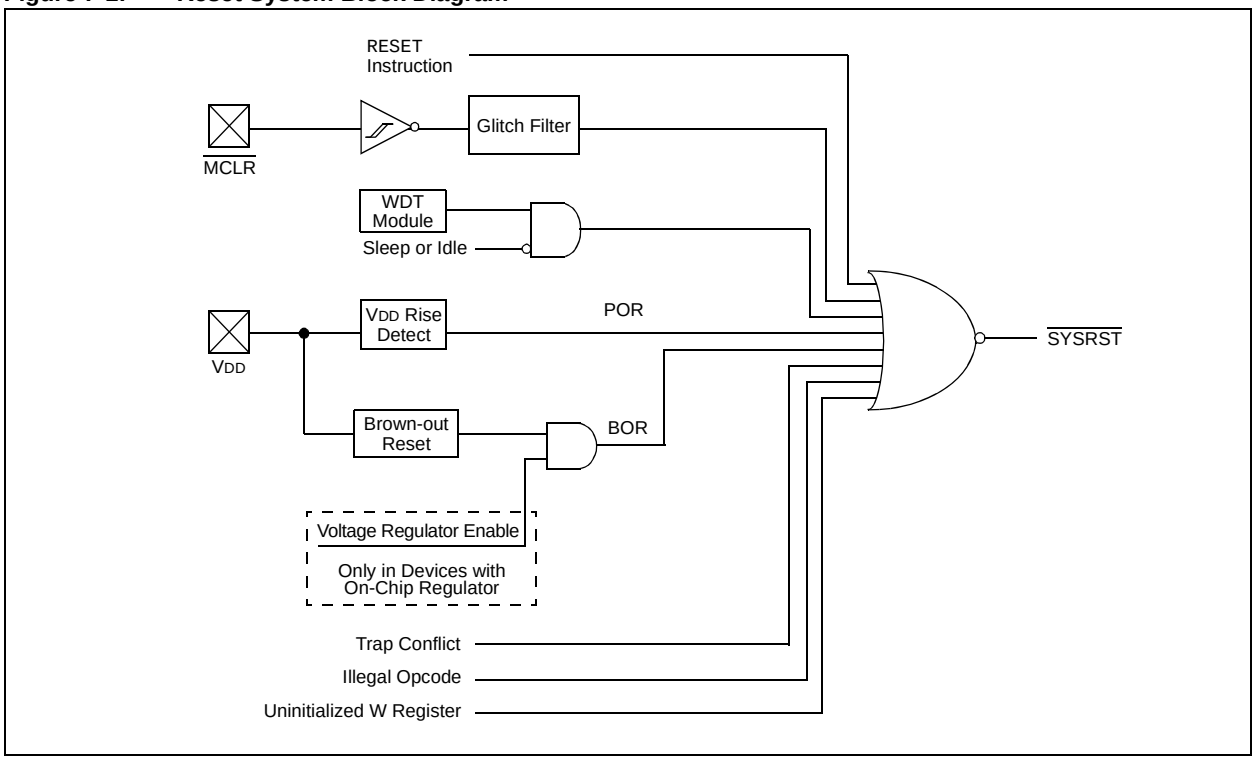
Figure 7-1 displays a simplified block diagram of the Reset module. Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known "Reset state". Most registers are unaffected by a Reset; their status is unknown on Power-on Reset (POR) and unchanged by all other Resets.

Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Resets will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A POR will clear all bits, except for the BOR and POR bits (RCON<1:0>) which are set. Users may set or clear any of the bits at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset.

The RCON register also has other bits associated with the Watchdog Timer (WDT) and device power-saving states. For more information on the function of these bits, refer to **Section 7.13.2 "Using the RCON Status Bits"**.

Figure 7-1: Reset System Block Diagram



Register 7-1: RCON: Reset Control Register(1)

R/W-0	R/W-0	U-0	R/W-0	U-0	R/C-0	U-0	R/W-0
TRAPR	IOPUWR	—	LVREN(2)	—	DPSLP(2)	CM	PMSLP(2,3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(4)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or an uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13 **Unimplemented:** Read as '0'

bit 12 **LVREN:** Low-Voltage Regulator Enabled(2)
1 = Regulated voltage supply provided solely by the low-voltage regulator during Sleep
0 = Regulated voltage supply provided by the main voltage regulator during Sleep

bit 11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Program Memory Power During Sleep bit(2)
1 = Deep Sleep has occurred
0 = Deep Sleep has not occurred

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **PMSLP:** Program Memory Power During Sleep Control bit(2,3)
1 = Program memory bias voltage remains powered during Sleep
0 = Program memory bias voltage is powered down during Sleep; voltage regulator enters Standby mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: Implemented on select PIC24F devices only; otherwise, unimplemented and read as '0'.

3: This bit is named VREGS in some earlier PIC24F devices, with a different description of the bit's functionality. Regardless of the name or description, its function in power reduction is identical in all devices.

4: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting. In devices with FWDTEN<1:0>, SWDTEN is only enabled when FWDTEN is '01'. Consult the specific device family data sheet for more information.

Register 7-1: RCON: Reset Control Register(1) (Continued)

bit 5 **SWDTEN:** Software WDT Enable/Disable bit(4)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device has been in Idle mode
0 = Device has not been in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred; the BOR is also set after a Power-on Reset
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: Implemented on select PIC24F devices only; otherwise, unimplemented and read as '0'.

3: This bit is named VREGS in some earlier PIC24F devices, with a different description of the bit's functionality. Regardless of the name or description, its function in power reduction is identical in all devices.

4: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting. In devices with FWDTEN<1:0>, SWDTEN is only enabled when FWDTEN is '01'. Consult the specific device family data sheet for more information.

Register 7-2: RCON2: Reset and System Control Register(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	r-0	R/CO-1	R/CO-1	R/CO-1	R/CO-0
—	—	—	r	VDDBOR(2)	VDDPOR(2,3)	VBPOR(2,4)	VBAT(2)
bit 7							bit 0

Legend:	CO = Clearable-Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **Reserved:** Maintain as '0'

bit 3 **VDDBOR**: VDD Brown-out Reset Flag bit(2)
1 = A VDD Brown-out Reset has occurred (set by hardware)
0 = A VDD Brown-out Reset has not occurred

bit 2 **VDDPOR**: VDD Power-on Reset Flag bit(2,3)
1 = A VDD Power-up Reset has occurred (set by hardware)
0 = A VDD Power-up Reset has not occurred

bit 1 **VBPOR**: VBPOR Flag bit(2,4)
1 = A VBAT POR occurred (no battery is connected to the VBAT pin or the battery is below the threshold voltage of the DSGPRx register)
0 = A VBAT POR has not occurred

bit 0 **VBAT**: VBAT Flag bit(2)
1 = A POR exit has occurred with the VBAT pin powered (battery connected to the VBAT pin)
0 = A POR exit from VBAT has not occurred

Note 1: This register is not implemented in all devices. Consult the device family's data sheet for more information.
2: This bit is set in hardware only. It can only be cleared in software.
3: Indicates VDD POR; the POR bit in the RCON register (RCON<0>) indicates the VDDCORE POR.
4: This bit is set when the device is originally powered up, even if power is present on VBAT.

7.2 CLOCK SOURCE SELECTION AT RESET

If clock switching is enabled (OSWEN), the system clock source at device Reset is chosen, as displayed in Table 7-1. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to **Section 6. "Oscillator"** in the *"PIC24F Family Reference Manual"* for further details.

Table 7-1: Oscillator Selection vs. Type of Reset (Clock Switching Enabled)

Reset Type	Clock Source Selected Based on
POR	Oscillator Configuration Bits FNOSC<2:0>
BOR	
$\overline{\text{MCLR}}$	COSC Control bits OSCCON<14:12>
WDTR	
SWR	
TRAPR	
IOPUWR	

7.3 POWER-ON RESET (POR)

The POR monitors the core power supply for adequate voltage levels to ensure proper chip operation. There are two threshold voltages associated with a POR. The first voltage is the device threshold voltage, VPOR. The device threshold voltage is the voltage at which the POR module becomes operable. The second voltage associated with a POR event is the POR circuit threshold voltage. Once the correct threshold voltage is detected, a power-on event occurs and the POR module hibernates to minimize current consumption.

A power-on event generates an internal POR pulse when a VDD rise is detected. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise rate specifications, refer to the **"Electrical Characteristics"** section of the specific device data sheet.

The POR pulse resets the POR timer and places the device in the Reset state. The POR also selects the device clock source identified by the oscillator Configuration bits. After the POR pulse is generated, the POR circuit inserts a small delay, TPOR, which is nominally 5 μs and ensures that internal device bias circuits are stable.

After the expiration of TPOR, a delay, TSTARTUP, is always inserted. TSTARTUP is applied every time the device resumes operation after any power-down. In the devices with an on-chip regulator, the TSTARTUP parameter depends on whether the on-chip voltage regulator is enabled or disabled. When the on-chip voltage regulator is enabled, there is a delay until the regulator can generate a proper voltage level, referred to as TVREG. During this time, code execution is disabled.

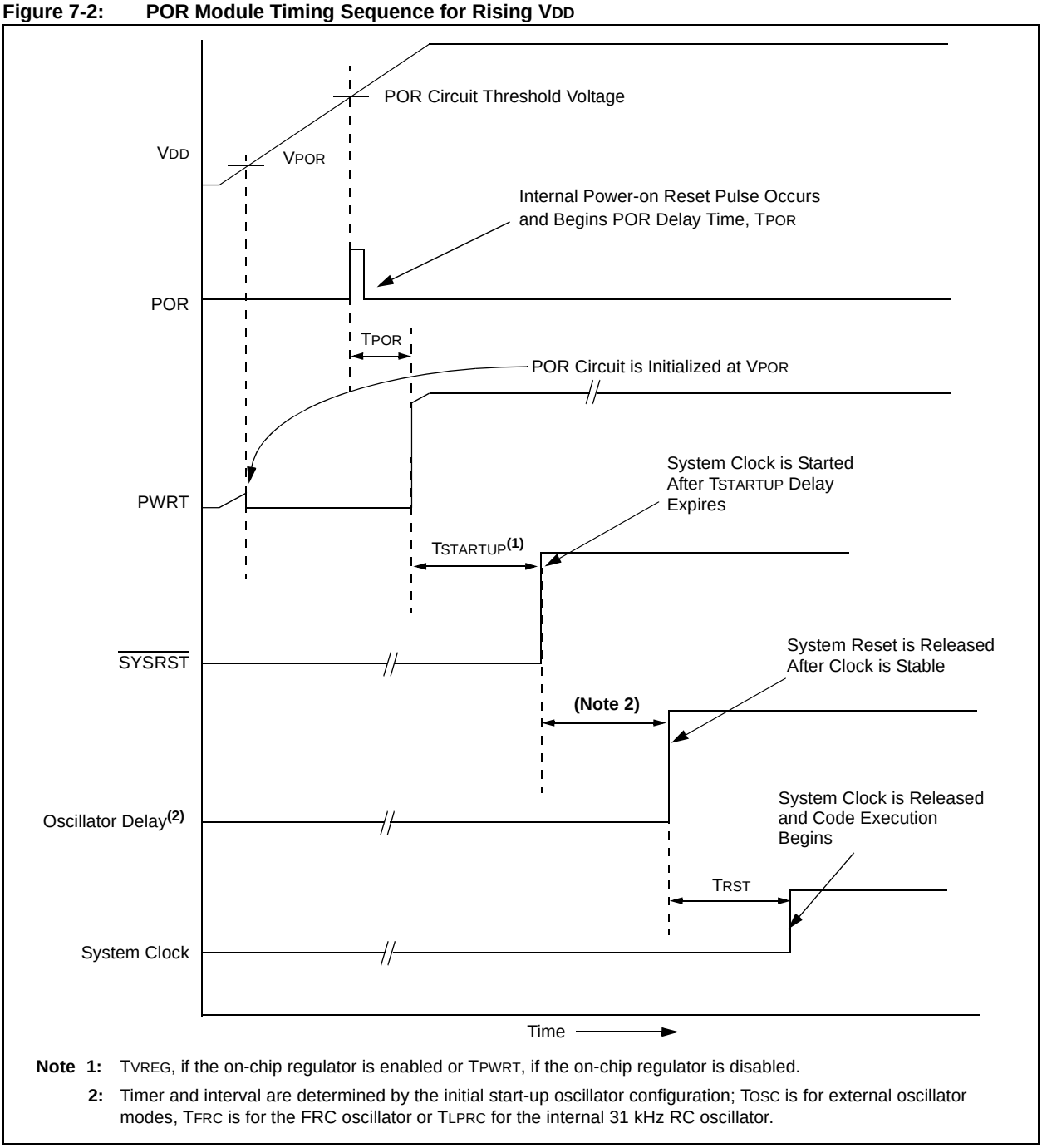
Note: Some device data sheets use the term, TPM (Program Memory Available Delay), in place of TVREG. The terms can be considered to be interchangeable.

If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed 64 ms nominal delay at device start-up. The PWRT is used to extend the duration of a power-up sequence when the on-chip voltage regulator is disabled and the core is supplied from an external power supply. Hence, the TSTARTUP delay can either be TVREG (for devices using an on-chip voltage regulator) or the Power-up Timer delay, TPWRT (for devices not using a regulator). The power-on event sets the BOR and POR status bits (RCON<1:0>). In some devices, the PWRT can be disabled by using the device Configuration bit. After TSTARTUP expires, an additional start-up time for the system clock (either TOST, TFRC or TLPRC, depending on the source) occurs while the clock source becomes stable.

Code execution is delayed further by a small delay, designated as TRST. The TRST delay is required to transfer the configuration values from the Flash Configuration Words (FCW) in the program memory into the Configuration registers, which occurs after any device Reset. SYSRST is released and the device is no longer held in Reset, but the device clocks are prevented from running during TRST, as depicted in Figure 7-2. Once all of the delays have expired, the system clock is released and code execution can begin.

Refer to **Section 7.16 "Electrical Specifications"** for more information on the values of the delay parameters.

Figure 7-2: POR Module Timing Sequence for Rising VDD



Note 1: TVREG, if the on-chip regulator is enabled or TPWRT, if the on-chip regulator is disabled.

2: Timer and interval are determined by the initial start-up oscillator configuration; TOSC is for external oscillator modes, TFRC is for the FRC oscillator or TLPRC for the internal 31 kHz RC oscillator.

Note:	When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user must ensure that the delay between the time power is first applied, and the time, SYSRST, becomes inactive is long enough to get all operating parameters within the specification.

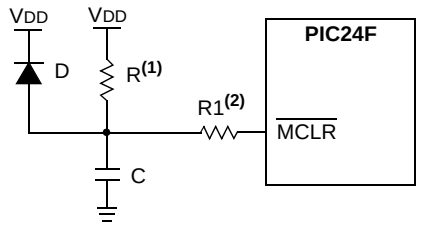
7.3.1 Using the POR Circuit

To take advantage of the POR circuit, just tie the MCLR pin directly to VDD. This will eliminate external RC components usually needed to create a POR delay. A minimum rise time for VDD is required. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for more information.

Depending on the application, a resistor may be required between the MCLR pin and VDD. This resistor can be used to decouple the MCLR pin from a noisy power supply rail.

Figure 7-3 displays a possible POR circuit for a slow power supply ramp up. The external POR circuit is only required if the device would exit Reset before the device VDD is in the valid operating range. The diode, D, helps discharge the capacitor quickly when VDD powers down.

Figure 7-3: External Power-on Reset Circuit (for Slow VDD Rise Time)



Note 1: The value of R should be low enough so that the voltage drop across it does not violate the VIH specification of the MCLR pin.

2: R1 limits any current flowing into MCLR from external capacitor, C, in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

7.4 MCLR RESET

Whenever the MCLR pin is driven low, the device asynchronously asserts SYSRST, provided the input pulse on MCLR is longer than a certain minimum width, SY10 (see **Section 7.16 "Electrical Specifications"**). When the MCLR pin is released, SYSRST is also released. The Reset vector fetch starts after the expiration of the TRST delay, starting from the SYSRST release. The processor continues to use the existing clock source that was in use before the MCLR Reset occurred. The EXTR status bit (RCON<7>) is set to indicate the MCLR Reset.

7.5 SOFTWARE RESET INSTRUCTION (SWR)

Whenever the RESET instruction is executed, the device asserts SYSRST. This Reset state does not re-initialize the clock. The clock source that is in effect prior to the RESET instruction remains in effect. SYSRST is released at the next instruction cycle, but the Reset vector fetch starts only after the TRST delay.

7.6 WATCHDOG TIMER RESET (WDTR)

Whenever a Watchdog Timer time-out occurs, the device asynchronously asserts SYSRST. The clock source remains unchanged. Note that a WDT time-out during Sleep or Idle mode will wake-up the processor, but NOT reset the processor. For more information, refer to **Section 9. "Watchdog Timer (WDT)"** in the *"PIC24F Family Reference Manual"*.

7.7 BROWN-OUT RESET (BOR)

When the on-chip regulator is enabled, PIC24F family devices have a simple brown-out capability. BOR is applicable only when the regulator is enabled. If the voltage supplied to the regulator is inadequate to maintain the tracking level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<0>).

Refer to **Section 7.16 "Electrical Specifications"** for further details.

7.7.1 Voltage Regulator Tracking Mode and Low-Voltage Detection

When enabled, the on-chip regulator provides a constant voltage to the digital core logic.(1,2)

Note 1:	Some devices have constantly enabled regulators. Refer to the specific device data sheet for more information.
2:	Refer to the device data sheet for the specific regulator voltage.

In order to prevent "brown-out" conditions when the voltage drops too low for the regulator, the regulator enters Tracking mode. In Tracking mode, the regulator output follows VDD with a typical voltage drop of 100 mV. When the device enters Tracking mode, it is no longer possible to operate at full speed. To provide information about when the device enters Tracking mode, the on-chip regulator includes a simple, Low-Voltage Detect (LVD) circuit. When VDD drops below full-speed operating voltage, the circuit sets the Low-Voltage Detect Interrupt Flag, LVDIF (IFS4<8>). This can be used to generate an interrupt and put the application into a Low-Power Operational mode or trigger an orderly shutdown. Low-Voltage Detection is only available when the regulator is enabled.

7.7.2 Detecting BOR

When the BOR is enabled, the BOR bit (RCON<1>) is always reset to '1' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both POR and BOR. This assumes that the POR bit is reset to '0' in the software immediately after any POR event. If the BOR bit is '1' while POR is '0', it can be reliably assumed that a BOR event has occurred.

7.7.3 Deep Sleep BOR (DSBOR) (Select Devices Only)

For devices with Deep Sleep capability, an independent Deep Sleep BOR (DSBOR) circuit provides simple BOR/POR protection during Deep Sleep operation. Rather than trigger a Reset in its own right, the DSBOR re-arms the regular POR circuit to ensure a device Reset if VDD drops below the POR threshold during Deep Sleep operation.

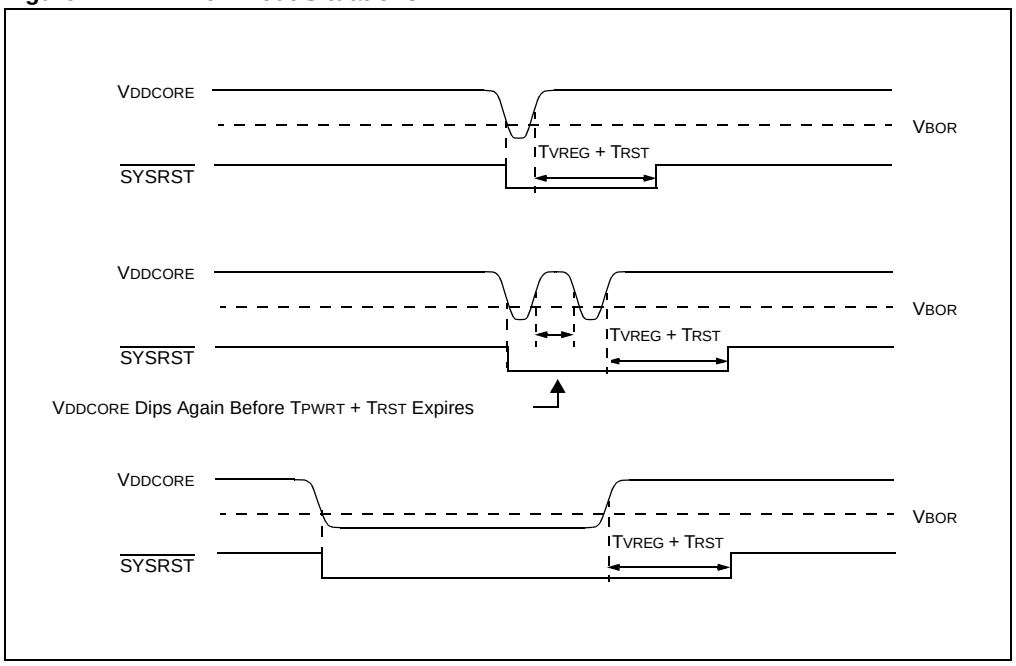
The DSBOR operates on a single trip point of 2.0V, nominal. Because it is designed for very low-current consumption, its accuracy may vary.

DSBOR events (BOR and POR) are monitored through the DSCON and DSWAKE registers, respectively. Refer to **Section 39. "Power-Saving Features with Deep Sleep"** for a more detailed discussion.

The DSBOR circuit can be selectively enabled or disabled using the DSBOREN Configuration bit. By default, the circuit is enabled.

Note:	As with other BOR events in other power-saving modes, both the POR and BOR are set when the device exits from the Deep Sleep mode.

Figure 7-4: Brown-out Situations



7.8 CONFIGURATION MISMATCH RESET

To maintain the integrity of the stored configuration values, all device Configuration bits are implemented as a complementary set of register bits. For each bit, as the actual value of the register is written as '1', a complementary value, '0', is stored in its corresponding background register and vice versa. The bit pairs are compared every time, including Sleep mode. During this comparison, if the Configuration bit values are not found opposite to each other, a Configuration Mismatch event is generated which causes a device Reset.

If a device Reset occurs as a result of a Configuration Mismatch, the CM status bit (RCON<9>) is set.

7.9 TRAP CONFLICT RESET (TCR)

A Trap Conflict Reset (TCR) occurs when a hard and a soft trap occur at the same time. The TRAPR status bit (RCON<15>) is set on this event. Refer to **Section 8. "Interrupts"** in the *"PIC24F Family Reference Manual"* for more information on traps.

7.10 ILLEGAL OPCODE RESET (IOPUWR)

A device Reset is generated if the device attempts to execute an illegal opcode value that was fetched from program memory. If a device Reset occurs as a result of an illegal opcode value, the IOPUWR status bit (RCON<14>) is set.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

7.11 UNINITIALIZED W REGISTER RESET

The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to. An attempt to use an uninitialized register as an Address Pointer causes a device Reset and sets the IOPUWR status bit (RCON<14>).

7.12 V_{BAT} MODE(1)

Entering V_{BAT} mode is made possible for the device by connecting an external power source (i.e., battery) to the VBAT pin. V_{BAT} mode is automatically triggered when the microcontroller's main power supply on V_{DD} fails. V_{BAT} mode can be entered from any of the other modes of operation (Run, Idle, Sleep, Deep Sleep). In addition, V_{BAT} mode is entered when V_{BAT} is powered from V_{DD}, if the V_{DDCORE} power is lost but the V_{DD} pin voltage is not. This maintains a few key systems at an extremely low-power draw until V_{DD} is restored. In order to successfully enter V_{BAT} mode, the device must have at least one BOR monitor active.

After running in V_{BAT} mode, the device automatically wakes up when V_{DD} is restored to the device. Wake-up occurs with a POR, after which the device starts executing code from the Reset vector. All SFRs, except the Deep Sleep semaphores, are reset to their POR values. If the RTCC was not configured to run during V_{BAT} mode, it will be reset upon exit from V_{BAT} mode. Wake-up timing is similar to that for a normal POR.

7.12.1 VBAT(1)

To differentiate a POR from a VBAT wake-up, check the VBAT bit (RCON2<0>). If the bit is set on a POR, then the device has returned from VBAT mode. The user must clear the VBAT bit after wake-up to ensure that future VBAT wake-up events are captured.

7.12.2 VBPOR(1)

The VBPOR bit (RCON2<1>) indicates if a VBAT POR has occurred. This entails the battery being removed, or VBAT falling below the operational level needed for the DSGPRx register(s). It is important to note that this bit will be set when the device is first powered on and will need to be cleared in order to capture authentic VBPOR events. The user will also have to clear the VBPOR bit after a VBAT POR in order to capture future POR events.

7.12.3 VDDPOR(1)

The VDDPOR bit (RCON2<2>) is set when the voltage on the VDD pin falls below the POR threshold. This is a different event from what is signified by the POR bit (RCON<0>), which is set when VDDCORE falls below the POR threshold. (See **Section 7.3 “Power-on Reset (POR)”** for more information on the Power-on Reset.)

7.12.4 VDDBOR(1)

This bit signifies when a BOR event has occurred. (See **Section 7.7 “Brown-out Reset (BOR)”** for more details.)

Note 1:	These bits are not implemented on all devices. Consult the device family’s data sheet for specific information regarding implementation.

7.13 REGISTERS AND STATUS BIT VALUES

Status bits from the RCON and RCON2 registers are set or cleared differently in different Reset situations, as indicated in Table 7-2.

Table 7-2: Status Bits, Their Significance and the Initialization Condition for the RCON Register

Condition	Program Counter	TRAPR	IOPUWR	DPSLP	EXTR	SWR	WDTO(1)	SLEEP(2)	IDLE(2)	CM	BOR	POR	VBAT(6)	VBPOR(6)	VDDPOR(6)	VDDBOR(6)
Power-on Reset	000000h	0	0	0	0	0	0	0	0	0	1	1	u	1(7)	1	1
RESET Instruction	000000h	u	u	u	u	1	u	u	u	u	u	u	u	u	u	u
Brown-out Reset	000000h	0	0	u	u	0	0	0	0	0	1	u	u	u	u	1
$\overline{MCLR}$ during Run Mode	000000h	u	u	u	1	u	u	u	u	u	u	u	u	u	u	u
$\overline{MCLR}$ during Idle Mode	000000h	u	u	u	1	u	0(1)	u	1(2)	u	u	u	u	u	u	u
$\overline{MCLR}$ during Sleep Mode	000000h	u	u	u	1	u	0(1)	1(2)	u	u	u	u	u	u	u	u
$\overline{MCLR}$ during Deep Sleep Mode(3)	000000h	0	0	1	1	0	0	0	0	0	1	1	u	u	1	1
WDT Time-out Reset during Run Mode	000000h	u	u	u	u	u	1	u	u	u	u	u	u	u	u	u
WDT Time-out Reset during Idle Mode	PC + 2	u	u	u	u	u	1	u	1(2)	u	u	u	u	u	u	u
WDT Time-out Wake-up during Sleep Mode	PC + 2	u	u	u	u	u	1	1(2)	u	u	u	u	u	u	u	u
Trap Event Reset	000000h	1	u	u	u	u	u	u	u	u	u	u	u	u	u	u
Illegal Opcode/ Uninitialized WREG	000000h	u	1	u	u	u	u	u	u	u	u	u	u	u	u	u
Configuration Word Mismatch Reset	000000h	u	u	u	u	u	u	u	u	1	u	u	u	u	u	u
Interrupt Exit from Idle Mode(4)	PC + 2(5)	u	u	u	u	u	u	u	1(2)	u	u	u	u	u	u	u
Interrupt Exit from Sleep Mode(4)	PC + 2(5)	u	u	u	u	u	0(2)	1(2)	u	u	u	u	u	u	u	u
Idle Mode (execute PWRSAV 1)	PC + 2	u	u	u	u	u	u	u	1	u	u	u	u	u	u	u
Sleep Mode (execute PWRSAV 0)	PC + 2	u	u	u	u	u	u	1	u	u	u	u	u	u	u	u
Deep Sleep Mode (set DSEN and execute PWRSAV 0)(3)	000000h	0	0	1	0	0	0	0	0	0	1	1	u	u	1	1
Wake from Battery Backup with Continuous VBAT	000000h	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1
Wake from VBAT mode with Discontinuous VBAT source	000000h	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
Power-on Reset on VDD	000000h	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

Legend: u = unchanged

Note 1: The PWRSAV instruction also clears the WDTO bit.

2: The state of the SLEEP and IDLE bits is defined by the previously executed PWRSAV instruction.

3: Select PIC24F devices only.

4: An interrupt's priority should not be changed while the interrupt is enabled. If a priority change is needed, clear the associated interrupt enable bit, select the new priority and set the interrupt to enable it.

5: The Program Counter (PC) is loaded with PC + 2 if the interrupt priority is less than, or equal to, the CPU interrupt priority level. The PC is loaded with the hardware vector address if the interrupt priority is greater than the CPU interrupt priority level.

6: This bit is not implemented on all devices. Consult the device family data sheet for more information.

7: This bit is set on the first POR; after that, it is set on VBAT POR events.

7.13.1 VBAT/Deep Sleep Status Bit Decoding

There are several unique Reset settings involving VBAT, VBPOR and DPSLP with regard to the device's Power-on Reset (POR), as indicated in Table 7-3.

Table 7-3: VBAT and Reset Flag Bit Operation

Flag Bit	Set By	Cleared By
VDDBOR (RCON2<3>)	POR, BOR	—
VDDPOR (RCON2<2>)	POR on VDD pin	—
VBPOR (RCON2<1>)	Battery failure in VBAT mode	—
VBAT (RCON<1>)	POR with VBAT	—

7.13.2 Using the RCON Status Bits

The user can read the RCON register after any device Reset to determine the cause of the Reset. Table 7-4 provides a summary of the Reset flag bit operation.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value, after a device Reset, will be meaningful.

Table 7-4: Reset Flag Bit Operation

Flag Bit(1)	Set By	Cleared By
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
DPSLP (RCON<10>)(2)	Deep Sleep Sequence (set DSEN, then execute PWRSAV #SLEEP instruction)	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)(1)	PWRSAV #SLEEP Instruction	POR, CLRWDT instruction
IDLE (RCON<2>)(1)	PWRSAV #IDLE Instruction	POR, CLRWDT instruction
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR on VDDCORE	—

Note 1: All Reset flag bits may be set or cleared by the user software. Setting a Reset flag does not trigger the associated Reset state.

2: This bit is only available on select PIC24F devices.

7.14 DEVICE RESET TO CODE EXECUTION START TIME

The delay between the end of a Reset event and when the device actually begins to execute code is determined by two main factors: the type of Reset and the system clock source coming out of the Reset. The code execution start time for various types of device Resets is summarized in Table 7-5. Individual delays are characterized in **Section 7.16 "Electrical Specifications"**.

For POR, the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR delay time (TPOR) and the TSTARTUP delay time expires. For BOR, $\overline{\text{SYSRST}}$ is released after the TSTARTUP delay time expires. For all other Resets, the system Reset signal, $\overline{\text{SYSRST}}$, is released immediately after the Reset condition is removed. For all Resets, the TRST delay starts after the $\overline{\text{SYSRST}}$ is released. The system clock starts at the expiration of TRST; code execution starts after the clock source is stable.

The time that the device actually begins to execute code also depends on the system oscillator delays, which include the Oscillator Start-up Timer delay (TOST) and the PLL lock time (TLOCK). The PLL lock is additive to (i.e., occurs after) the OST.

Table 7-5: Reset Delay Times for Various Device Resets

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR(6)	EC	TPOR + TRST + TSTARTUP	—	1, 2, 3
	FRC, FRCDIV	TPOR + TRST + TSTARTUP	TFRC	1, 2, 3, 4, 7
	LPRC	TPOR + TRST + TSTARTUP	TLPRC	1, 2, 3, 4
	ECPLL	TPOR + TRST + TSTARTUP	TLOCK	1, 2, 3, 5
	FRCPLL	TPOR + TRST + TSTARTUP	TFRC + TLOCK	1, 2, 3, 4, 5
	XT, HS, SOSC	TPOR + TRST + TSTARTUP	TOST	1, 2, 3, 6
	XTPLL, HSPLL	TPOR + TRST + TSTARTUP	TOST + TLOCK	1, 2, 3, 5, 6
BOR	EC	TRST + TSTARTUP	—	2, 3
	FRC, FRCDIV	TRST + TSTARTUP	TFRC	2, 3, 4, 7
	LPRC	TRST + TSTARTUP	TLPRC	2, 3, 4
	ECPLL	TRST + TSTARTUP	TLOCK	2, 3, 5
	FRCPLL	TRST + TSTARTUP	TFRC + TLOCK	2, 3, 4, 5
	XT, HS, SOSC	TRST + TSTARTUP	TOST + TLOCK	2, 3, 6
	XTPLL, HSPLL	TRST + TSTARTUP	TFRC + TLOCK	2, 3, 4, 5
All Others	Any Clock	TRST	—	2

Note 1: TPOR = Power-on Reset delay.

2: TRST = Internal State Reset time.

3: TSTARTUP = TVREG if the regulator is enabled or TPWRT (64 ms nominal) if the regulator is disabled.

4: TFRC and TLPRC = RC oscillator start-up times.

5: TLOCK = PLL lock time.

6: TOST = Oscillator Start-up Timer (OST). A 10-bit counter waits 1024 oscillator periods before releasing the oscillator clock to the system.

7: If Two-Speed Start-up is enabled, regardless of the primary oscillator selected, the device starts with FRC, and in such cases, FRC start-up time is valid.

Note: For nominal operating frequency and timing specifications, see **Section 7.16 "Electrical Specifications"**.For a particular device's specifications, refer to the **"Electrical Specifications"** section of the appropriate data sheet.

7.14.1 POR and Long Oscillator Start-up Times

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after SYSRST is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has NOT expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

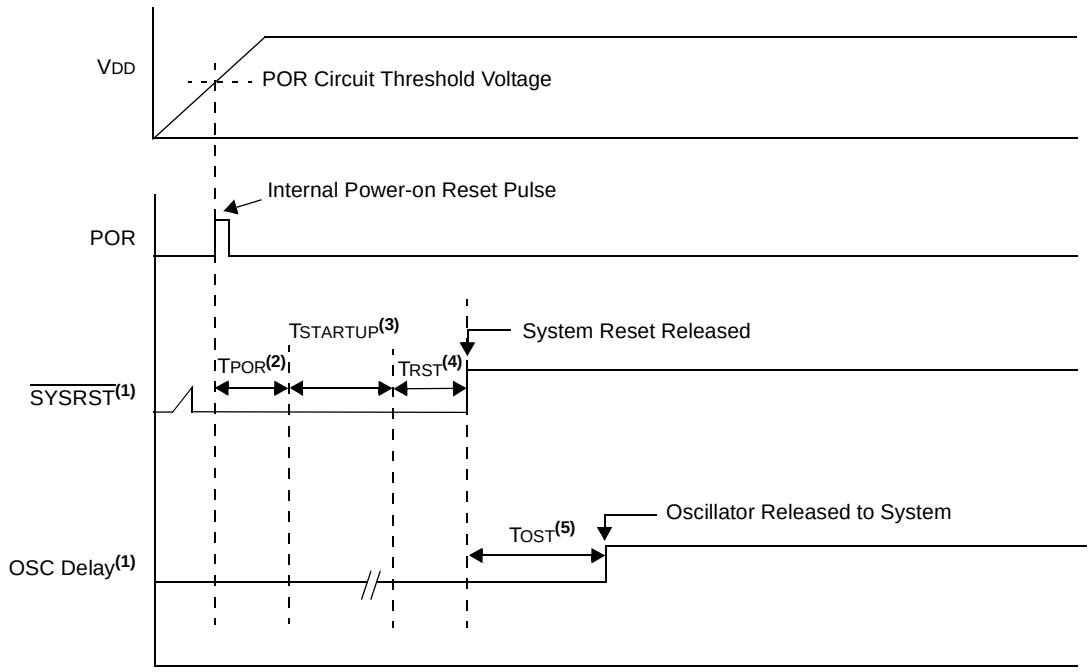
The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.14.2 Examples of Device Start-up Sequences

Figure 7-5 through Figure 7-8 depict graphical sequences for the delays associated with device Reset for several operating scenarios. The individual delays are characterized in **Section 7.16 "Electrical Specifications"**.

Figure 7-5 displays the delay time line when a crystal oscillator is used as the system clock. The internal POR pulse occurs at the VPOR threshold. TPOR, TSTARTUP and TRST delays occur after the internal POR pulse.

Figure 7-5: Device Reset Delay, Crystal (XT/HS/SOSC) Clock Source

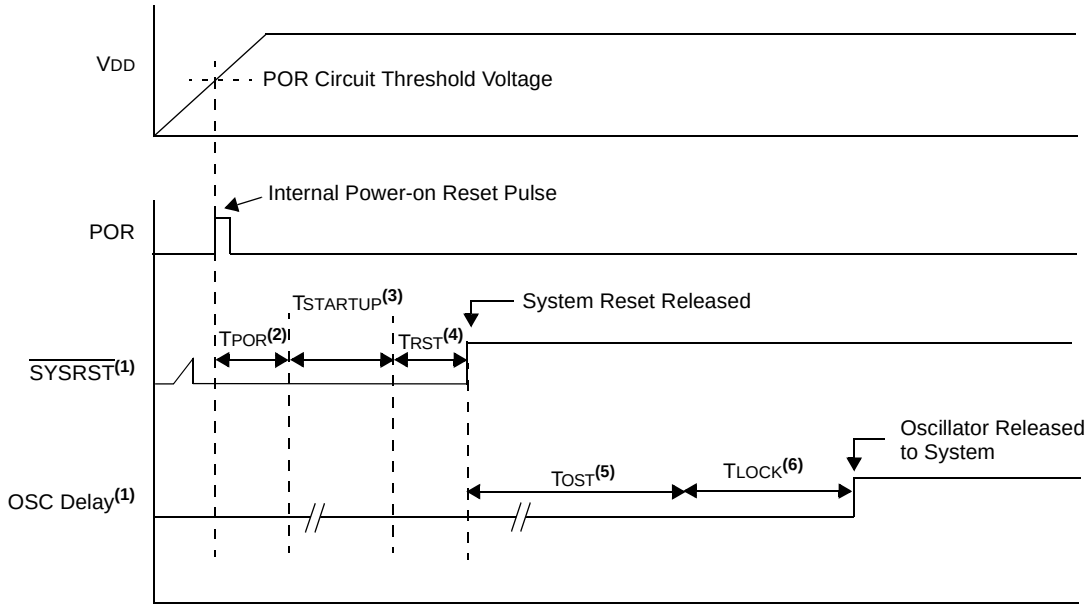


Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if the on-chip regulator is enabled or TPWRT if it is disabled.
4: TRST = Internal State Reset time.
5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

The Reset time line, displayed in Figure 7-6, is similar to that displayed in Figure 7-5, except that the PLL has been enabled, which increases the oscillator stabilization time.

The FSCM, if enabled, will begin to monitor the system clock after TFSCM expires. Figure 7-6 displays that the oscillator and PLL delays expire before the FSCM is enabled. However, it is possible that these delays may not expire until after FSCM is enabled. If a valid clock source is not available at this time, the device will automatically switch to the FRC oscillator and a clock failure trap will be generated. The user can switch to the desired crystal oscillator in the TSR.

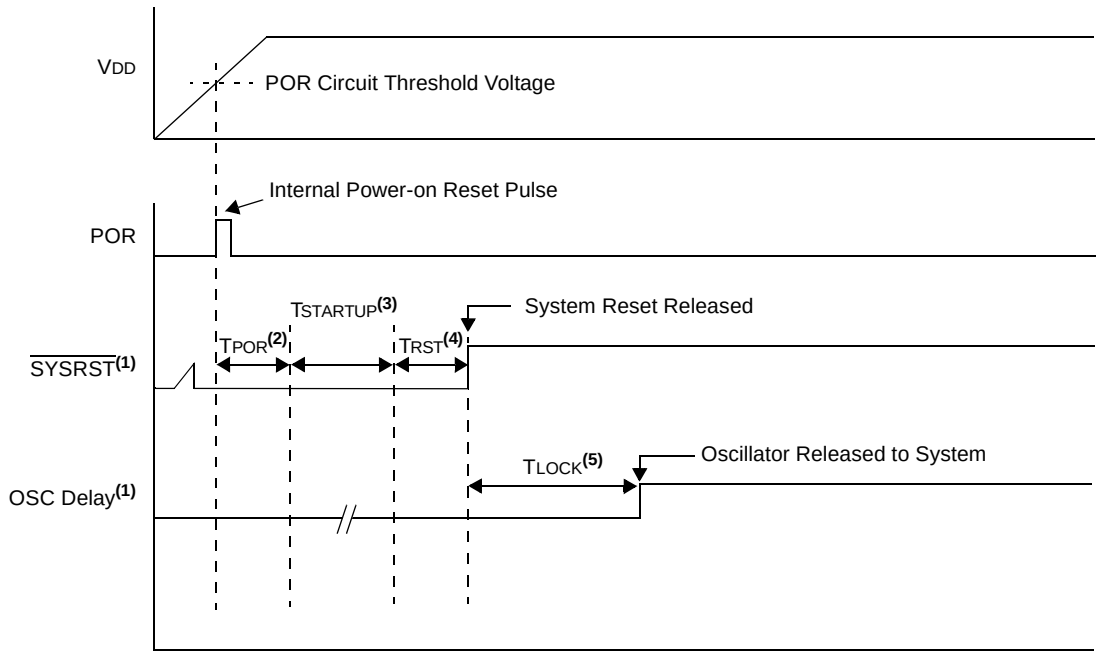
Figure 7-6: Device Reset Delay, Crystal (XT/HS/SOSC) + PLL Clock Source



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if the on-chip regulator is enabled or TPWRT if it is disabled.
4: TRST = Internal State Reset time.
5: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.
6: TLOCK is not inserted when PLL is disabled.

The Reset time line in Figure 7-7 displays an example of when the EC clock source is used as the system clock. This example is similar to the one provided in Figure 7-6, except that the Oscillator Start-up Timer delay, TOST, does not occur.

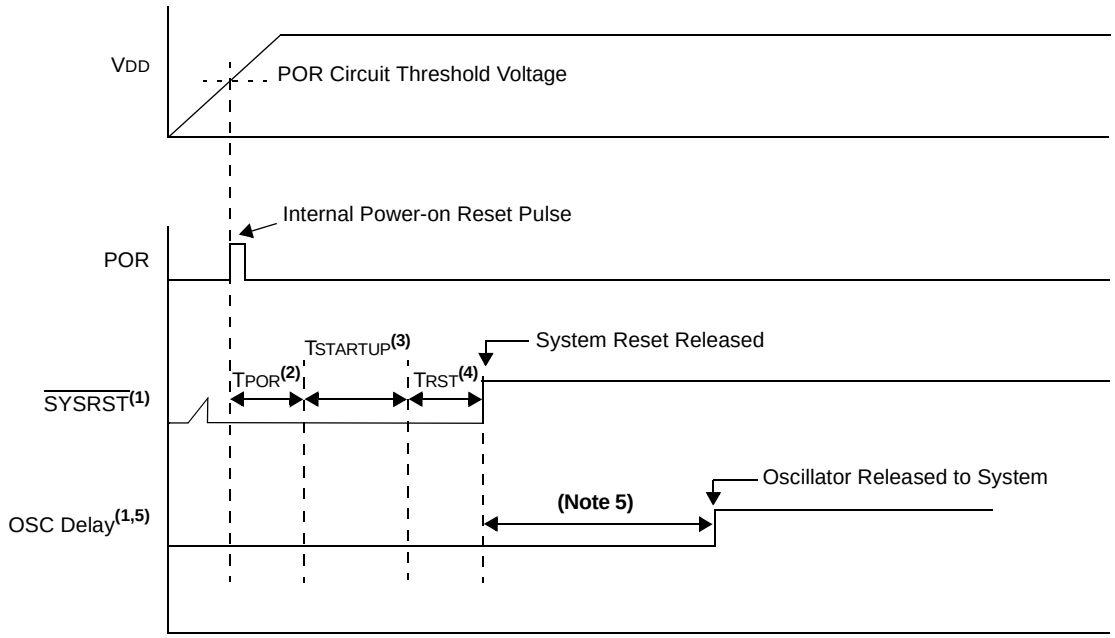
Figure 7-7: Device Reset Delay, EC and ECPLL Clocks



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if the on-chip regulator is enabled or TPWRT if it is disabled.
4: TRST = Internal State Reset time.
5: ECPLL mode shown. When PLL is disabled, TLOCK is not inserted. The system clock is released immediately following TRST.

The Reset time line displayed in Figure 7-8 provides an example of where the FRC or LPRC system clock source is selected. This sequence also applies if an external clock source is used with two-speed start-up enabled.

Figure 7-8: Device Reset Delay, FRC or LPRC Clocks



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if the on-chip regulator is enabled or TPWRT if it is disabled.
4: TRST = Internal State Reset time.
5: TFRC for the FRC oscillator, TLPRC for the internal 31 kHz RC oscillator.

7.15 SPECIAL FUNCTION REGISTER (SFR) RESET STATES

Most of the Special Function Registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in the corresponding section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the oscillator Configuration bits in the FOSC Device Configuration register (see Table 7-1).

7.16 ELECTRICAL SPECIFICATIONS

Figure 7-9: Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Characteristics

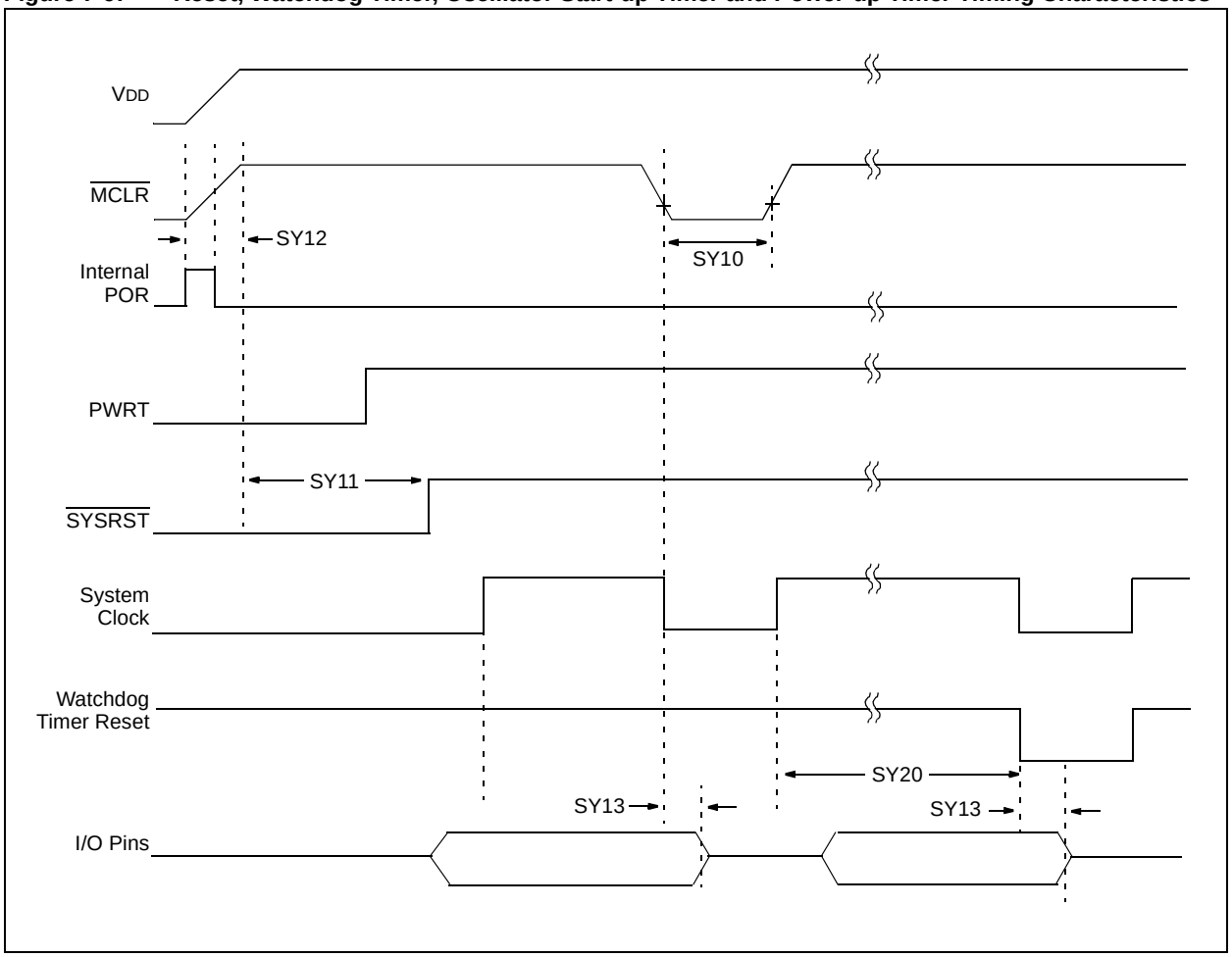


Table 7-6: Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out Reset Timing Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SY10	TmcL	MCLR Pulse Width (low)	2	—	—	µs	
SY11	TPWRT	Power-up Timer Period	—	64	—	ms	
SY12	TPOR	Power-on Reset Delay	1	5	10	µs	
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85 3.4	1.0 4.0	1.15 4.6	ms ms	1:32 prescaler 1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	µs	VDD ≤ VBOR, voltage regulator disabled

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

7.17 DESIGN TIPS

Question 1: ***How do I use the RCON registers?***

Answer: The initialization code after a Reset should examine RCON and RCON2 to confirm the source of the Reset. In some applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All Reset status bits in the RCON register should be cleared after reading them to ensure the RCON value provides meaningful results after the next device Reset.

Question 2: ***I initialized a W register with a 16-bit address; why does the device appear to reset when I attempt to use the register as an address?***

Answer: Because all data addresses are 16-bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two-byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an Address Pointer in an operation.

7.18 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Reset for PIC24F 'K' Devices are:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

7.19 REVISION HISTORY

Revision A (September 2006)

This is the initial released revision of this document.

Revision B (October 2008, not released)

Added Configurable BOR section.

Added material on Deep Sleep functionality and device Resets.

Revision C (March 2010)

Removed material on configurable BOR; this material has been incorporated into **Section 40, "Reset with Programmable BOR"** of the *"PIC24F Family Reference Manual"* (DS39728).

Removed all references to the Fail-Safe Clock Monitor and its role in device Resets.

Updated **Section 7.3 "Power-on Reset (POR)"** with a corrected description of the POR start-up sequence.

Replaced Figures 7-2, 7-5, 7-6, 7-7 and 7-8 with new start-up sequence diagrams.

Updated Tables 7-2 and 7-4 with new versions.

Other minor typographic corrections throughout the chapter.

Revision D (April 2011)

Added Register 7-2 RCON2 (Reset and System Control Register 2).

Added **Section 7.7.1 "Voltage Regulator Tracking Mode and Low-Voltage Detection"**.

Added **Section 7.12 "VBAT Mode"**, **Section 7.12.1 "VBAT"**, **Section 7.12.2 "VBPOR"**, **Section 7.12.3 "VDDPOR" and Section 7.12.4 "VDDBOR"**.

Added **Section 7.13.1 "VBAT/Deep Sleep Status Bit Decoding"**.

Replaced Table 7-2 with a new version that includes VBAT, VBPOR, VDDPOR and VDDBOR status bits.

Added Table 7-3: VBAT and Reset Flag Bit Operation.

Other typographical corrections throughout the chapter.

NOTES:

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