
Section 6. Oscillator

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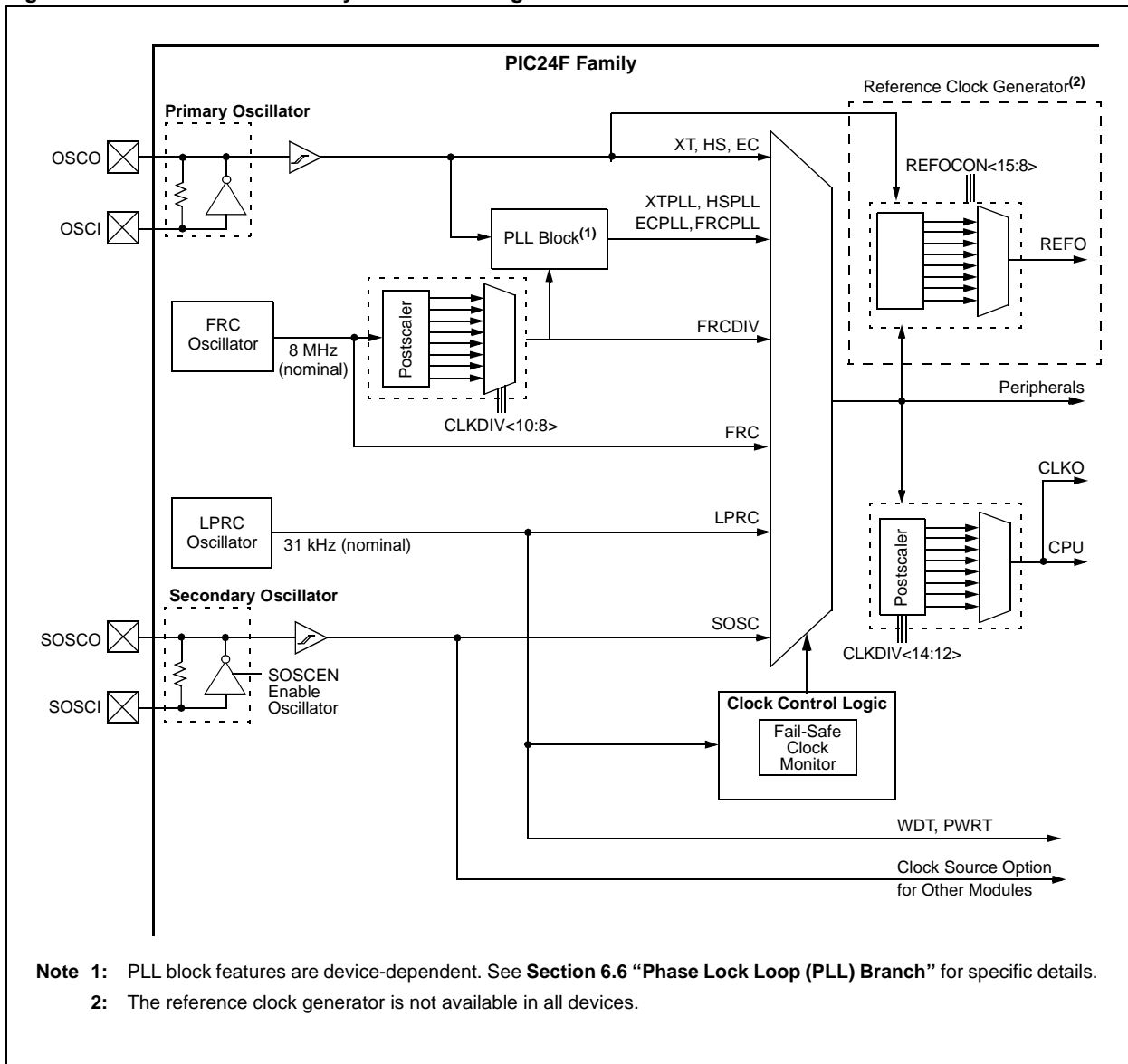
6.1 INTRODUCTION

This section describes the PIC24F oscillator system and its operation. The PIC24F oscillator system has the following modules and features:

- A total of four external and internal oscillator options as clock sources, providing up to 11 different clock modes
- An on-chip PLL block to boost internal operating frequency on select internal and external oscillator sources, or (in select devices only) to provide a precise clock source for special peripheral features
- Software-controllable switching between various clock sources
- Software-controllable postscaler for selective clocking of CPU for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- A programmable reference clock generator to provide a clock source with a wide range of frequencies for synchronizing external devices (select devices only)

A simplified diagram of the oscillator system is shown in Figure 6-1.

Figure 6-1: PIC24F General System Clock Diagram



6.2 CPU CLOCKING SCHEME

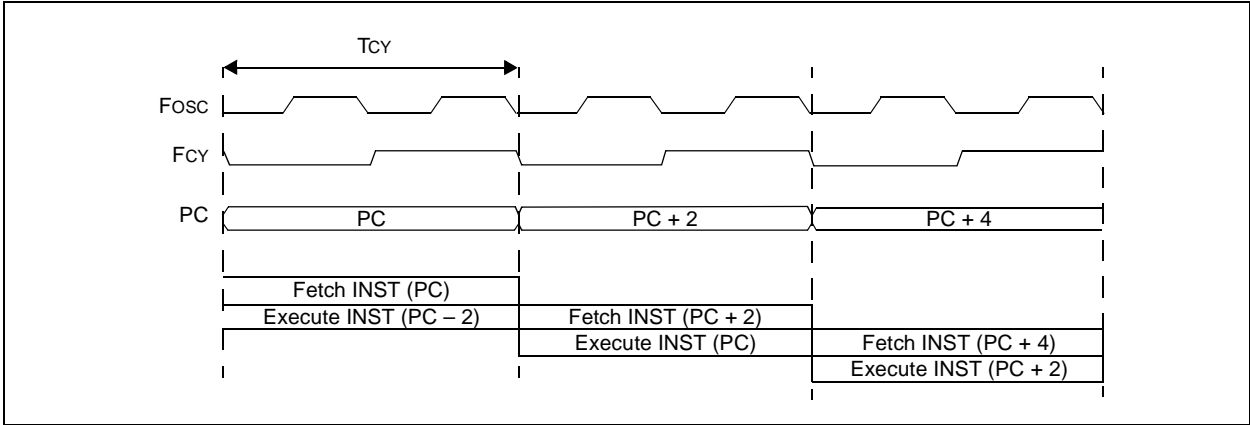
The system clock source can be provided by one of four sources:

- Primary Oscillator (POSC) on the OSC1 and OSC2 pins
- Secondary Oscillator (SOSC) on the SOSC1 and SOSCO pins
- Internal Fast RC Oscillator (FRC)
- Internal Low-Power RC Oscillator (LPRC)

The Primary Oscillator and FRC sources have the option of using the internal 4x PLL. The frequency of the FRC clock source can optionally be reduced by the programmable clock divider. The selected clock source generates the processor and peripheral clock sources.

The processor clock source is divided by two to produce the internal instruction cycle clock, F_{cy}. In this document, the instruction cycle clock is also denoted by F_{osc}/2. The timing diagram in Figure 6-2 shows the relationship between the processor clock source and instruction execution. The internal instruction cycle clock, F_{osc}/2, can be provided on the OSC2 I/O pin for some operating modes of the Primary Oscillator.

Figure 6-2: Clock or Instruction Cycle Timing



6.3 OSCILLATOR CONFIGURATION

The oscillator source (and operating mode) that is used at a device Power-on Reset (POR) event is selected using Configuration bit settings. The oscillator Configuration bit settings are in the Configuration registers located in the program memory (refer to the specific product data sheet for further details). The Primary Oscillator Configuration bits, POSCMD<1:0> (Configuration Word 2<1:0>), and oscillator Configuration bits, FNOSC<2:0> (Configuration Word 2<10:8>), select the oscillator source that is used at a POR. The FRC Oscillator with Postscaler (FRCDIV) is the default (unprogrammed) selection. The Secondary Oscillator, or one of the internal oscillators, may be chosen by programming these bit locations.

The Configuration bits allow users to choose between 11 different clock modes, shown in Table 6-1.

Table 6-1: Configuration Bit Values for Clock Selection

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	Note
Fast RC Oscillator with Postscaler (FRCDIV)	Internal	11	111	1, 2
(Reserved)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	11	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	11	100	1
Primary Oscillator (HS) with PLL Module (HSPLL)	Primary	10	011	—
Primary Oscillator (XT) with PLL Module (XTPLL)	Primary	01	011	—
Primary Oscillator (EC) with PLL Module (ECPLL)	Primary	00	011	—
Primary Oscillator (HS)	Primary	10	010	—
Primary Oscillator (XT)	Primary	01	010	—
Primary Oscillator (EC)	Primary	00	010	—
Fast RC Oscillator with PLL Module (FRCPLL)	Internal	11	001	1
Fast RC Oscillator (FRC)	Internal	11	000	1

Note 1: OSC2 pin function is determined by the OSCIOFCN Configuration bit.

2: Default oscillator mode for an unprogrammed (erased) device.

6.3.1 Clock Switching Mode Configuration Bits

The FCKSM Configuration bits (Configuration Word 2<7:6>) are used to jointly configure device clock switching and the FSCM. Clock switching is enabled only when FCKSM1 is programmed ('0'). The FSCM is enabled only when FCKSM<1:0> are both programmed ('00').

6.3.2 OSC1 and OSC2 Pin Functions in Non-Crystal Modes

When the Primary Oscillator on OSC1 and OSC2 is not configured as the clock source (POSCMD<1:0> = 11), the OSC1 pin is automatically reconfigured as a digital I/O. In this configuration, as well as when the Primary Oscillator is configured for EC mode (POSCMD<1:0> = 00), the OSC2 pin can also be configured as a digital I/O by programming the OSCIOFCN Configuration bit (Configuration Word 2<5>).

When OSCIOFCN is unprogrammed ('1'), a Fosc/2 clock output is available on OSC2 for testing or synchronization purposes. With OSCIOFCN programmed ('0'), the OSC2 pin becomes a general purpose I/O pin. In both of these configurations, the feedback device between OSC1 and OSC2 is turned off to save current.

6.4 CONTROL REGISTERS

The operation of the oscillator is controlled by three (or up to five for some devices) Special Function Registers (SFRs):

- OSCCON
- CLKDIV
- OSCTUN
- REFOCON (select devices only)
- CLKDIV2 (select devices only)

6.4.1 Oscillator Control Register (OSCCON)

The OSCCON register (Register 6-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources.

The COSC status bits are read-only bits that indicate the current oscillator source the device is operating from. The COSC bits default to the Internal Fast RC Oscillator with Postscaler (FRCDIV), configured for 4 MHz, on a Power-on Reset (POR) and Master Clear Reset (MCLR). A clock switch will automatically be performed to the new oscillator source selected by the FNOSC Configuration bits (Configuration Word 2<10:8>). The COSC bits will change to indicate the new oscillator source at the end of a clock switch operation.

The NOSC status bits select the clock source for the next clock switch operation. On POR and MCLR, these bits automatically select the oscillator source defined by the FNOSC Configuration bits. These bits can be modified by software.

Note: An unlock sequence must be performed before writing to OSCCON. Refer to **Section 6.11.2 “Oscillator Switching Sequence”** for more information.

Setting the CLKLOCK bit (OSCCON<7>) prevents clock switching if the FCKSM1 Configuration bit is set. If the FCKSM1 bit is clear, the CLKLOCK bit state is ignored and clock switching can occur.

The IOLOCK bit (OSCCON<6>) is used to unlock the Peripheral Pin Select (PPS) feature; it has no function in the system clock's operation.

The LOCK status bit (OSCCON<5>) is read-only and indicates the status of the PLL circuit. It is set when the PLL achieves a frequency lock and is RESET when a valid clock switching sequence is initiated. It reads as '0' whenever the PLL is not used as part of the current clock source.

The CF status bit (OSCCON<3>) is a readable/clearable status bit that indicates a clock failure; it is reset whenever a valid clock switch occurs.

The POSCEN bit (OSCCON<2>) is used to control the operation of the Primary Oscillator in Sleep mode. Setting this bit bypasses the normal automatic shutdown of the oscillator whenever Sleep mode is invoked.

The SOSSEN control bit (OSCCON<1>) is used to enable or disable the 32 kHz crystal SOSC Oscillator.

The OSWEN control bit (OSCCON<0>) is used to initiate a clock switch operation. OSWEN is cleared automatically after a successful clock switch, any redundant clock switch and by the FSCM module after the switch to the FRC has completed.

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Register 6-1: OSCCON: Oscillator Control Register

U-0	R-0	R-0	R-0	U-0	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾	R/W-x ⁽¹⁾
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

R/SO-0	R/W-0	R-0 ⁽³⁾	U-0	R/CO-0	R/W-0	R/W-0	R/W-0
CLKLOCK	IOLOCK ⁽²⁾	LOCK	—	CF	POSCEN ⁽⁴⁾	SOSCEN	OSWEN
bit 7							bit 0

Legend:	CO = Clear Only bit	SO = Set Only bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

- 111 = Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = Reserved
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽¹⁾

- 111 = Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = Reserved
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Selection Lock Enabled bit

If FSCM is enabled (FCKSM1 = 1):

- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit

If FSCM is disabled (FCKSM1 = 0):

Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **IOLOCK:** I/O Lock Enable bit⁽²⁾

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit⁽³⁾

- 1 = PLL module is in lock or PLL module start-up timer is satisfied
- 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

Note 1: Reset values for these bits are determined by the FNOSC Configuration bits.

Note 2: IOLOCK is available only on devices with Peripheral Pin Select; refer to the particular device data sheet for more information. IOLOCK can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1', once the IOLOCK bit is set, it cannot be cleared.

Note 3: Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

Note 4: POSCEN is only available on select device families; refer to the particular device data sheet for more information.

Register 6-1: OSCCON: Oscillator Control Register (Continued)

bit 3	CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected
bit 2	POSCEN: Primary Oscillator Sleep Enable bit ⁽⁴⁾ 1 = Primary Oscillator continues to operate during Sleep mode 0 = Primary Oscillator is disabled during Sleep mode
bit 1	SOSCCN: 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enable Secondary Oscillator 0 = Disable Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Initiate an oscillator switch to the clock source specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Reset values for these bits are determined by the FNOSC Configuration bits.
- 2:** IOLOCK is available only on devices with Peripheral Pin Select; refer to the particular device data sheet for more information. IOLOCK can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1', once the IOLOCK bit is set, it cannot be cleared.
- 3:** Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.
- 4:** POSCEN is only available on select device families; refer to the particular device data sheet for more information.

6.4.2 Clock Divider Register (CLKDIV)

The Clock Divider register (Register 6-2) controls the features associated with Doze mode, as well as the postscaler for the FRC Oscillator.

The ROI bit (CLKDIV<15>) allows an interrupt to exit Doze mode and automatically selects a 1:1 ratio for the processor and peripheral clocks. The DOZEN bit (CLKDIV<11>) is cleared after the exit from Doze mode. Clearing the ROI bit prevents interrupts from affecting Doze mode.

The DOZE bits (CLKDIV<14:12>) select the ratio of processor clocks to peripheral clocks. The range is software-selectable between 1:1 to 1:128. The MCLR and PORs default to the 1:1 ratio. This feature allows the CPU to consume less power without disrupting the peripheral's operations.

Setting the DOZEN bit places the device into Doze mode and engages the processor clock postscaler. This bit is cleared when the ROI bit is set and an interrupt occurs.

The RCDIV bits (CLKDIV<10:8>) select the postscaler option for the FRC Oscillator output, allowing users to choose a lower clock frequency than the nominal 8 MHz. This option is described in **Section 6.8.2 "FRC Postscaler Mode (FRCDIV)"** and **Section 6.8.3 "FRC Oscillator with PLL Mode (FRCPLL)"**.

For PIC24F devices featuring USB functionality (for example, the PIC24FJ256GB110 family), the CPDIV<1:0> bits (CLKDIV<7:6>) select the system clock speed when the USB module is enabled and active. Their function is covered in more detail in **Section 6.6.2 "96 MHz PLL Block"**.

Where available, the PLEN bit (CLKDIV<5>) enables the 96 MHz PLL module that generates the 96 MHz clock source for USB and graphics controller modules. The G1CLKSEL bit (CLKDIV<4>) further selects the clock source for the graphics controller module. This selection is also described in **Section 6.6.2 "96 MHz PLL Block"**.

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Register 6-2: CLKDIV: Clock Divider Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2	DOZE1	DOZE0	DOZEN ⁽¹⁾	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
CPDIV1 ⁽²⁾	CPDIV0 ⁽²⁾	PLLEN ⁽²⁾	G1CLKSEL ⁽²⁾	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ROI:** Recover on Interrupt bit
 1 = Interrupts clear the DOZEN bit and reset the CPU peripheral clock ratio to 1:1
 0 = Interrupts have no effect on the DOZEN bit
- bit 14-12 **DOZE<2:0>:** CPU Peripheral Clock Ratio Select bits
 111 = 1:128
 110 = 1:64
 101 = 1:32
 100 = 1:16
 011 = 1:8
 010 = 1:4
 001 = 1:2
 000 = 1:1
- bit 11 **DOZEN:** DOZE Enable bit⁽¹⁾
 1 = When the DOZE<2:0> bits specify the CPU peripheral clock ratio
 0 = The CPU peripheral clock ratio set to 1:1
- bit 10-8 **RCDIV<2:0>:** FRC Postscaler Select bits
 111 = 31.25 kHz (divide-by-256)
 110 = 125 kHz (divide-by-64)
 101 = 250 kHz (divide-by-32)
 100 = 500 kHz (divide-by-16)
 011 = 1 MHz (divide-by-8)
 010 = 2 MHz (divide-by-4)
 001 = 4 MHz (divide by 2)
 000 = 8 MHz (divide by 1)
- bit 7-6 **CPDIV<1:0>:** System Clock Select bits⁽²⁾
 11 = 4 MHz (divide-by-8)⁽³⁾
 10 = 8 MHz (divide-by-4)⁽³⁾
 01 = 16 MHz (divide-by-2)
 00 = 32 MHz (divide-by-1)
- bit 5 **PLLEN:** 96 MHz PLL Enable bit⁽²⁾
 The 96 MHz PLL must be enabled when the USB or the graphics controller module is enabled; This control bit can be overridden by Configuration bits in some PIC24F devices. Refer to **Section 6.6.2 “96 MHz PLL Block”** for details.
 1 = Enable the 96 MHz PLL for USB and/or graphics controller operation
 0 = Disable the 96 MHz PLL

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.
Note 2: These bits are available on USB-enabled or graphics-enabled devices only.
Note 3: These system clock options are not compatible with the operation of the USB module. They may be used in those instances when the PLL branch is selected as a clock source and the USB module is disabled.

Register 6-2: CLKDIV: Clock Divider Register (Continued)

- bit 4 **G1CLKSEL:** Display Controller Module Clock Select bit⁽²⁾
1 = Use the 96 MHz clock as the graphics controller module clock (graphics clock option 1 branch, refer to Figure 6-8)
0 = Use the 48 MHz clock as graphics controller module clock (graphics clock option 2 branch, refer to Figure 6-8)
- bit 3-0 **Unimplemented:** Read as '0'

- Note 1:** This bit is automatically cleared when the ROI bit is set and an interrupt occurs.
- 2:** These bits are available on USB-enabled or graphics-enabled devices only.
- 3:** These system clock options are not compatible with the operation of the USB module. They may be used in those instances when the PLL branch is selected as a clock source and the USB module is disabled.

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6.4.3 Oscillator Tuning Register (OSCTUN)

The FRC Oscillator Tuning register (Register 6-3) allows the user to fine tune the FRC Oscillator. Refer to the data sheet of the specific device for further information regarding the FRC Oscillator tuning.

The tuning response of the FRC Oscillator may not be monotonic or linear; the next closest frequency may be offset by a number of steps. It is recommended that users try multiple values of OSCTUN to find the closest value to the desired frequency.

Register 6-3: OSCTUN: FRC Oscillator Tuning Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at all Resets	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Maximum frequency deviation

011110 =

.

.

.

000001 =

000000 = Center frequency; oscillator is running at factory calibrated frequency

111111 =

.

.

.

100001 =

100000 = Minimum frequency deviation

6.4.4 Reference Clock Output Control Register (REFOCON)

For PIC24F devices that include a reference clock output generator, the REFOCON register (Register 6-4) controls the operations of this feature.

Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) select one of 16 different clock divider options.

The ROSSLP and ROSEL bits (REFOCON<13:12>) control the clock source for the reference output. The ROSEL bit determines if the Primary Oscillator on OSC1 and OSC2, or on the current system clock source, provides the reference clock output. If the Primary Oscillator is selected, the ROSSLP bit determines its availability in Sleep mode.

Additional information is provided in **Section 6.13 “Reference Clock Output Generator”**.

Register 6-4: REFOCON: Reference Oscillator Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **ROEN:** Reference Oscillator Output Enable bit
1 = Reference oscillator enabled on REFO pin
0 = Reference oscillator disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ROSSLP:** Reference Oscillator Output Stop in Sleep bit
1 = Reference oscillator continues to run in Sleep
0 = Reference oscillator is disabled in Sleep
- bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Primary Oscillator used as the base clock. Note that the crystal oscillator must be enabled using the FOSC<2:0> bits; the crystal maintains the operation in Sleep mode
0 = System clock is used as the base clock; the base clock reflects any clock switching of the device
- bit 11-8 **RODIV<3:0>:** Reference Oscillator Divisor Select bits
1111 = Base clock value divided by 32,768
1110 = Base clock value divided by 16,384
1101 = Base clock value divided by 8,192
1100 = Base clock value divided by 4,096
1011 = Base clock value divided by 2,048
1010 = Base clock value divided by 1,024
1001 = Base clock value divided by 512
1000 = Base clock value divided by 256
0111 = Base clock value divided by 128
0110 = Base clock value divided by 64
0101 = Base clock value divided by 32
0100 = Base clock value divided by 16
0011 = Base clock value divided by 8
0010 = Base clock value divided by 4
0001 = Base clock value divided by 2
0000 = Base clock value
- bit 7-0 **Unimplemented:** Read as '0'

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6.4.5 Clock Divider Register 2 (CLKDIV2)

The Clock Divider 2 register (Register 6-5) is provided to PIC24F devices that have a graphics controller module. This register controls the frequency of the clock input to the display module interface in the display controller. The frequency selection is controlled by writing to the selector bits (GCLKDIV<6:0>). To cover the various frequency range of different displays, the clock division starts from a divide-by-1 value, incrementing initially by 0.25. Half way through the 128 possible values, the clock increases to 0.50, then after 32 values, increases to 1. The range covered for a 96 MHz input is from 1.5 MHz to 96 MHz, and for 48 MHz input, from 750 kHz to 48 MHz.

Register 6-5: CLKDIV2: Clock Divider Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
GCLKDIV6 ⁽¹⁾	GCLKDIV5 ⁽¹⁾	GCLKDIV4 ⁽¹⁾	GCLKDIV3 ⁽¹⁾	GCLKDIV2 ⁽¹⁾	GCLKDIV1 ⁽¹⁾	GCLKDIV0 ⁽¹⁾	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at all Resets	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-9 **GCLKDIV<6:0>**: Display Module Interface Clock Divider Selection bits⁽¹⁾
 Values are based on a 96 MHz clock source set by G1CLKSEL (CLKDIV<4>) = 1. When the 48 MHz clock source is selected, G1CLKSEL (CLKDIV<4>) = 1, all values are divided by 2.
 0000000 = (0) 96.00 MHz (divide-by-1)
 0000001 = (1) 76.80 MHz (divide-by-1.25); from here increment the divisor by 0.25
 0000010 = (2) 64.00 MHz (divide-by-1.5)
 0000011 = (3) 54.86 MHz (divide-by-1.75)
 .
 .
 .
 0111111 = (63) 5.73 MHz (divide-by-16.75)
 1000000 = (64) 5.65 MHz (divide-by-17.00); from here increment the divisor by 0.50
 1000000 = (65) 5.49 MHz (divide-by-17.50)
 .
 .
 .
 1011111 = (95) 2.95 MHz (divide-by-32.50)
 1100000 = (96) 2.91 MHz (divide-by-33); from here increment the divisor by 1
 1100001 = (97) 2.82 MHz (divide-by-34)
 .
 .
 .
 1111110 = (126) 1.52 MHz (divide-by-63)
 1111111 = (127) 1.50 MHz (divide-by-64)

bit 8-0 **Unimplemented:** Read as '0'

Note 1: These bits take effect only when the 96 MHz PLL is enabled.

6.5 PRIMARY OSCILLATOR (POSC)

The Primary Oscillator is available on the OSC1 and OSC2 pins of the PIC24F family. In general, the Primary Oscillator can be configured for an external clock input or an external crystal. Further details of the Primary Oscillator operating modes are described in subsequent sections. The Primary Oscillator has up to 6 operating modes, summarized in Table 6-2.

Table 6-2: Primary Oscillator Operating Modes

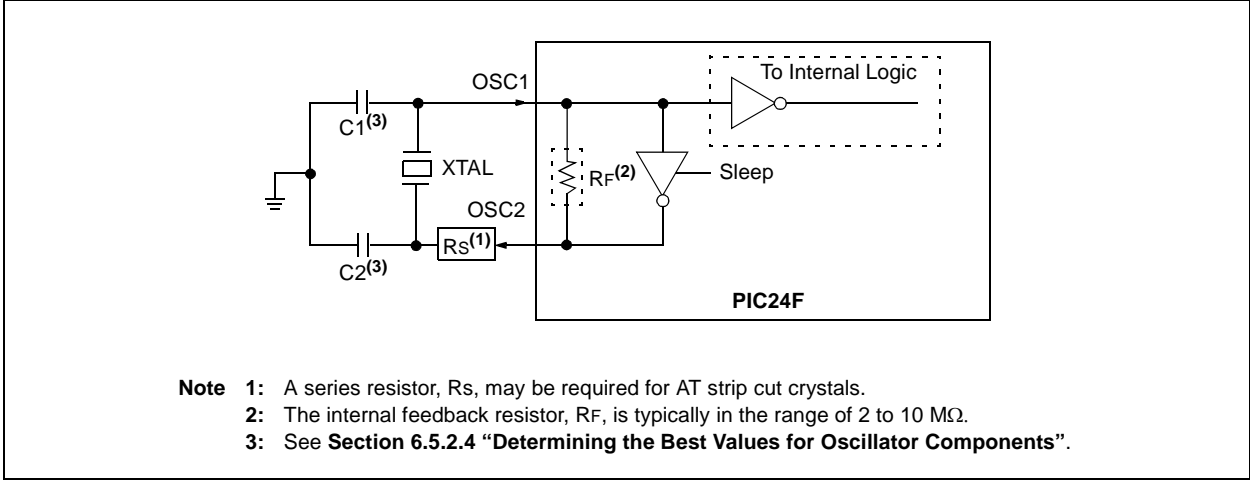
Oscillator Mode	Description	OSC2 Pin Function
EC	External clock input (0-32 MHz)	Fosc/2
ECPLL	External clock input (4-48 MHz), PLL enabled	Fosc/2, Note 2
HS	10 MHz-32 MHz crystal	Note 1
HSPLL	10 MHz-32 MHz crystal	Note 2
XT	3.5 MHz-10 MHz crystal	Note 1
XTPLL	3.5 MHz-8 MHz crystal, PLL enabled	Note 1

- Note 1:** External crystal connected to OSC1 and OSC2 in these modes.
- 2:** Available only in devices with special PLL blocks (such as the 96 MHz PLL); the basic 4x PLL block generates clock frequencies beyond the device’s operating range.

The POSCMD and FNOOSC Configuration bits (Configuration Word 2<1:0> and <10:8>, respectively) select the operating mode of the Primary Oscillator. The POSCMD<1:0> bits select the particular submode to be used (XT, HS or EC), while the FNOOSC<2:0> bits determine if the oscillator will be used by itself or with the internal PLL. The PIC24F operates from the Primary Oscillator whenever the COSC bits (OSCCON<14:12>) are set to ‘010’ or ‘011’.

Refer to the “**Electrical Characteristics**” section in the specific device data sheet for further information regarding frequency range for each crystal mode.

Figure 6-3: Crystal or Ceramic Resonator Operation (XT or HS Oscillator Mode)



- Note 1:** A series resistor, Rs, may be required for AT strip cut crystals.
- 2:** The internal feedback resistor, Rf, is typically in the range of 2 to 10 MΩ.
- 3:** See Section 6.5.2.4 “Determining the Best Values for Oscillator Components”.

6.5.1 Selecting a Primary Oscillator Mode

The main difference between the XT and HS modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges. The XT mode is a medium power, medium frequency mode. HS mode provides the highest oscillator frequencies with a crystal. OSC2 provides crystal feedback in both HS and XT Oscillator modes.

The EC and HS modes that use the PLL circuit provide the highest device operating frequencies. The oscillator circuit will consume the most current in these modes because the PLL is enabled to multiply the frequency of the oscillator by 4.

In general, users should select the oscillator option with the lowest possible gain that still meets their specifications. This will result in lower dynamic currents (I_{DD}). The frequency range of each oscillator mode is the recommended frequency cutoff, but the selection of a different gain mode is acceptable as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry).

The oscillator feedback circuit is disabled in all EC modes. The OSC1 pin is a high-impedance input and can be driven by a CMOS driver.

If the Primary Oscillator is configured for an external clock input, the OSC2 pin is not required to support the oscillator function. For these modes, the OSC2 pin can be used as an additional device I/O pin or a clock output pin. When the OSC2 pin is used as a clock output pin, the output frequency is $F_{OSC}/2$.

6.5.2 Crystal Oscillators and Ceramic Resonators

In XT and HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 6-3). The PIC24F oscillator design requires the use of a parallel cut crystal. Using a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

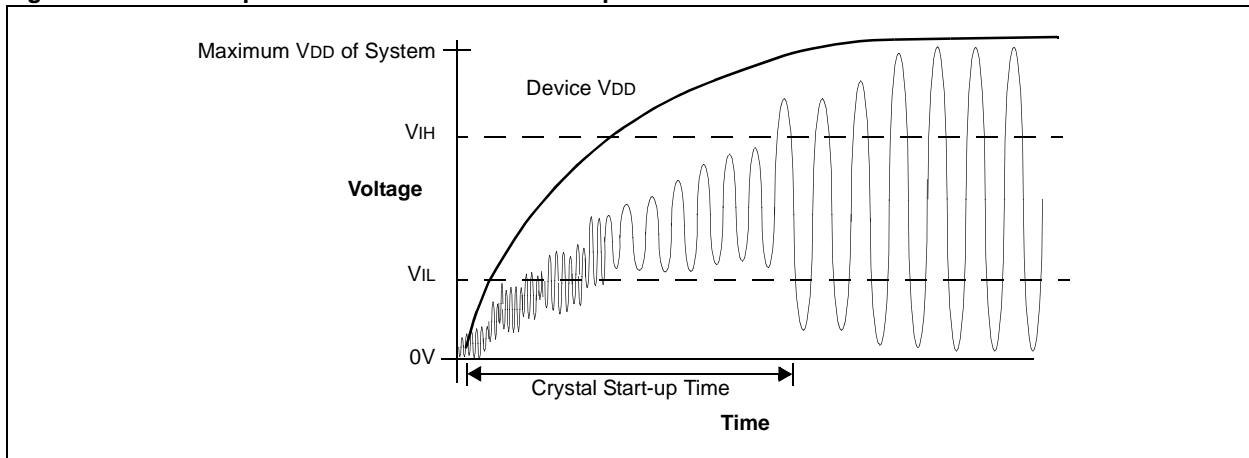
6.5.2.1 OSCILLATOR/RESONATOR START-UP

As the device voltage increases from V_{SS} , the oscillator will start its oscillations. The time required for the oscillator to start oscillating depends on many factors, including:

- Crystal/resonator frequency
- Capacitor values used
- Series resistor, if used, and its value and type
- Device V_{DD} rise time
- System temperature
- Oscillator mode selection of device (selects the gain of the internal oscillator inverter)
- Crystal quality
- Oscillator circuit layout
- System noise

The course of a typical crystal or resonator start-up is shown in Figure 6-4. Notice that the time to achieve stable oscillation is not instantaneous.

Figure 6-4: Example Oscillator/Resonator Start-up Characteristics



6.5.2.1.1 Primary Oscillator Start-up from Sleep Mode

The most difficult time for the oscillator to start-up is when waking up from Sleep mode. This is because the load capacitors have both partially charged to some quiescent value and phase differential at wake-up is minimal. Thus, more time is required to achieve stable oscillation. Also remember that low-voltage, high temperatures and the lower frequency clock modes also impose limitations on loop gain, which in turn, affects start-up.

Each of the following factors increases the start-up time:

- Low-frequency design (with a Low Gain Clock mode)
- Quiet environment (such as a battery operated device)
- Operating in a shielded box (away from the noisy RF area)
- Low voltage
- High temperature
- Wake-up from Sleep mode

Circuit noise, on the other hand, may actually help to “kick start” the oscillator and help to lower the oscillator start-up time.

6.5.2.2 OSCILLATOR START-UP TIMER

In order to ensure that a crystal oscillator (or ceramic resonator) has started and stabilized, an Oscillator Start-up Timer (OST) is provided. The OST is a simple, 10-bit counter that counts 1024 TOSC cycles before releasing the oscillator clock to the rest of the system. This time-out period is designated as TOST. The amplitude of the oscillator signal must reach the VIL and VIH thresholds for the oscillator pins before the OST can begin to count cycles.

The TOST interval is required every time the oscillator has to restart (i.e., on POR, BOR and wake-up from Sleep mode). The Oscillator Start-up Timer is applied to the XT and HS modes for the Primary Oscillator, as well as the Secondary Oscillator, SOS (see **Section 6.7 “Secondary Oscillator (SOSC)”**).

6.5.2.3 TUNING THE OSCILLATOR CIRCUIT

Since Microchip devices have wide operating ranges (frequency, voltage and temperature; depending on the part and version ordered) and external components (crystals, capacitors, etc.) of varying quality and manufacture, validation of operation needs to be performed to ensure that the component selection will comply with the requirements of the application. There are many factors that go into the selection and arrangement of these external components. Depending on the application, these may include any of the following:

- Amplifier gain
- Desired frequency
- Resonant frequency(s) of the crystal
- Temperature of operation
- Supply voltage range
- Start-up time
- Stability
- Crystal life
- Power consumption
- Simplification of the circuit
- Use of standard components
- Component count

6.5.2.4 DETERMINING THE BEST VALUES FOR OSCILLATOR COMPONENTS

The best method for selecting components is to apply a little knowledge and a lot of trial measurement and testing. Crystals are usually selected by their parallel resonant frequency only; however, other parameters may be important to your design, such as temperature or frequency tolerance. Microchip Application Note *AN588, "PICmicro® Microcontroller Oscillator Design Guide"* is an excellent reference to learn more about crystal operation and ordering information.

The PIC24F internal oscillator circuit is a parallel oscillator circuit which requires that a parallel resonant crystal be selected. The load capacitance is usually specified in the 22 pF to 33 pF range. The crystal will oscillate closest to the desired frequency with a load capacitance in this range. It may be necessary to alter these values, as described later, in order to achieve other benefits.

The clock mode is primarily chosen based on the desired frequency of the crystal oscillator. The main difference between the XT and HS Oscillator modes is the gain of the internal inverter of the oscillator circuit which allows the different frequency ranges. In general, use the oscillator option with the lowest possible gain that still meets specifications. This will result in lower dynamic currents (I_{DD}). The frequency range of each oscillator mode is the recommended frequency cutoff, but the selection of a different gain mode is acceptable as long as a thorough validation is performed (voltage, temperature and component variations, such as resistor, capacitor and internal oscillator circuitry). C1 and C2 should also be initially selected based on the load capacitance, as suggested by the crystal manufacturer, and the tables supplied in the device data sheet. The values given in the device data sheet can only be used as a starting point since the crystal manufacturer, supply voltage and other factors, already mentioned, may cause your circuit to differ from the one used in the factory characterization process.

Ideally, the capacitance is chosen so that it will oscillate at the highest temperature and the lowest V_{DD} that the circuit will be expected to perform under. High temperature and low V_{DD} both have a limiting effect on the loop gain, such that if the circuit functions at these extremes, the designer can be more assured of proper operation at other temperatures and supply voltage combinations. The output sine wave should not be clipped in the highest gain environment (highest V_{DD} and lowest temperature) and the sine output amplitude should be large enough in the lowest gain environment (lowest V_{DD} and highest temperature) to cover the logic input requirements of the clock, as listed in the device data sheet. OSC1 may have specified V_{IL} and V_{IH} levels (refer to the specific product data sheet for more information).

A method for improving start-up is to use a value of C2 greater than C1. This causes a greater phase shift across the crystal at power-up, which speeds oscillator start-up. Besides loading the crystal for proper frequency response, these capacitors can have the effect of lowering loop gain if their value is increased. C2 can be selected to affect the overall gain of the circuit. A higher C2 can lower the gain if the crystal is being overdriven (also, see discussion on Rs). Capacitance values that are too high can store and dump too much current through the crystal, so C1 and C2 should not become excessively large. Unfortunately, measuring the wattage through a crystal is difficult, but if you do not stray too far from the suggested values, you should not have to be concerned with this.

A series resistor, Rs, is added to the circuit if, after all other external components are selected to satisfaction, the crystal is still being overdriven. This can be determined by looking at the OSC2 pin, which is the driven pin, with an oscilloscope. Connecting the probe to the OSC1 pin will load the pin too much and negatively affect performance. Remember that a scope probe adds its own capacitance to the circuit, so this may have to be accounted for in your design (i.e., if the circuit worked best with a C2 of 22 pF and the scope probe was 10 pF, a 33 pF capacitor may actually be called for). The output signal should not be clipping or flattened. Overdriving the crystal can also lead to the circuit jumping to a higher harmonic level, or even, crystal damage.

The OSC2 signal should be a clean sine wave that easily spans the input minimum and maximum of the clock input pin. An easy way to set this is to again test the circuit at the minimum temperature and maximum VDD that the design will be expected to perform in, then look at the output. This should be the maximum amplitude of the clock output. If there is clipping, or the sine wave is distorted near VDD and VSS, increasing load capacitors may cause too much current to flow through the crystal or push the value too far from the manufacturer's load specification. To adjust the crystal current, add a trimmer potentiometer between the crystal inverter output pin and C2, and adjust it until the sine wave is clean. The crystal will experience the highest drive currents at the low temperature and high VDD extremes.

The trimmer potentiometer should be adjusted at these limits to prevent overdriving. A series resistor, Rs, of the closest standard value can now be inserted in place of the trimmer. If Rs is too high, perhaps more than 20 kΩ, the input will be too isolated from the output, making the clock more susceptible to noise. If you find a value this high is needed to prevent overdriving the crystal, try increasing C2 to compensate or changing the oscillator operating mode. Try to get a combination where Rs is around 10 kΩ, or less, and load capacitance is not too far from the manufacturer's specification.

6.5.3 External Clock Input

In EC mode, the OSC1 pin is in a high-impedance state and can be driven by CMOS drivers. The OSC2 pin can be configured as either an I/O or the clock output (FOSC/2) by selecting the OSCIOFCN bit (Configuration Word 2<5>). With OSCIOFCN set (Figure 6-5), the clock output is available for testing or synchronization purposes. With OSCIOFCN clear (Figure 6-6), the OSC2 pin becomes a general purpose I/O pin. The feedback device between OSC1 and OSC2 is turned off to save current.

Figure 6-5: External Clock Input Operation (OSCIOFCN = 1)

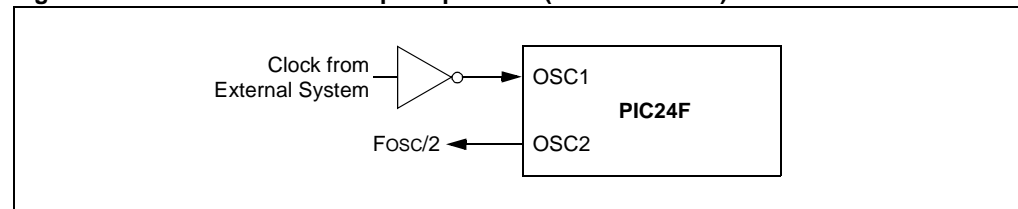
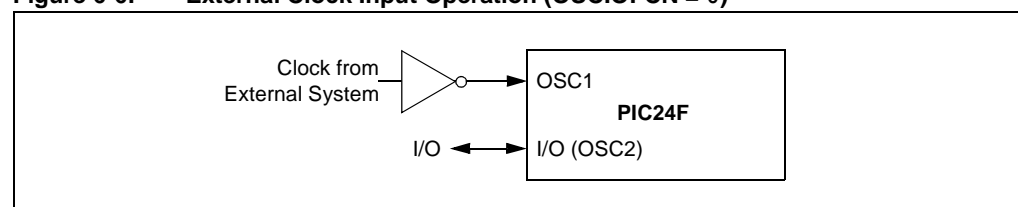


Figure 6-6: External Clock Input Operation (OSCIOFCN = 0)



6.6 PHASE LOCK LOOP (PLL) BRANCH

The system clock for all PIC24F devices includes a frequency multiplier branch built around a Phase Lock Loop (PLL). This branch allows the user to obtain a higher clock speed using a low-speed Primary Oscillator or external clock source, eliminating the need for an expensive high-speed crystal or resonator. It also allows the use of the Internal Fast RC Oscillator (FRC) to clock the device at its maximum operating speed without the use of an external oscillator.

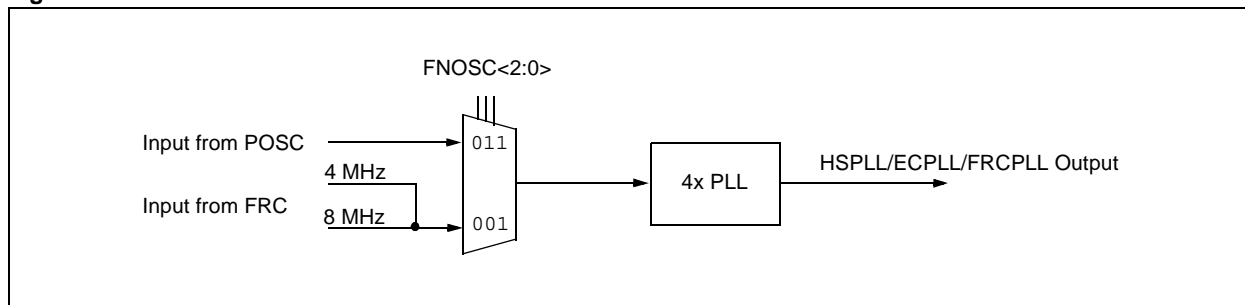
There are several different versions of the PLL block implemented on PIC24F devices; the version implemented depends on the particular device family. Some PLL blocks provide a single branch, frequency multiplied output. Others provide multiple branches with clocks at different frequencies, including a special clock for a particular peripheral. Users should refer to the particular device data sheet to see which PLL block is implemented.

6.6.1 Basic 4x PLL Block

In most PIC24F devices, the implemented PLL block is the basic PLL (Figure 6-7). This provides a fixed 4x multiplier, which can be used with XT and EC Primary Oscillators and the FRC Oscillator. The PLL accepts any frequency input from approximately 3.5 MHz to 8 MHz.

Whenever the clock source of the PLL is changed, the PLL ready timer must be reset to allow the PLL to synchronize to the new clock source. After the ready timer has counted the required time, the PLL output is ready for use.

Figure 6-7: Basic 4x PLL Block



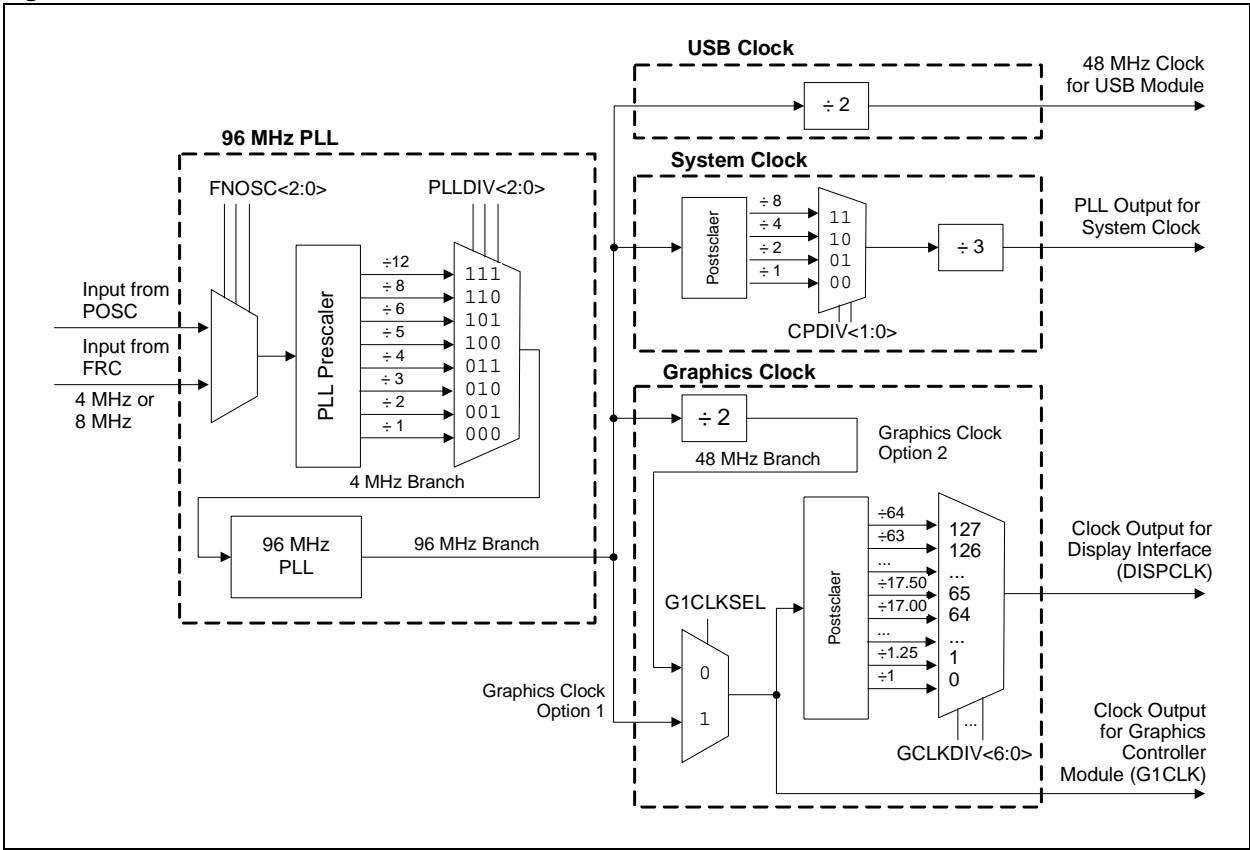
6.6.2 96 MHz PLL Block

For PIC24F devices with USB features (such as the PIC24FJ256GB110 family) and graphics controller features (such as the PIC24FJ256DA210 family), a 96 MHz PLL block is implemented to generate the stable 48 MHz clock required for full-speed USB operation, a programmable clock output for the graphics controller module and the system clock from the same oscillator source. The 96 MHz PLL block is shown in Figure 6-8.

The 96 MHz PLL block requires a 4 MHz input signal; it uses this to generate a 96 MHz signal from a fixed, 24 x PLL. This is, in turn, divided into three branches. The first branch generates the USB clock, the second branch generates the system clock and the third branch generates the graphics clock. The 96 MHz PLL block can be enabled and disabled using the PLL96MHZ Configuration bit (Configuration Word 2 <11> in most devices) or through the PLEN (CLKDIV<5>) control bit when the PLL96MHZ Configuration bit is not set. Note that the PLL96MHZ Configuration bit and the PLEN register bit are available only for PIC24F devices with USB and graphics controller modules.

The 96 MHz PLL prescaler does not automatically sense the incoming oscillator frequency. The user must manually configure the PLL divider to generate the required 4 MHz output, using the PLLDIV<2:0> Configuration bits (Configuration Word 2 <14:12> in most devices).

Figure 6-8: 96 MHz PLL Block



6.6.2.1 SYSTEM CLOCK GENERATION

The system clock is generated from the 96 MHz branch using a configurable postscale/divider to generate a range of frequencies for the system clock multiplexer. The output of the multiplexer is further passed through a fixed divide-by-3 divider and the final output is used as the system clock. Figure 6-8 shows this logic in the system clock subblock. Since the source is a 96 MHz signal, the possible system clock frequencies are listed in Table 6-3. The available system clock options are always the same, regardless of the setting of the PLLDIV Configuration bits.

Table 6-3: System Clock Options for 96 MHz PLL Block

MCU Clock Division (CPDIV<1:0>)	System Clock Frequency (Instruction Rate in MIPS)
None (00)	32 MHz (16)
÷2 (01)	16 MHz (8)
÷4 (10)	8 MHz (4) ⁽¹⁾
÷8 (11)	4 MHz (2) ⁽¹⁾

Note 1: These options are not compatible with USB operation. They may be used whenever the PLL branch is selected and the USB module is disabled.

6.6.2.2 USB CLOCK GENERATION

For PIC24F devices with USB functionality, the Primary Oscillator combined with this PLL block can be used as a valid clock source for USB operation. In some PIC24F devices, the FRC Oscillator that meets USB clocking accuracy requirements can be combined with this PLL block providing another option for a valid clock source for USB operation. There is no provision to provide a separate external 48 MHz clock to the USB module. The USB module sources its clock signal from the 96 MHz PLL. Due to the requirement that a 4 MHz input must be provided to generate the 96 MHz signal, the oscillator operation is limited to a range of possible values. Table 6-4 shows the valid oscillator configurations (i.e., ECPLL, HSPLL, XTPLL and FRCPLL) for USB operation. This sets the correct PLLDIV configuration for a specified oscillator frequency and the output frequency of the USB clock branch is always 48 MHz.

Table 6-4: Valid Oscillator Configurations for USB Operations

Input Oscillator Frequency	Clock Mode	PLL Division (PLLDIV<2:0>)
48 MHz	ECPLL	÷12 (111)
32 MHz	ECPLL	÷ 8 (110)
24 MHz	HSPLL, ECPLL	÷6 (101)
20 MHz	HSPLL, ECPLL	÷5 (100)
16 MHz	HSPLL, ECPLL	÷4 (011)
12 MHz	HSPLL, ECPLL	÷3 (010)
8 MHz	ECPLL, XTPLL, FRCPLL ⁽¹⁾	÷2 (001)
4 MHz	ECPLL, XTPLL, FRCPLL ⁽¹⁾	÷1 (000)

Note 1: FRCPLL with ±0.25% accuracy can be used for USB operation.

Note: For USB devices, the use of a Primary Oscillator or external clock source with a frequency above 32 MHz does not imply that the device's system clock can be run at the same speed when the USB module is not used. The maximum system clock for all PIC24F devices is 32 MHz.

Because of USB clocking accuracy requirements (±0.25%), not all PIC24F devices support the use of the FRCPLL system clock configuration for USB operation. Refer to the specific device data sheet for details on the FRC Oscillator module.

6.6.2.3 GRAPHICS CLOCK GENERATION

For PIC24F devices with graphics controller features, two stable clock signals are generated. The first clock is for the graphics controller module logic and the second clock is for the display module interface logic that generates the signals for the display glass. Figure 6-8 shows this logic in the graphics clock subblock. Both clock signals are generated from either the graphics clock option 1 (96 MHz branch) or the graphics clock option 2 (48 MHz branch). Selection is set in the multiplexer using the G1CLKSEL (CLKDIV<4>) control bit. The graphics controller module logic directly uses the output of that multiplexer, while the display module interface clock is further conditioned through a postscaler to generate 128 possible frequencies. The final clock output signal is selected through a multiplexer using the GCLKDIV<6:0> (CLKDIV2<15:9>) control bits. The 128 selections vary in increments of 0.25, 0.5 and 1. Refer to Table 6-5 for details. Note that for applications that use the graphics controller module, the 96 MHz PLL must be enabled.

Table 6-5: Display Module Clock Frequency Division

GCLKDIV<6:0>	Frequency Divisor	Display Module Clock Frequency 96 MHz Input (48 MHz Input)
0000000	1	96 MHz (48 MHz)
0000001	1.25 (start incrementing by 0.25)	76.80 MHz (38.4 MHz)
0000010	1.5	64 MHz (32 MHz)
...
0111111	16.75	5.73 MHz (2.86 MHz)
1000000	17	5.65 MHz (2.82 MHz)
1000001	17.5 (start incrementing by 0.5)	5.49 MHz (2.74 MHz)
1000010	18	5.33 MHz (2.66 MHz)
...
1011111	32.5	2.95 MHz (1.47 MHz)
1100000	33	2.91 MHz (1.45 MHz)
1100001	34 (start incrementing by 1)	2.82 MHz (1.41 MHz)
1100010	35	2.74 MHz (1.37 MHz)
...
1111110	63	1.52 MHz (762 kHz)
1111111	64	1.50 MHz (750 kHz)

6.6.3 Considerations for Using the PLL Block

All PLL blocks use the LOCK bit (OSCCON<5>) as a read-only status bit to indicate the lock status of the PLL. It is automatically set after the typical time delay for the PLL to achieve lock, designated as TLOCK. It is cleared at a POR and on clock switches when the PLL is selected as a destination clock source. It remains clear when any clock source not using the PLL is selected.

If the PLL does not stabilize properly during start-up, LOCK may not reflect the actual status of the PLL lock, nor does it detect when the PLL loses lock during normal operation. Refer to the “**Electrical Characteristics**” section in the specific device data sheet for further information on the PLL lock interval.

Using any PLL block with the FRC Oscillator provides a stable system clock for microcontroller operations. In specific devices or families, this combination may not meet the frequency accuracy requirements for use in synchronous communications. USB operation is only possible with FRC Oscillators that are implemented with $\pm 1/4\%$ frequency accuracy. Serial communications using UART is only possible when FRC Oscillators are implemented with $\pm 2\%$ frequency accuracy. Refer to the “**Electrical Characteristics**” section of the particular device data sheet for specific information.

If an application is being migrated between PIC24F platforms with different PLL blocks (e.g., from a GA0 family device to a GB1 family device), the differences in PLL and clock options may require the reconfiguration of peripherals that use the system clock. This is particularly true with serial communications peripherals, such as the UARTs.

6.7 SECONDARY OSCILLATOR (SOSC)

In most PIC24F devices, the low-power Secondary Oscillator (SOSC) is implemented to run with a 32.768 kHz crystal. The oscillator is located on the SOSCO and SOSCI device pins and serves as a secondary crystal clock source for low-power operation. It is used to drive Timer1, Real-Time Clock and Calendar (RTCC) and other modules requiring a clock signal while in low-power operation.

In some PIC24F devices, selectable Low-Current and High-Current Drive mode is available. High-Current Drive mode results in a faster start-up time and is less susceptible to noise.

6.7.1 Enabling the Secondary Oscillator

The operation of SOSC is selected by the FNO SC Configuration bits and is further controlled by the SOS CEN bit (OSCCON<1>). In most PIC24F devices, SOS CEN must be set to enable the oscillator and use it for modules requiring the SOSC. In some PIC24F devices, applications do not need to set SOS CEN to use modules requiring the SOSC. Enabling the modules will automatically turn on the SOSC when the clock signal is needed. The SOSC, however, has a long start-up time. To avoid delays for peripheral start-up, the SOSC can be manually started using the SOS CEN bit. Refer to the specific PIC24F device data sheet for details.

Note: An unlock sequence is required before a write to OSCCON can occur. Refer to Section 6.11.2 “Oscillator Switching Sequence” for more information.
--

6.7.2 Secondary Oscillator Operation

6.7.2.1 CONTINUOUS OPERATION

The SOSC is always enabled when SOS CEN is set. Leaving the oscillator running at all times allows a fast switch to the 32 kHz system clock for lower power operation. Returning to the faster main oscillator will still require an oscillator start-up time if it is a crystal type source (see **Section 6.5.2.2 “Oscillator Start-up Timer”**).

In addition, the oscillator will need to remain running at all times for Real-Time Clock application using Timer1 or the RTCC module. Refer to **Section 14. “Timers”** (DS39704) and **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS39696) in the *“PIC24F Family Reference Manual”* for further details.

6.7.2.2 INTERMITTENT OPERATION

When SOS CEN is cleared, the oscillator will only operate when it is selected as the current device clock source (COS C<2:0> = 100). It will be disabled automatically if it is the current device clock source and the device enters Sleep mode.

6.7.2.3 OPERATING MODES

6.7.2.3.1 Low and High-Current Drive Modes

In some PIC24F devices, the SOSC can be run in Low or High-Current Drive mode. The selection is done through the Secondary Oscillator Mode Configuration bits, SOS CSEL<1:0>. Refer to the specific device data sheet for details.

Using the lower Current Drive mode makes the SOSC more sensitive to noise and requires a longer start-up time. When using this mode, care must be taken in the design and layout of the SOSC circuit to ensure that the oscillator starts up and oscillates properly.

6.7.2.3.2 Digital Mode

In some PIC24F device, the SOSC can also be configured to operate in Digital mode. The selection is also done through the Secondary Oscillator Mode Configuration bits, SOS CSEL<1:0>. Refer to the specific device data sheet for details.

When running in this mode, the SOS CI and SOS CO pins are configured as digital I/O pins. An external 32 kHz clock source can be used to drive the SOS CI (SCLKI) pin giving clock signals to modules configured to use the SOSC. The crystal driving circuit is disabled and the SOS CEN bit (OSCCON<1>) has no effect.

6.8 INTERNAL FAST RC OSCILLATOR (FRC)

The FRC Oscillator is a fast (8 MHz nominal), internal RC Oscillator. This oscillator is intended to provide reasonable device operating speeds without the use of an external crystal or ceramic resonator. The PIC24F operates from the FRC Oscillator whenever the COSC bits are '111', '001' or '000'.

Note: Due to specified FRC accuracy, the FRC Oscillator modes may not meet the minimum frequency accuracy requirements for serial communications (such as UART and USB). Refer to the product family data sheet for more information about the FRC accuracy.

6.8.1 Enabling the FRC Oscillator

Since it serves as the reference clock during device initialization, the FRC Oscillator is always enabled at a POR. After the device is configured and PWRT expires, FRC remains active only if it is selected as the device clock source.

6.8.2 FRC Postscaler Mode (FRCDIV)

Users are not limited to the nominal 8 MHz FRC output if they wish to use the fast internal oscillator as a clock source. An additional FRC mode, FRCDIV, implements a selectable postscaler that allows the choice of a lower clock frequency from 7 different options, plus the direct 8 MHz output. The postscaler is configured using the RCDIV<2:0> bits (CLKDIV<10:8>). Assuming a nominal 8 MHz output, available lower frequency options range from 4 MHz (divide-by-2) to 31 kHz (divide-by-256). The range of frequencies allows users the ability to save power at any time in an application by simply changing the RCDIV bits.

The FRCDIV mode is selected whenever the COSC bits are '111'.

6.8.3 FRC Oscillator with PLL Mode (FRCPLL)

The FRCPLL mode is selected whenever the COSC bits are '001'. In addition, this mode only functions when the direct or divide-by-2 FRC postscaler options are selected (RCDIV<2:0> = 000 or 001).

For devices with the basic 4x PLL block, the output of the FRC postscaler block may also be combined with the PLL to produce a nominal system clock of either 16 MHz or 32 MHz. Although somewhat less precise in frequency than using the Primary Oscillator with a crystal or resonator, it still allows high-speed operation of the device without the use of external oscillator components.

For devices with the 96 MHz PLL block, the output of the FRC postscaler block may also be combined with the PLL to produce a nominal system clock of either 4 MHz, 8 MHz, 16 MHz or 32 MHz. It also produces a 48 MHz USB clock; however, this USB clock must be generated with the FRC Oscillator meeting the frequency accuracy requirement of USB for proper operation. Refer to the specific device data sheet for details on the FRC Oscillator electrical characteristics. In cases where the frequency accuracy is not met for USB operation, the FRCPLL mode should not be used when USB is active.

6.9 INTERNAL LOW-POWER RC OSCILLATOR (LPRC)

The LPRC Oscillator is separate from the FRC and oscillates at a nominal frequency of 31 kHz. LPRC is the clock source for the Power-up Timer (PWRT), Watchdog Timer (WDT) and FSCM circuits. It may also be used to provide a low-frequency clock source option for the device in those applications where power consumption is critical and timing accuracy is not required.

6.9.1 Enabling the LPRC Oscillator

Since it serves the PWRT clock source, the LPRC Oscillator is enabled at PORs whenever the on-board voltage regulator is disabled. After the PWRT expires, the LPRC Oscillator will remain on if any one of the following is true:

- The FSCM is enabled.
- The WDT is enabled.
- The LPRC Oscillator is selected as the system clock ($\text{COSC}<2:0> = 100$).

If none of the above is true, the LPRC will shut off after the PWRT expires.

6.10 FAIL-SAFE CLOCK MONITOR (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming the FCKSM (Clock Switch and Monitor) bits in the Configuration Word 2. FSCM is only enabled when both bits are programmed ('00'). When FSCM is enabled, the internal LPRC Oscillator will run at all times (except during Sleep mode).

In the event of an oscillator failure, the FSCM will generate a clock failure trap and will switch the system clock to the FRC Oscillator. The user will then have the option to either attempt to restart the oscillator or execute a controlled shutdown. FSCM will monitor the system clock source regardless of its source or oscillator mode. This includes the Primary Oscillator for all oscillator modes and the Secondary Oscillator, SOSC, when configured as the system clock.

The FSCM module takes the following actions when switching to the FRC Oscillator:

1. The COSC bits are loaded with '000'.
2. The CF status bit is set to indicate the clock failure.
3. The OSWEN control bit is cleared to cancel any pending clock switches.

Note: For more information about the oscillator failure trap, refer to **Section 8. "Interrupts"** in the *"PIC24F Family Reference Manual"*.

6.10.1 FSCM Delay

On a POR, BOR or wake from Sleep mode event, a nominal delay (T_{FSCM}) may be inserted before the FSCM begins to monitor the system clock source. The purpose of the FSCM delay is to provide time for the oscillator and/or PLL to stabilize when the PWRT is not utilized. The FSCM delay will be generated after the internal System Reset signal, $\overline{\text{SYSRST}}$, has been released. Refer to **Section 7. "Reset"** in the *"PIC24F Family Reference Manual"* for FSCM delay timing information.

The T_{FSCM} interval is applied whenever the FSCM is enabled and the EC, HS or SOSC Oscillator modes are selected as the system clock.

Note: Please refer to the **"Electrical Characteristics"** section of the specific device data sheet for T_{FSCM} specification values.

6.10.2 FSCM and Slow Oscillator Start-up

If the chosen device oscillator has a slow start-up time coming out of POR, BOR or Sleep mode, it is possible that the FSCM delay will expire before the oscillator has started. In this case, the FSCM will initiate a clock failure trap. As this happens, the COSC bits are loaded with the FRC Oscillator selection. This will effectively shut off the original oscillator that was trying to start. The user can detect this situation and initiate a clock switch back to the desired oscillator in the Trap Service Routine (TSR).

6.10.3 FSCM and WDT

The FSCM and the WDT both use the LPRC Oscillator as their time base. In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC.

6.11 CLOCK SWITCHING OPERATION

With few limitations, applications are free to switch between any of the four clock sources (Primary, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switch process.

Note: Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMD Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

6.11.1 Enabling Clock Switching

To enable clock switching, the FCKSM1 Configuration bit must be programmed to '0'. (Refer to the specific device data sheet for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

6.11.2 Oscillator Switching Sequence

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

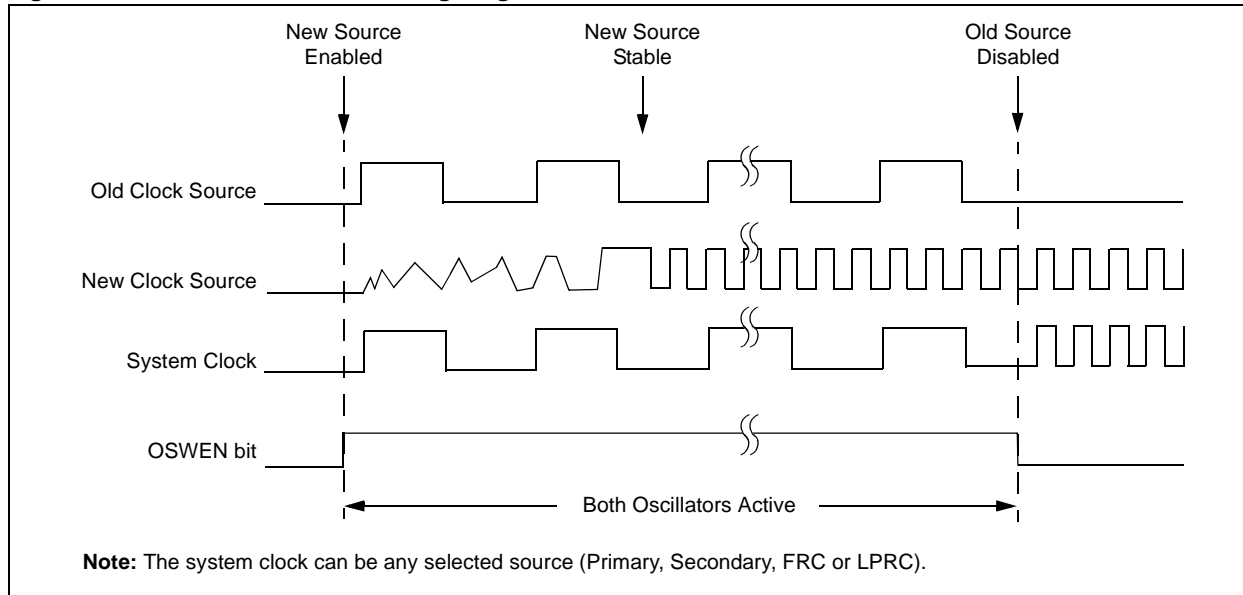
Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) status bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for the new clock source to stabilize and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM is enabled) or SOSC (if SOSSEN remains set).

The timing of the transition between clock sources is shown in Figure 6-9.

Note: The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.

Figure 6-9: Clock Transition Timing Diagram



A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8> in two back-to-back instructions.
3. Write new oscillator source to NOSC control bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0> in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 6-1.

Example 6-1: Basic Code Sequence for Clock Switching

```

;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV     #OSCCONH,w1
MOV     #0x78, w2
MOV     #0x9A, w3
MOV.b   w2, [w1]
MOV.b   w3, [w1]
;Set new oscillator selection
MOV.b   WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV     #OSCCONL,w1
MOV.b   #0x01, w0
MOV     #0x46, w2
MOV     #0x57, w3
MOV.b   w2, [w1]
MOV.b   w3, [w1]
;Start oscillator switch operation
MOV.b   w0, [w1]

```

6.11.2.1 CLOCK SWITCHING CONSIDERATIONS

When incorporating clock switching into an application, users should keep certain things in mind when designing their code.

- The OSCCON unlock sequence is extremely timing-critical. The OSCCON register byte is only writable for one instruction cycle following the sequence. Some high-level languages, such as C, may not preserve the timing-sensitive sequence of instructions when compiled. When clock switching is required for an application written in a high-level language, it is best to create the routine in assembler and link it to the application, calling it as a function when it is required.
- If the destination clock source is a crystal oscillator, the clock switch time will be dominated by the oscillator start-up time.
- If the new clock source does not start, or is not present, the clock switching hardware will wait indefinitely for the new clock source. The user can detect this situation because the OSWEN bit remains set indefinitely.
- If the new clock source uses the PLL, a clock switch will not occur until lock has been achieved. The user can detect a loss of PLL lock because the LOCK bit will be cleared and the OSWEN bit is set.
- Switching to a low-frequency clock source, such as the Secondary Oscillator, will result in very slow device operation.

Note: The application should not attempt to switch to a clock with a frequency lower than 100 kHz when the FSCM is enabled. Clock switching in these instances may generate a false oscillator fail trap and result in a switch to the Internal Fast RC Oscillator.

6.11.3 Aborting a Clock Switch

In the event the clock switch did not complete, the clock switch logic can be reset by clearing the OSWEN bit. This will abandon the clock switch process, stop and reset the OST (if applicable), and stop the PLL (if applicable). Typical assembly code for aborting a clock switch is shown in Example 6-2.

A clock switch procedure can be aborted at any time. A clock switch that is already in progress can also be aborted by performing a second clock switch.

Example 6-2: Aborting a Clock Switch

```
MOV      #OSCCON,W1      ; pointer to OSCCON
MOV.b    #0x46,W2        ; first unlock code
MOV.b    #0x57,W3        ; second unlock code
MOV.b    W2, [W1]        ; write first unlock code
MOV.b    W3, [W1]        ; write second unlock code
BCLR     OSCCON,#OSWEN   ; ABORT the switch
```

6.11.4 Entering Sleep Mode During a Clock Switch

If the device enters Sleep mode during a clock switch operation, the clock switch operation is aborted. The processor keeps the old clock selection and the OSWEN bit is cleared. The `PWRSVAV` instruction is then executed normally.

6.12 TWO-SPEED START-UP

Two-Speed Start-up is an automatic clock switching feature that is independent of the manually controlled clock switching previously described. It helps to minimize the latency period, from oscillator start-up to code execution, by allowing the microcontroller to use the FRC Oscillator as a clock source until the primary clock source is available. This feature is controlled by the IES0 Configuration bit (Configuration Word 2<15>) and operates independently of the state of the FCKSM Configuration bits.

Two-Speed Start-up is particularly useful when an external oscillator is selected by the FNOSC Configuration bits and a crystal-based oscillator (either a Primary or Secondary Oscillator) may have a longer start-up time. As an internal RC Oscillator, the FRC clock source is available almost immediately following a POR or device wake-up.

With Two-Speed Start-up, the device starts executing code on POR in its default oscillator configuration (FRC). It continues to operate in this mode until the external oscillator source specified by the FNOSC Configuration bits becomes stable; at which time, it automatically switches to that source.

Two-Speed Start-up is used on wake-up from the power-saving Sleep mode. The device uses the FRC clock source until the selected primary clock is ready. It is not used in Idle mode, as the device will be clocked by the currently selected clock source until the primary clock source becomes available.

6.12.1 Special Considerations for Using Two-Speed Start-up

While using the FRC Oscillator in Two-Speed Start-up, the device still obeys the normal command sequences for entering power-saving modes, including serial `PWRSV` instructions. In practice, this means that user code can change the `NOSC<2:0>` bit settings or issue `PWRSV #SLEEP` instructions before the OST times out. This would allow an application to briefly wake-up, perform routine “housekeeping” tasks and return to Sleep before the device starts to operate from the external oscillator.

User code can also check which clock source is currently providing the device clocking by checking the status of the `COSC<2:0>` bits against the `NOSC<2:0>` bits. If these two sets of bits match, the clock switch has been completed successfully and the device is running from the intended clock source; the Primary Oscillator is providing the clock. Otherwise, FRC is providing the clock during wake-up from Reset or Sleep mode.

6.13 REFERENCE CLOCK OUTPUT GENERATOR

The CLKO output available on OSC2 in select oscillator modes can be useful for synchronizing external logic to the microcontroller. However, it is limited in that it is only available in a few modes, and at only one frequency ($F_{OSC}/2$). For select PIC24F families, the reference clock output generator provides another option: a separate synchronous and programmable clock source to the REFO port pin.

The reference clock output generator receives inputs from both the Primary Oscillator and the currently selected system clock. This allows the user to select an output clock signal with a constant frequency, or an output clock that changes as the system clock changes during run time (e.g., on a change to or from a lower power mode). A 16-step divider allows for the selection of a wide range of system clock submultiples. Reference clock changes due to system clock frequency changes occur in a glitchless fashion.

This reference clock output is controlled by the REFOCON register (Register 6-4). Setting the ROEN bit (REFOCON<15>) makes the clock signal available on the REFO pin. The RODIV bits (REFOCON<11:8>) select a range of output frequencies, from divide-by-1 through divide-by-32,768. This postscaler can be changed as needed at run time. It is recommended that the clock generator be disabled prior to changing the RODIV bits to ensure the smoothest speed transition.

The ROSEL bit (REFOCON<12>) determines if the Primary Oscillator, or the current system clock source designated by COSC<2:0>, provides the reference clock output. Clearing the ROSEL bit allows the reference output frequency to change as the system clock changes during any clock switches.

If one of the Primary Oscillator modes (EC, HS or XT) is used for the system clock, the ROSEL and ROSSLP bits determine if the reference clock output is available when the device is in Sleep mode. Both the ROSSLP and ROSEL bits must be set, and the POSCEN bit (OSCCON<2>) must also be set. Otherwise, the oscillator on OSC1 and OSC2 will be powered down when the device enters Sleep mode.

6.14 DESIGN TIPS

Question 1: *When looking at the OSC2 pin after power-up with an oscilloscope, there is no clock. What can cause this?*

Answer: There are several possible causes:

1. Entering Sleep mode with no source for wake-up (such as WDT, $\overline{\text{MCLR}}$ or an interrupt). Verify that the code does not put the device to Sleep without providing for wake-up. If it is possible, try waking it up with a low pulse on $\overline{\text{MCLR}}$. Powering up with $\overline{\text{MCLR}}$ held low will also give the crystal oscillator more time to start-up, but the program counter will not advance until the $\overline{\text{MCLR}}$ pin is high.
2. The wrong clock mode is selected for the desired frequency. For a blank device, the default oscillator is FRCDIV. Most parts come with the clock selected in the Default mode which will not start oscillation with a crystal or resonator. Verify that the clock mode has been programmed correctly.
3. The proper power-up sequence has not been followed. If a CMOS part is powered through an I/O pin prior to power-up, bad things can happen (latch-up, improper start-up, etc.). It is also possible for brown-out conditions, noisy power lines at start-up and slow VDD rise times to cause problems. Try powering up the device with nothing connected to the I/O, and power-up with a known, good, fast rise power supply. Refer to the power-up information in the specific device data sheet for considerations on brown-out and power-up sequences.
4. The C1 and C2 capacitors attached to the crystal have not been connected properly or are not the correct values. Make sure all connections are correct. The device data sheet values for these components will usually get the oscillator running; however, they just might not be the optimal values for your design.

Question 2: *Why does my device run at a frequency much higher than the resonant frequency of the crystal?*

Answer: The gain is too high for this oscillator circuit. Refer to **Section 6.5.2.4 “Determining the Best Values for Oscillator Components”** to aid in the selection of C2 (may need to be higher), Rs (may be needed) and clock mode (wrong mode may be selected). This is especially possible for low-frequency crystals, like the common 32.768 kHz.

Question 3: *The design runs fine, but the frequency is slightly off. What can be done to adjust this?*

Answer: Changing the value of C1 has some effect on the oscillator frequency. If a series resonant crystal is used, it will resonate at a different frequency than a parallel resonant crystal of the same frequency call-out. Ensure that you are using a parallel resonant crystal.

Question 4: *What would cause my application to work fine, but then suddenly quit or lose time?*

Answer: Other than the obvious software checks that should be done to investigate losing time, it is possible that the amplitude of the oscillator output is not high enough to reliably trigger the oscillator input. Also, look at the C1 and C2 values and ensure that the device Configuration bits are correct for the desired oscillator mode.

Question 5: *If I put an oscilloscope probe on an oscillator pin, I do not see what I expect. Why?*

Answer: Remember that an oscilloscope probe has capacitance. Connecting the probe to the oscillator circuitry will modify the oscillator characteristics. Consider using a low capacitance (active) probe.

6.15 REGISTER MAPS

A summary of the registers associated with the PIC24F oscillator module is provided in Table 6-6.

Table 6-6: Oscillator Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OSCCON	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK ⁽¹⁾	LOCK	—	CF	POSCEN ⁽¹⁾	SOSCEN	OSWEN	xxxx ⁽²⁾
CLKDIV	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	CPDIV1 ⁽¹⁾	CPDIV0 ⁽¹⁾	PLLEN ⁽¹⁾	G1CLKSEL ⁽¹⁾	—	—	—	—	0100
CLKDIV2 ⁽¹⁾	GCLKDIV6	GCLKDIV5	GCLKDIV4	GCLKDIV3	GCLKDIV2	GCLKDIV1	GCLKDIV0	—	—	—	—	—	—	—	—	—	0000
OSCTUN	—	—	—	—	—	—	—	—	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000
REFOCON ⁽¹⁾	ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for the fully-implemented registers.

Note 1: These bits or registers are implemented in select devices only. Refer to the specific device data sheet for actual implementation and Reset value.

Note 2: OSCCON register Reset values depend on the FOSC Configuration bits and by type of Reset.

6.16 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Oscillator module are:

Title	Application Note #
Crystal Oscillator Basics and Crystal Selection for rPIC [®] and PICmicro [®] Devices	AN826
Basic PICmicro [®] Oscillator Design	AN849
Practical PICmicro [®] Oscillator Analysis and Design	AN943
Making Your Oscillator Work	AN949

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

6.17 REVISION HISTORY

Revision A (September 2006)

This is the initial released revision of this document.

Revision B (February 2008)

Expansion to include PIC24F devices in the GA1 and GB1 families. Made the following revisions:

- Updated Figure 6-1 to reflect new clock topology.
- Updated registers in **Section 6.2 “CPU Clocking Scheme”** to reflect new clock functionality.
- Replaced **Section 6.6 “4x PLL”** with new **Section 6.6 “Phase Lock Loop (PLL) Branch”**. Added separate sections on 4x PLL and USB PLL block.

Added new **Section 6.13 “Reference Clock Output Generator”**. Previous Section 6.13 and subsequent sections are renumbered as Section 6.14 and following.

Revision C (August 2009)

Added **Section 6.4.5 “Clock Divider Register 2 (CLKDIV2)”**. Appended to **Section 6.4.2 “Clock Divider Register (CLKDIV)”**. Added bits 5 and 4 to Register 6-2. Modified **Section 6.6.2 “96 MHz PLL Block”**. Replaced Figure 6-8 with new diagram. Added **Section 6.6.3 “Considerations for Using the PLL Block”**. Modified Table 6-6.