
Section 35. Output Compare with Dedicated Timer

HIGHLIGHTS

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35.1 INTRODUCTION

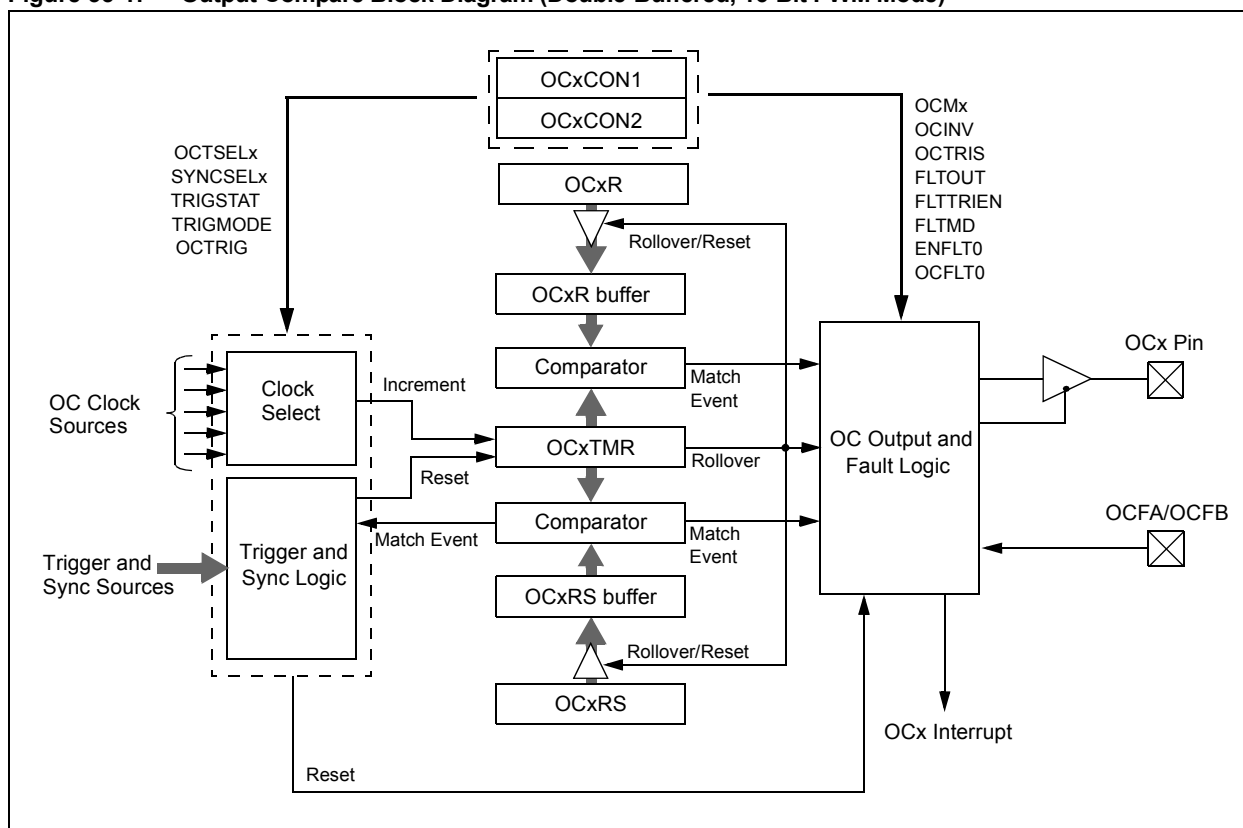
The output compare module in PIC24F devices compares the Timer register value with the value of one or two Compare registers, depending on its mode of operation. The output compare module on compare match events has the ability to generate a single output transition or a train of output pulses. Like most PIC[®] MCU peripherals, the output compare module can also generate interrupts on a compare match event.

Each output compare timer can use one of the available six selectable time clocks. The clock is selected using the OCTSEL<2:0> (OCxCON1<12:10>) bits. Refer to the applicable device data sheet for more information about specific timers that can be used as a time base for the output compare timer.

Figure 35-1 illustrates the block diagram of the output compare module.

- Note 1:** For complete information on the number of available channels, refer to the specific device data sheet.
- 2:** All of the output compare channels are functionally identical. In this section, an 'x' in the pin, register or bit name denotes the specific output compare channel.
- 3:** The OCx output must be assigned to an available RPN pin before use if the device supports Peripheral Pin Select (PPS). Refer to the Peripheral Pin Select section in the data sheet for more information.

Figure 35-1: Output Compare Block Diagram (Double-Buffered, 16-Bit PWM Mode)



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35.2 OUTPUT COMPARE REGISTERS

Each output compare channel is comprised of the following registers:

- OCxCON1 and OCxCON2 – Control registers for the output compare channel
- OCxR – Data register for the output compare channel
- OCxRS – Secondary Data register for the output compare channel
- OCxTMR – The Internal Time Base register

The Control registers for the 9 output compare channels are named OC1CON1 and OC1CON2 through OC9CON1 and OC9CON2.

All of the nine control registers have identical bit definitions. They can be represented by a common register definition as listed in Register 35-1. The 'x' in OCxCON1 represents the output compare channel number.

Register 35-1: OCxCON1: Output Compare x Control Register 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—
bit 15						bit 8	

R/W-0	U-0	U-0	R/W-0 HCS	R/W-0	R/W-0	R/W-0	R/W-0
ENFLT0	—	—	OCFLT0	TRIGMODE	OCM2 ⁽¹⁾	OCM1 ⁽¹⁾	OCM0 ⁽¹⁾
bit 7						bit 0	

Legend:	HCS = Hardware Clearable/Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown
	U = Unimplemented bit, read as '0'

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **OCSIDL:** Stop Output Compare x in Idle Mode Control bit
 - 1 = Output compare x halts in CPU Idle mode
 - 0 = Output compare x continues to operate in CPU Idle mode
- bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits
 - 111 = Peripheral clock (FCY)
 - 110 = Reserved
 - 101 = Reserved
 - 100 = Timer1 clock (only synchronous clock is supported)
 - 011 = Timer5 clock
 - 010 = Timer4 clock
 - 001 = Timer3 clock
 - 000 = Timer2 clock
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **ENFLT0:** Fault 0 Input Enable bit
 - 1 = Fault inputs are enabled
 - 0 = Fault inputs are disabled
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **OCFLT0:** PWM Fault Condition Status bit
 - 1 = PWM Fault condition has occurred
 - 0 = No PWM Fault condition has occurred
- bit 3 **TRIGMODE:** Trigger Status Mode Select bit
 - 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
 - 0 = TRIGSTAT is cleared only by software

- Note 1:** The OCx output must also be configured to an available RPn pin if the device supports Peripheral Pin Select. For more information, refer to the specific device data sheet.
- 2:** OCFA pin controls the OC1-OC4 channels; OCFB pin controls the OC5-OC9 channels. OCxR and OCxRS are double-buffered only in PWM modes.

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Register 35-1: OCxCON1: Output Compare x Control Register 1 (Continued)

- bit 2-0 **OCM<2:0>**: Output Compare Mode Select bits⁽¹⁾
- 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS⁽²⁾
 - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR⁽²⁾
 - 101 = Double Compare Continuous Pulse mode: Initialize OCx pin low, toggle OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initialize OCx pin low, toggle OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare events with OCxR, continuously toggle OCx pin
 - 010 = Single Compare Single-Shot mode: Initialize OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initialize OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled

Note 1: The OCx output must also be configured to an available RPN pin if the device supports Peripheral Pin Select. For more information, refer to the specific device data sheet.

2: OCFA pin controls the OC1-OC4 channels; OCFB pin controls the OC5-OC9 channels. OCxR and OCxRS are double-buffered only in PWM modes.

Register 35-2: OCxCON2: Output Compare x Control Register 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0 HS	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSELO
bit 7							bit 0

Legend:	HS = Hardware Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **FLTMD**: Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLT0 bit is cleared in software and a new PWM period starts
 - 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts
- bit 14 **FLTOUT**: Fault Out bit
- 1 = PWM output is driven high on a Fault
 - 0 = PWM output is driven low on a Fault
- bit 13 **FLTTRIEN**: Fault Output State Select bit
- 1 = OCx pin is tri-stated on Fault condition
 - 0 = OCx pin I/O state defined by FLTOUT bit on Fault condition
- bit 12 **OCINV**: OCMP Invert bit
- 1 = OCx output is inverted
 - 0 = OCx output is not inverted
- bit 11-9 **Unimplemented**: Read as '0'
- bit 8 **OC32**: Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation enabled
 - 0 = Cascade module operation disabled

Note 1: Never use an OCx module as its own trigger source, either by selecting this mode or other equivalent SYNCSEL settings.

2: Use these inputs as trigger sources only and never as Sync sources.

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Register 35-2: OCxCON2: Output Compare x Control Register 2 (Continued)

bit 7	OCTRIG: OCx Trigger/Sync Select bit 1 = Trigger OCx from source designated by SYNCSELx bits 0 = Synchronize OCx with source designated by SYNCSELx bits
bit 6	TRIGSTAT: Timer Trigger Status bit 1 = Timer source has been triggered and is running 0 = Timer source has not been triggered and is being held clear
bit 5	OCTRIS: OCx Output Pin Direction Select bit 1 = OCx is tri-stated 0 = Output compare module drives the OCx pin
bit 4-0	SYNCSEL<4:0>: Trigger/Synchronization Source Selection bits 11111 = This OCx module ⁽¹⁾ 11110 = Input Capture 9 ⁽²⁾ 11101 = Input Capture 6 ⁽²⁾ 11100 = CTMU ⁽²⁾ 11011 = A/D ⁽²⁾ 11010 = Comparator 3 ⁽²⁾ 11001 = Comparator 2 ⁽²⁾ 11000 = Comparator 1 ⁽²⁾ 10111 = Input Capture 4 ⁽²⁾ 10110 = Input Capture 3 ⁽²⁾ 10101 = Input Capture 2 ⁽²⁾ 10100 = Input Capture 1 ⁽²⁾ 10011 = Input Capture 8 ⁽²⁾ 10010 = Input Capture 7 ⁽²⁾ 1000x = Reserved 01111 = Timer5 01110 = Timer4 01101 = Timer3 01100 = Timer2 01011 = Timer1 01010 = Input Capture 5 ⁽²⁾ 01001 = Output Compare 9 01000 = Output Compare 8 00111 = Output Compare 7 00110 = Output Compare 6 00101 = Output Compare 5 00100 = Output Compare 4 00011 = Output Compare 3 00010 = Output Compare 2 00001 = Output Compare 1 00000 = Not synchronized to any other module

Note 1: Never use an OCx module as its own trigger source, either by selecting this mode or other equivalent SYNCSEL settings.

2: Use these inputs as trigger sources only and never as Sync sources.

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Register 35-3: OCxR: Compare Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRB15	OCRB14	OCRB13	OCRB12	OCRB11	OCRB10	OCRB9	OCRB8
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRB7	OCRB6	OCRB5	OCRB4	OCRB3	OCRB2	OCRB1	OCRB0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **OCRB<15:0>**: Primary Compare Register Value bits
 When OCxR<2:0> = 0b110: This register is used for the duty cycle in an edge-aligned PWM
 When OCxR<2:0> = 0b111, 0b101, 0b100: This register is used for generating a positive edge
 When OCxR<2:0> = 0b001, 0b010, 0b011: This register is used for generating all edges

Register 35-4: OCxRS: Secondary Compare Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRSB15	OCRSB14	OCRSB13	OCRSB12	OCRSB11	OCRSB10	OCRSB9	OCRSB8
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCRSB7	OCRSB6	OCRSB5	OCRSB4	OCRSB3	OCRSB2	OCRSB1	OCRSB0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **OCRSB<15:0>**: Secondary Compare Register Value bits
This is the Period register:
 If OCxCON2.SYNCSEL<4:0> = 0x1F
 If OCxCON2.SYNCSEL<4:0> = N (where N is the alternate value to select this as the Period register)
 If OCxCON2.OCTRIG = 1
All other conditions:
 The period is determined outside this module. Used for generating a negative edge when
 OCM<2:0> = 0b111, 0b101 or 0b100

35.3 MODES OF OPERATION

Each output compare module comprises the following modes of operation:

- Single Compare Match mode
- Dual Compare Match mode generating:
 - Single output pulse
 - Continuous output pulse
- Simple Pulse-Width Modulation mode with/without Fault protection:
 - Edge-aligned
 - Center-aligned
- Cascade mode (32-bit operation)

Before understanding the modes, it is necessary to understand the synchronization/trigger. In synchronous operation, the internal timer is reset (to zero) when the source selected by the SYNCSEL<4:0> (OCxCON2<4:0>) bits send a Sync signal. In Trigger mode, the internal timer is held in the Reset state until the selected trigger source sends a Sync signal.

The Synchronous or Trigger mode is selected by the OCTRIG (OCxCON2<7>) bit and the synchronization/trigger source can be selected by the SYNCSEL<4:0> bits as indicated in **Section 35.2 “Output Compare Registers”**.

- | |
|---|
| <p>Note 1: SYNCSEL<4:0> = 0b00000 puts the timer in a Free-Running mode with no synchronization.</p> <p>2: SYNCSEL<4:0> = 0b11111 makes the timer reset when it reaches the value of OCxRS, making the OCx module use its own Sync signal.</p> <p>3: OCx module sends out a synchronization/trigger signal when its timer matches OCxRS.</p> |
|---|

For more information on Synchronous/Trigger mode, refer to **Section 35.3.3.7 “Synchronous Operation”**.

35.3.1 Single Compare Match Mode

When control bits, OCM2:OCM0 of the OCxCON1 register = 0b001, 0b010 or 0b011, the selected output compare channel is configured as:

- If OCM = 0b001: The OCx pin is initially set low; a subsequent compare event with OCxR sets the pin high
- If OCM = 0b010: The OCx pin is initially set high; a subsequent compare event with OCxR sets the pin low
- If OCM = 0b011: The OCx pin is initially set low, a subsequent compare event with OCxR toggles the pin

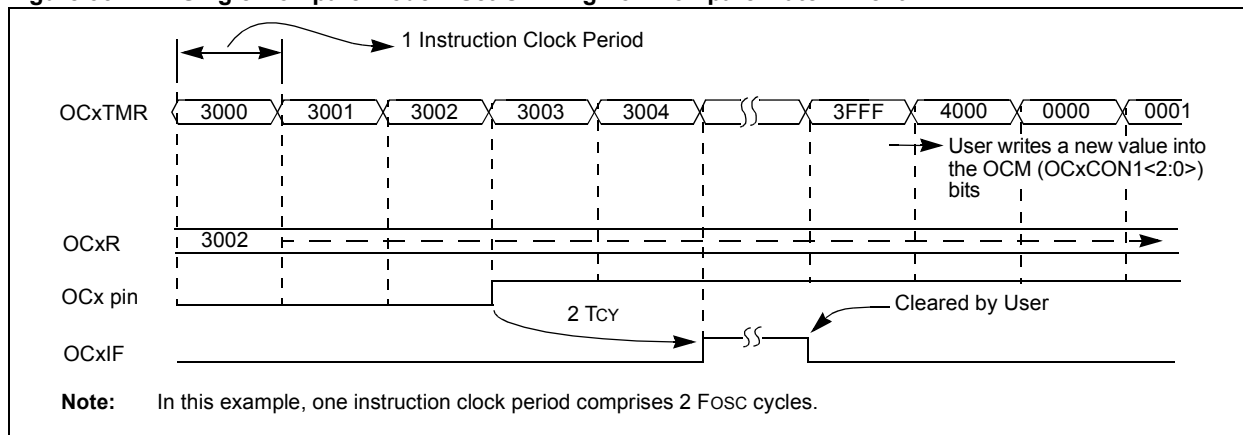
In Single Compare mode, the OCxR register is used to generate compare events. This register is loaded with a value and is compared with the module Timer register. The interrupt is set on each compare event if there is a level change in the OCx pin.

35.3.1.1 SINGLE COMPARE MODE OUTPUT DRIVEN HIGH

To configure the module for this mode, set control bits, $OCM\langle 2:0 \rangle$ ($OCxCON1\langle 2:0 \rangle$) = $0b001$. Once this Compare mode is enabled, the output pin, OCx , would be initially driven low and remain low until a match between the timer and the $OCxR$ registers occurs. Figure 35-2 provides the following key timing events:

- The OCx pin is driven high one instruction clock after a compare match between the timer and the $OCxR$ register. The OCx pin remains high until a mode change or the module is turned off.
- The timer counts up until it rolls over, or a synchronization event occurs, and then resets (to $0x0000$) on the next instruction clock.
- The respective channel interrupt flag, $OCxIF$, is asserted two instruction clocks after the OCx pin is driven high.

Figure 35-2: Single Compare Mode – Set OCx High on Compare Match Event



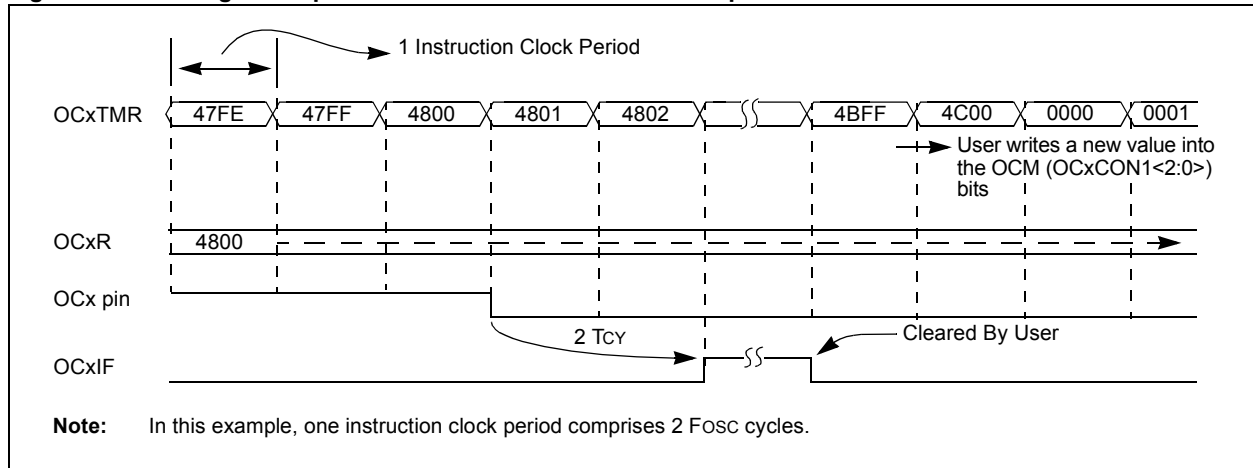
35.3.1.2 SINGLE COMPARE MODE OUTPUT DRIVEN LOW

To configure the output compare module for this mode, set control bits, $OCM\langle 2:0 \rangle$ = $0b010$. Once this Compare mode is enabled, the output pin and the OCx would be initially driven high and remain high until a match occurs between the Timer and the $OCxR$ registers. Figure 35-3 provides the key timing events.

- The OCx pin is driven low one instruction clock after a compare match event occurs between the timer and the $OCxR$ register. The OCx pin remains low until a mode change or the module is turned off.
- The timer counts up until it rolls over or a synchronization event occurs, and then resets to $0x0000$ on the next instruction clock.
- The respective channel interrupt flag, $OCxIF$, is asserted two instruction clocks after OCx pin is driven low.

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Figure 35-3: Single Compare Mode – Force OCx Low on Compare Match Event

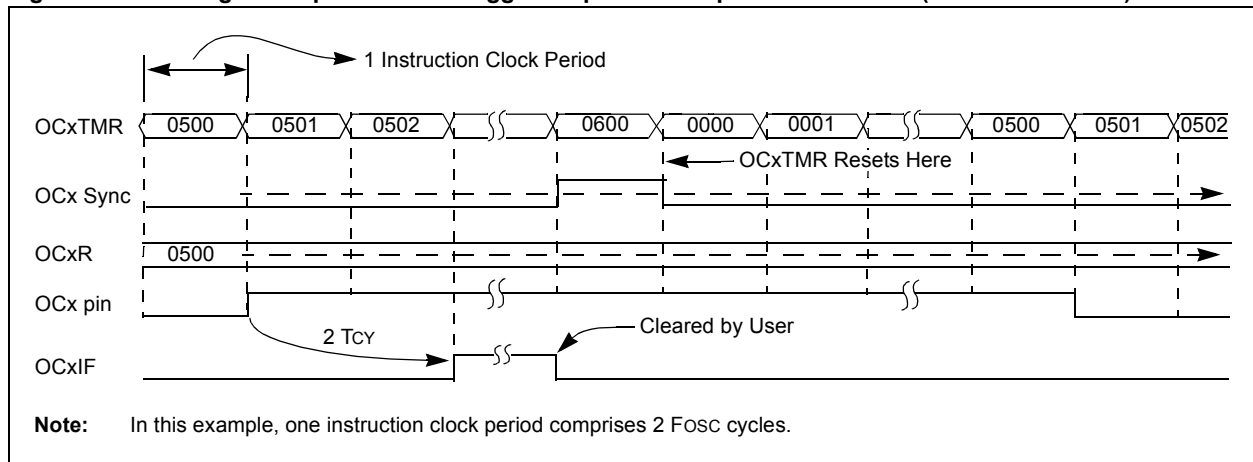


35.3.1.3 SINGLE COMPARE MODE TOGGLE OUTPUT

To configure the output compare module for this mode, set control bits, $OCM\langle 2:0 \rangle = 0b011$. Once this Compare mode has been enabled, the output pin and the OCx toggle on every match event between the timer and the OCxR registers. Figure 35-4 provides the key timing events.

- The OCx pin is toggled one instruction clock after a compare match occurs between the timer and OCxR register. The OCx pin remains at this new state until the next toggle event, or until a mode change has been made or the module is turned off.
- The timer counts up until it rolls over or synchronization occurs, and then resets to 0x0000 on the next instruction clock.
- The respective channel interrupt flag, OCxIF, is asserted two instruction clocks after the OCx pin is toggled.
- The internal OCx pin output logic is set to a logic '0' on a device Reset. However, the operational OCx pin state for the Toggle mode can be set by the user software.

Figure 35-4: Single Compare Mode – Toggle Output on Compare Match Event (OCxTMR > OCxR)



Example 35-1: Single Compare Mode Toggle Output

```

OC1CON1 = 0;          /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                             module */
OC1R = 1000;         /* This is just a typical number, user must calculate based on the
                             waveform requirements and the system clock */
OC1CON1bits.OCM = 3; /* This selects the toggle mode */
    
```

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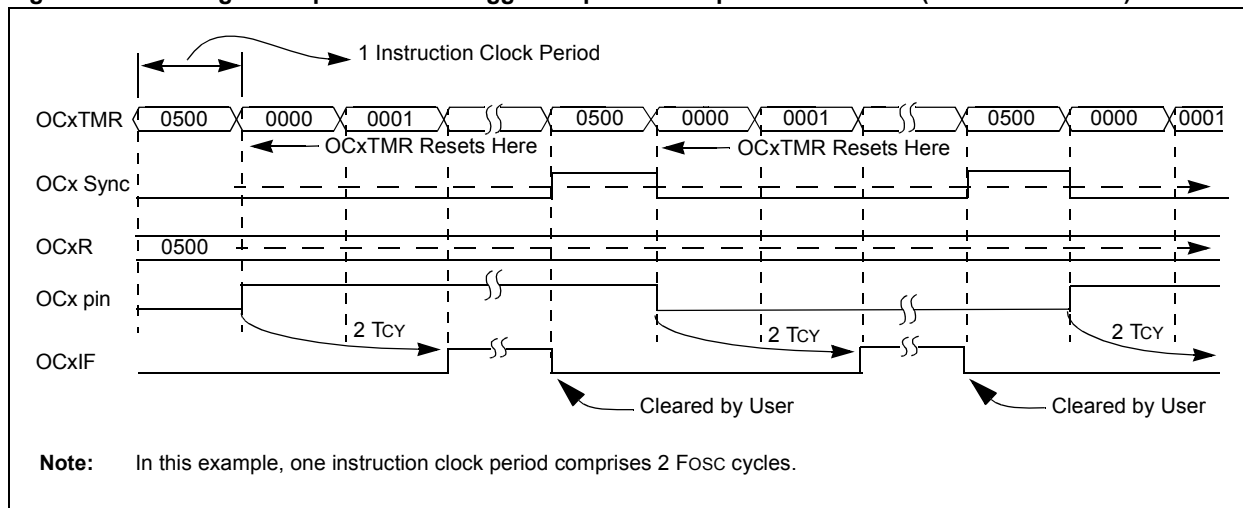
35.3.1.4 SPECIAL CASES OF SINGLE COMPARE MODE

Consider the following few special cases:

Table 35-1: Special Cases of Single Compare Mode

Special Condition	Operation	Output
When OCxR > timer period (as determined by the Sync source)	No compare event occurs and the compare output remains at the initial condition.	No change in output level
When OCxR = timer period (as determined by the Sync source)	The compare output functions normally. Combining this with the Toggle mode can be used to generate a fixed frequency square wave as illustrated in Figure 35-5.	Output level transition
When the module is enabled into a Single Compare mode, OCxR = 0x0000, and the timer is held in Reset, the Sync source is active	The compare output remains in the initial condition.	No change in output level
If, after a compare event, the OCxR register is cleared and the Sync source becomes active	Output remains in the new state.	No further change in output level

Figure 35-5: Single Compare Mode – Toggle Output on Compare Match Event (OCxTMR = OCxR)



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35.3.2 Dual Compare Match Mode

When control bits, $OCM<2:0> = 0b100$ or $0b101$, the selected output compare channel is configured for one of the two following Dual Compare Match modes:

- Single Output Pulse mode
- Continuous Output Pulse mode

In the Dual Compare mode, the module uses both the OCxR and OCxRS registers for the compare match events. The OCxR register is compared with the incrementing timer count, OCxTMR, and the rising (leading) edge of the pulse is generated at the OCx pin on a compare match event. The OCxRS register is then compared to the same incrementing timer count, OCxTMR, and the falling (trailing) edge of the pulse is generated at the OCx pin on a compare match event.

35.3.2.1 DUAL COMPARE SINGLE PULSE MODE

When control bits, $OCM<2:0> = 0b100$, the selected output compare channel is configured so that the OCx pin is initialized low and a single output pulse is generated. Refer to Figure 35-6 and Figure 35-7.

1. Once the Dual Compare Single Pulse mode is enabled, the OCx pin would be driven low.
2. Upon the first timer compare match with OCxR, the Compare register, its pin (OCx) would be driven high.
3. When the incrementing timer count matches Compare register, OCxRS, the second and trailing edge (high-to-low) of the pulse is driven onto the OCx pin. At this second compare, the OCxIF interrupt flag bit gets set.

Note 1: While the mode bits do not change after the falling edge of the pulse, if another write with the same value occurs on the same control bits, a new single output pulse sequence is generated.

2: OCxRS must be greater than the OCxR by a minimum of 2.

Figure 35-6: Dual Compare Mode Single Output Pulse

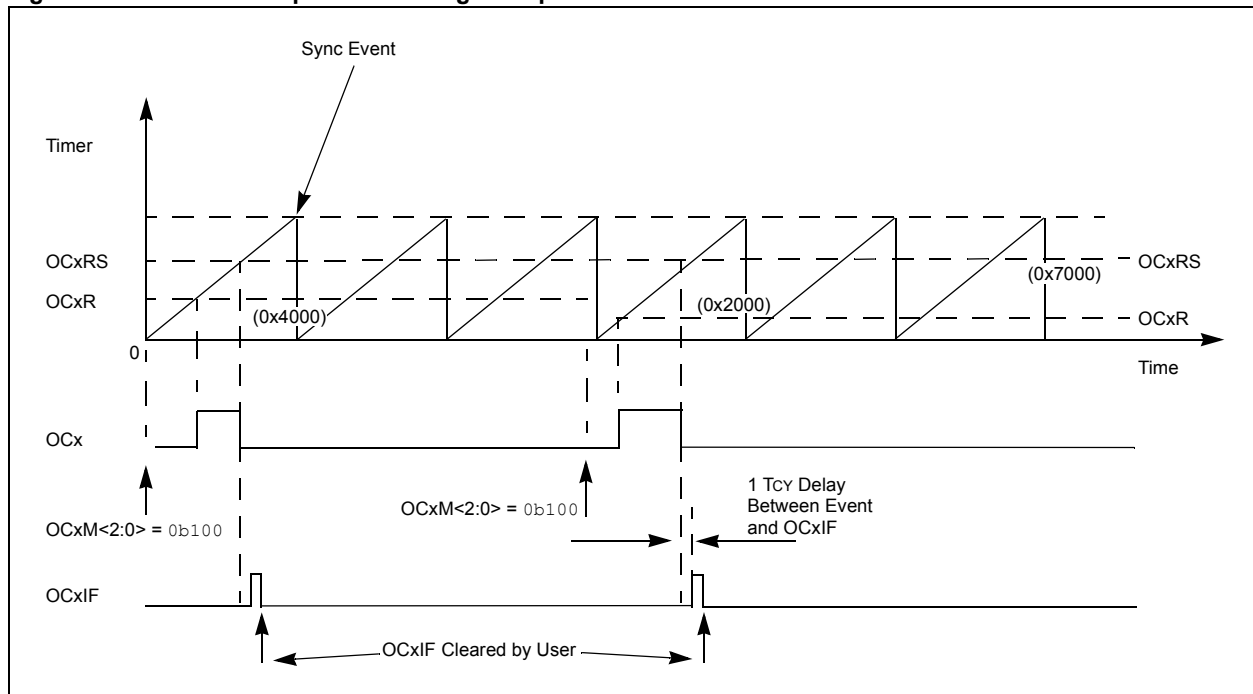
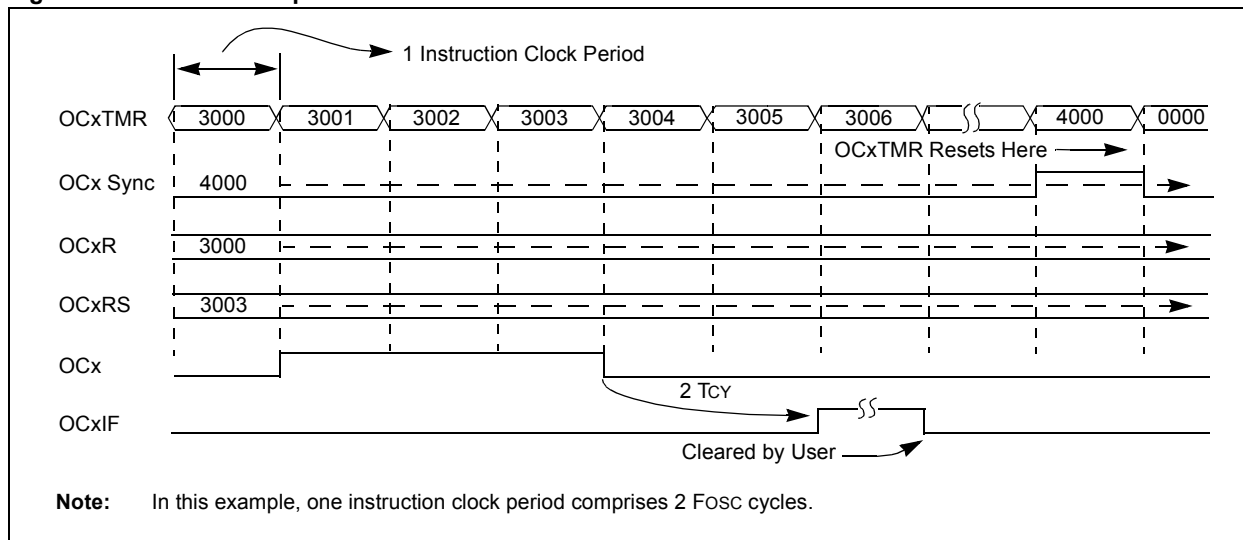


Figure 35-7: Dual Compare Mode



35.3.2.2 TO SET UP SINGLE OUTPUT PULSE GENERATION

To configure the module for the generation of a single output pulse, perform the following steps:

1. Determine the instruction cycle time, T_{CY} .
2. Calculate the desired pulse-width value base upon T_{CY} .
3. Calculate the time to start pulse from timer start value of 0x0000.
4. Write pulse-width start and stop times into OCxR and OCxRS Compare registers.
5. Select SYNCSEL<4:0> so that the synchronization is active after the timer is equal to or greater than the value in OCxRS.
6. Set OCM<2:0> = 0b100.
7. Issue another write to set OCM<2:0> = 0b100, to initiate another single pulse with the same parameters.
8. Disable the OCx by writing OCM<2:0> = 0b000, change the parameters, and then enable the OCx by writing OCM<2:0> = 0b100 to initiate another single pulse with different parameters.

Note 1: Refer to Table 35-2 for several simple examples of single output pulse-width calculations.

Note 2: Refer to Table 35-3 for several simple examples of Dual Compare Match mode generating a single output pulse.

Table 35-2: Dual Compare Mode – Single Output Pulse-Width Calculation Examples

Instruction Cycle Time (T_{CY})	Desired on Time		Start Pulse Time From Timer = 0x0000		End Pulse Time (OCxRS) Register
	Time	Hex Value	Time	Hex Value (OCxR)	
30 ns	1 μ s	0x0021	10 μ s	0x014D	0x016E
30 ns	2 μ s	0x0042	10 μ s	0x014D	0x018F
50 ns	3 μ s	0x003C	10 μ s	0x00C8	0x0104
100 ns	5 μ s	0x0032	50 μ s	0x0064	0x0096
300 ns	10 μ s	0x0021	100 μ s	0x014D	0x018F
500 ns	20 μ s	0x0028	500 μ s	0x03E8	0x0410
500 ns	30 μ s	0x003C	2 ms	0x0FA0	0x0FDC

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Equation 35-1:

$$\text{OCxR Value} = \text{Desired Time/Instruction Cycle Time (TCY)}$$

Example 35-2: Dual Compare Mode – Single Output Pulse Width

```

OC1CON1 = 0;          /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                             module */
OC1R = 1000;          /* This is just a typical number, user must calculate based on the
                       waveform requirements and the system clock */
OC1RS = 2000;
OC1CON1bits.OCM = 4; /* This selects the Single Output Pulse mode */
    
```

Table 35-3: Special Cases for Dual Compare Match Mode Generating a Single Output Pulse

Special Condition	Operation	Output
Synchronization occurs when timer value is equal to OCxRS	Timer resets to zero in the next cycle, but the pulse is unaffected.	Pulse
Synchronization occurs before the timer value reaches OCxR	Timer resets to zero before any output transition.	Remains low
Synchronization occurs before the timer value reaches OCxRS but after it reaches OCxR	Only a single transition (low-to-high) is generated (see Figure 35-8).	Low-High
OCxR = OCxRS = 0x0000 and Sync occurs	The output is initialized low and does not change. No interrupt is generated.	Remains low
OCxRS < OCxR	The timer counts up to the first compare (TMRx = OCxR) and the first (rising) edge is generated. The timer then continues to count and eventually resets when the synchronization occurs or rolls over. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS) and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition.	Pulse
OCxR = OCxRS	The timer counts up to the first compare (Timer = OCxR) and the first (rising) edge is generated. The timer continues to count and eventually resets when the synchronization occurs or a rollover from 0xFFFF occurs. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS), and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition.	Pulse
OCxR = 0x0000 and OCxRS > OCxR	The first cycle of the timer counts until the synchronization occurs or rolls over; the output compare pin remains low. After the Timer register resets to zero, the output compare pin goes high. Upon the next timer match with the register, OCxRS, the output compare pin goes low and remains. The falling edge of the output pulse generates an interrupt condition (see Figure 35-9).	Pulse except for the first cycle

Figure 35-8: Dual Compare Mode – Single Output Pulse (Sync Before Timer Reaches OCxRS)

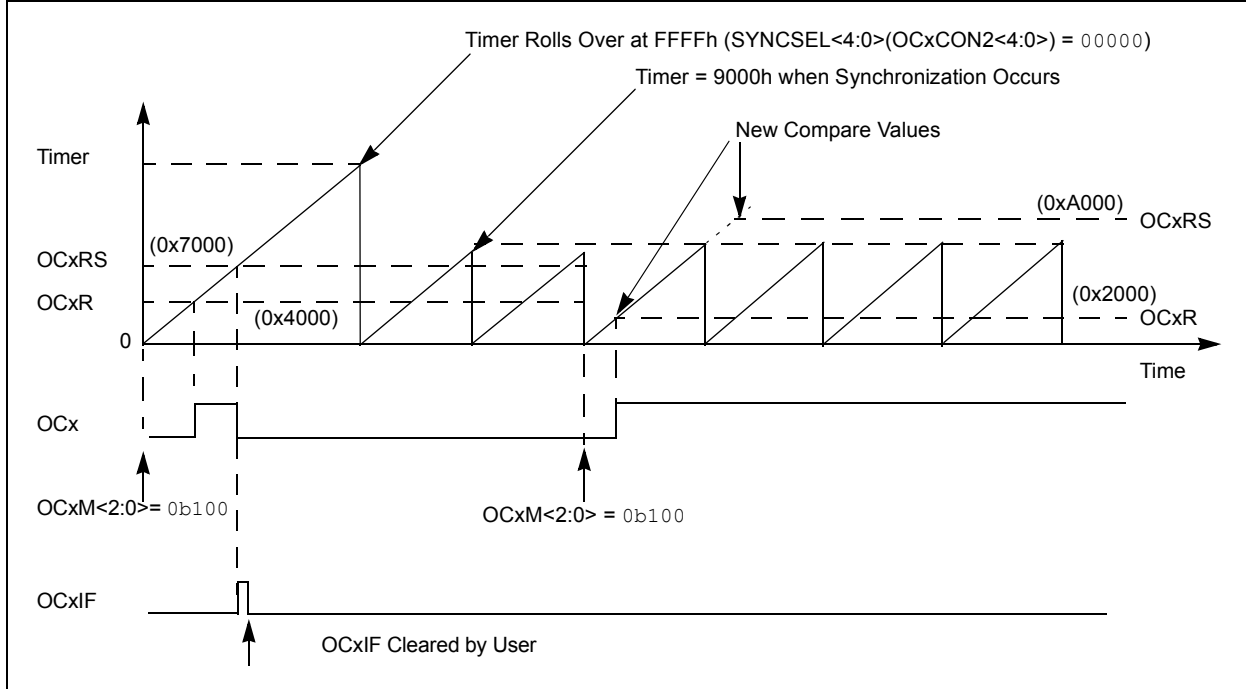
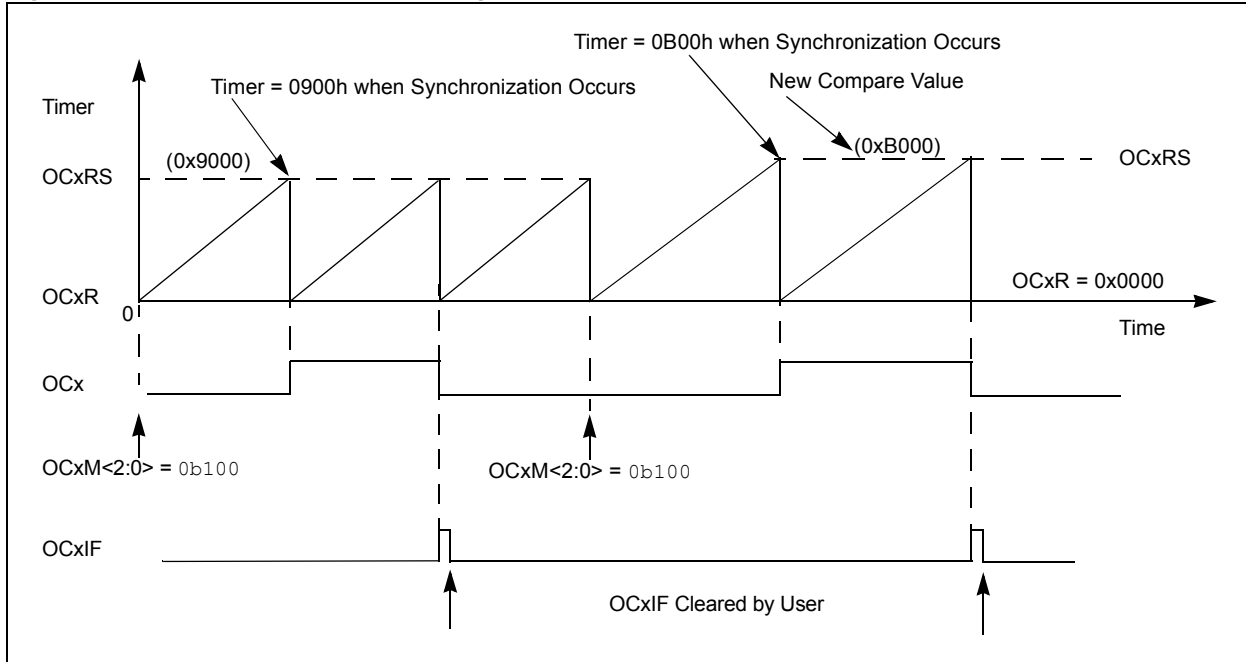


Figure 35-9: Dual Compare Mode – Single Output Pulse (OCxR = 0x0000, OCxRS > OCxR)



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35.3.2.3 DUAL COMPARE CONTINUOUS PULSE MODE

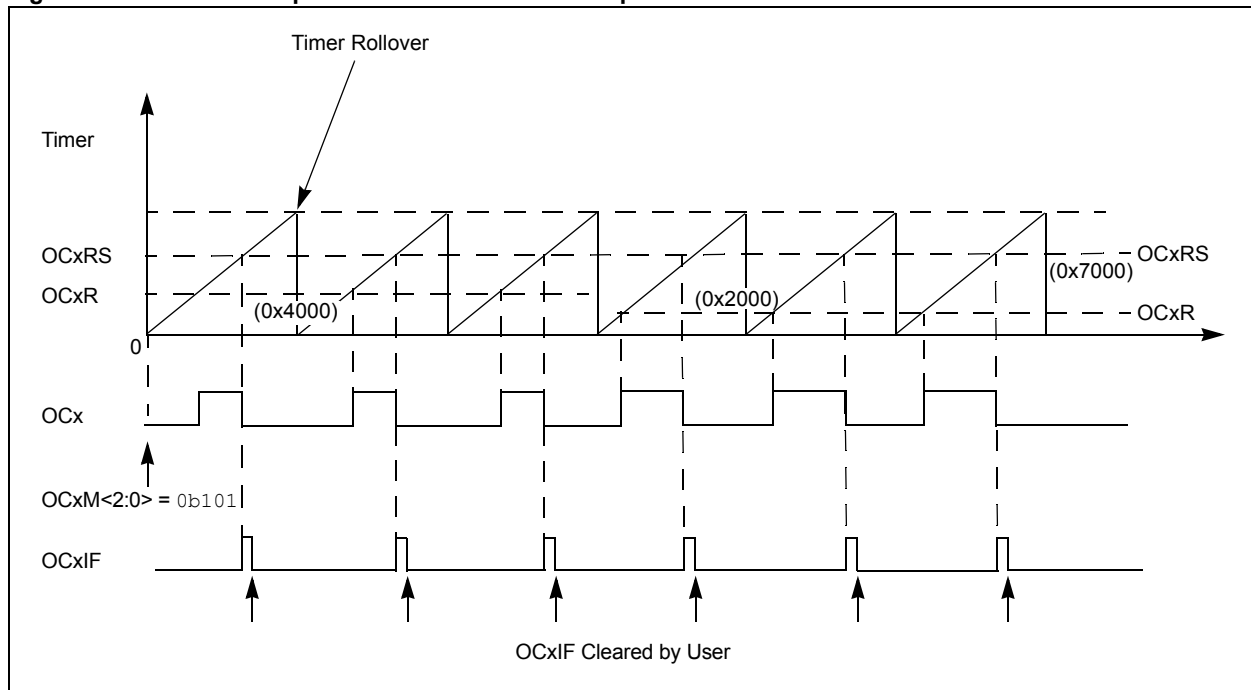
When control bits, $OCM\langle 2:0 \rangle = 0b101$, the selected output compare channel is configured so that the OCx pin is initialized low and continuous output pulses are generated. Figure 35-10 illustrates the Dual Compare Continuous Output Pulse mode.

- Once the Dual Compare Continuous Output Pulse mode is enabled, the pin state would be driven low.
- Upon the first timer compare match with compare register, OCxR, the OCx pin would be driven high.
- When the incrementing timer count matches Compare register, OCxRS, the second and the trailing edge (high-to-low) of the pulse are driven onto the OCx pin. At this second compare, the OCxIF interrupt flag bit is set.

Note 1: Unlike the Single Output Pulse mode, the output pulses continue indefinitely until the mode is terminated by user firmware or by a Reset. The falling edge of each output pulse sets the interrupt flag.

2: One way of generating a pulse with 50% duty cycle is by setting $OCxR = OCxRS$ (this value must be within the Period register range as the period is determined by the Sync source).

Figure 35-10: Dual Compare Mode – Continuous Output Pulses



35.3.2.4 SETUP FOR CONTINUOUS OUTPUT PULSE GENERATION

To configure this module for the generation of a continuous stream of output pulses, perform the following steps:

1. Determine instruction cycle time, T_{CY} .
2. Calculate the timer to start pulse width from the timer start value of 0x0000.
3. Calculate the timer to stop pulse width from the timer start value of 0x0000.
4. Write pulse-width start and stop times into the OCxR and OCxRS Compare registers, respectively. The Sync signal should occur when OCxRS = timer or after.
5. Set OCM<2:0> = 0b101; the timer must be enabled.

Example 35-3: Continuous Output Pulse Generation

```

OC1CON1 = 0;
OC1CON2 = 0;           /* It is a good practice to clear off the control bits initially */
OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                           module */
OC1R = 1000;          /* This is just a typical number, user must calculate based on the
                       waveform requirements and the system clock */
OC1RS = 2000;
T1CON = 0;
PR1 = 3000;           /* Determines the period */
OC1CON2bits.SYNCSEL = 0x0B; /* TMR1 is the sync source */
OC1CON1bits.OCM = 5;  /* This selects the Continuous Pulse mode*/
T1CONbits.TON = 1;    /* OC1TMR does not run until the sync source is switched on */
    
```

Table 35-4: Dual Compare Mode – Continuous Output Pulse-Width Calculation Examples

Instruction Cycle Time (T _{CY})	Desired Pulse Width		Start Pulse Time From Timer = 0x0000		Period Register Contents	End Pulse Time (OCxRS) Register (for 50% duty cycle)
	Time	Hex Value	Time	Hex Value (OCxR)		
30 ns	1 μs	0x0021	10 μs	0x014D	0x016F	0x015D
30 ns	2 μs	0x0042	10 μs	0x014D	0x0190	0x016F
50 ns	3 μs	0x003C	10 μs	0x00C8	0x0105	0x00E6
100 ns	5 μs	0x0032	50 μs	0x0064	0x0097	0x007D
300 ns	10 μs	0x0021	100 μs	0x014D	0x0190	0x015D
500 ns	20 μs	0x0028	500 μs	0x03E8	0x057A	0x03FC
500 ns	30 μs	0x003C	2 ms	0x0FA0	0x0FC9	0x0FBE

Equation 35-2:

$$\text{Hex Value} = \text{Desired Time} / \text{Instruction Cycle Time (T}_{CY}\text{)}$$

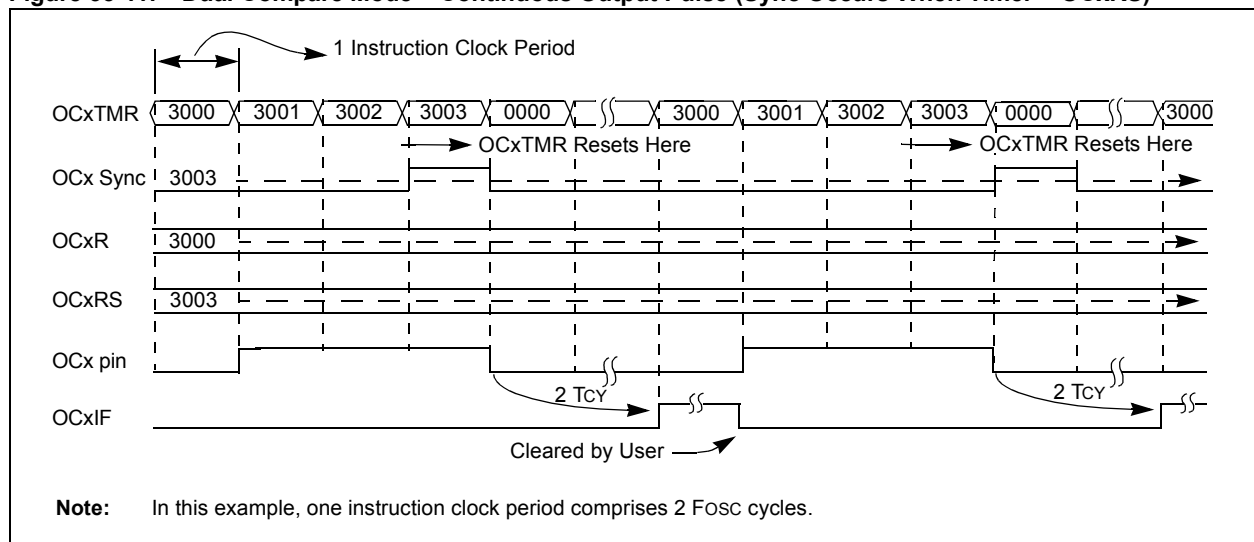
Note: Timer module with the same clock as OCx is used as the Sync source in this example.

Section 35. Output Compare with Dedicated Timer

Table 35-5: Special Cases for Dual Compare Match Mode Generating Continuous Output Pulse

Special Condition	Operation	Output
Synchronization occurs when the timer value is equal to OCxRS	Timer resets to zero in the next cycle, but the pulse is unaffected (see Figure 35-11).	Pulses
Synchronization occurs before the timer value reaches OCxR	Timer resets to zero before any output transition.	Remains low
Synchronization occurs before the timer value reaches OCxRS but after it reaches OCxR	Only a single transition (low-to-high) is generated (see Figure 35-12).	Low-High
OCxR = OCxRS = 0x0000 and synchronization occurs	The output is initialized low and does not change. No interrupt is generated.	Remains low
OCxRS < OCxR	The timer counts up to the first compare (TMRx = OCxR) and the first (rising) edge is generated. The timer then continues to count and eventually resets when synchronization occurs or rolls over. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS) and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition. The sequence repeats until the module is disabled.	Pulses
OCxR = OCxRS	The timer counts up to the first compare (Timer = OCxR) and the first (rising) edge is generated. The timer continues to count and eventually resets when synchronization occurs or a rollover from FFFFh occurs. The timer then restarts from 0x0000 and counts up to the second compare (TMRx = OCxRS), and the second (falling) edge of the signal is generated. The falling edge of the output pulse generates an interrupt condition. The sequence repeats until the module is disabled.	Pulses
OCxR = 0x0000 and OCxRS > OCxR	The first cycle of the timer counts until synchronization occurs or rolls over; the output compare pin remains low. After the Timer register resets to zero, the output compare pin goes high. Upon the next timer match with the register, OCxRS, the output compare pin goes low and remains low. The falling edge of the output pulse generates an interrupt condition (see Figure 35-13). The sequence repeats until the module is disabled.	Pulses except for the first cycle

Figure 35-11: Dual Compare Mode – Continuous Output Pulse (Sync Occurs When Timer = OCxRS)



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Figure 35-12: Dual Compare Mode – Continuous Output Pulse (Sync Before Timer Reaches OCxRS)

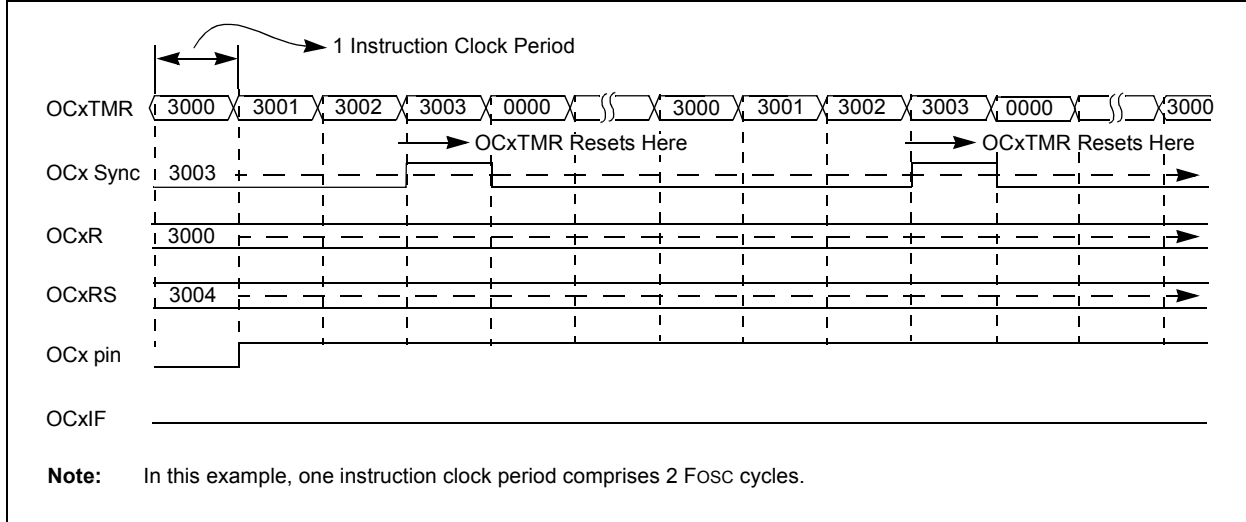
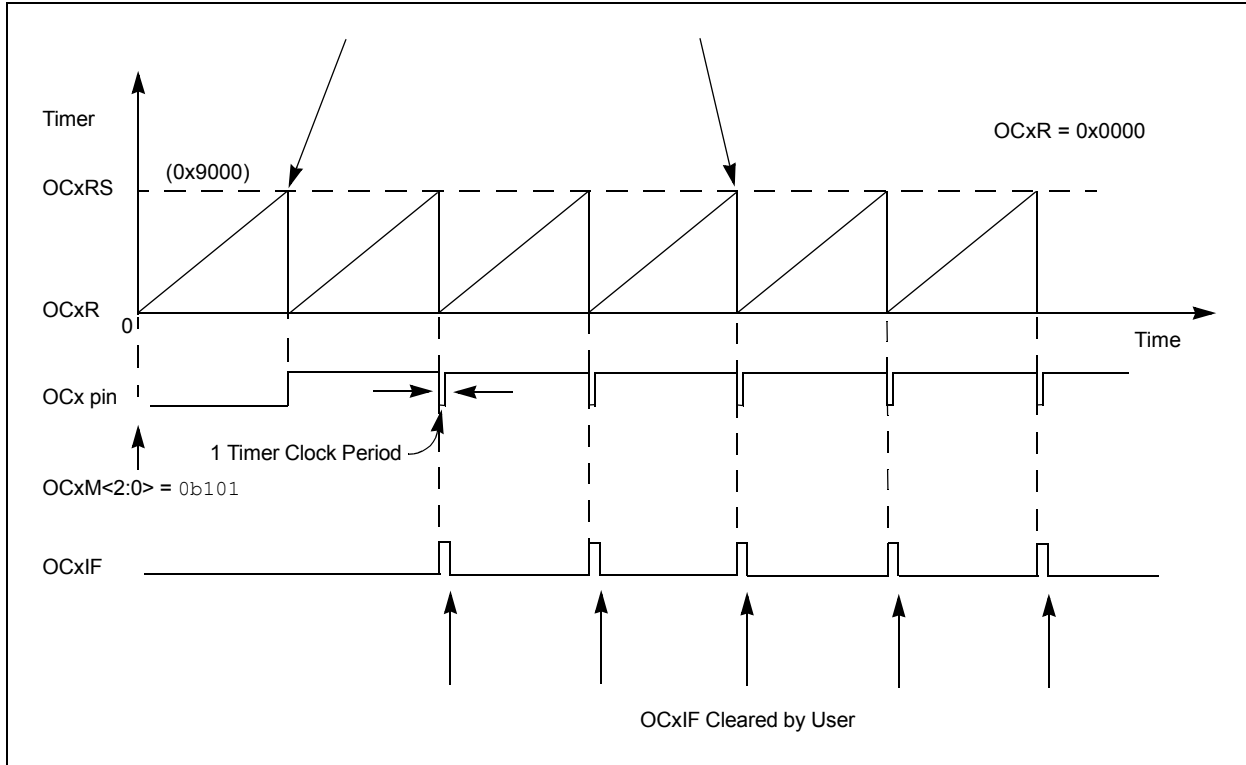


Figure 35-13: Dual Compare Mode – Continuous Output Pulse (OCxR = 0x0000 (SYNCSEL<4:0> = 0x1F))



Section 35. Output Compare with Dedicated Timer

35.3.3 Pulse-Width Modulation Mode

When control bits, $OCxCON1<OCM2:OCM0> = 0b110$ or $0b111$, then the PWM mode is selected. The registers, $OCxR$ and $OCxRS$, are double-buffered in these modes. This means that the changes on these registers would be reflected only after a timer rollover from $0xFFFF$ or after a Sync event occurs. As a result, any changes in these registers during operation occurs only with the next pulse. Also, in these modes, Fault input is supported (described in the next sections).

35.3.3.1 EDGE-ALIGNED PWM MODE

When control bits, $OCM<2:0> = 0b110$, the Edge-Aligned PWM mode of operation is selected. $OCxR$ contains the current duty cycle and the $SYNCSEL$ bits determine the period. $OCxRS$ can be made to determine the period by setting $SYNCSEL<4:0> = 0x1F$.

Note: This is a migration issue for applications. In the old module, $OCxRS$ is served as a double-buffer to $OCxR$. In this version, both the registers are double-buffered.

Figure 35-14 and Figure 35-15 illustrate the PWM mode operation.

Edge-Aligned PWM Mode Operation:

- When synchronization occurs, the following four events occur on the next increment cycle:
 - The timer is reset to zero and resumes counting
 - The OCx pin is set high (exception: if $OCxRS = 0b0000$, the OCx pin would not be set)
 - The $OCxR$ and $OCxRS$ Buffered registers are updated from $OCxR$ and $OCxRS$
 - Interrupt flag, $OCxIF$, is set
- When the timer and $OCxR$ match, the pin would be set low. This match does not generate interrupts.

Figure 35-14: PWM Output Timing

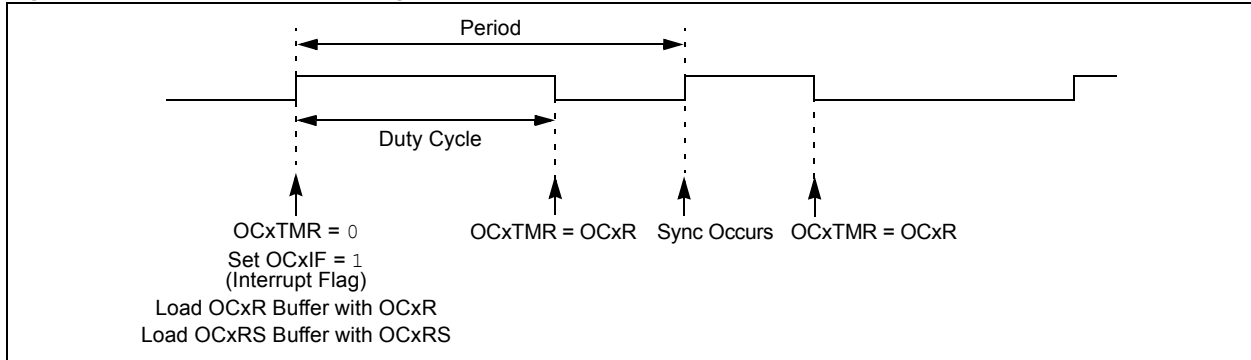
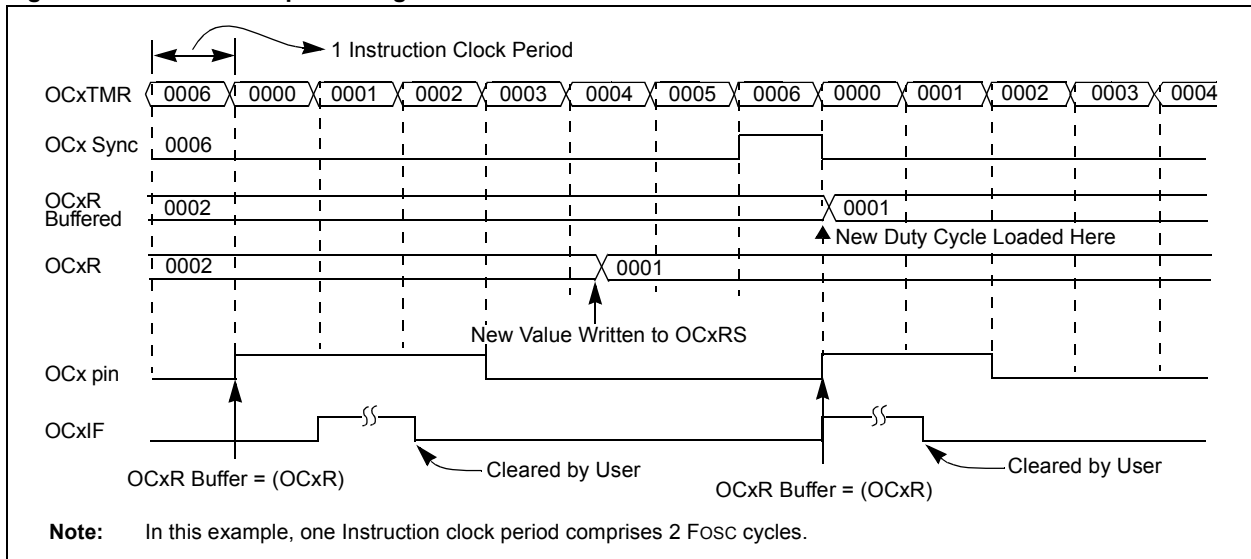


Figure 35-15: PWM Output Timing



35.3.3.2 EDGE-ALIGNED PWM MODE INITIALIZATION

1. Once the PWM mode is enabled by setting $OCM<2:0> = 0b110$, the OCx pin would be driven low if $OCxR = 0x0000$. If $OCxR$ is not equal to zero, the OCx pin would be set high (see Figure 35-16 and Figure 35-17).
2. When $OCxR$ is not equal to zero and the pin state is set to high, the first match between the $OCxR$ and the timer clears the OCx pin. The OCx pin would remain low until a valid compare between synchronization occurs or a rollover occurs (see Figure 35-17).

Figure 35-16: Edge-Aligned PWM Mode with $OCxR = 0$ – At Module Initialization, $OCxR = 0x0000$, $OCxRS = 0x5000$

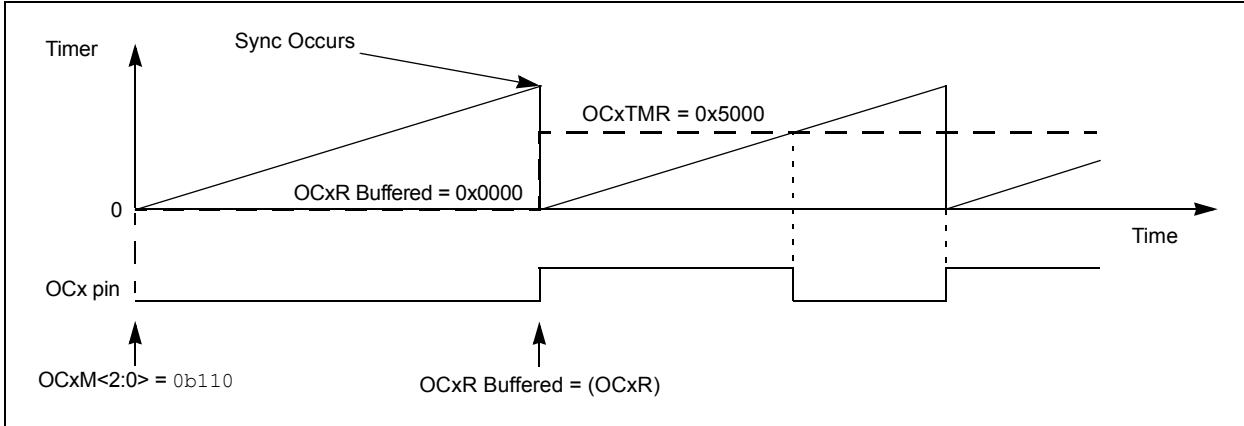
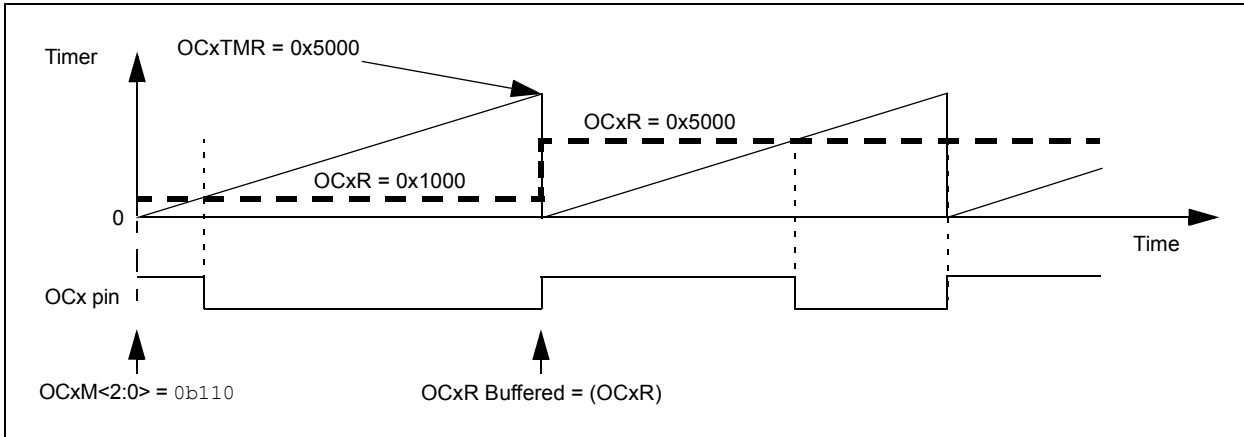


Figure 35-17: Edge-Aligned PWM Mode with $OCxR > 0$ – At Module Initialization, $OCxR = 0x1000$, $OCxRS = 0x5000$



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Figure 35-19: PWM Output Timing (100% Duty Cycle, OCxR > OCxRS (SYNCSEL<4:0> = 0x1F))

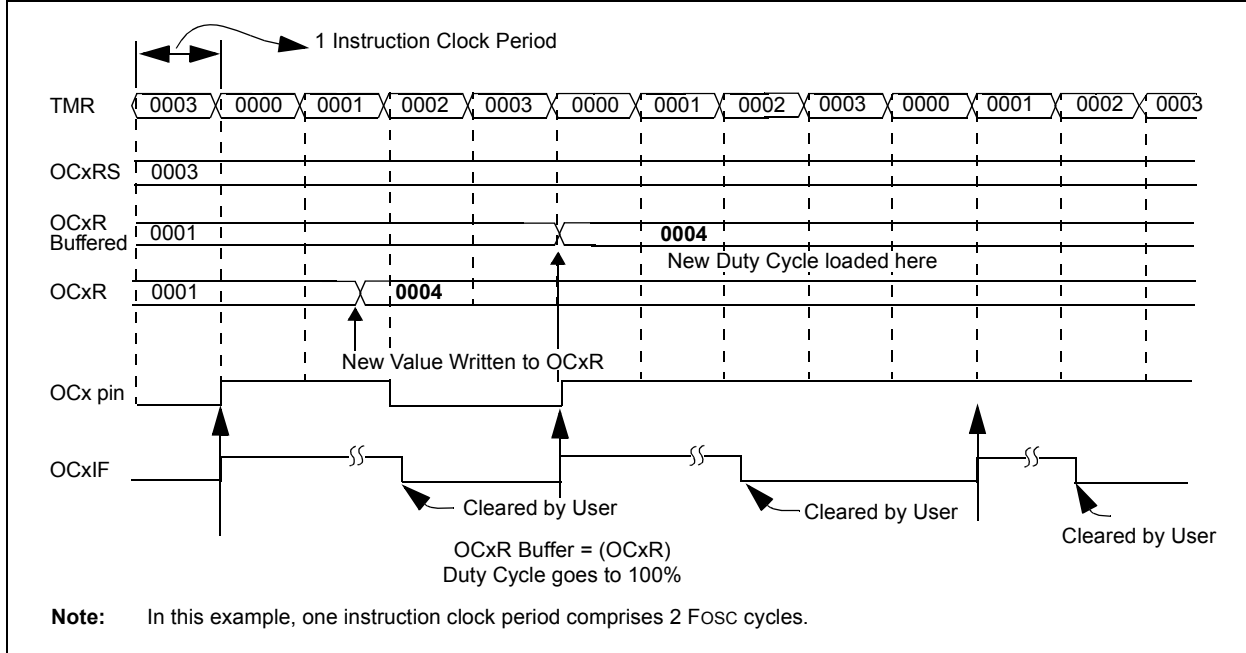
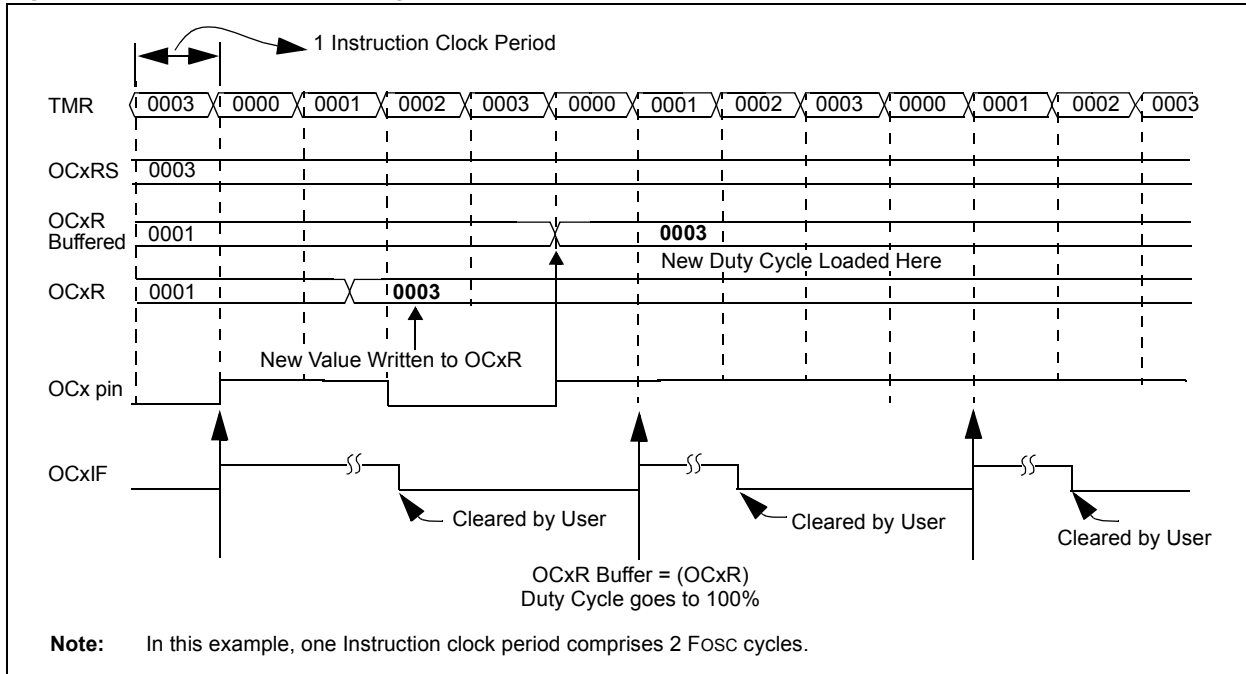


Figure 35-20: PWM Output Timing (OCxR = OCxRS (SYNCSEL<4:0> = 0x1F))



Section 35. Output Compare with Dedicated Timer

35.3.3.5 CENTER-ALIGNED PWM MODE

These mode (OCM<2:0> = 0b111) functions are the same as Continuous Pulse mode (OCM<2:0> = 0b101). The only differences are:

- OCxR and OCxRS are double-buffered, which means that the new register value would be effective only after a timer rollover or synchronization
- Fault control and pins are used

Note 1: Center alignment does not mean the pulse is exactly aligned to the center of the pulse width. It only indicates that the on time of the pulse can be positioned anywhere within the period.

35.3.3.6 FAULT INPUT AND CONTROL

When operating in either the Center-Aligned PWM mode or Edge-aligned PWM mode (OCM<2:0> (OCxCON1<2:0>) = 0b111 or 0b110), the Fault pin and its controls can be activated. Two Fault inputs, OCFA and OCFB, where OCFA controls OC1-OC4 and OCFB controls OC5-OC9, are available. The Fault pin is controlled by the register bit, ENFLT0 (OCxCON1<15>). If this bit is zero, the corresponding Fault input pin (OCFA or OCFB) is ignored. The status of the Fault input can be observed in the register bit, OCFLT0 (OCxCON1<4>).

When a Fault occurs (OCFx = 0), the OCx pin output level is determined by the FLTOUT (OCxCON2<14>) bit. The tri-stating of the OCx pin during a Fault condition is controlled by FLTTRIEN (OCxCON2<13>).

The Fault control can operate in two modes based on the FLTMODE (OCxCON2<15>) bit:

- Inactive mode
- Cycle-by-Cycle mode. Refer to the product data sheet for details on how Fault pins are assigned to the various OCx peripherals.

Note: The Output Compare Fault pins, OCFA and OCFB, are active-low signals.

35.3.3.6.1 Inactive Mode

When FLTMODE (OCxCON2<15>) = 1, the Fault inputs operate in the Inactive mode (see Figure 35-21). If the Fault input goes active ('0'), the OCFLT0 (OCxCON1<12>) bit would be set and the module would be in the Fault condition.

It remains in the Fault condition until:

- The Fault input goes inactive and
- The OCFLT0 (OCxCON1<12>) bit is cleared in software and
- A new timer cycle is started (timer goes to 0000h)

35.3.3.6.2 Cycle-by-Cycle Mode

When FLTMODE (OCxCON2<15>) = 0, the Fault inputs operate in the Cycle-by-Cycle mode (see Figure 35-22). If a Fault input goes active ('0'), the OCFLT0 (OCxCON1<12>) bit would be set and the module would be in the Fault condition.

It remains in the Fault condition until:

- The Fault input goes inactive and
- A new timer cycle is started (timer goes to 0x0000)

Figure 35-21: Fault Input Pin Timing, Inactive Mode

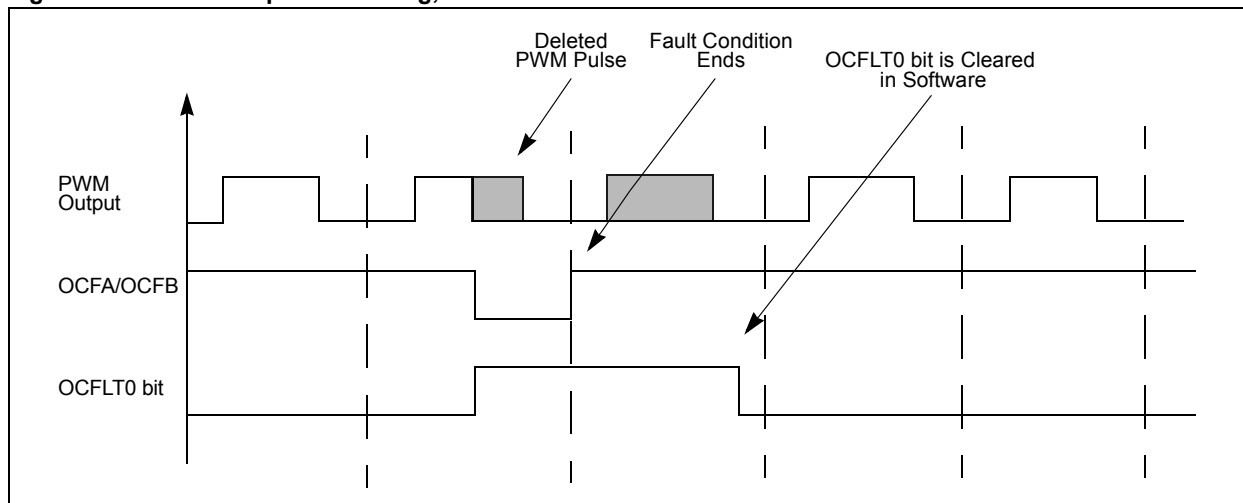
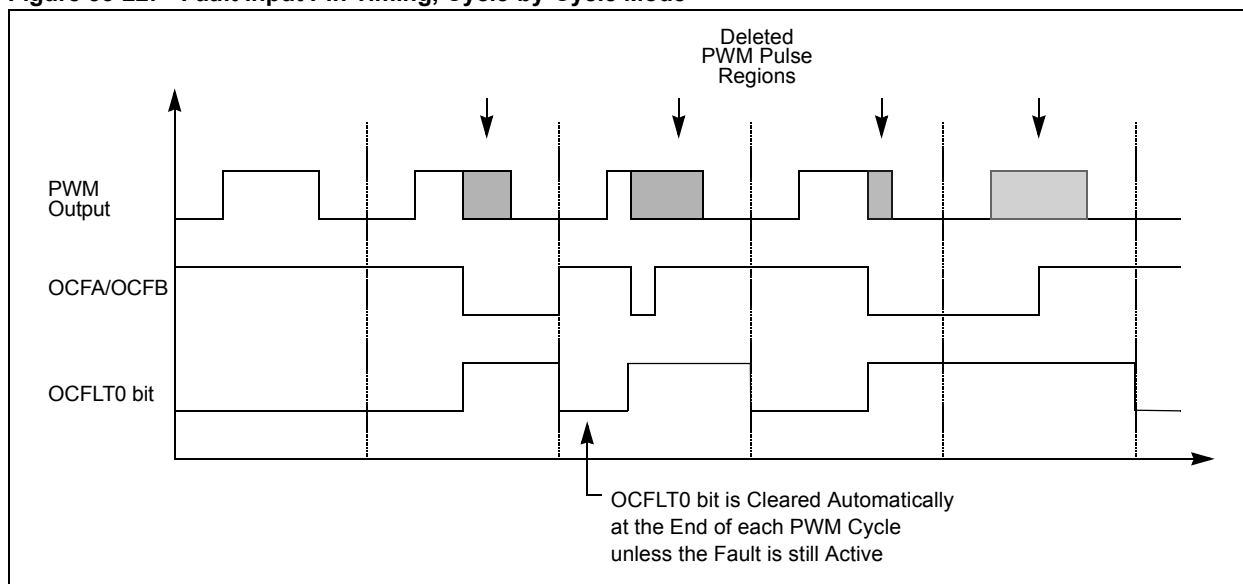


Figure 35-22: Fault Input Pin Timing, Cycle-by-Cycle Mode



35.3.3.7 SYNCHRONOUS OPERATION

Synchronous operation of the timer is enabled when the OCTRIG (OCxCON2<7>) = 0.

In synchronous operation, the TRIGSTAT (OCxCON2<6>) bit has no function. The timer can be synchronized with the other modules using the synchronization/trigger inputs (see Register 35-2). Whenever the selected module receives a synchronization signal, the timer would roll over to 0x0000 on the next positive edge of the selected clock.

35.3.3.8 USE OF THE MODULE TIMER IN A SYNCHRONIZED APPLICATION

Figure 35-23 illustrates the connections for synchronization and Figure 35-24 illustrates the timing for multiple modules being synchronized. OC2 is being synchronized to OC1. The synchronization signal from OC1 is selected for synchronization by both OC1 and OC2 using the SYNCSEL<4:0>(OCxCON2<4:0>) bits. The OC1RS register now becomes the Period register for both OC1 and OC2.

When the OC1RS register matches the OC1 timer value, the OC1 module produces the synchronization signal. This causes the timers in both OC1 and OC2 to go to zero on the next positive clock edge.

Note: Synchronized modules should select the same clock source to ensure proper function.

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Figure 35-23: Synchronous Operation Integration (TRIGEN = 0)

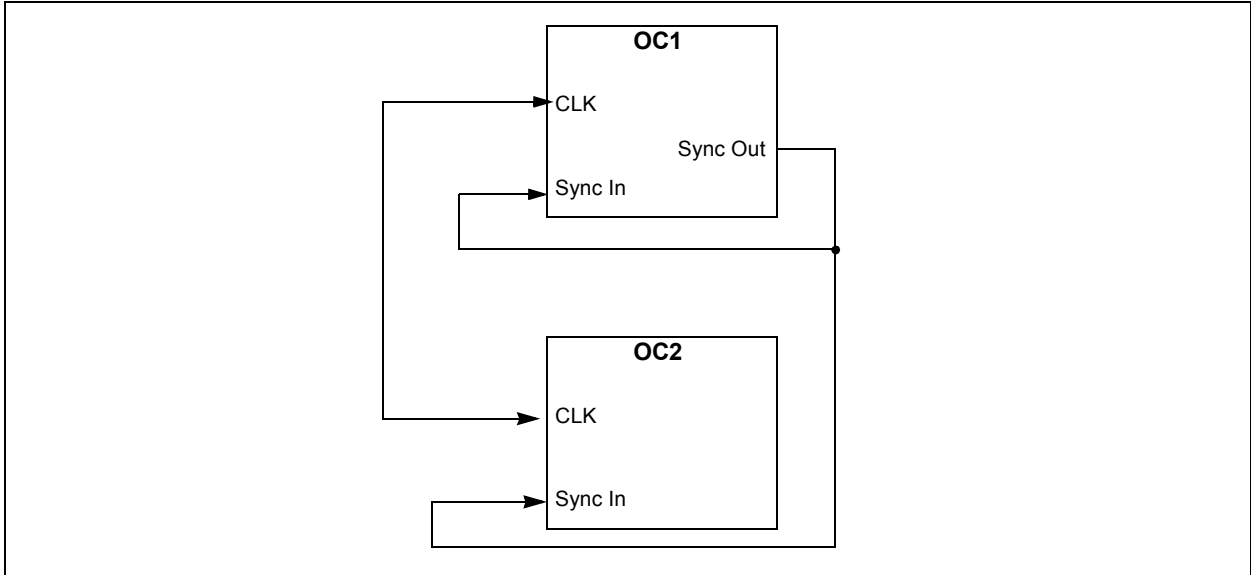
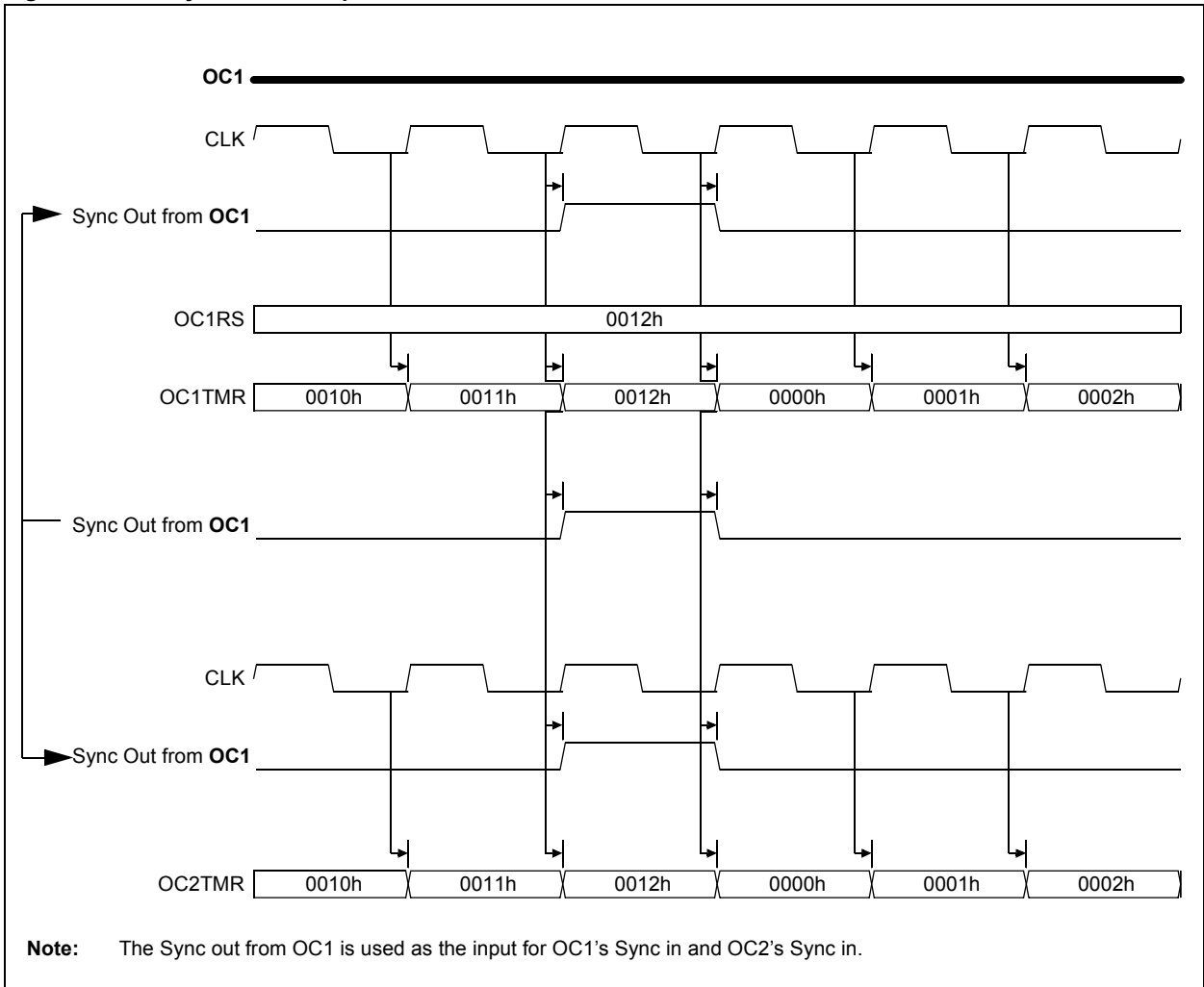


Figure 35-24: Synchronous Operation



When initializing synchronized modules, the module being used as the source of synchronization should be enabled last. As illustrated in Figure 35-23, OC2 should be initialized first and OC1 should be initialized last. This ensures that the timers of all synchronized modules are maintained in a Reset condition until the last module is initialized.

35.3.3.9 TRIGGER OPERATION

Trigger operation of the timer is enabled when OCTRIG (OCxCON2<7>) = 1. When configured for trigger operation, the module timer is held in Reset until a trigger event occurs. After the trigger event occurs, the timer begins to count. The trigger source is selected by the SYNCSEL bits.

35.3.3.10 OCxCON2 TRIGGER FUNCTION

The TRIGSTAT (OCxCON2<6>) bit holds the timer in Reset or releases it to count. It controls the timer in the following manner:

- TRIGSTAT = 0
 - Timer is held in Reset
- TRIGSTAT = 1
 - Timer released from Reset
 - Timer increments on every positive clock

There are two types of trigger conditions when operating in Trigger mode:

- Hardware/software TRIGSTAT bit set
- Software only TRIGSTAT bit set

In both cases, the trigger is always cleared in software.

35.3.3.10.1 Hardware/Software TRIGSTAT Set

The TRIGSTAT (OCxCON2<6>) bit can be set by hardware or software when:

- The SYNCSEL (OCxCON2<4:0>) bits are not equal to 0b00000 (see **Section 35.3.3.12 “Illegal Settings”**)

When the module is enabled for a triggered response, the timer would be held in a cleared state. It remains in this cleared state until a trigger event occurs, which sets the TRIGSTAT bit. Additionally, the timer can be released from Reset by writing to the TRIGSTAT bit and setting it.

35.3.3.10.2 Software Only TRIGSTAT Set

The TRIGSTAT bit can be set only by software when SYNCSEL<4:0> = 0b00000.

35.3.3.11 CLEARING TRIGSTAT BIT

The TRIGSTAT bit can only be cleared in software by writing a '0' to it. When the TRIGSTAT bit is cleared in software, the timer is reset to 0x0000 on the next timer clock's rising edge and is ready for another trigger.

35.3.3.12 ILLEGAL SETTINGS

It is illegal for the module to select itself as a trigger source. Therefore, two possible values of the SYNCSEL<4:0> in Trigger mode are not allowed:

- SYNCSEL<4:0> = 0x1F
- SYNCSEL<4:0> = N, where N is the second setting that selects the same module (see Register 35-2).

<p>Note 1: TRIGSTAT cannot be changed in software when operating in One-Shot mode. See Section 35.3.3.13.2 “One-Shot Functionality” for more information on this mode.</p> <p>2: The trigger source would be synchronized with the OCx clock.</p> <p>3: Preventing these illegal conditions should be taken care of in the user software.</p>

Section 35. Output Compare with Dedicated Timer

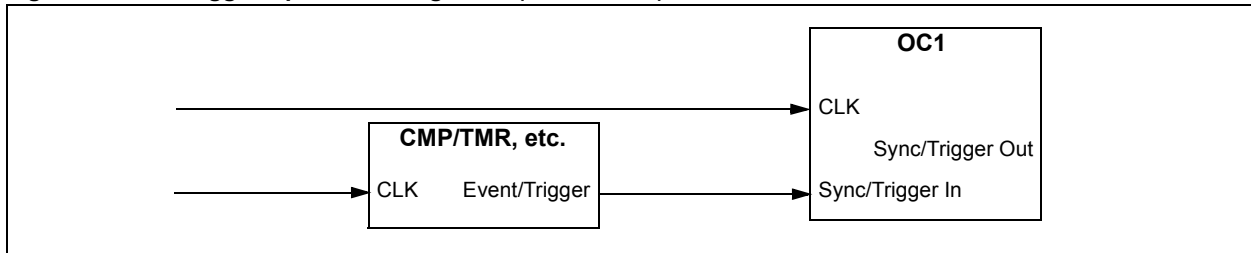
35.3.3.13 USE OF THE OCx MODULE IN A TRIGGERED APPLICATION

Figure 35-25 illustrates a typical application of the module timer in a triggered application. In this application, a trigger event can be generated by another output compare module, timer module, IC module, analog comparator or other peripheral functions. Refer to the product data sheet for a complete list of trigger sources.

35.3.3.13.1 Initialization of the OCx Module in a Triggered Application

The user misses any trigger event that occurs before the OCx module is initialized. Therefore, to avoid missing a trigger, it is recommended that the module be enabled before the trigger source.

Figure 35-25: Trigger Operation Integration (TRIGEN = 1)



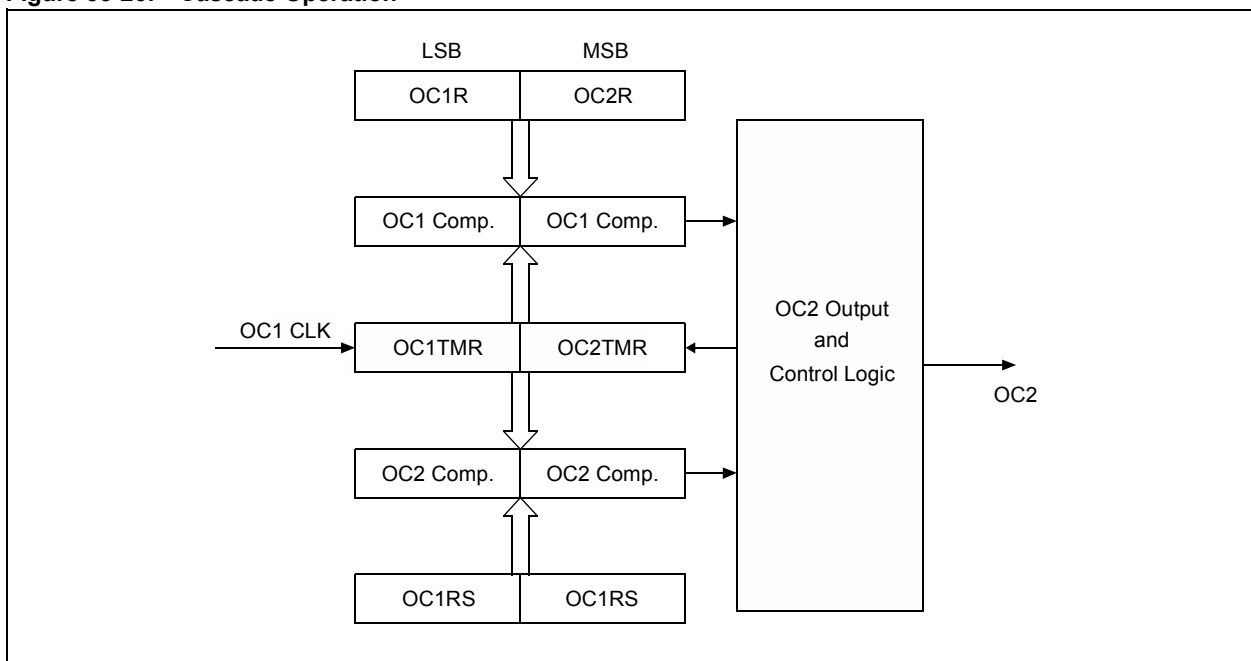
35.3.3.13.2 One-Shot Functionality

While operating as a trigger, the timer can operate in One-Shot mode. This produces one pulse for every trigger. The One-Shot mode is enabled by setting the TRIGMODE (OCxCON1<3>) bit. In One-Shot mode, the timer remains in Reset until a trigger event occurs. This event sets the TRIGSTAT bit and the timer begins to count. When the timer rolls over to 0000h, the TRIGSTAT bit would be cleared by the hardware if TRIGMODE = 1. This holds the timer in Reset until the next trigger event, creating a one-shot timer.

35.3.4 Cascade Mode

When 16-bit timers are not enough, the OCx modules can be grouped in pairs to cascade them into 32-bit timers (see Figure 35-26). They are grouped as odd and even pairs (1-2, 3-4, 5-6, etc.). When cascading, the odd OCx module forms the Least Significant 16 bits of the timer/compare and the even module forms the Most Significant 16 bits. The OCx pin of the even module would be the output of the cascaded timers.

Figure 35-26: Cascade Operation



35.3.5 Setting Up Modules for Cascade

In this section, it is assumed that OC1 is the odd OC module and OC2 is the even.

The odd module is set up as follows:

- OC32 (OC1CON1<8>) = 1
- OCTRIG (OC1CON2<7>) can either be '1' or '0' as the timer can either be synchronized or triggered
- OCTRIS (OC1CON2<5>) = 1 (since the OC1 pin would not be used, the output should be tri-stated)

The even module is set up as follows:

- OC32 (OC2CON1<8>) = 1
- OCTRIG (OC2CON2<7>) = 0 (even timer must be operated in Synchronized mode when cascaded)
- OCTRIS (OC2CON2<5>) = 0 (since OC2 would not be used, the output should be enabled)

35.3.5.1 INITIALIZATION OF THE MODULES IN A CASCADE APPLICATION

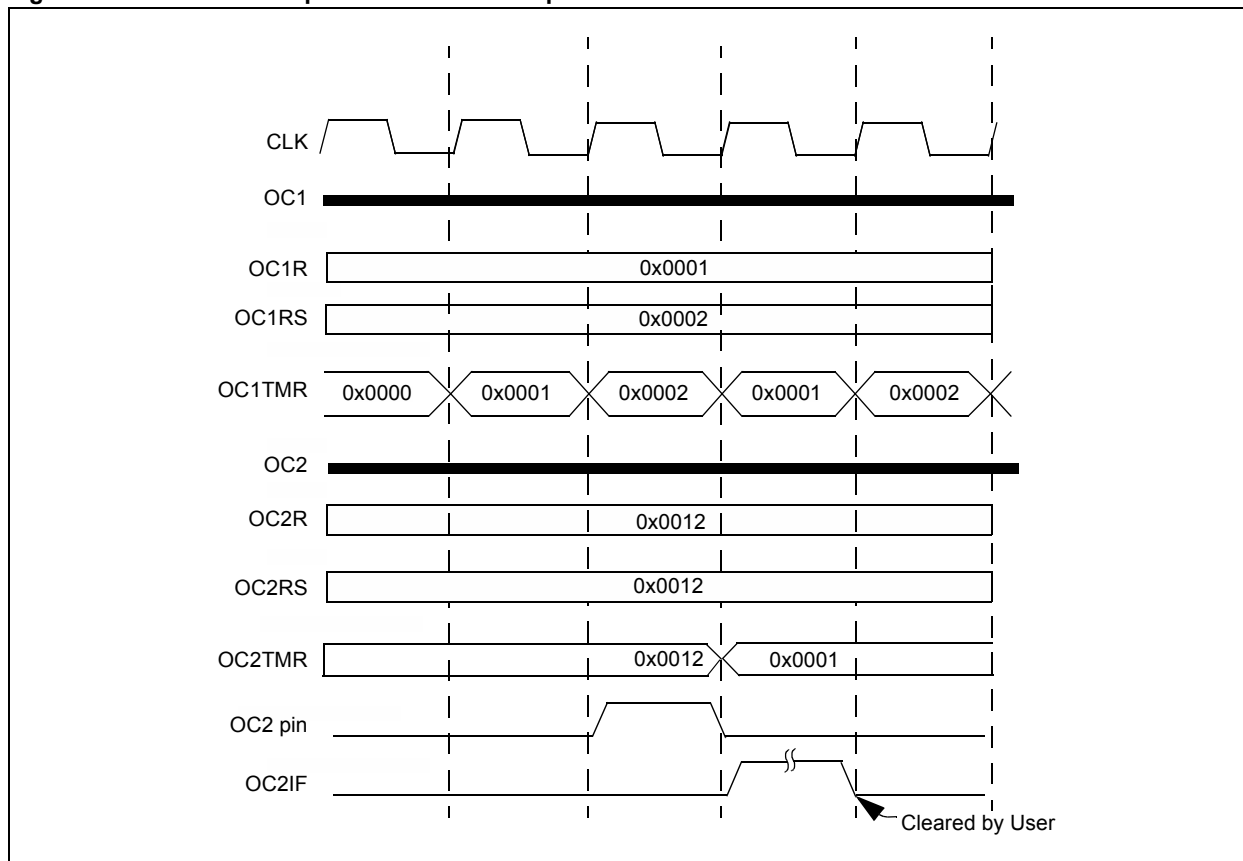
When initializing cascaded modules, the even module should be initialized first and the odd module should be initialized last.

35.3.5.2 TIMER CLOCK SELECTION

This clock should be selected before the module is enabled, and should not be changed during the operation. The waveform for the cascade operation is illustrated in Figure 35-27.

Note: The even and odd OC modules must have the same clock.

Figure 35-27: Cascade Operation in Dual Compare Mode



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35.3.5.3 CASCADE OPERATION WITH THE ODD MODULE TRIGGERED

When two modules are cascaded to form a 32-bit timer, the timer can be triggered by setting the odd module (OCTRIG = 1). The odd module remains in Reset until a trigger event occurs. Once a trigger event occurs, the odd and even modules count as usual.

35.3.5.4 SYNCHRONIZING MULTIPLE CASCADED MODULE PAIRS

Multiple 32-bit pairs can also be synchronized, for example:

- To synchronize the OC3 + OC4 pair with the OC1 + OC2 pair:
 - OC1 and OC2 are set up as defined in **Section 35.3.5 “Setting Up Modules for Cascade”**
 - OC3 and OC4 are set up in the same way, but also SYNCSEL = 1 (synchronization out from OC1); this allows the Sync out from OC1 to hold OC3 in Reset

Example 35-5: Output Compare in Cascade Mode

```
OC1CON1 = 0;          /* It is a good practice to clear off the control bits initially */
OC1CON2 = 0;
OC2CON1 = 0;
OC2CON2 = 0;

OC1CON1bits.OCTSEL = 0x07; /* This selects the peripheral clock as the clock input to the OC
                             module */
OC2CON1bits.OCTSEL = 0x07;

OC1R = 0x1000;        /* Determines the On-Time */
OC2R = 0x0002;        /* Determines the On-Time */

OC1RS = 0x2000;       /* Determines the Period */
OC2RS = 0x0003;       /* Determines the Period */

OC1CON2bits.SYNCSEL = 0x1F;
OC2CON2bits.SYNCSEL = 0x1F;

OC1CON2bits.OCTRIS = 1; /* Odd module's output is not required */

/* Even module must be enabled first */
/* Odd module must be enabled last */

OC2CON2bits.OC32 = 1;
OC1CON2bits.OC32 = 1;

OC2CON1bits.OCM = 6;   /* This selects the Edge Aligned PWM mode */
OC1CON1bits.OCM = 6;
```

35.4 OUTPUT COMPARE OPERATION IN POWER-SAVING STATES

35.4.1 Output Compare Operation in Sleep Mode

When the device enters Sleep mode, the system clock is disabled. During Sleep, the output compare channel drives the pin to the same active state as it was driven prior to entering the Sleep state. The module then Halts at this state.

For example:

If the pin was high and the CPU enters the Sleep state, the pin stays high. Likewise, if the pin was low and the CPU enters the Sleep state, the pin stays low. In both cases, when the device awakes, the output compare module resumes operation.

35.4.2 Sleep with PWM Fault Mode

- When the module is in PWM Fault mode, the asynchronous portions of the Fault circuit remain active.
- If a Fault is detected, the output of OCx is determined by the FLTOUT and the OCTRIS setting of OCxCON2 register.
- The OCFLT0 bit would be set. An interrupt would not be generated at a Fault occurrence. However, the interrupt would be queued and occurs at the time the part wakes up.

35.4.3 Output Compare Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The OCSIDL (OCxCON1<13>) bit selects if the output capture module stops in Idle mode or continues operation in Idle mode.

- If OCSIDL = 1, the module discontinues the operation in Idle mode. The module performs the same procedures when stopped in the Idle mode (OCSIDL = 1) as it does for the Sleep mode.
- If OCSIDL = 0, the output compare channel(s) operate during the CPU Idle mode if the OCSIDL bit is a logic '0'. Furthermore, the time base must be enabled with the respective TSIDL bit set to a logic '0'; if internal, the timer is used as the clock source.

Note: The external Fault pins, if enabled for use, continue to control the associated OCx output pins while the device is in Sleep or Idle mode.

35.4.4 Doze Mode

Output compare operation in Doze mode is the same as in normal mode. When the device enters Doze mode, the system clock sources remain functional and the CPU may run at a slower clock rate.

35.4.5 Selective Peripheral Module Control

The Peripheral Module Disable (PMD) registers provide a method to disable the output compare module by stopping all the clock sources supplied to it. When the module is disabled via the appropriate PMD control bit, it is in minimum power consumption state. The control and status registers associated with the module would also be disabled. Therefore, a write to these registers would have no effect, and the read values would be invalid and return zero.

35.5 I/O PIN CONTROL

When the output compare module is enabled, the I/O pin direction is controlled by the compare module. The compare module returns the I/O pin control back to the appropriate LAT and TRIS control bits when it is disabled. When the Simple PWM with Fault Protection Input mode is enabled, the OCFA/OCFB Fault pins must be configured as an input by setting the respective TRIS bit. Enabling this special PWM mode does not configure the OCFA/OCFB Fault pin as an input.

Note: Refer to the product data sheet for available output compare pins.

35.6 REGISTER MAPS

A summary of the registers associated with the PIC24F Output Compare with Dedicated Timer module is provided in Table 35-7.

Table 35-7: Output Compare with Dedicated Timer Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OCXCON1	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLT0	—	—	OCFLT0	TRIGMODE	OCM2	OCM1	OCM0	0000
OCXCON2	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	0000
OCXRS	Output Compare x Secondary Register																
OCXR	Output Compare x Register																
OCXTMR	Timer Value x Register																

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For details on the Output Compare with Dedicated Timer map, refer to the specific device data sheet.

PIC24F Family Reference Manual

35.7 ELECTRICAL SPECIFICATIONS

35.7.1 AC Characteristics

Figure 35-28: Output Compare Timings

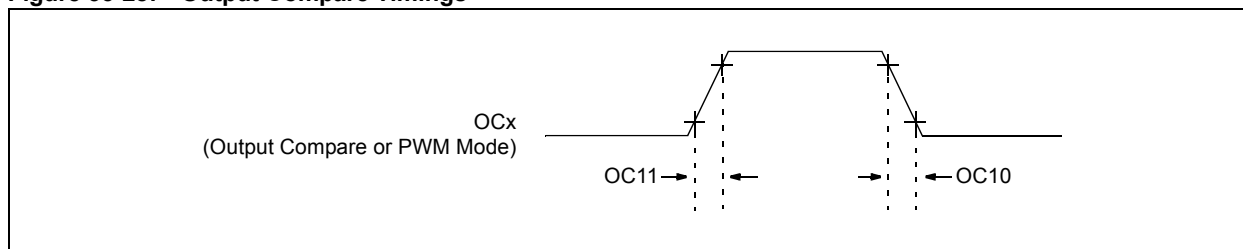


Table 35-8: Output Capture

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
OC11	TccR	OC1 Output Rise Time	—	10	ns	—
			—	—	ns	—
OC10	TccF	OC1 Output Fall Time	—	10	ns	—
			—	—	ns	—

Figure 35-29: PWM Module Timing Requirements

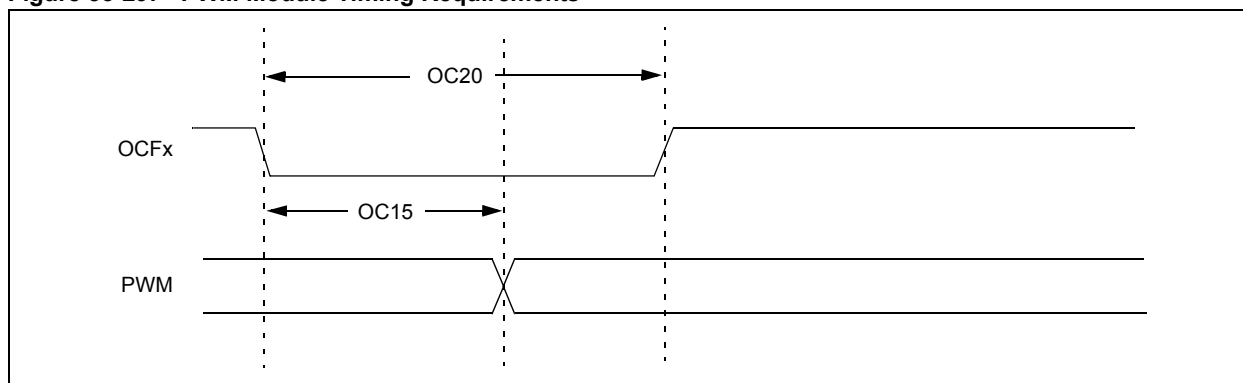


Table 35-9: PWM Timing Requirements

Param. No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	25	ns	V _{DD} = 3.0V, -40°C to +85°C
OC20	TFH	Fault Input Pulse Width	50	—	—	ns	V _{DD} = 3.0V, -40°C to +85°C

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

35.8 DESIGN TIPS

Question 1: *The output compare pin stops functioning even when the OCSIDL bit is not set. Why?*

Answer: This is most likely to occur when the TSIDL (TxCON<13>) bit of the associated timer source is set if it is used as the clock source. Therefore, it is the timer that actually goes into the Idle mode when the `PWRSAV` instruction is executed and the clock is not generated.

Question 2: *Can I cascade OC2 and OC3?*

Answer: No; cascading can be done only in pairs of OC1-OC2, OC3-OC4, etc., and OC9 cannot be paired.

35.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Output Compare with Dedicated Timer module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.
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Section 35. Output Compare with Dedicated Timer

35.10 REVISION HISTORY

Revision A (February 2008)

This is the initial released revision of this document.

NOTES: