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## Section 33. Programming and Diagnostics

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### HIGHLIGHTS

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## 33.1 INTRODUCTION

PIC24F devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire interfaces
- Enhanced debugging capabilities
- Boundary scan testing for device and board diagnostics

PIC24F devices incorporate three different programming and diagnostic modalities that provide a range of useful functions to the application developer. They are summarized in Table 33-1.

**Table 33-1: Comparison of PIC24F Programming and Diagnostic Features**

Feature	Interface	Device Integration	Functions
ICSP™	PGCx and PGDx pins	Integrated with device core	Programming, debugging
Enhanced ICSP (EICSP)		Hardware integrated with device core; firmware-based control	Programming
JTAG	TDI, TDO, TMS and TCK pins	Peripheral to device core, partly integrated with I/O logic	Programming, diagnostics (BST)

## 33.2 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

In-Circuit Serial Programming (ICSP) is Microchip's original solution to providing microcontroller programming in the target application. Originally introduced for 8-bit PIC16 devices, it is used for virtually all Microchip microcontrollers. ICSP is also the most direct method to program the device, whether the controller is embedded in a system or loaded into a device programmer.

### 33.2.1 ICSP Interface

ICSP uses two pins as the core of its interface. The programming data line (PGD) functions as both an input and an output, allowing programming data to be read in and device information to be read out on command. The programming clock line (PGC) is used to clock in data and control the overall process.

Most PIC24F devices have more than one pair of PGC and PGD pins; these are multiplexed with other I/O or peripheral functions. Individual ICSP pin pairs are indicated by number (e.g., PGC1/PGD1, etc.), and are generically referred to as 'PGCx' and 'PGDx'. The multiple PGCx/PGDx pairs provide additional flexibility in system design by allowing users to incorporate ICSP on the pair of pins that is least constrained by the circuit design. All PGCx and PGDx pins are functionally tied together and behave identically, and any one pair can be used for successful device programming. The only limitation is that both pins from the same pair must be used.

In addition to the PGCx and PGDx pins, ICSP requires that all voltage supply and ground pins on the device must be connected, as well as voltage regulator pins (ENVREG or DISVREG). The MCLR pin, which is used with PGCx to enter and control the programming process, must also be connected to the programming device.

### 33.2.2 ICSP Operation

ICSP uses a combination of internal hardware and external control to program the target device. Programming data and instructions are provided on PGD. ICSP uses a special set of 4-bit commands to control the overall process, combined with standard PIC24F instructions to execute the actual writing of the program memory. PGD also returns data to the external programmer when responding to queries.

Control of the programming process is achieved by manipulating PGC and  $\overline{\text{MCLR}}$ . Entry into and exit from Programming mode involves applying (or removing) voltage to MCLR while supplying a code sequence to PGD and a clock to PGC. Any one of the PGCx/PGDx pairs can be used to enter programming. During programming, the clock train on PGC is also used to indicate the difference between 4-bit commands, programming control commands and payload data to be programmed.

The internal process is regulated by a state machine built into the PIC24F core logic; however, overall control of the process must be provided by the external programming device. Microchip programming devices, such as the MPLAB® PM 3 (used with MPLAB IDE software), include the necessary hardware and algorithms to manage the programming process for PIC24F. Users who are interested in a more detailed description, or who are considering designing their own programming interface for PIC24F devices, should consult the appropriate PIC24F device programming specification.

### 33.2.3 ICSP and In-Circuit Debugging

ICSP also provides a hardware channel for the In-Circuit Debugger (ICD) which allows externally controlled debugging of software. Using the appropriate hardware interface and software environment, users can force the device to single-step through its code, track the actual content of multiple registers and set software breakpoints.

To use ICD, an external system that supports ICD must load a debugger executive program into the microcontroller. This is automatically handled by many debugger tools, such as the MPLAB ICD 2. For PIC24F devices, the program is loaded into the executive program memory, located at 800000h through 8007FFh in the configuration memory space. While memory at these addresses is implemented, and code can be executed from these addresses, the executive memory space is not available to the user during normal operating modes.

Because of its location, use of the debugger executive has no impact on the size of the application being examined. The executive memory space allows the entire program memory to be used for program code, without needing to leave reserve space for application debugging. In addition, its use means that the program memory contents in normal and debug states is identical, which helps to simplify troubleshooting.

In contrast with programming, only one of the ICSP ports may be used for ICD. Depending on the particular PIC24F device, there may be two or more ICSP ports that can be selected for this function. The active ICSP debugger port is selected by the ICS Configuration bit(s). For information on specific devices, refer to the appropriate device data sheet.

## 33.3 ENHANCED IN-CIRCUIT SERIAL PROGRAMMING

The Enhanced ICSP protocol is an extension of the original ICSP. It uses the same physical interface as the original, but changes the location and execution of programming control.

ICSP uses a simple state machine to control each step of the programming process; however, that state machine is controlled by an external programmer. In contrast, Enhanced ICSP uses an on-board bootloader, known as the program executive, to manage the programming process. While overall device programming is still overseen by an external programmer, the program executive manages most of the things that must be directly controlled by the programmer in standard ICSP.

The program executive implements its own command set, wider in range than the original ICSP, that can directly erase, program and verify the microcontroller's program memory. This avoids the need to repeatedly run ICSP command sequences to perform simple tasks. As a result, Enhanced ICSP is capable of programming or reprogramming a device more quickly than the original ICSP.

Like the ICD debugger executive, the program executive does not reside in the user program space; it is also loaded into the executive program memory (800000h through 8007FFh). Since the debugger and Enhanced ICSP executives both use this memory space, ICD is not available while Enhanced ICSP is being used.

The program executive is not preprogrammed into PIC24F devices. If Enhanced ICSP is needed, the user must use standard ICSP to program the executive to the executive memory space. This can be done directly by the user, or automatically, using a compatible Microchip programming system.

For additional information on Enhanced ICSP and the program executive, refer to the appropriate PIC24F device programming specification.

## 33.4 JTAG BOUNDARY SCAN

As the complexity and density of board designs increases, testing electrical connections between the components on fully assembled circuit boards poses many challenges. To address these challenges, the Joint Test Action Group (JTAG) developed a method for boundary scan testing that was later standardized as IEEE 1149.1-2001, "IEEE Standard Test Access Port and Boundary Scan Architecture". Since its adoption, many microcontroller manufacturers have added device programming to the capabilities of the test port.

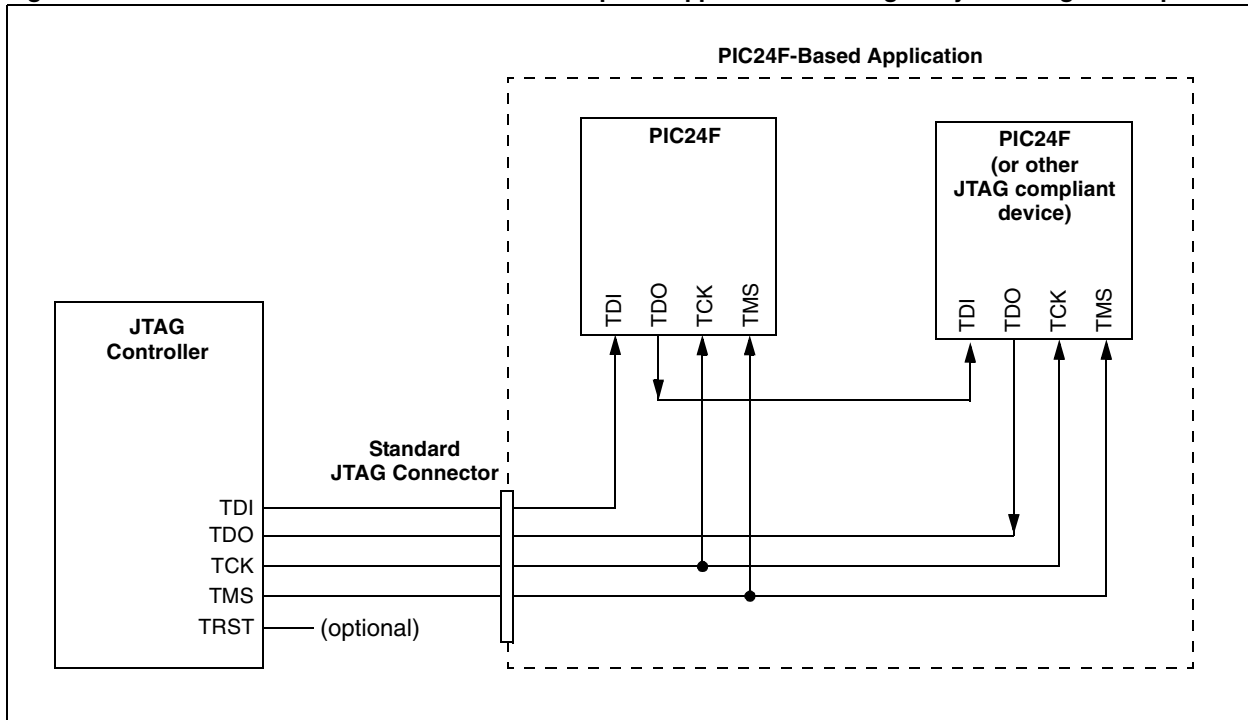
The JTAG boundary scan method is the process of adding a Shift register stage adjacent to each of the component's I/O pins. This permits signals at the component boundaries to be controlled and observed, using a defined set of scan test principles. An external tester or controller provides instructions and reads the results in a serial fashion. The external device also provides common clock and control signals. Depending on the implementation, access to all test signals is provided through a standardized 4-pin or 5-pin interface.

In system-level applications, individual JTAG enabled components are connected through their individual testing interfaces (in addition to their more standard application-specific connections). Devices are connected in a series or daisy-chained fashion, with the test output of one device connected exclusively to the test input of the next device in the chain. Instructions in the JTAG boundary scan protocol allow the testing of any one device in the chain, or any combination of devices, without testing the entire chain. In this method, connections between components, as well as connections at the boundary of the application, may be tested.

A typical application incorporating the JTAG boundary scan interface is shown in Figure 33-1. In this example, a PIC24F microcontroller is daisy-chained to a second JTAG compliant device. Note that the TDI line from the external tester supplies data to the TDI pin of the first device in the chain (in this case, the microcontroller). The resulting test data for this two-device chain is provided from the TDO pin of the second device to the TDO line of the tester.

This section describes the JTAG module and its general use. Users interested in using the JTAG interface for device programming should refer to the appropriate PIC24F device programming specification for more information.

**Figure 33-1: Overview of PIC24F-Based JTAG Compliant Application Showing Daisy-Chaining of Components**

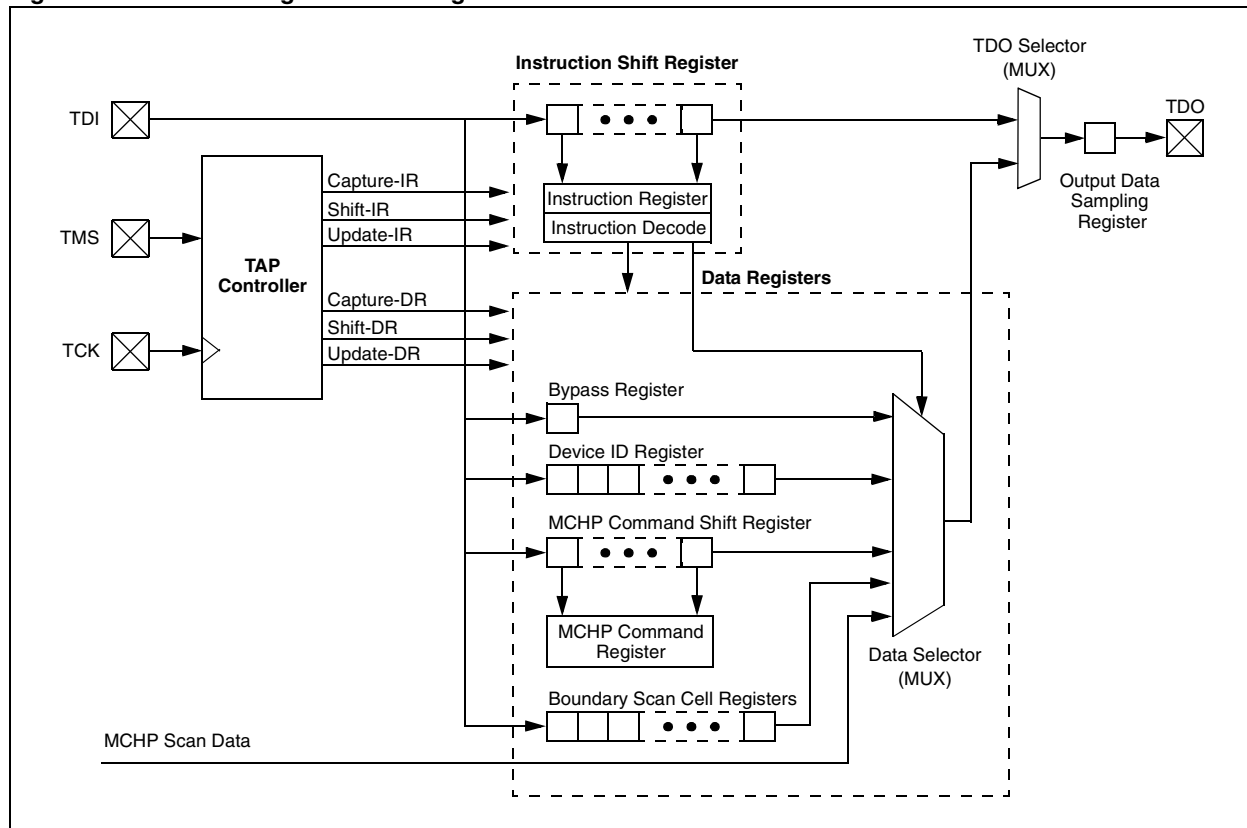


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In PIC24F family devices, the hardware for the JTAG boundary scan is implemented as a peripheral module (i.e., outside of the CPU core) with additional integrated logic in all I/O ports. A logical block diagram of the JTAG module is shown in Figure 33-2. It consists of the following key elements:

- TAP Interface Pins (TDI, TMS, TCK and TDO)
- TAP Controller
- Instruction Shift register and Instruction Register (IR)
- Data Registers

Figure 33-2: JTAG Logical Block Diagram



### 33.4.1 Test Access Port (TAP) and TAP Controller

The Test Access Port (TAP) on the PIC24F device family is a general purpose port that provides test access to many built-in support functions and test logic defined in IEEE Standard 1149.1. The TAP is disabled by programming the JTAGEN bit in Configuration Word 1 (the TAP, by default, is enabled in the bit's unprogrammed state). While enabled, the designated I/O pins become dedicated TAP pins. See the appropriate PIC24F device data sheet for details about disabling/enabling the JTAG module and identifying JTAG control pins.

The PIC24F family implements a 4-pin JTAG interface with these pins:

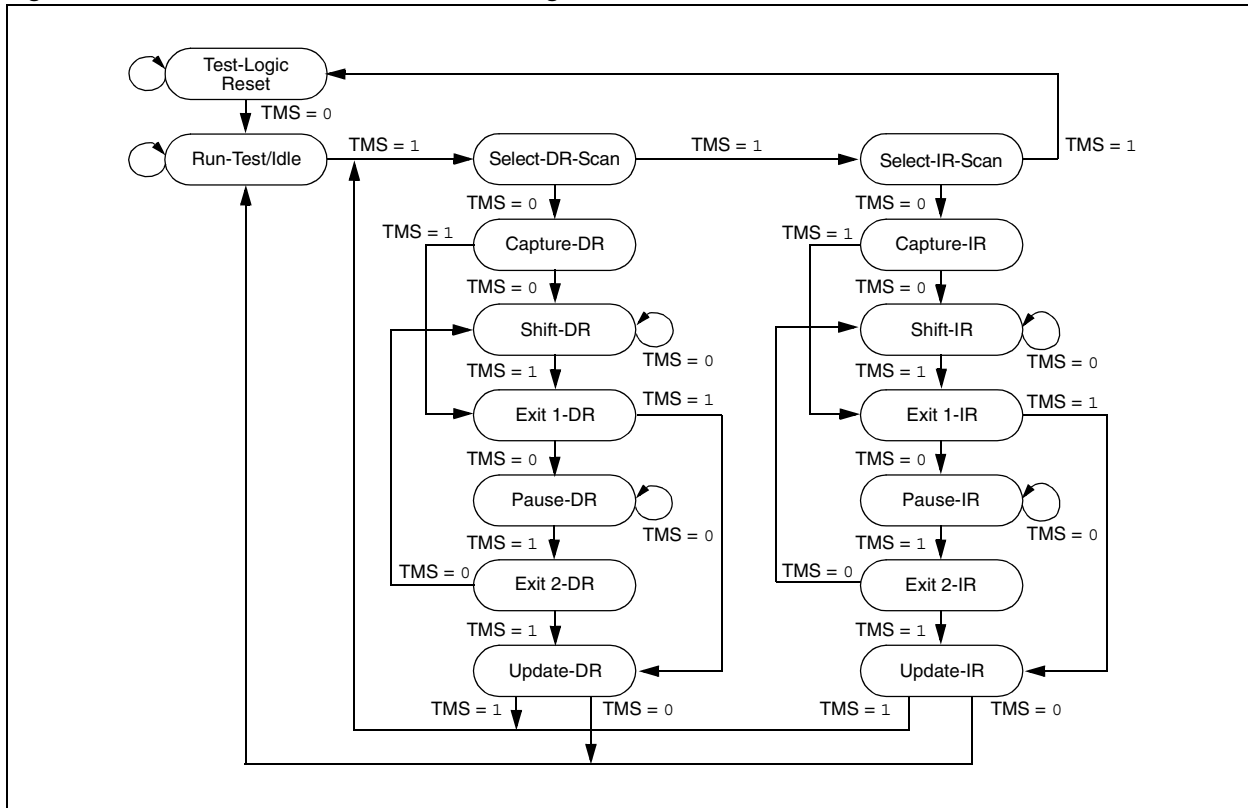
- TCK (Test Clock Input): Provides the clock for test logic.
- TMS (Test Mode Select Input): Used by the TAP to control test operations.
- TDI (Test Data Input): Serial input for test instructions and data.
- TDO (Test Data Output): Serial output for test instructions and data.

To minimize I/O loss due to JTAG, the optional TAP Reset ( $\overline{\text{TRST}}$ ) input pin, specified in the standard, is not implemented on PIC24F devices. For convenience, a “soft” TAP Reset has been included in the TAP controller, using the TMS and TCK pins. To force a port Reset, apply a logic high to the TMS pin for at least 5 rising edges of TCK. Note that device Resets (including POR) do not automatically result in a TAP Reset; this must be done by the external JTAG controller using the soft TAP Reset.

# PIC24F Family Reference Manual

The TAP controller on the PIC24F family devices is a synchronous finite state machine that implements the standard 16 states for JTAG. Figure 33-3 shows all the module states of the TAP controller. All Boundary Scan Test (BST) instructions and test results are communicated through the TAP via the TDI pin in a serial format, Least Significant bit first.

**Figure 33-3: TAP Controller Module State Diagram**



By manipulating the state of TMS and the clock pulses on TCK, the TAP controller can be moved through all of the defined module states to capture, shift and update various instruction and/or data registers. Figure 33-3 shows the state changes on TMS as the controller cycles through its state machine. Figure 33-4 shows the timing of TMS and TCK while transitioning the controller through the appropriate module states for shifting in an instruction. In this example, the sequence shown demonstrates how an instruction is read by the TAP controller.

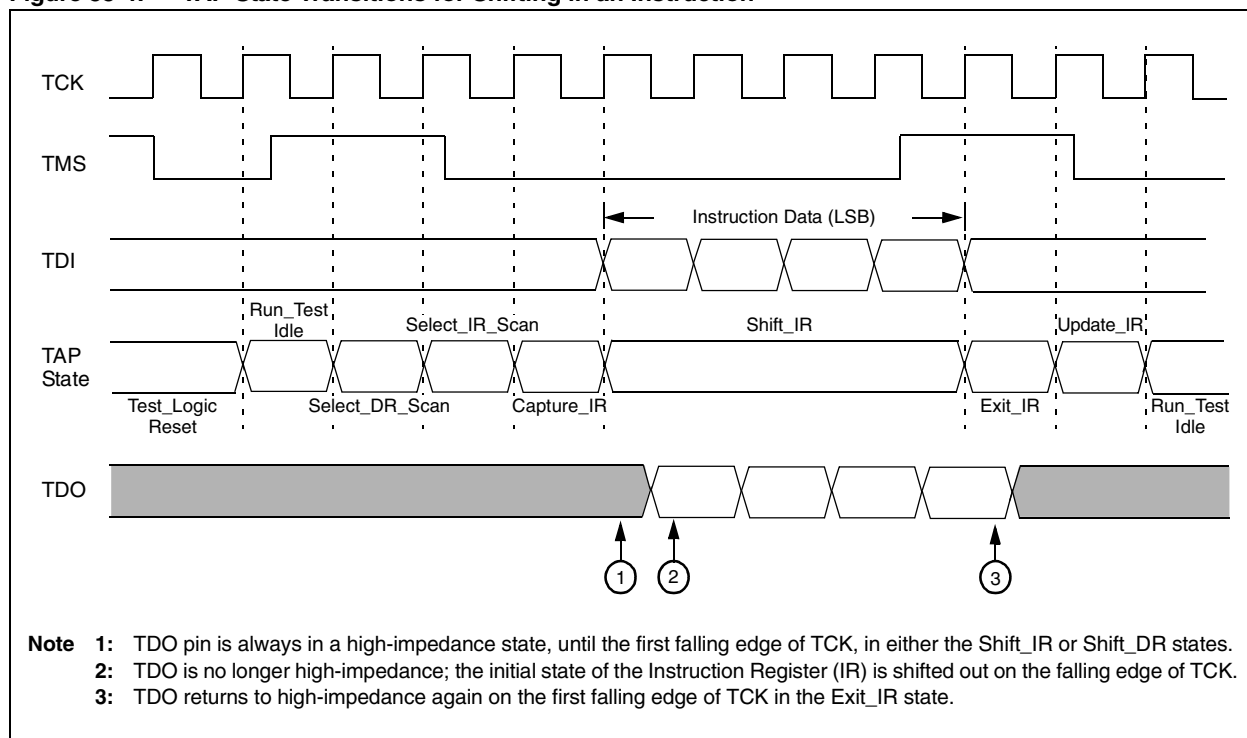
All TAP controller states are entered on the rising edge of the TCK pin. In this example, the TAP controller starts in the Test-Logic Reset state. Since the state of the TAP controller is dependent on the previous instruction, and therefore could be unknown, it is good programming practice to begin in the Test-Logic Reset state.

When TMS is asserted low on the next rising edge of TCK, the TAP controller will move into the Run-Test/Idle state. On the next two rising edges of TCK, TMS is high; this moves the TAP controller to the Select-IR-Scan state.

On the next two rising edges of TCK, TMS is held low; this moves the TAP controller into the Shift-IR state. An instruction is shifted in to the Instruction Shift register via the TDI on the next four rising edges of TCK. After the TAP controller enters this state, the TDO pin goes from a high-impedance state to active. The controller shifts out the initial state of the Instruction Register (IR) on the TDO pin, on the falling edges of TCK, and continues to shift out the contents of the Instruction Register while in the Shift-IR state. The TDO returns to the high-impedance state on the first falling edge of TCK upon exiting the shift state.

On the next three rising edges of TCK, the TAP controller exits the Shift-IR state, updates the Instruction Register and then moves back to the Run-Test/Idle state. Data, or another instruction, can now be shifted in to the appropriate Data or Instruction Register.

**Figure 33-4: TAP State Transitions for Shifting in an Instruction**



## 33.4.2 JTAG Registers

The JTAG module uses a number of registers of various sizes as part of its operation. In terms of bit count, most of the JTAG registers are single-bit register cells, integrated into the I/O ports. Regardless of their location within the module, none of the JTAG registers are located within the device data memory space, and cannot be directly accessed by the user in normal operating modes.

### 33.4.2.1 INSTRUCTION SHIFT REGISTER AND INSTRUCTION REGISTER

The Instruction Shift register is a 4-bit shift register used for selecting the actions to be performed and/or what data registers to be accessed. Instructions are shifted in, Least Significant bit first, and then decoded.

A list and description of implemented instructions is given in **Section 33.4.4 “JTAG Instructions”**.

### 33.4.2.2 DATA REGISTERS

Once an instruction is shifted in and updated into the Instruction Register, the TAP controller places certain data registers between the TDI and TDO pins. Additional data values can then be shifted into these data registers as needed.

The PIC24F device family supports three data registers:

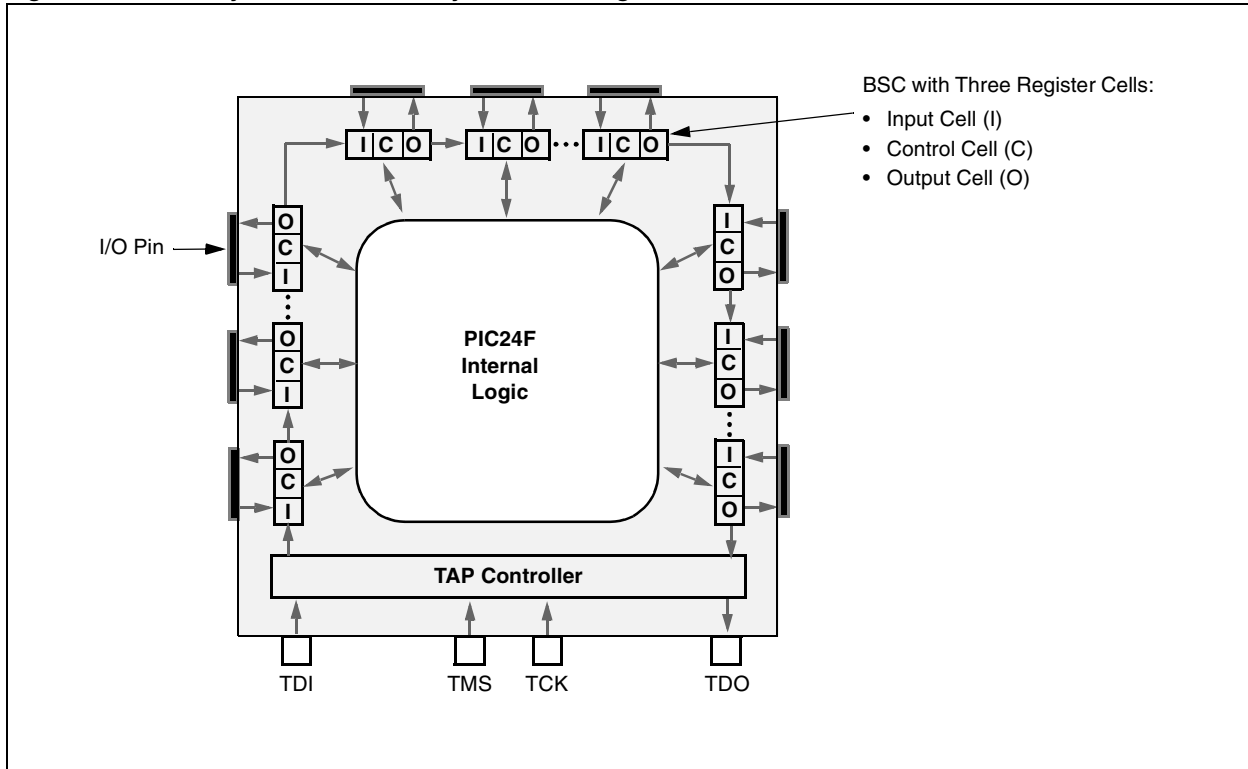
- **BYPASS Register:** A single-bit register which allows the boundary scan test data to pass through the selected device to adjacent devices. The BYPASS register is placed between the TDI and TDO pins when the BYPASS instruction is active.
- **Device ID Register:** A 32-bit part identifier. It consists of an 11-bit manufacturer ID assigned by the IEEE (29h for Microchip Technology), device part number and device revision identifier. When the IDCODE instruction is active, the Device ID register is placed between the TDI and TDO pins. The device data ID is then shifted out on to the TDO pin, on the next 32 falling edges of TCK, after the TAP controller is in the Shift-DR.
- **MCHP Command Shift Register:** An 8-bit shift register that is placed between the TDI and TDO pins when the MCHP\_CMD instruction is active. This shift register is used to shift in Microchip commands.

## 33.4.3 Boundary Scan Register (BSR)

The BSR is a large shift register that is comprised of all the I/O Boundary Scan Cells (BSCs), daisy-chained together (Figure 33-5). Each I/O pin has one BSC, each containing 3 BSC registers: an input cell, an output cell and a control cell. When the `SAMPLE/PRELOAD` or `EXTEST` instructions are active, the BSR is placed between the TDI and TDO pins, with the TDI pin as the input and the TDO pin as the output.

The size of the BSR depends on the number of I/O pins on the device. For example, the PIC24FJ128GA010 has 82 I/O pins. With 3 BSC registers for each of the 82 I/Os, this yields a Boundary Scan register length of 246 bits. Information on the I/O port pin count of other PIC24F devices can be found in their specific device data sheets.

**Figure 33-5: Daisy-Chained Boundary Scan Cell Registers on a PIC24F Microcontroller**



### 33.4.3.1 BOUNDARY SCAN CELL (BSC)

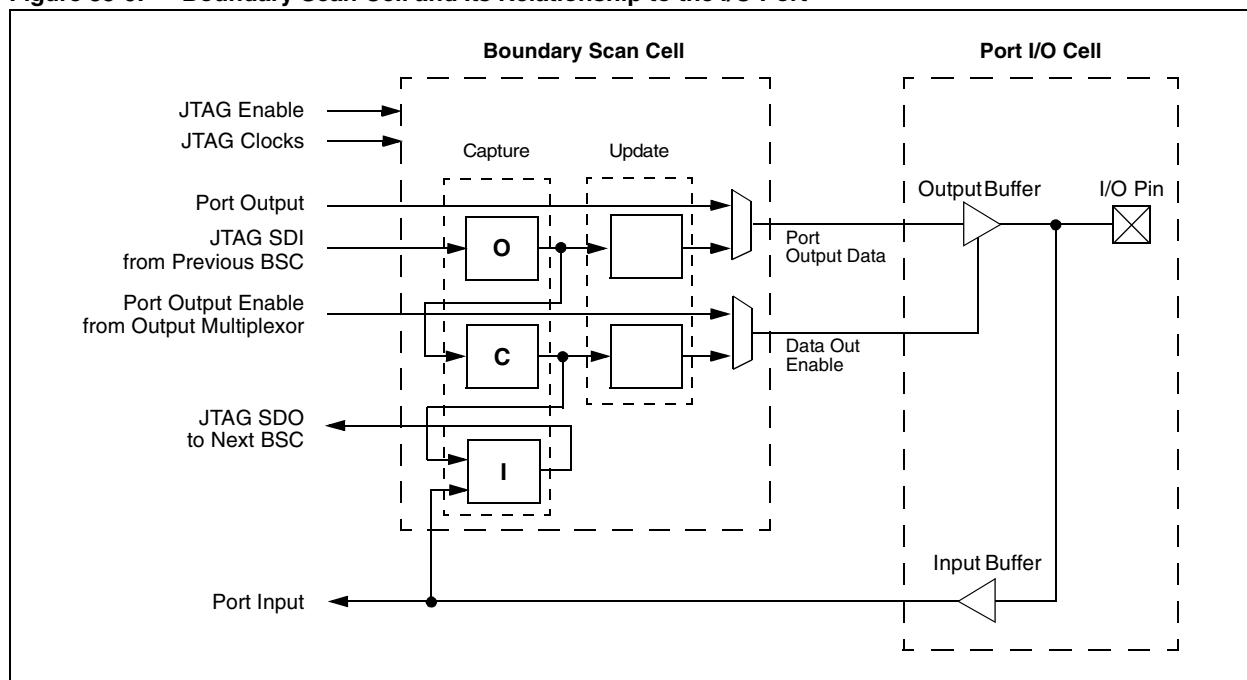
The function of the BSC is to capture and override I/O input or output data values when JTAG is active. The BSC consists of three Single-Bit Capture register cells and two Single-Bit Holding register cells. The capture cells are daisy-chained to capture the port's input, output and control (output-enable) data, as well as pass JTAG data along the Boundary Scan register. Command signals from the TAP controller determine if the port of JTAG data is captured, and how and when it is clocked out of the BSC.

The first register either captures internal data destined to the output driver, or provides serially scanned in data for the output driver. The second register captures internal output-enable control from the output driver and also provides serially scanned in output-enable values. The third register captures the input data from the I/O's input buffer.



Figure 33-6 shows a typical BSC and its relationship to the I/O port's structure.

**Figure 33-6: Boundary Scan Cell and Its Relationship to the I/O Port**



## 33.4.4 JTAG Instructions

PIC24F family devices support the mandatory instruction set specified by IEEE 1149.1, as well as several optional public instructions defined in the specification. These devices also implement instructions that are specific to Microchip devices.

The mandatory JTAG instructions are:

- **BYPASS (0Fh)**: Used for bypassing a device in a test chain; this allows the testing of off-chip circuitry and board-level interconnections.
- **SAMPLE/PRELOAD (01h)**: Captures the I/O states of the component, providing a snapshot of its operation.
- **EXTEST (03h)**: Allows the external circuitry and interconnections to be tested, by either forcing various test patterns on the output pins, or capturing test results from the input pins.

The optional JTAG instructions implemented in PIC24F devices are:

- **IDCODE (02h)**: Causes the 32-bit device identification word to be shifted out on the TDO pin.
- **HIGHZ (04h)**: Places the device into a state in which all I/O pins are in a high-impedance state (driven inactive).

The manufacturer-specific JTAG commands used for JTAG device programming are:

- **MCHP\_SCAN (07h)**: Places the device in and manages various JTAG modes.
- **MCHP\_CMD (08h)**: Alerts the TAP controller that a programming instruction specific to Microchip follows. The data following **MCHP\_CMD** is placed in the MCHP Command Shift register and parsed as an instruction.

There are currently two instructions implemented for use with **MCHP\_CMD**:

- **JTAG\_MCLR (01h)**: Performs a device Master Clear Reset while the JTAG interface is active; functionally equivalent to a hardware **MCLR**. The TAP interface itself is not reset.
- **JTAG\_MUX (02h)**: Switches the JTAG interface to ICSP operation. After this command, TDI and TDO assume the PGD functions (split input and output, respectively), and TCK functions as PGC.

## 33.4.5 Boundary Scan Testing (BST)

Boundary Scan Testing (BST) is the method of controlling and observing the boundary pins of the JTAG compliant device, like those of the PIC24F family, utilizing software control. BST can be used to test connectivity between devices by daisy-chaining JTAG compliant devices to form a single scan chain. Several scan chains can exist on a PCB to form multiple scan chains. These multiple scan chains can then be driven simultaneously to test many components in parallel. Scan chains can contain both JTAG compliant devices and non-JTAG compliant devices.

A key advantage of BST is that it can be implemented without physical test probes; all that is needed is a 4-wire or 5-wire interface and an appropriate test platform. Since JTAG boundary scan has been available for many years, many software tools exist for testing scan chains without the need for extensive physical probing. The main drawback to BST is that it can only evaluate digital signals and circuit continuity; it cannot measure input or output voltage levels or currents.

### 33.4.5.1 RELATED JTAG FILES

To implement BST, all JTAG test tools will require a Boundary Scan Description Language (BSDL) file. BSDL is a subset of VHDL (VHSIC Hardware Description Language), and is described as part of IEEE Std. 1149.1. The device-specific BSDL file describes how the standard is implemented on a particular device and how it operates.

The BSDL file for a particular device includes the following:

- The pinout and package configuration for the particular device
- The physical location of the TAP pins
- The Device ID register and the device ID
- The length of the Instruction Register
- The supported BST instructions and their binary codes
- The length and structure of the Boundary Scan register
- The boundary scan cell definition

Device-specific BSDL files are available at Microchip's web site, [www.microchip.com](http://www.microchip.com). The name for each BSDL file is the device name and silicon revision. For example, `PIC24FJ128GA010_A2.BSD`, is the BSDL file for the PIC24FJ128GA010, silicon revision A2.

## 33.4.6 JTAG Device Programming

The JTAG interface can also be used to program PIC24F family devices in their target applications. Using the JTAG interface allows application designers to include a dedicated test and programming port into their applications, with a single 4-pin interface, without imposing the circuit constraints that the ICSP interface may require.

JTAG device programming actually uses the standard ICSP method over the four pins of the TAP interface. When triggered by the appropriate JTAG command sequence, the TDI, TDO and TCK pins assume the functions of the PGD and PGC pins. Aside from this pin remapping, ICSP programming over the JTAG interface behaves exactly as it does over the standard ICSP interface.

Because of the added time overhead for switching the TAP interface, JTAG device programming takes slightly longer than standard ICSP programming over the PGC and PGD pins. Enhanced ICSP programming is not available with JTAG programming.

### 33.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the programming and diagnostics are:

Title	Application Note #
No related application notes at this time.	

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC24F family of devices.

## 33.6 REVISION HISTORY

### Revision A (December 2006)

This is the initial released revision of this document.