
Section 3. Data Memory

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3.1 INTRODUCTION

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and busses. The PIC24F architecture also allows the direct access of program memory from the data space during code execution.

3.2 DATA MEMORY ORGANIZATION

3.2.1 Data Address Space

The PIC24F core has a 16-bit wide data memory space, addressable as a single linear range. The data space is accessed using two Address Generation Units (AGUs), one each for read and write operations. The data space memory map is shown in Figure 3-1.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This gives a data space address range of 64 Kbytes or 32K words. The lower 32 Kbytes of the data memory space (that is, when $EA_{\langle 15 \rangle} = 0$) is used for implemented memory addresses, while the upper half ($EA_{\langle 15 \rangle} = 1$) is reserved for the Program Space Visibility (PSV) area. For details on PSV, refer to **Section 4.4 “Program Space Visibility from Data Space”**.

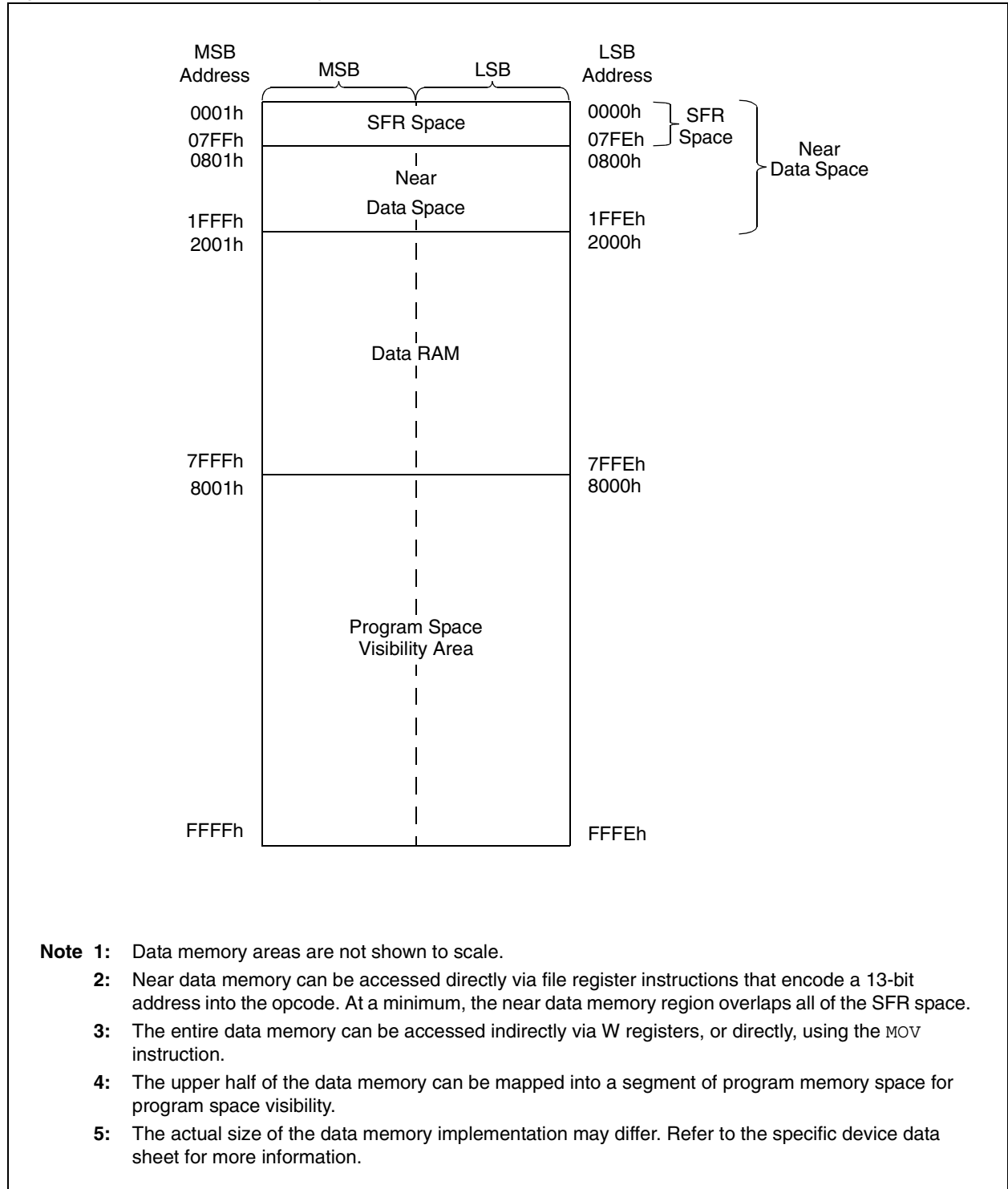
Note 1: Please refer to the specific device data sheet for actual implementation of data memory in a specific device.

2: Should an EA point to a location outside of the physically implemented data memory area in a device, an all zero word or byte will be returned.

3.2.2 Data Space Width

The data memory space is organized in byte addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all the data space EAs resolve to bytes. The Least Significant Bytes of each word have even addresses, while the Most Significant Bytes have odd addresses.

Figure 3-1: Data Space Memory Map for PIC24F Devices



3.2.3 Near Data Memory

An 8-Kbyte address space, between 0x0000 and 0x1FFF, is referred to as near data memory. Near data memory is directly addressable via a 13-bit absolute address field within all the file register instructions.

Near data memory is also addressable by all the Indirect Addressing modes, where the data memory address can be pointed to by any of the 16-bit working registers. Data memory region beyond 0x1FFF is addressable only by the Indirect Addressing modes.

The memory regions included in the near data region will depend on the amount of data memory implemented for each PIC24F family device variant. At a minimum, the near data region will include all of the SFRs. Refer to Figure 3-1 for more details.

3.2.4 SFR Space

The first 2 Kbytes of the near data space, from 0000h to 07FFh, are primarily occupied with Special Function Registers (SFRs). These are used by the PIC24F core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A diagram of the SFR space that describes where SFRs are actually implemented is shown in Table 3-1. Each implemented area indicates a 32-byte region where at least one address is implemented as an SFR.

Table 3-1: Implemented Regions of SFR Data Space⁽¹⁾

SFR Space Address								
	xx00	xx20	xx40	xx60	xx80	xxA0	xxC0	xxE0
000h	Core			ICN	Interrupts			—
100h	Timers		Capture	—	Compare	—	—	—
200h	I ² C™	UART	SPI		—	—	I/O	
300h	A/D		—	—	—	—	—	—
400h	—	—	—	—	—	—	—	—
500h	—	—	—	—	—	—	—	—
600h	PMP	RTC/Comp	CRC	—	—	—	I/O	
700h	—	—	System	NVM/PMD	—	—	—	—

Legend: — = No implemented SFRs in this block

Note 1: Refer to the specific device data sheet for actual register implementation.

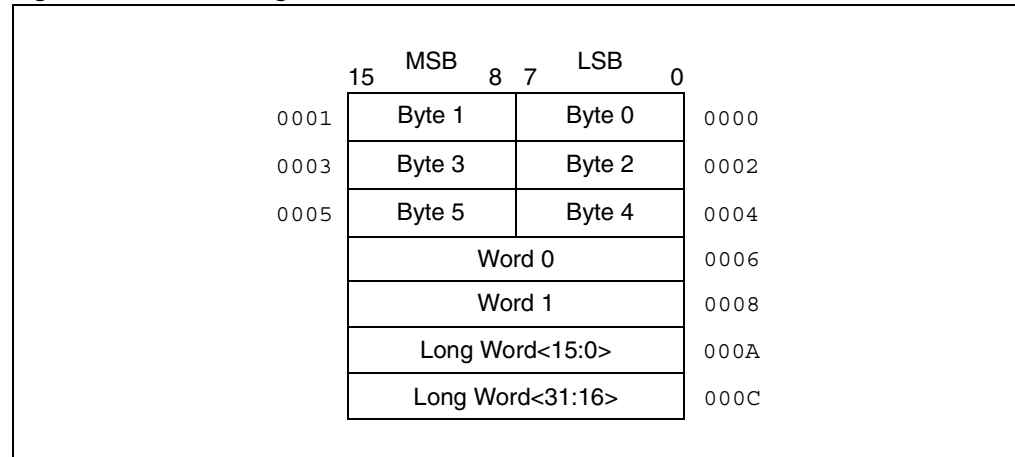
3.3 DATA ALIGNMENT

To maintain backward compatibility with PIC® devices and to improve the data space memory usage efficiency, the PIC24F instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory.

The LSb of a 16-bit data address is ignored during word operations. Word data is aligned in the little-endian format with the Least Significant Byte (LSB) at the even address (LSb = 0) and the Most Significant Byte (MSB) at the odd address (LSb = 1).

For byte operations, the LSb of the data address is used to select the byte that is accessed. Figure 3-2 shows the data alignment for word and byte operations.

Figure 3-2: Data Alignment



Data byte reads will read the complete word, which contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

All effective address calculations are automatically adjusted depending on whether a byte or a word access is performed. For example, an address will be incremented by 2 for a word operation that post-increments the Address Pointer. Similarly, the address will be incremented by 1 for a byte operation that post-increments the Address Pointer.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap will be generated. If the error occurred on a read, the instruction underway is completed; if it occurred on a write, the instruction will be executed but the write will not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address Fault. For additional details regarding the interrupts, refer to **Section 8. “Interrupts”**.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (SE) is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 8-bit unsigned data, users can clear the MSB of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions operate only on words.

3.4 SOFTWARE STACK

For stack operations, some portion of the data memory of the PIC24F devices needs to be allocated as stack. For additional details on software stack, refer to **Section 2.3 “Software Stack Pointer”**.

3.5 INTERFACING PROGRAM AND DATA MEMORY SPACES

The PIC24F architecture uses a 24-bit wide program space and 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the program space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the PIC24F architecture provides two methods by which program space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the program space
- Remapping a portion of the program space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This makes the method ideal for accessing data tables that need to be updated from time to time. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. It can only access the least significant word of the program memory.

For additional details regarding the program and data memory interface, please refer to **Section 4.3 “Data Access from Program Memory”**.

3.6 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Data Memory are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

3.7 REVISION HISTORY

Revision A (January 2007)

This is the initial released revision of this document.