



Section 29. Real-Time Clock and Calendar (RTCC)

HIGHLIGHTS

This section of the manual contains the following major topics:

29.1	Introduction	29-2
29.2	RTCC Module Registers	29-3
29.3	Operation	29-11
29.4	Alarm.....	29-17
29.5	Sleep Mode.....	29-19
29.6	Reset.....	29-19
29.7	Peripheral Module Disable (PMD) Register	29-19
29.8	Register Maps.....	29-20
29.9	Related Application Notes.....	29-21
29.10	Revision History	29-22

PIC24F Family Reference Manual

29.1 INTRODUCTION

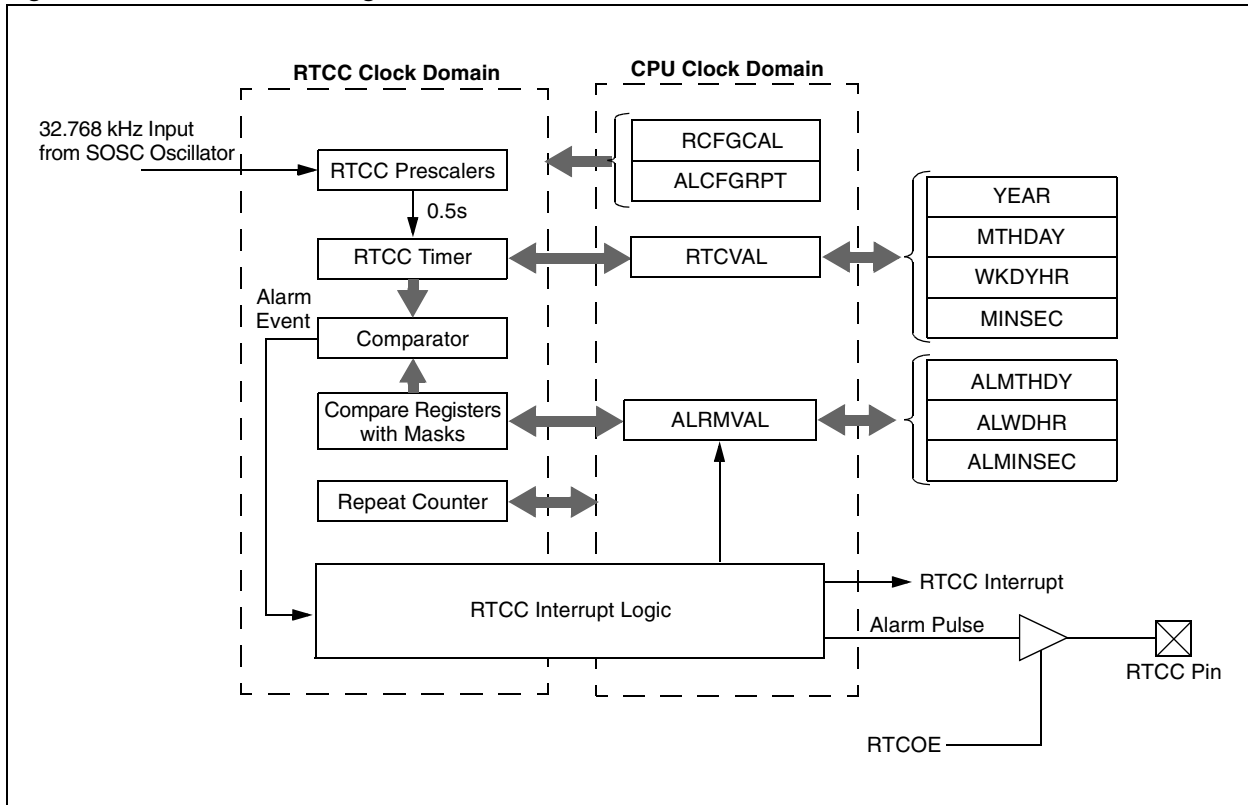
This section discusses the Real-Time Clock and Calendar hardware module, available on PIC24F devices, and its operation. Listed below are some of the key features of this module:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (Military Time)
- Calendar: Weekday, Date, Month and Year
- Alarm Configurable
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- User Calibration with Auto-Adjust
- Calibration Range: ± 2.64 Seconds Error per Month
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC pin

This module provides a Real-Time Clock and Calendar (RTCC) function. The module is intended for applications where accurate time must be maintained for extended periods of time with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099. The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

Figure 29-1: RTCC Block Diagram



29.2 RTCC MODULE REGISTERS

This section discusses the RTCC module registers which are organized into the following three categories:

RTCC Control Registers

- RCFGAL
- PADCFG1
- ALCFGRPT

RTCC Value Registers

- RTCVAL (the following four registers are addressed through the RTCVAL register)
 - YEAR
 - MTHDY
 - WKDYHR
 - MINSEC

Alarm Value Registers

- ALRMVAL (the following three registers are addressed through the ALRMVAL register)
 - ALMTHDY
 - ALWDHR
 - ALMINSEC

Note: For reference purposes, the upper half of the RTCVAL register will be referred to as RTCVAL<15:8> and the lower half as RTCVAL<7:0>. The same applies to ALRMVAL, where the upper half is ALRMVALH and the lower half is ALRMVALL.

PIC24F Family Reference Manual

29.2.1 RTCC Control Registers

Register 29-1: RCFGCAL: RTCC Calibration and Configuration Register⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
 1 = RTCC module is enabled
 0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
 1 = RTCVAL<15:8> and RTCVAL<7:0> registers can be written to by the user
 0 = RTCVAL<15:8> and RTCVAL<7:0> registers are locked out from being written to by the user
- bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
 1 = RTCVAL<15:8>, RTCVAL<7:0> and ALCFGRPT registers can change while reading due to a rollover ripple resulting in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
 0 = RTCVAL<15:8>, RTCVAL<7:0> or ALCFGRPT registers can be read without concern over a rollover ripple
- bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾
 1 = Second half period of a second
 0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
 1 = RTCC clock output enabled
 0 = RTCC clock output disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Window Pointer bits
 Points to the corresponding RTCC Value registers when reading RTCVAL<15:8> and RTCVAL<7:0> registers; the RTCPTR<1:0> value decrements on every read or write of RTCVAL<15:8> until it reaches '00'.
 RTCVAL<15:8>:
 00 = MINUTES
 01 = WEEKDAY
 10 = MONTH
 11 = Reserved
 RTCVAL<7:0>:
 00 = SECONDS
 01 = HOURS
 10 = DAY
 11 = YEAR

- Note 1:** The RCFGCAL register is only affected by a POR.
Note 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
Note 3: This bit is read-only. It is cleared to '0' on a write to the lower half of the MINSEC register.

Section 29. Real-Time Clock and Calendar (RTCC)

Register 29-1: RCFGAL: RTCC Calibration and Configuration Register⁽¹⁾ (Continued)

bit 7-0 **CAL<7:0>**: RTC Drift Calibration bits
 01111111 = Maximum positive adjustment; adds 508 RTC clock pulses every one minute
 ...
 00000001 = Minimum positive adjustment; adds 4 RTC clock pulses every one minute
 00000000 = No adjustment
 11111111 = Minimum negative adjustment; subtracts 4 RTC clock pulses every one minute
 ...
 10000000 = Maximum negative adjustment; subtracts 512 RTC clock pulses every one minute

- Note 1:** The RCFGAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only. It is cleared to '0' on a write to the lower half of the MINSEC register.

Register 29-2: PADCFG1: Pad Configuration Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL ⁽¹⁾	PMP TTL
bit 7						bit 0	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'
 bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit⁽¹⁾
 1 = RTCC seconds clock is selected for the RTCC pin
 0 = RTCC alarm pulse is selected for the RTCC pin
 bit 0 **PMP TTL:** PMP Module TTL Input Buffer Select bit
 1 = PMP module uses TTL input buffers
 0 = PMP module uses Schmitt input buffers

- Note 1:** To enable the actual RTCC output, the RTCOE (RCFGAL<10>) bit must be set.

PIC24F Family Reference Manual

Register 29-3: ALCFGRPT: Alarm Configuration Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit
 1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 00 and CHIME = 0)
 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit
 1 = Chime is enabled; ARPT<7:0> is allowed to roll over from 00h to FFh
 0 = Chime is disabled; ARPT<7:0> stops once it reaches 00h

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits
 0000 = Every half second
 0001 = Every second
 0010 = Every 10 seconds
 0011 = Every minute
 0100 = Every 10 minutes
 0101 = Every hour
 0110 = Once a day
 0111 = Once a week
 1000 = Once a month
 1001 = Once a year (except when configured for February 29th, once every 4 years)
 101x = Reserved – do not use
 11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits
 Points to the corresponding Alarm Value registers when reading ALRMVALH and ALRMVALL registers; the ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches '00'.

ALRMVAL<15:8>:
 00 = ALRMMIN
 01 = ALRMWD
 10 = ALRMMNTH
 11 = Unimplemented

ALRMVAL<7:0>:
 00 = ALRMSEC
 01 = ALRMHR
 10 = ALRMDAY
 11 = Unimplemented

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits
 11111111 = Alarm will repeat 255 more times
 ...
 00000000 = Alarm will not repeat
 The counter decrements on any alarm event. The counter is prevented from rolling over from 00h to FFh unless CHIME = 1.

Section 29. Real-Time Clock and Calendar (RTCC)

29.2.2 RTCVAL Register Mappings

Register 29-4: YEAR: Year Value Register⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit; Contains a value from 0 to 9
- bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit; Contains a value from 0 to 9

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

Register 29-5: MTHDY: Month and Day Value Register⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MHTTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **MHTTEN0:** Binary Coded Decimal Value of Month's Tens Digit; Contains a value of 0 or 1
- bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit; Contains a value from 0 to 9
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal value of Day's Tens Digit; Contains a value from 0 to 3
- bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

PIC24F Family Reference Manual

Register 29-6: WKDYHR: Weekday and Hours Value Register⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15					bit 8		

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7					bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; Contains a value from 0 to 6
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit; Contains a value from 0 to 2
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

Register 29-7: MINSEC: Minutes and Seconds Value Register

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15					bit 8		

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7					bit 0		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit; Contains a value from 0 to 5
- bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit; Contains a value from 0 to 9
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit; Contains a value from 0 to 5
- bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit; Contains a value from 0 to 9

Section 29. Real-Time Clock and Calendar (RTCC)

29.2.3 ALRMVAL Register Mappings

Register 29-8: ALMTHDY: Alarm Month and Day Value Register⁽¹⁾

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	—	MHTTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0	
bit 15								bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **MHTTEN0:** Binary Coded Decimal Value of Month's Tens Digit; Contains a value of 0 or 1
- bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit; Contains a value from 0 to 9
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit; Contains a value from 0 to 3
- bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

Register 29-9: ALWDHR: Alarm Weekday and Hours Value Register⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	
—	—	—	—	—	WDAY2	WDAY1	WDAY0	
bit 15								bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit; Contains a value from 0 to 6
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit; Contains a value from 0 to 2
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit; Contains a value from 0 to 9

Note 1: A write to this register is only allowed when RTCWREN = 1.

PIC24F Family Reference Manual

Register 29-10: ALMINSEC: Alarm Minutes and Seconds Value Register

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit; Contains a value from 0 to 5
- bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit; Contains a value from 0 to 9
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit; Contains a value from 0 to 5
- bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit; Contains a value from 0 to 9

29.2.4 RTCEN Bit Write

An attempt to write to the RTCEN bit while RTCWREN = 0 will be ignored. RTCWREN must be set and then a write to RTCEN will take place.

Like the RTCEN bit, the RTCVAL<15:8> and RTCVAL<7:0> registers can only be written to when RTCWREN = 1. A write to these registers while RTCWREN = 0 will be ignored as well.

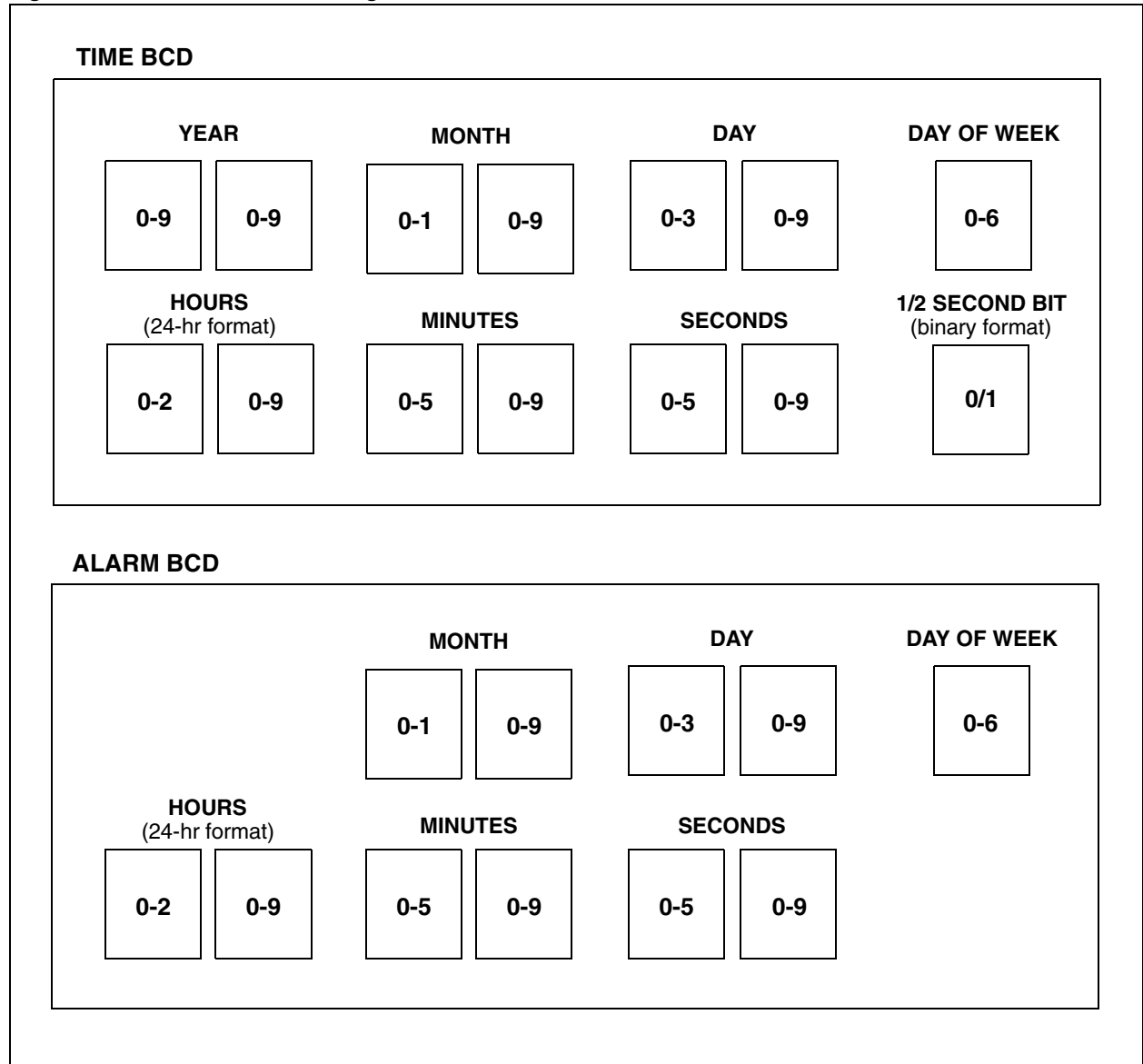
Section 29. Real-Time Clock and Calendar (RTCC)

29.3 OPERATION

29.3.1 Register Interface

The register interface for the RTCC and alarm values is implemented using the Binary Coded Decimal (BCD) format. This simplifies the firmware, when using the module, as each of the digit values is contained within its own 4-bit value (see Figure 29-2).

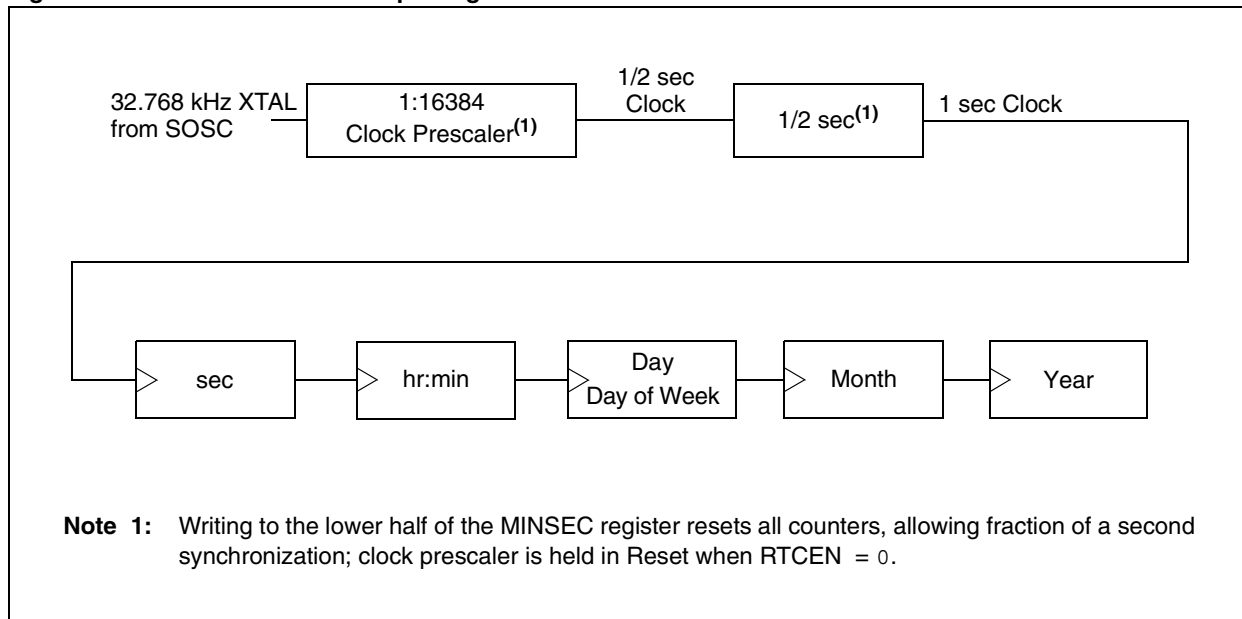
Figure 29-2: Timer and Alarm Digit Format



29.3.2 Clock Source

As mentioned earlier, the RTCC module is intended to be clocked by an external Real-Time Clock crystal oscillating at 32.768 kHz. Calibration of the crystal can be accomplished through this module yielding an error of 3 seconds or less per month (see **Section 29.3.9 “Calibration”** for further details).

Figure 29-3: Clock Source Multiplexing



29.3.2.1 REAL-TIME CLOCK CRYSTAL ENABLE

To allow the RTCC module to be clocked by an external 32.768 kHz crystal, the SOSCEN bit in the OSCCON register (see **Section 6. “Oscillator”**, Register 6-1) must be set. This is the only bit outside of the RTCC module that the user must be concerned with for enabling the RTCC.

Section 29. Real-Time Clock and Calendar (RTCC)

29.3.3 Digit Carry Rules

This section explains which timer values are affected when there is a rollover.

- Time of Day: from 23:59:59 to 00:00:00 with a carry to the day field
- Month: from 12/31 to 01/01 with a carry to the year field
- Day of Week: from 6 to 0 with no carry (refer to Table 29-1)
- Year Carry: from 99 to 00; this also surpasses the use of the RTCC

Refer to Table 29-2 for the day to month rollover schedule.

Considering that the following values are in BCD format, the carry to the upper BCD digit will occur at a count of 10 and not a count of 16 (SECONDS, MINUTES, HOURS, WEEKDAY, DAYS, MONTHS).

Table 29-1: Day of Week Schedule

Day of Week	
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

Table 29-2: Day to Month Rollover Schedule

Month	Maximum Day Field
01 (January)	31
02 (February)	28 or 29 (see Section 29.3.4 “Leap Year”)
03 (March)	31
04 (April)	30
05 (May)	31
06 (June)	30
07 (July)	31
08 (August)	31
09 (September)	30
10 (October)	31
11 (November)	30
12 (December)	31

29.3.4 Leap Year

Since the year range on the RTCC module is 2000 to 2099, the leap calculation is determined by any year divisible by 4 in the above range. The only month to be affected in a leap year is February. The month of February will have 29 days in a leap year, while any other year will have 28 days.

29.3.5 General Functionality

All Timer registers containing a time value of seconds or greater are writable. The user can configure the time by simply writing to these registers the desired year, month, day, hour, minutes and seconds via register pointers (see **Section 29.3.8 “Register Mapping”**). The timer will then use the newly written values and proceed with the count from the desired starting point. The RTCC module is enabled by setting the RTCEN bit (RCFGCAL<15>). If enabled while adjusting these registers, the timer will still continue to increment. However, any time the MINSEC register is written to, both of the timer prescalers are reset to '0'. This allows fraction of a second synchronization.

The Timer registers are updated in the same cycle as the write instruction is executed by the CPU. The user is responsible to assure that when RTCEN = 1, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- Checking the RTCSYNC bit (RCFGCAL<12>)
- Checking the preceding digits from which a carry can occur
- Updating the registers immediately following the seconds pulse (or alarm interrupt)

The user has visibility to the half-second field of the counter. This value is read-only and can only be reset by writing to the lower half of the MINSEC register.

Note: Although the above precautions should be taken when updating the registers, for some of the registers, large windows of time are available for updating. For example, the upper byte of the MTHDY register is only clocked once a month, whereas the lower byte is clocked once a day.

29.3.6 Safety Window for Register Reads and Writes

The RTCSYNC bit indicates a time window during which the RTCC clock domain registers can be safely read and written without concern about a rollover. When RTCSYNC = 0, the registers can be safely accessed by the CPU. Whether RTCSYNC = 1 or 0, the user should employ a firmware solution to assure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then comparing the two values. If the two values match, then a rollover did not occur.

29.3.7 Write Lock

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RCFGCAL<13>) must be set (refer to Example 29-1).

Example 29-1: Setting the RTCWREN Bit

```
MOV    #NVMKEY, W1           ;move the address of NVMKEY into W1
MOV.b  #0x55, W2
MOV.b  #0xAA, W3
MOV.b  W2, [W1]              ;start 55/AA sequence
MOV.b  W3, [W1]
BSET   RCFGCAL, #13         ;set the RTCWREN bit
```

Note: To avoid accidental writes to the timer, it is recommended that the RTCWREN bit (RCFGCAL<13>) is kept clear at any other time. For the RTCWREN bit to be set, there is only 1 instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN; therefore, it is recommended that the code example in Example 29-1 be followed.

Section 29. Real-Time Clock and Calendar (RTCC)

29.3.8 Register Mapping

To limit the register interface, the RTCC Timer and Alarm Time registers are accessed through corresponding register pointers. The RTCC Value register window (RTCVAL<15:8> and RTCVAL<7:0>) uses the RTCPTR bits (RCFGCAL<9:8>) to select the desired Timer register pair (see Table 29-3).

By reading or writing the RTCVAL<15:8> register, the RTCC pointer value, RTCPTR<1:0>, decrements by one until it reaches '00'. Once it reaches '00', the MINUTES and SECONDS value will be accessible through RTCVAL<15:8> and RTCVAL<7:0> until the pointer value is manually changed.

Table 29-3: RTCVAL Register Mapping

RTCPTR<1:0>	RTCC Value Register Window	
	RTCVAL<15:8>	RTCVAL<7:0>
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

The Alarm Value register window (ALRMVALH and ALRMVALL) uses the ALRMPTR bits (ALCFGRPT<9:8>) to select the desired Alarm register pair (see Table 29-4).

By reading or writing the ALRMVALH register, the alarm pointer value, ALRMPTR<1:0>, decrements by one until it reaches '00'. Once it reaches '00', the ALRMMIN AND ALRMSEC value will be accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

Table 29-4: ALRMVAL Register Mapping

ALRMPTR<1:0>	Alarm Value Register Window	
	ALRMVAL<15:8>	ALRMVAL<7:0>
00	ALRMMIN	ALRMSEC
01	ALRMWD	ALRMHR
10	ALRMMNTH	ALRMDAY
11	—	—

Considering that the 16-bit core does not distinguish between 8-bit and 16-bit read operations, the user must be aware that when reading either the ALRMVALH or ALRMVALL register, it will decrement the ALRMPTR<1:0> value. The same applies to the RTCVAL<15:8> or RTCVAL<7:0> register with the RTCPTR<1:0> being decremented.

Note: This only applies to read operations and not write operations. Write operations can be byte specific.

29.3.9 Calibration

The real-time crystal input can be calibrated using the periodic auto-adjust feature. When properly calibrated, the RTCC can provide an error of less than 3 seconds per month. This is accomplished by finding the number of error clock pulses and storing the value into the lower half of the RCFGAL register. The 8-bit signed value loaded into the lower half of RCFGAL is multiplied by four and will be either added or subtracted from the RTCC timer once every minute. Refer to the steps below for RTCC calibration:

1. Using another timer resource on the device, the user must find the error of the 32.768 kHz crystal.
2. Once the error is known, it must be converted to the number of error clock pulses per minute. Formula box:
(Ideal Frequency (32,758) – Measured Frequency) * 60 = Error Clocks per Minute
3. a) If the oscillator is *faster* than ideal (negative result from step 2), the RCFGAL register value needs to be negative. This causes the specified number of clock pulses to be subtracted from the timer counter once every minute.
b) If the oscillator is *slower* than ideal (positive result from step 2), the RCFGAL register value needs to be positive. This causes the specified number of clock pulses to be added to the timer counter once every minute.
4. Load the RCFGAL register with the correct value.

Writes to the lower half of the RCFGAL register should only occur when the timer is turned off, or immediately after the rising edge of the seconds pulse.

Note: It is up to the user to include in the error value the initial error of the crystal, drift due to temperature and drift due to crystal aging.
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Section 29. Real-Time Clock and Calendar (RTCC)

29.4 ALARM

- Configurable from half second to one year
- Enabled using the ALRMEN bit (ALCFGRPT<15>, Register 29-3)
- One-time alarm and repeat alarm options available

29.4.1 Configuring the Alarm

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. This bit will not be cleared if the CHIME bit = 1, or if the lower half of ALCFGRPT ≠ 00.

The interval selection of the alarm is configured through the AMASK bits (ALCFGRPT<13:10>), see Figure 29-4. These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur. The alarm can also be configured to repeat based on a pre-configured interval. The amount of times this occurs once the alarm is enabled is stored in the lower half of the ALCFGRPT register.

Note: Changing any of the registers, other than the RCFGCAL and ALCFGRPT registers and the CHIME bit while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0). It is recommended that the ALCFGRPT register and CHIME bit be changed when RTCSYNC = 0.

Figure 29-4: Alarm Mask Settings

Alarm Mask Setting AMASK<3:0>	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 – Every half second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>
0001 – Every second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>
0010 – Every 10 seconds	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s
0011 – Every minute	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s <input type="checkbox"/> s
0100 – Every 10 minutes	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0101 – Every hour	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0110 – Every day	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
0111 – Every week	<input type="checkbox"/> d	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
1000 – Every month	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> d <input type="checkbox"/> d	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s
1001 – Every year ⁽¹⁾	<input type="checkbox"/>	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> d <input type="checkbox"/> d	<input type="checkbox"/> h <input type="checkbox"/> h	<input type="checkbox"/> m <input type="checkbox"/> m	<input type="checkbox"/> s <input type="checkbox"/> s

Note 1: Annually, except when configured for February 29.

When $ALCFGRPT = 00$ and $CHIME$ bit = 0 ($ALCFGRPT < 14 >$), the repeat function is disabled and only a single alarm will occur. The alarm can be repeated up to 255 times by loading the lower half of the $ALCFGRPT$ register with FFh.

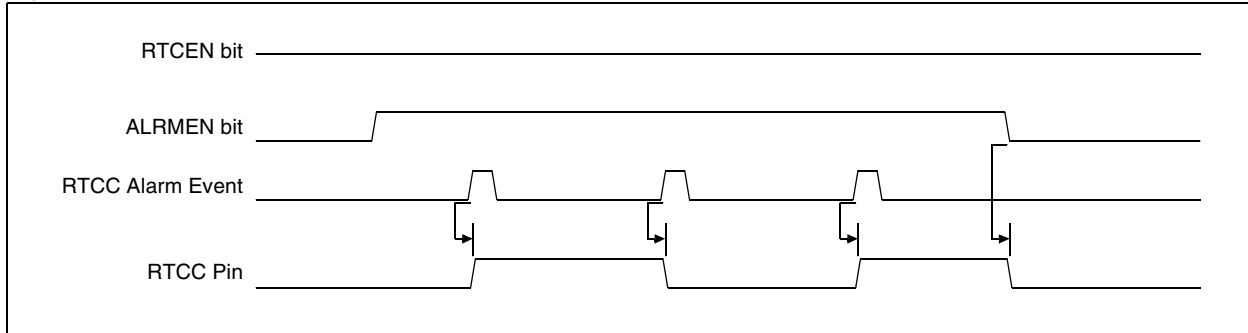
After each alarm is issued, the $ALCFGRPT$ register is decremented by one. Once the register has reached '00', the alarm will be issued one last time, after which the $ALRMEN$ bit will be cleared automatically and the alarm will turn off. Indefinite repetition of the alarm can occur if the $CHIME$ bit = 1. Instead of the alarm being disabled when the $ALCFGRPT$ register reaches '00', it will roll over to FF and continue counting indefinitely when $CHIME = 1$.

29.4.2 Alarm Interrupt

At every alarm event, an interrupt is generated. In addition, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a trigger clock to other peripherals. This output is available on the RTCC pin. The output pulse is a clock with a 50% duty cycle and a frequency half that of the alarm event (see Figure 29-5).

The RTCC pin is also capable of outputting the seconds clock. The user can select between the alarm pulse, generated by the RTCC module, or the seconds clock output. The $RTSECSEL$ ($PADCFG1 < 1 >$) bit selects between these two outputs. When $RTSECSEL = 0$, the alarm pulse is selected. When $RTSECSEL = 1$, the seconds clock is selected.

Figure 29-5: Timer Pulse Generation



29.5 SLEEP MODE

The timer and alarm continue to operate while in Sleep mode. The operation of the alarm is not affected by Sleep, as an alarm event can always wake-up the CPU.

Idle mode does not affect the operation of the timer or alarm.

29.6 RESET

29.6.1 Device Reset

When a device Reset occurs, the ALCFGRPT register is forced to its Reset state, causing the alarm to be disabled (if enabled prior to the Reset). If the RTCC was enabled, it will continue to operate when a basic device Reset occurs.

29.6.2 Power-on Reset (POR)

The RCFGCAL and ALCFGRPT registers are only reset on a POR. Once the device exits the POR state, the clock registers should be reloaded with the desired values.

The timer prescaler values can only be reset by writing to the Seconds register. No device Reset can affect the prescalers.

29.7 PERIPHERAL MODULE DISABLE (PMD) REGISTER

The Peripheral Module Disable (PMD) registers provide a method to disable the RTCC module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. A peripheral module will only be enabled if the RTCCMD bit in the the PMDx register is cleared.

29.8 REGISTER MAPS

A summary of the registers associated with the PIC24F RTCC module is provided in Table 29-5 and Table 29-6.

Table 29-5: Pad Configuration Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSESEL	PMPTTL	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for 100-pin devices.

Table 29-6: Real-Time Clock and Calendar Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	Alarm Value Register Window based on APTR<1:0>																
ALCFGRRPT	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	RTC Value Register Window based on RTCPTR<1:0>																
RCFGCAL ⁽¹⁾	RTCEN	—	RTWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTTR1	RTCPTTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCFGCAL register Reset value dependent on type of Reset.

Section 29. Real-Time Clock and Calendar (RTCC)

29.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Real-Time Clock and Calendar (RTCC) module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

29.10 REVISION HISTORY

Revision A (April 2006)

This is the initial released revision of this document.