Section 13. Parallel Master Port (PMP)

HIGHLIGHTS

This section of the manual contains the following major topics:

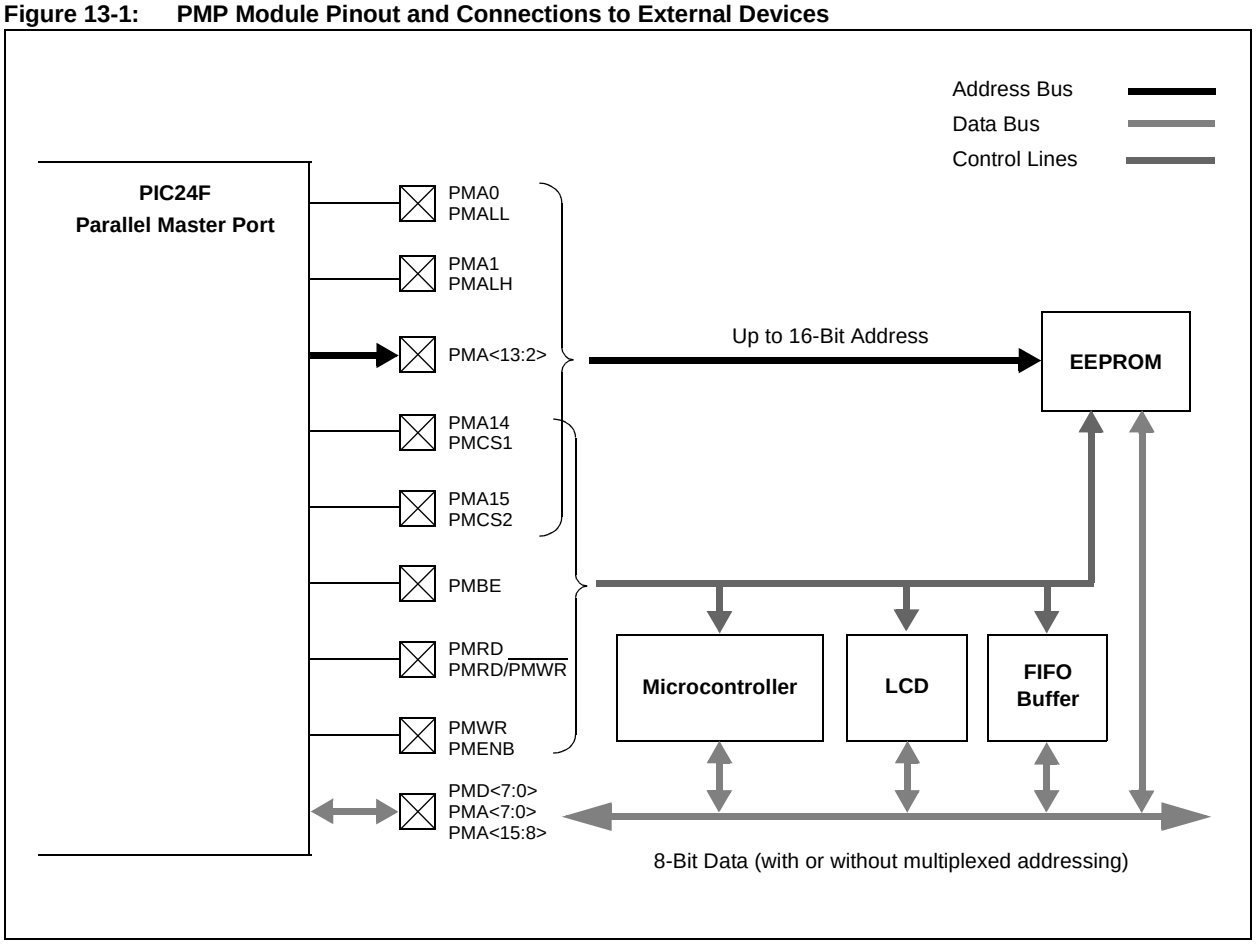
13.1 INTRODUCTION

The Parallel Master Port (PMP) is a parallel, 8-bit I/O module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

Key features of the PMP module include:

- 8 Data Lines
- Up to 16 Programmable Address Lines
- Up to 2 Chip Select Lines
- Programmable Strobe Options:
  - individual read and write strobes, or
  - read/$\overline{\text{write}}$ strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait States

Figure 13-1: PMP Module Pinout and Connections to External Devices



13.2 MODULE REGISTERS

The PMP module uses these Special Function Registers:

- PMCON
- PMMODE
- PMADDR/PMDOUT1
- PMDOUT2
- PMDIN1
- PMDIN2
- PMAEN
- PMSTAT

13.2.1 PMCON Register

The Parallel Master Port Control register (Register 13-1) contains the bits that control much of the module's basic functionality. A key bit is PMPEN, which is used to reset the module as well as enable or disable the module. When the module is disabled, all the associated I/O pins revert to their designated I/O function. In addition, any read or write operations, active or pending, are stopped and the BUSY bit is cleared. The data within the module registers is retained, including PMSTAT. Thus, the module could be disabled after a reception, and the last received data and status would still be available for processing. When the module is enabled, all buffer control logic is reset along with PMSTAT.

All other bits in the PMCON register control address multiplexing, enable various port control signals and select control signal polarity. These are discussed in more detail in **Section 13.4.1 "Parallel Master Port Configuration Options"**.

13.2.2 PMMODE Register

The Parallel Master Port Mode register (Register 13-2) contains bits that control the operational modes of the module. Master/Slave mode selection, as well as configuration options for both modes, are set by this register. It also contains the universal status flag, BUSY, used in Master modes to indicate that an operation by the module is in progress.

Details on the use of the PMMODE bits to configure PMP operation are provided in **Section 13.3 "Slave Port Modes"** and **Section 13.4 "Master Port Modes"**.

13.2.3 PMADDR/PMDOUT1 Register

Depending on the selected mode, this single register can have one of two functions. In Master modes, the register functions as PMADDR, the Parallel Port Address register (Register 13-3). It contains the address to which outgoing data is to be written to, as well as the chip select control bits for addressing parallel slave devices.

In Slave modes, the register functions as PMDOUT1, and acts as a buffer for outgoing data. Its operation is described in **Section 13.3.2 "Buffered Parallel Slave Port Mode"**.

13.2.4 PMDOUT2 Register

The Parallel Master Port Data Output 2 register is only used in Slave mode for buffered output data. It is used in the same manner as PMDOUT1.

13.2.5 PMDIN1 and PMDIN2 Registers

The Parallel Master Port Data Input 1 and Data Input 2 registers are used to buffer incoming data. PMDIN1 is used by the module in both Master and Slave modes. In Slave mode, this register is used to hold data that is asynchronously clocked in. Its operation is described in **Section 13.3.2 "Buffered Parallel Slave Port Mode"**.

In Master mode, PMDIN1 is the holding register for both incoming and outgoing data. Its operation in Master mode is described in **Section 13.4.2 "Read Operation"** and **Section 13.4.3 "Write Operation"**.

PMDIN2 is only used in Buffered Slave modes for incoming data. Its operation is similar to that of PMDIN1 in Buffered Slave modes.

13.2.6 PMAEN Register

The Parallel Master Port Address Enable register (Register 13-4) controls the operation of address and chip select pins associated with this module. Setting these bits allocates the corresponding microcontroller pins to the PMP module; clearing the bits allocates the pins to port I/O or other peripheral modules associated with the pins.

13.2.7 PMSTAT Register

The Parallel Master Port Status register (Register 13-5) contains status bits associated with buffered operating modes when the port is functioning as a slave port. This includes the overflow, underflow and full flag bits. These flags are discussed in detail in **Section 13.3.2 "Buffered Parallel Slave Port Mode"**.

13.2.8 Additional Registers

In addition to the PMP-specific registers, the PADCFG1 register also affects the configuration of the PMP module. The PMPTTL bit (PADCFG1<0>) allows the user to select between TTL and Schmitt Trigger (ST) digital input buffers for greater compatibility with external circuits. Setting PMPTTL selects TTL input buffers; the default configuration is ST buffers.

The PADCFG1 register is also described in **Section 29. "Real-Time Clock and Calendar (RTCC)"**.

Register 13-1: PMCON: Parallel Master Port Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX1:ADRMUX0:** Address/Data Multiplexing Selection bits
11 = Reserved
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 8 bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
1 = PMBE port enabled
0 = PMBE port disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port enabled
0 = PMWR/PMENB port disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port enabled
0 = PMRD/$\overline{\text{PMWR}}$ port disabled

bit 7-6 **CSF1:CSF0:** Chip Select Function bits
11 = Reserved
10 = PMCS1 and PMCS2 function as chip select
01 = PMCS2 functions as chip select, PMCS1 functions as address bit 14
00 = PMCS1 and PMCS2 function as address bits 15 and 14

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 1 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS2}}$)
0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 0 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS1}}$/$\overline{\text{PMCS2}}$)
0 = Active-low ($\overline{\text{PMCS1}}$/$\overline{\text{PMCS2}}$)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 13-1: PMCON: Parallel Master Port Control Register (Continued)

bit 2 **BEP:** Byte Enable Polarity bit
1 = Byte enable active-high (PMBE)
0 = Byte enable active-low ($\overline{\text{PMBE}}$)

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Read strobe active-high (PMWR)
0 = Read strobe active-low ($\overline{\text{PMWR}}$)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Read strobe active-high (PMRD)
0 = Read strobe active-low ($\overline{\text{PMRD}}$)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 13-2: PMMODE: Parallel Master Port Mode Register

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB1(1,2)	WAITB0(1,2)	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1(2)	WAITE0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM1:IRQM0:** Interrupt Request Mode bits
- 11 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
- 10 = Reserved
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 **INCM1:INCM0:** Increment Mode bits
- 11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
- 10 = Decrement ADDR<15,13:0> by 1 every read/write cycle
- 01 = Increment ADDR<15,13:0> by 1 every read/write cycle
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-Bit Mode bit
- 1 = 16-Bit mode: data register is 16 bits, a read or write to the data register invokes two 8-bit transfers
- 0 = 8-Bit mode: data register is 8 bits, a read or write to the data register invokes one 8-bit transfer

bit 9-8 **MODE1:MODE0:** Parallel Port Mode Select bits
- 11 = Master Mode 1 (PMCSx, PMRD/$\overline{\text{PMWR}}$, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
- 10 = Master Mode 2 (PMCSx, PMRD, $\overline{\text{PMWR}}$, $\overline{\text{PMBE}}$, PMA<x:0> and PMD<7:0>)
- 01 = Enhanced PSP, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCSx}}$, PMD<7:0> and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals ($\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, $\overline{\text{PMCSx}}$ and PMD<7:0>)

bit 7-6 **WAITB1:WAITB0:** Data Setup to Read/Write/Address Phase Wait State Configuration bits(1,2)
- 11 = Data wait of 4 TCY (demultiplexed/multiplexed); address phase of 4 TCY (multiplexed)
- 10 = Data wait of 3 TCY (demultiplexed/multiplexed); address phase of 3 TCY (multiplexed)
- 01 = Data wait of 2 TCY (demultiplexed/multiplexed); address phase of 2 TCY (multiplexed)
- 00 = Data wait of 1 TCY (demultiplexed/multiplexed); address phase of 1 TCY (multiplexed)

bit 5-2 **WAITM3:WAITM0:** Read to Byte Enable Strobe Wait State Configuration bits
- 1111 = Wait of additional 15 TCY
- **...**
- 0001 = Wait of additional 1 TCY
- 0000 = No additional Wait cycles (operation forced into one TCY)

bit 1-0 **WAITE1:WAITE0:** Data Hold After Strobe Wait State Configuration bits(2)
- 11 = Wait of 4 TCY
- 10 = Wait of 3 TCY
- 01 = Wait of 2 TCY
- 00 = Wait of 1 TCY

Note 1: The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 13.4.1.8 "Wait States"** for more information.

2: WAITBx and WAITEx bits are ignored whenever WAITM3:WAITM0 = 0000.

Register 13-3: PMADDR: Parallel Master Port Address Register (Master modes only)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS2	CS1	ADDR<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CS2:** Chip Select 2 bit
If PMCON<7:6> = 10 or 01:
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive
If PMCON<7:6> = 11 or 00:
Bit functions as ADDR<15>.

bit 14 **CS1:** Chip Select 1 bit
If PMCON<7:6> = 10:
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive
If PMCON<7:6> = 11 or 0x:
Bit functions as ADDR<14>.

bit 13-0 **ADDR13:ADDR0:** Destination Address bits

Note 1: In Enhanced Slave mode, PMADDR functions as PMDOUT1, one of the two data buffer registers. See **Section 13.2.3 "PMADDR/PMDOUT1 Register"** for information.

Register 13-4: PMAEN: Parallel Master Port Address Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-2 **PTEN13:PTEN2:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN1:PTEN0:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O

Register 13-5: PMSTAT: Parallel Master Port Status Register (Slave mode only)

R-0	R/W-0 HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0 HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable input buffer registers are full
0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full input byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer x Status Full bit
1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable output buffer registers are empty
0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer x Status Empty bit
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

13.3 SLAVE PORT MODES

In Slave mode, the PMP module provides an 8-bit data bus and all the necessary control signals to operate as a slave parallel device. It is also configurable for operation in Legacy, Buffered and Addressable modes. Slave mode provides several options for a more flexible interface:

- 8-bit data bus
- 2 address lines (Addressable mode only)
- 3 control lines (read, write and chip select)
- Selectable polarity on all control lines

To use the PMP as a slave, the module must be enabled (PMPEN = 1) and the mode must be set to one of the two possible Slave modes (PMMODE<9:8> = 01 or 00).

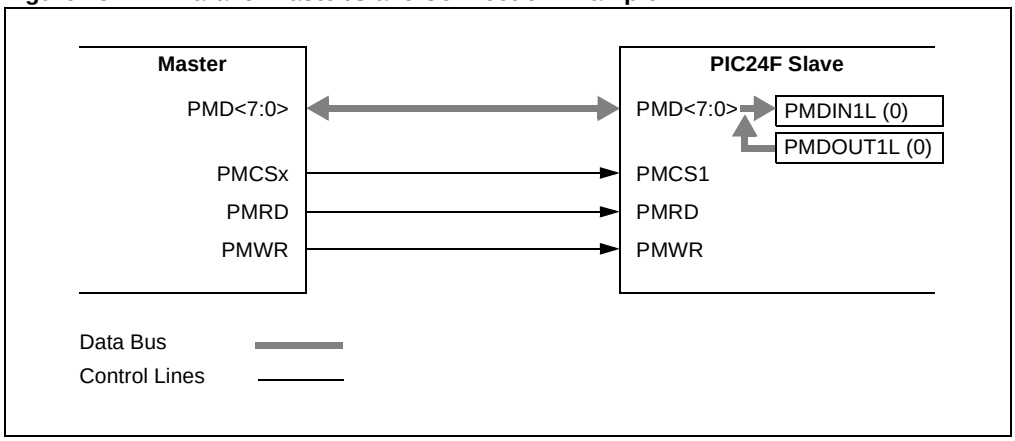
Note:	For all control lines (and PMA<1:0> in Addressable PSP mode), the corresponding control bits in the PMCON and PMAEN registers must be configured for parallel port operation. See **Section 13.4.1.2 "Port Pin Control"** for more details.

13.3.1 Legacy Mode

In Legacy mode (PMMODE<9:8> = 00 and PMMODE<12:11> ≠ 11), the module is configured as a Parallel Slave Port (PSP) with the associated enable module pins dedicated to the module. In this mode, an external device, such as another microcontroller or microprocessor, can asynchronously read and write data using the 8-bit data bus (PMD<7:0>), the read (PMRD), write (PMWR) and chip select (PMCSx) inputs.

Note:	PMCS1 is used as the chip select input in all Slave modes. PMCS2 is only used in Master modes.

Figure 13-2: Parallel Master/Slave Connection Example



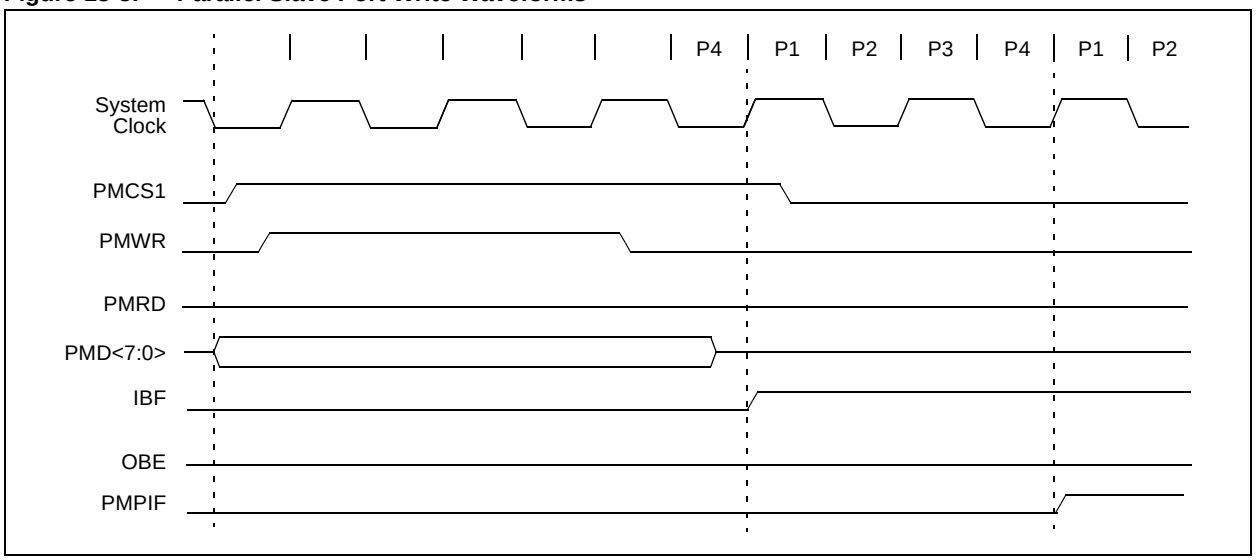
13.3.1.1 WRITE TO SLAVE PORT

When chip select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into the lower 8 bits of the PMDIN1 register (PMDIN1<7:0>). The PMPIF and IBF flag bits are set when the write ends.

The timing for the control signals in Write mode is shown in Figure 13-3. The polarity of the control signals is configurable.

Note 1:	The relationship between the P clock and system clock cycles, shown in Figure 13-3 and Figure 13-4, apply to all timing diagrams shown in this section.

Figure 13-3: Parallel Slave Port Write Waveforms

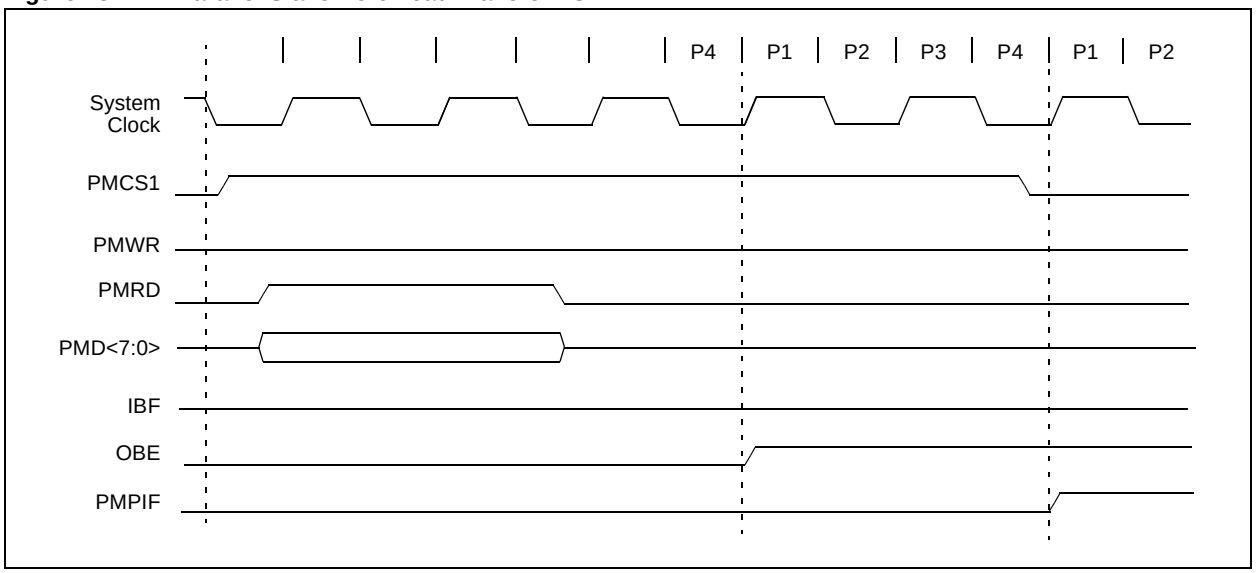


13.3.1.2 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from the lower 8 bits of the PMDOUT1 register (PMDOUT1<7:0>) is presented onto PMD<7:0>. The data in PMDIN1<7:0> is read out, and the Output Buffer Empty flag, OBE, is set. If the user writes new data to PMDIN1<7:0> to clear OBE, the data is immediately read out; however, the OBE is not cleared.

The timing for the control signals in Read mode is shown in Figure 13-4.

Figure 13-4: Parallel Slave Port Read Waveforms



13.3.1.3 INTERRUPT OPERATION

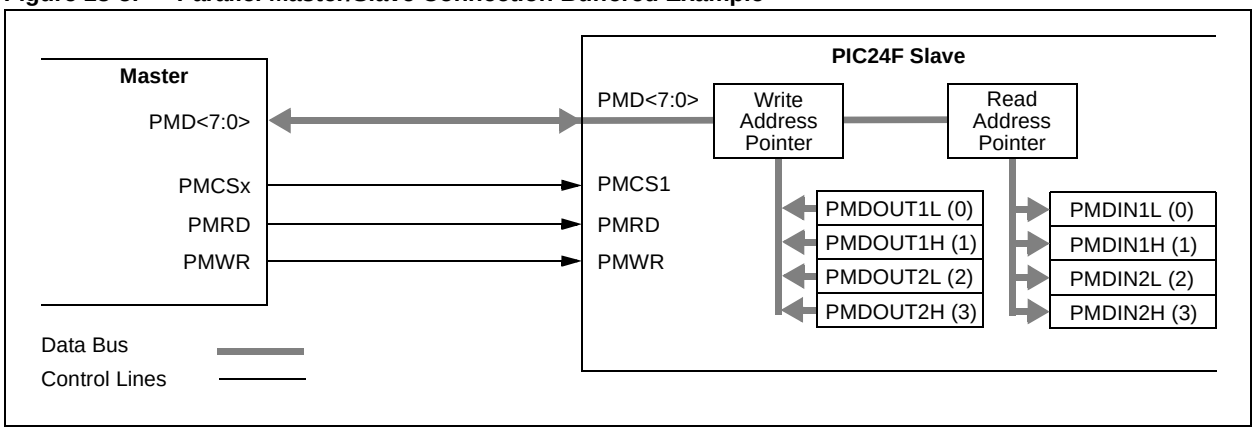
When either the PMCS1 or PMRD lines are detected high, the port pins return to the input state and the PMPIF bit is set. User applications should wait for PMPIF to be set before servicing the module. When this happens, the IBF and OBE bits can be polled and the appropriate action taken.

13.3.2 Buffered Parallel Slave Port Mode

Buffered Parallel Slave Port mode is functionally identical to the Legacy Parallel Slave Port mode with one exception: the implementation of 4-level read and write buffers. Buffered PSP mode is enabled by setting the INCM<1:0> bits (PMMODE<12:11>) to '11'.

When the Buffered mode is active, the module uses the PMDIN1 and PMDIN2 registers as write buffers and the PMDOUT1 and PMDOUT2 registers as read buffers. Each register is split into two single-byte buffer registers, producing separate read and write buffers that are each 4 bytes deep. Buffers are numbered 0 through 3, starting with the lower byte of PMDIN1 or PMDOUT1 and progressing upward through the high byte of PMDIN2 (PMDOUT2).

Figure 13-5: Parallel Master/Slave Connection Buffered Example



13.3.2.1 READ FROM SLAVE PORT

For read operations, the bytes will be sent out sequentially, starting with Buffer 0 (PMDOUT1<7:0>) and ending with Buffer 3 (PMDOUT2<15:8>) for every read strobe. The module maintains an internal pointer to keep track of which buffer is to be read.

Each of the buffers has a corresponding read status bit, OBxE, in the PMSTAT register. This bit is cleared when a buffer contains data that has not been written to the bus, and is set when data is written to the bus. If the current buffer location being read from is empty, a buffer underflow is generated, and the Buffer Overflow Flag bit, OBUF (PMSTAT<6>), is set. If all four OBxE status bits are set, then the OBE bit will also be set.

13.3.2.2 WRITE TO SLAVE PORT

For write operations, the data is be stored sequentially, starting with Buffer 0 (PMDIN1<7:0>) and ending with Buffer 3 (PMDIN2<15:8>). As with read operations, the module maintains an internal pointer to the buffer that is to be written next.

The input buffers have their own write status bits, IBxE. The bit is set when the buffer contains unread incoming data, and cleared when the data has been read. The flag bit is set on the write strobe. If a write occurs on a buffer when its associated IBxE bit is set, the Input Buffer Overflow Flag, IBOV, is set; any incoming data in the buffer will be lost. If all 4 IBxE flags are set, the Input Buffer Full Flag (IBF) is set.

13.3.2.3 INTERRUPT OPERATION

In Buffered Slave mode, the module can be configured to generate an interrupt on every read or write strobe (IRQM<1:0> = 01). It can also be configured to generate an interrupt on a read from Read Buffer 3 or a write to Write Buffer 3 (IRQM<1:0> = 11), which is essentially an interrupt every fourth read or write strobe. When interrupting every fourth byte for input data, all input buffer registers should be read to clear the IBxF flags. If these flags are not cleared, then there is a risk of hitting an overflow condition. The PMSTAT register provides status information on all buffers.

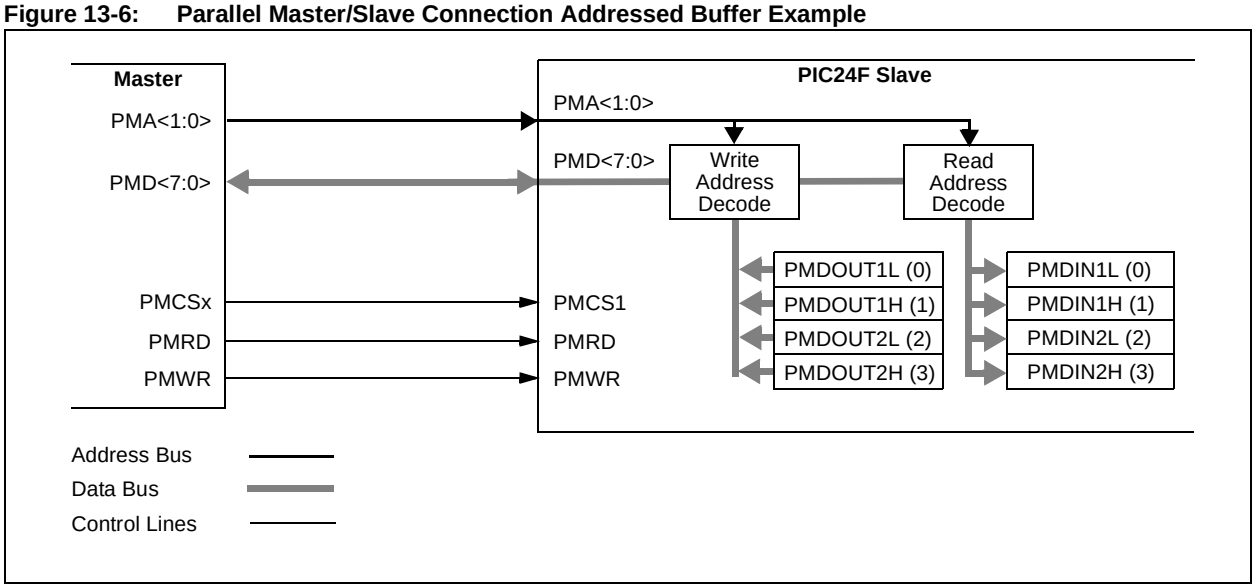
13.3.3 Addressable Parallel Slave Port Mode

In Addressable Parallel Slave Port mode, the module is configured with two extra inputs, PMA<1:0>. This makes the 4-byte buffer space directly addressable as fixed pairs of read and write buffers. The Addressable PSP mode is enabled by setting the MODE<1:0> bits (PMMODE<9:8>) to '01'. As with Buffered Legacy mode, data is output from PMDOUT1 and PMDOUT2 and is read in PMDIN1 and PMDIN2. Table 13-1 shows the address resolution for the incoming address to the input and output registers.

Table 13-1: Slave Mode Address Resolution

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1<7:0> (0)	PMDIN1<7:0> (0)
01	PMDOUT1<15:8> (1)	PMDIN1<15:8> (1)
10	PMDOUT2<7:0> (2)	PMDIN2<7:0> (2)
11	PMDOUT2<15:8> (3)	PMDIN2<15:8> (3)

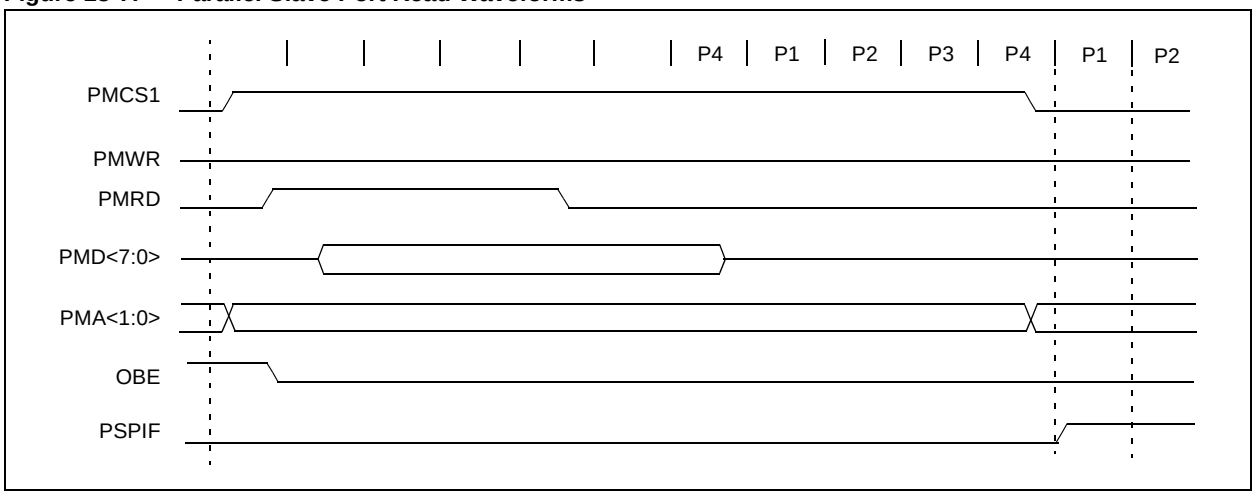
Figure 13-6: Parallel Master/Slave Connection Addressed Buffer Example



13.3.3.1 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from one of the four output bytes is presented onto PMD<7:0>. Which byte is read depends on the 2-bit address placed on PMA<1:0>. Table 13-1 shows the corresponding output registers and their associated address. When an output buffer is read, the corresponding OBxE bit is set. The OBE flag bit is set when all the buffers are empty. If any buffer is already empty, OBxE = 1, the next read to that buffer will set the OBUF (PMSTAT<6>) flag.

Figure 13-7: Parallel Slave Port Read Waveforms

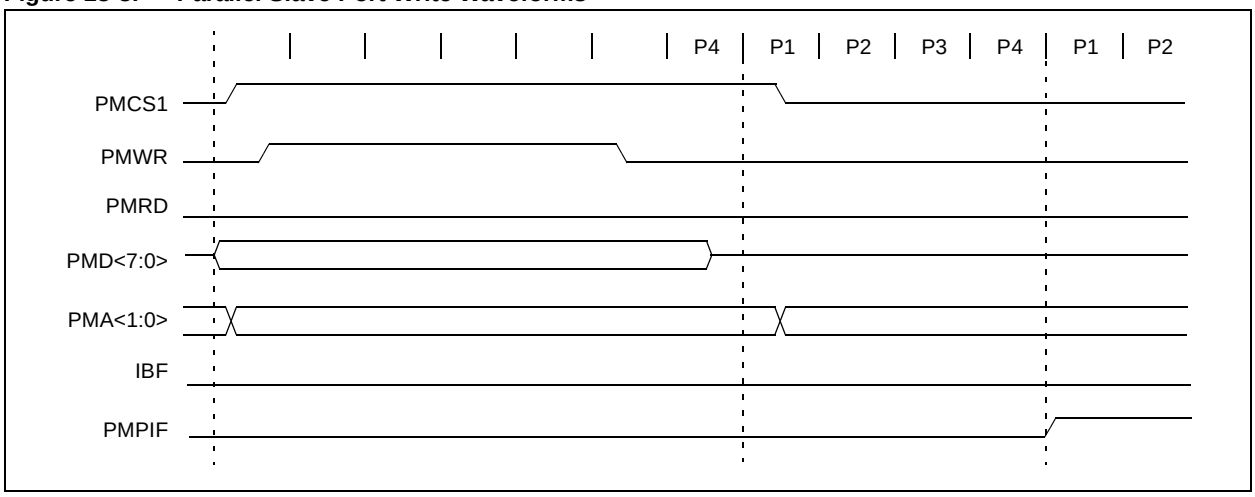


13.3.3.2 WRITE TO SLAVE PORT

When chip select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into one of the four input buffer bytes. Which byte is written depends on the 2-bit address placed on PMA<1:0>. Table 13-1 shows the corresponding input registers and their associated address.

When an input buffer is written, the corresponding IBxF bit is set. The IBF flag bit is set when all the buffers are written. If any buffer is already written, IBxF = 1, the next write strobe to that buffer will generate an OBUF event and the byte will be discarded.

Figure 13-8: Parallel Slave Port Write Waveforms



13.3.3.3 INTERRUPT OPERATION

In Addressable PSP mode, the module can be configured to generate an interrupt on every read or write strobe. It can also be configured to generate an interrupt on any read from Read Buffer 3 or write to Write Buffer 3; in other words, an interrupt will occur whenever a read or write occurs when the PMA<1:0> pins are '11'.

13.4 MASTER PORT MODES

In its Master modes, the PMP module provides an 8-bit data bus, up to 16 bits of address and all the necessary control signals to operate a variety of external parallel devices, such as memory devices, peripherals and slave microcontrollers. To use the PMP as a master, the module must be enabled (PMPEN = 1) and the mode must be set to one of the two possible Master modes (PMMODE<9:8> = 10 or 11).

Because there are a number of parallel devices with a variety of control methods, the PMP module is designed to be extremely flexible to accommodate a range of configurations. Some of these features include:

- 8 and 16-Bit Data modes on an 8-bit data bus
- Configurable address/data multiplexing
- Up to 2 chip select lines
- Up to 16 selectable address lines
- Address auto-increment and auto-decrement
- Selectable polarity on all control lines
- Configurable Wait states at different stages of the read/write cycle

13.4.1 Parallel Master Port Configuration Options

13.4.1.1 CHIP SELECTS

Up to two chip select lines, PMCS1 and PMCS2, are available for the Master modes of the PMP. The two chip select lines are multiplexed with the Most Significant bits of the address bus (PMA<14> and PMA<15>). When a pin is configured as a chip select, it is not included in any address auto-increment/decrement. The function of the chip select signals is configured using the Chip Select Function bits, CSF1:CSF0 (PMCON <7:6>). It is also necessary to set the CS1 and CS2 bits in PMADDR (PMADDR<15:14>) to enable the corresponding chip select.

13.4.1.2 PORT PIN CONTROL

The PTBEEN, PTWREN and PTRDEN bits (PMCON<10:8>) and the PTENx bits (PMAEN<15:0>) allow the user to conserve PMP pins for other functions, and allow flexibility to control the external address. When any one of these bits is set, the associated PMP function is present on its associated pin; when clear, the associated pin reverts to its defined I/O port function.

For the PMA<13:2> pins, setting the corresponding PTENx bit enables the pin as an address pin and drives the corresponding data contained in the PMADDR register. For the pins configured as chip select (PMCS1 or PMCS2) with PTEN14 or PTEN15 set, the chip select pins drive the inactive state (configured through the CSxP bits in PMCON) when a read or write operation is not being performed. For the pins configured as address latches, the PTEN0 and PTEN1 bits also control the PMALL and PMALH signals. When multiplexing is used, the associated address latch signals should be enabled.

13.4.1.3 ADDRESS MULTIPLEXING

In either of the Master modes (MODE1:MODE0 = 1x), the user can configure the address bus to be multiplexed together with the data bus. This is accomplished using the ADRMUX1:ADRMUX0 bits. There are three Address Multiplexing modes available. Typical pinout configurations for these modes are shown in Figure 13-9, Figure 13-10 and Figure 13-11.

In Demultiplexed mode (ADRMUX1:ADRMUX0 = 00), data and address information are completely separated. Data bits are presented on PMD<7:0> and address bits are presented on PMA<15:0>. Without any additional Wait states enabled, a read or write operation takes one TCY.

In Partially Multiplexed mode (ADRMUX1:ADRMUX0 = 01), the lower eight bits of the address are multiplexed with the data pins on PMD<7:0>. The upper eight bits of the address are unaffected and are presented on PMA<15:8>. The PMA<0> pin is used as an address latch, and presents the Address Latch Low enable strobe (PMALL). The read and write sequences are extended by a complete CPU cycle, during which, the address is presented on the PMD<7:0> pins. This means that without any additional Wait states enabled, a read or write operation takes two TCY.

In Fully Multiplexed mode (ADRMUX1:ADRMUX0 = 10), the entire 16 bits of the address are multiplexed with the data pins on PMD<7:0>. The PMA<0> and PMA<1> pins are used to present Address Latch Low enable (PMALL) and Address Latch High enable (PMALH) strobes, respectively.

The read and write sequences are extended by two complete CPU cycles. During the first cycle the lower eight bits of the address are presented on the PMD<7:0> pins with the PMALL strobe active. During the second cycle, the upper eight bits of the address are presented on the PMD<7:0> pins with the PMALH strobe active. In the event the upper address bits are configured as chip select pins, the corresponding address bits are automatically forced to '0'. Without any additional Wait states enabled, a read or write operation takes three TCY.

For sample timings of the different multiplexing modes, see **Section 13.4.5 "Master Mode Timing"**.

Figure 13-9: Demultiplexed Addressing Mode (Separate Read and Write Strobes, Two Chip Selects)

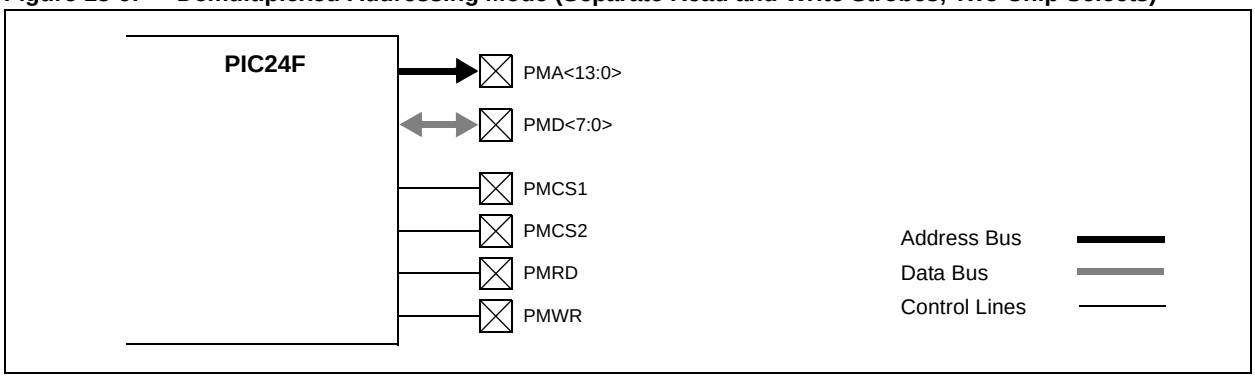


Figure 13-10: Partially Multiplexed Addressing Mode (Separate Read and Write Strobes, Two Chip Selects)

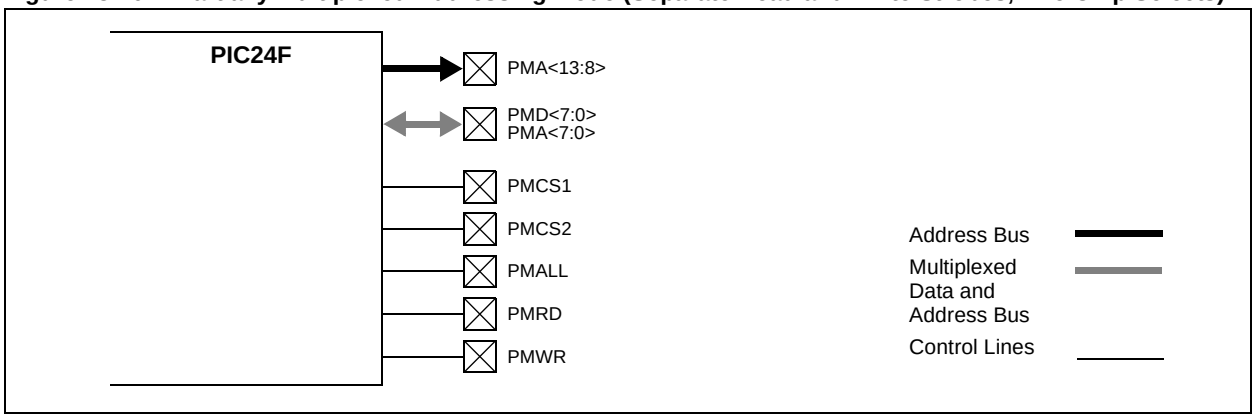


Figure 13-11: Fully Multiplexed Addressing Mode (Separate Read and Write Strobes, Two Chip Selects)

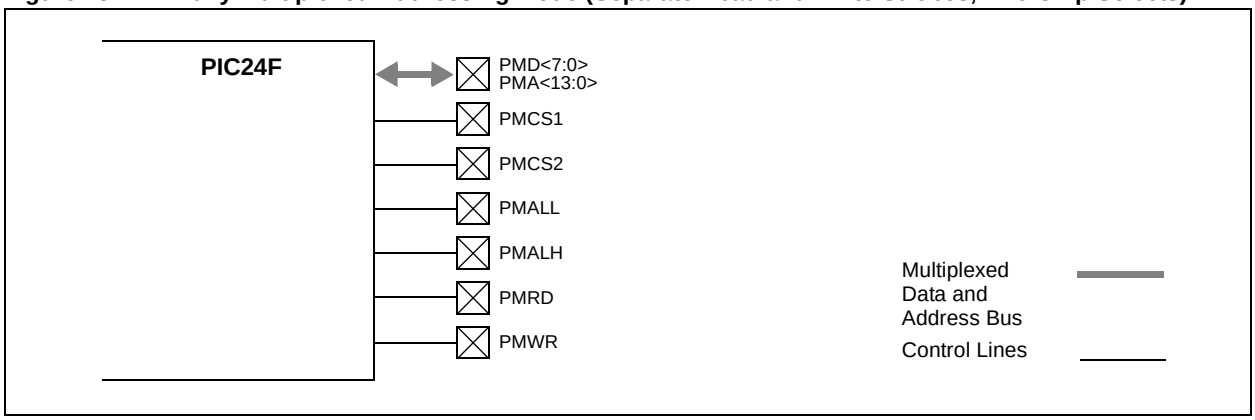
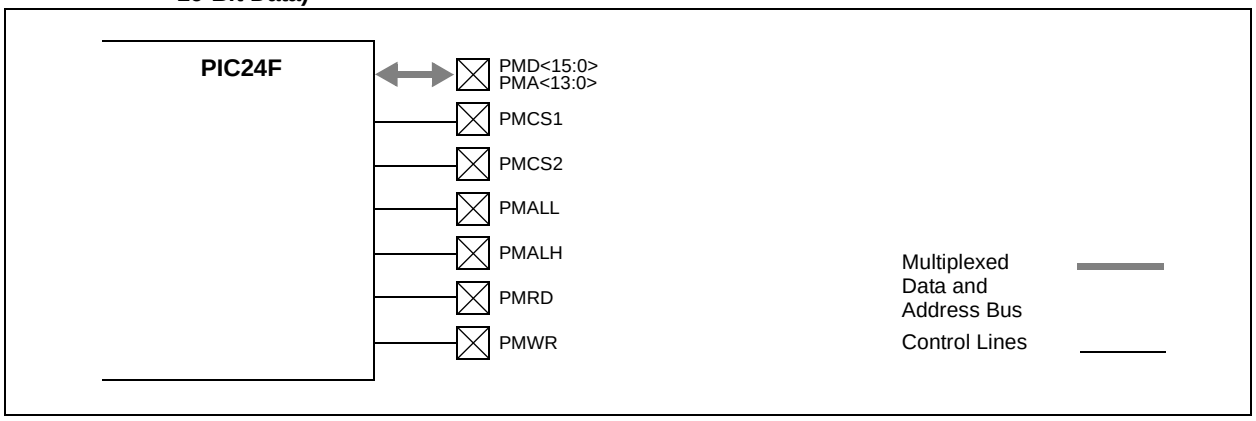


Figure 13-12: Fully Multiplexed Addressing Mode (Separate Read and Write Strobes, Two Chip Selects and 16-Bit Data)



13.4.1.4 8-BIT AND 16-BIT DATA MODES

The PMP supports data widths of both 8 and 16 bits. The data width is selected by the MODE16 bit (PMMODE<10>). Because the data path into and out of the module is only 8 bits wide, 16-bit operations are always handled in a multiplexed fashion, with the Least Significant Byte of data being presented first. To differentiate data bytes, the Byte Enable Control Strobe, PMBE, is used to signal when the Most Significant Byte of data is being presented on the data lines.

13.4.1.5 READ/WRITE CONTROL

The PMP module supports two distinct read/write signaling methods. In Master Mode 1, the read and write strobe are combined into a single control line, PMRD/$\overline{\text{PMWR}}$; a second control line, PMENB, determines when a read or write action is to be taken. In Master Mode 2, separate read and write strobes (PMRD and PMWR) are supplied on separate pins. Chip selects and Byte Enable Control Strobe (PMBE) are optionally available in both modes.

13.4.1.6 CONTROL LINE POLARITY

All control signals (PMRD, PMWR, PMBE, PMENB, PMAL and PMCSx) can be individually configured for either positive or negative polarity. Configuration is controlled by separate bits in the PMCON register. Note that the polarity of control signals that share the same output pin (for example, PMWR and PMENB) are controlled by the same bit; the configuration depends on which Master Port mode is being used. Additionally, the polarity of both PMALH and PMALL are controlled by a single bit.

13.4.1.7 AUTO-INCREMENT/DECREMENT

While the module is operating in one of the Master modes, the INCMx bits (PMMODE<12:11>) control the behavior of the address value. The address can be made to automatically increment or decrement after each read and write operation. The address increments once each operation is completed and the BUSY bit goes to '0'. If the chip select signals are disabled and configured as address bits, the bits will participate in the increment and decrement operations; otherwise, the CS2 and CS1 bit values will be unaffected.

13.4.1.8 WAIT STATES

In Master mode, the user has control over the duration of the read, write and address cycles, by configuring the module Wait states as multiples of TCY. Three portions of the cycle, the beginning, middle and end, are configured using the corresponding WAITBx, WAITMx and WAITEx bits in the PMMODE register.

The WAITB1:WAITB0 bits (PMMODE<7:6>) set the number of Wait states at the beginning of the cycle. The Wait states are applied between data setup and the PMRD or PMWR strobes in Master Mode 2, or the PMENB strobe in Master Mode 1. In addition, when the address bus is multiplexed with the data bus (ADRMUX1:ADRMUX0 = 01 or 10), the Wait states are also added to the length of each part of the address phase.

The four WAITMx bits (PMMODE<5:2>) set the number of Wait cycles for the PMRD or PMWR strobes in Master Mode 1, or for the PMENB strobe in Master Mode 2. When this Wait state setting is 0, then WAITBx and WAITEx have no effect.

The two WAITEx bits (PMMODE<1:0>) set the number of Wait cycles for the data hold time after the PMRD or PMWR strobes in Master Mode 1, or after the PMENB strobe in Master Mode 2.

13.4.1.9 PIN FUNCTIONS BASED ON OPERATING MODE

Depending on the options selected, many of the physical pins of the PMP can assume different functions in different Master modes. In some modes, certain pins may become available for microcontroller I/O or other device features. Table 13-2 summarizes the differences in control and address pin functions based on the selected Master mode, Address Multiplexing mode and number of chip selects enabled. Table 13-3 shows how data and addressing are multiplexed in different data width and Address Multiplexing modes.

Note: For a PMP pin to function as a general I/O pin, its corresponding port control bit must also be configured correctly. See **Section 13.4.1.2 "Port Pin Control"** for more information.

Table 13-2: PMP Address and Control Pin Functions in All Master Modes

PMP Pin Name	Pin Functions in Address Multiplexing Modes (ADRMUX1:ADRMX0) and Chip Selects (CSF1:CSF0)								
	Demultiplexed (00)			Partial (01)			Full (10)		
	0 CS (00)	1 CS (01)	2 CS (10)	0 CS (00)	1 CS (01)	2 CS (10)	0 CS (00)	1 CS (01)	2 CS (10)
Master Mode 1 (Shared Read/Write Strobe), 8-Bit and 16-Bit Data Modes									
PMRD	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR
PMWR	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB
PMBE	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)
	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)
PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2
PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1
PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	I/O	I/O	I/O
PMA<7:2>	PMA<7:2>	PMA<7:2>	PMA<7:2>	I/O	I/O	I/O	I/O	I/O	I/O
PMA1	PMA1	PMA1	PMA1	I/O	I/O	I/O	PMALH	PMALH	PMALH
PMA0	PMA0	PMA0	PMA0	PMALL	PMALL	PMALL	PMALL	PMALL	PMALL
Master Mode 2 (Separate Read and Write Strobes), 8-Bit and 16-Bit Data Modes									
PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD
PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR
PMBE	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)	I/O(1)
	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)	PMBE(2)
PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2
PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1
PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	I/O	I/O	I/O
PMA<7:2>	PMA<7:2>	PMA<7:2>	PMA<7:2>	I/O	I/O	I/O	I/O	I/O	I/O
PMA1	PMA1	PMA1	PMA1	I/O	I/O	I/O	PMALH	PMALH	PMALH
PMA0	PMA0	PMA0	PMA0	PMALL	PMALL	PMALL	PMALL	PMALL	PMALL

Note 1: 8-Bit Data modes only.
2: 16-Bit data modes only.

Table 13-3: PMP Data Pin Functions for All Master Modes

PMP Data Mode (MODE16)	Pin Functions for PMD<7:0> in Address Multiplexing Modes (ADRMUX1:ADRMX0) and Chip Selects (CSF1:CSF0)						
	Demultiplexed (00)	Partial (01)			Full (10)		
	All Chip Select Options	0 CS (00)	1 CS (01)	2 CS (10)	0 CS (00)	1 CS (01)	2 CS (10)
8-bit (0)	PMD<7:0>	PMA<7:0>, PMD<7:0>	PMA<7:0>, PMD<7:0>	PMA<7:0>, PMD<7:0>	PMA<7:0>, PMA<15:8>, PMD<7:0>	PMA<7:0>, PMA<14:8>, PMD<7:0>	PMA<7:0>, PMA<13:8>, PMD<7:0>
16-bit (1)	PMD<7:0> PMD<15:8>	PMA<7:0>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMA<15:8>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMA<14:8>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMA<13:8>, PMD<7:0>, PMD<15:8>

13.4.2 Read Operation

To perform a read on the parallel port, the user reads the low byte of the PMDIN1 register. This causes the PMP to output the desired values on the chip select lines and the address bus. Then, the read line (PMRD) is strobed. The read data is placed into the low byte of the PMDIN1 register.

If the 16-bit mode is enabled (MODE16 = 1), the read of the low byte of the PMDIN1 register will initiate two bus reads. The first read data byte is placed into the lower byte of the PMDIN1 register, and the second read data is placed into the upper byte of PMDIN1.

Note that the read data obtained from the PMDIN1 register is actually the read value from the previous read operation. Hence, the first user read will be a dummy read to initiate the first bus read and fill the read register. Also, the requested read value will not be ready until after the BUSY bit is observed low. Thus, in a back-to-back read operation, the data read from the register will be the same for both reads. The next read of the register will yield the new value.

To summarize this section, perform two reads of the PMDIN1 register to read a random byte/word; the second read gives the actual data. To perform a sequential read, perform one dummy read followed by the required number of actual reads of the PMDIN1 register.

13.4.3 Write Operation

To perform a write onto the parallel bus, the user writes to the low byte of the PMDIN1 register. This causes the module to first output the desired values on the chip select lines and the address bus. The write data from the low byte of the PMDIN1 register is placed onto the PMD<7:0> data bus. Then, the write line (PMWR) is strobed.

If the 16-bit mode is enabled (MODE16 = 1), the write to the low byte of the PMDIN1 register will initiate two bus writes. The first write will consist of the data contained in the lower byte of PMDIN1 and the second write will contain the upper byte of PMDIN1.

13.4.4 Parallel Master Port Status

13.4.4.1 THE BUSY BIT

In addition to the PMP interrupt, a BUSY bit is provided to indicate the status of the module. This bit is only used in Master mode.

While any read or write operation is in progress, the BUSY bit is set for all but the very last CPU cycle of the operation. In effect, if a single-cycle read or write operation is requested, the BUSY bit will never be active. This allows back-to-back transfers. It is only helpful if Wait states are enabled or multiplexed address/data is selected.

While the bit is set, any request by the user to initiate a new operation will be ignored (i.e., writing or reading the lower byte of the PMDIN1 register will not initiate either a read nor a write). The user needs to try again after the BUSY flag is cleared.

13.4.4.2 INTERRUPTS

When the PMP module interrupt is enabled for Master mode, the module will interrupt on every completed read or write cycle. Otherwise, the BUSY bit is available to query the status of the module.

13.4.5 Master Mode Timing

This section contains a number of timing examples that represent the common Master mode configuration options. These options vary from 8-bit to 16-bit data, fully demultiplexed to fully multiplexed address, as well as Wait states.

Note:	Refer to Figure 13-3 and Figure 13-4 for the relationship of P clock and system clock cycles.

Figure 13-13: Read and Write Timing, 8-Bit Data, Demultiplexed Address

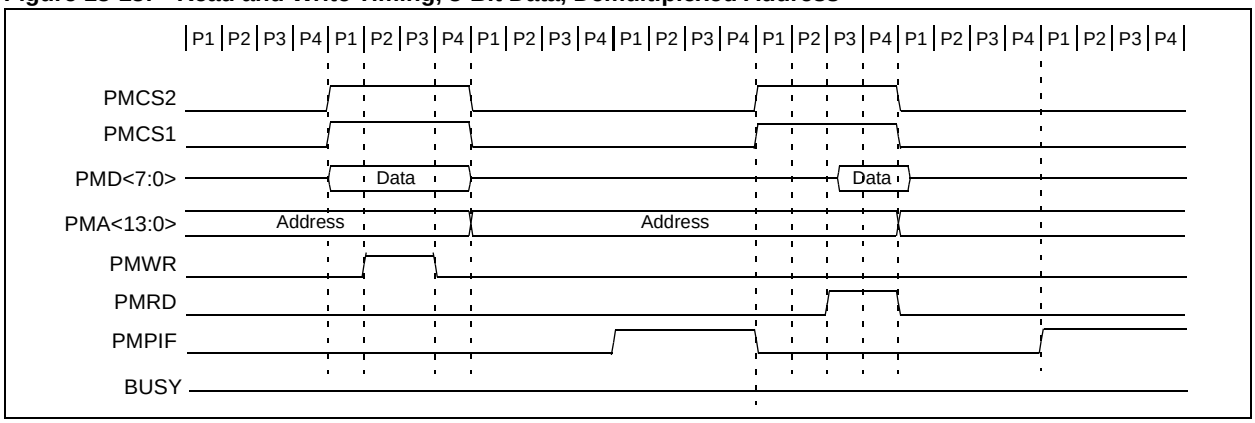


Figure 13-14: Read Timing, 8-Bit Data, Demultiplexed Address, Wait States Enabled

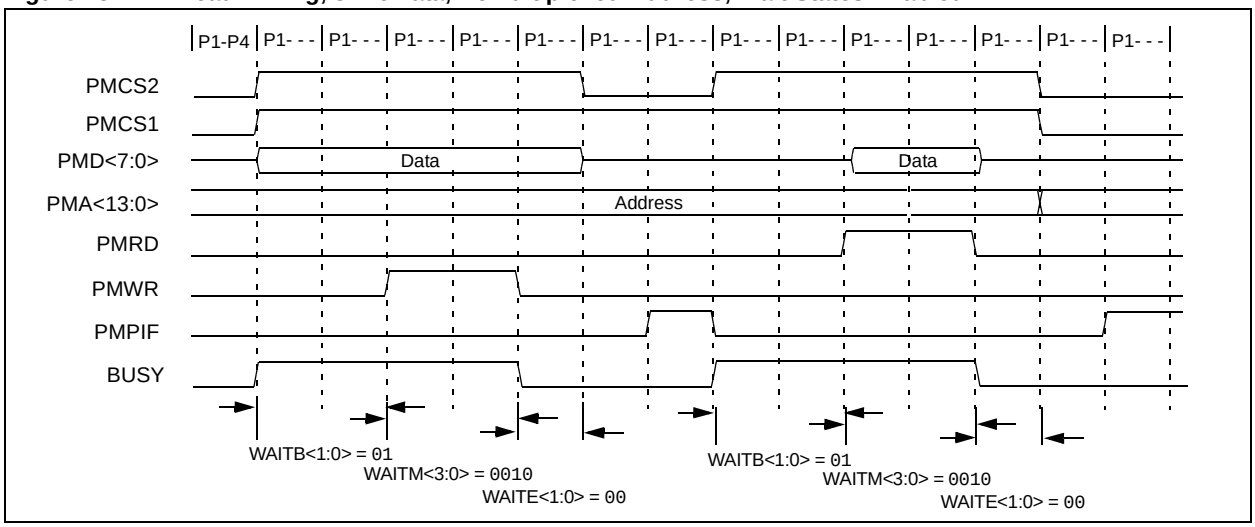


Figure 13-15: Read Timing, 8-Bit Data, Partially Multiplexed Address

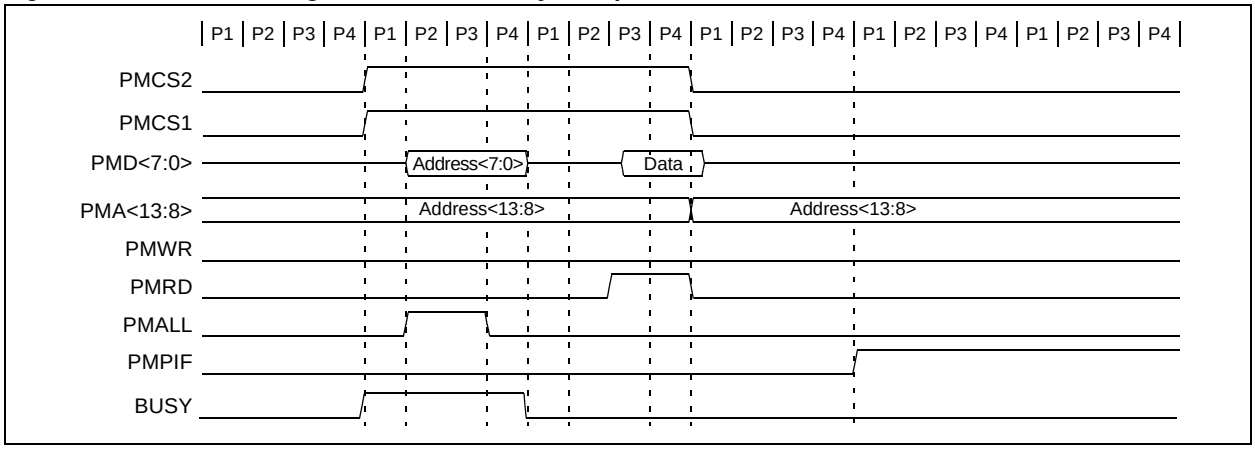


Figure 13-16: Read Timing, 8-Bit Data, Partially Multiplexed Address, Wait States Enabled

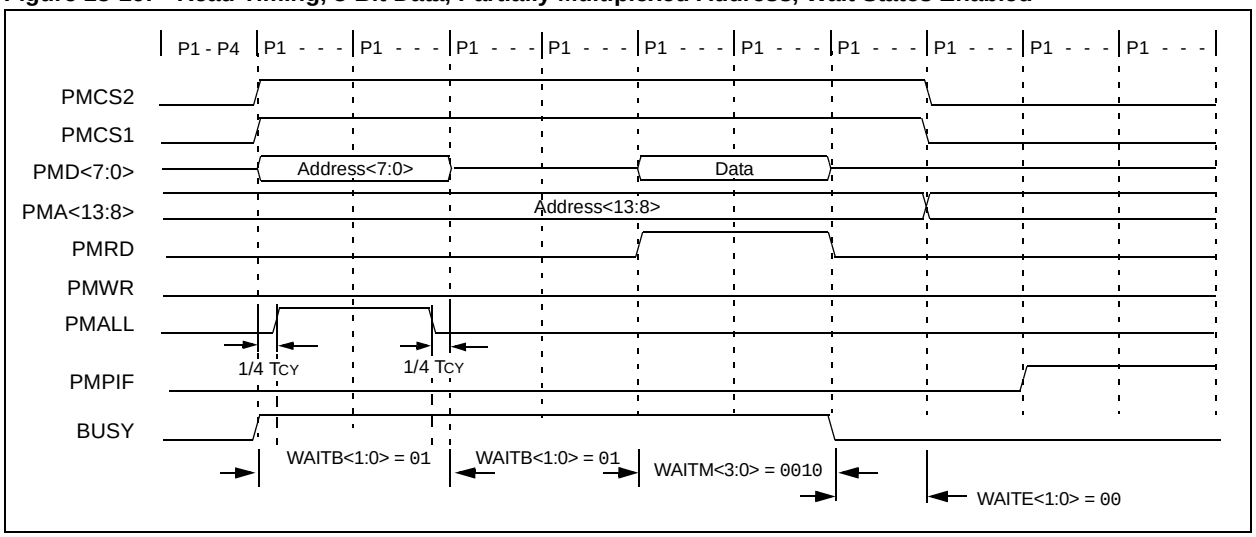


Figure 13-17: Write Timing, 8-Bit Data, Partially Multiplexed Address

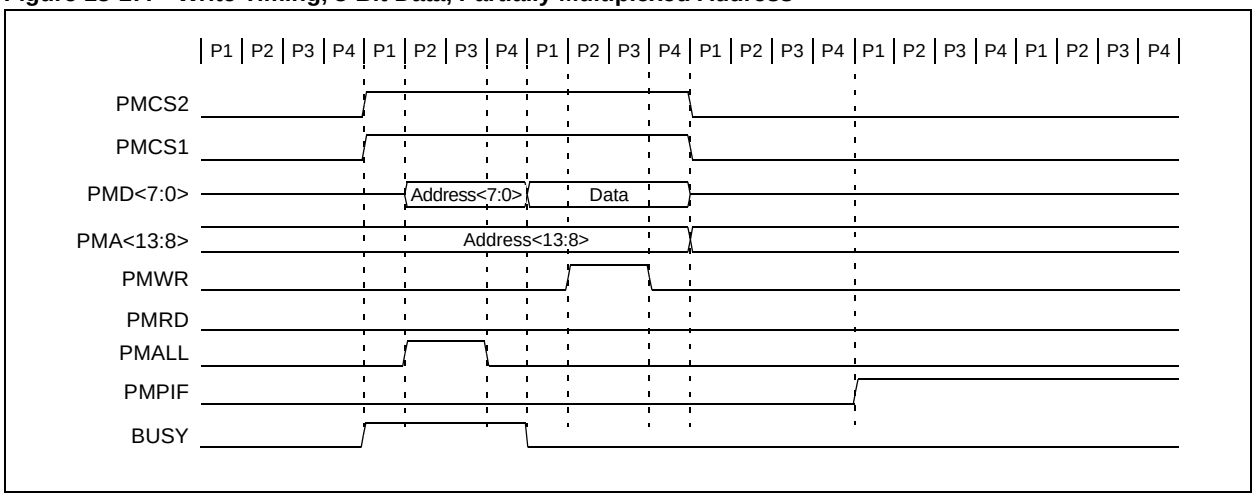


Figure 13-18: Write Timing, 8-Bit Data, Partially Multiplexed Address, Wait States Enabled

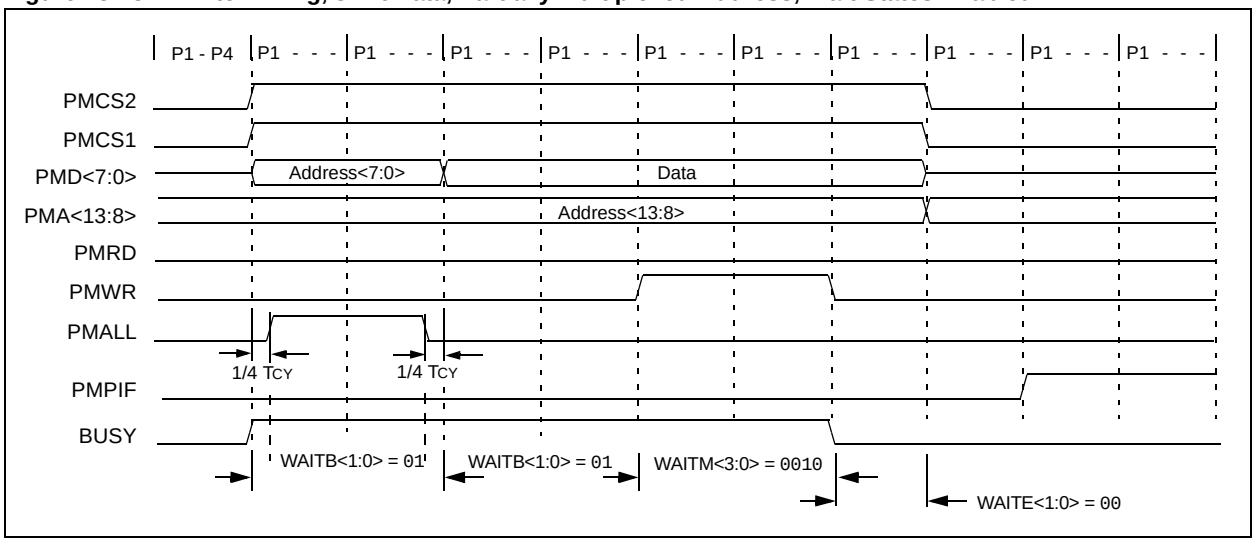


Figure 13-19: Read Timing, 8-Bit Data, Partially Multiplexed Address, Enable Strobe

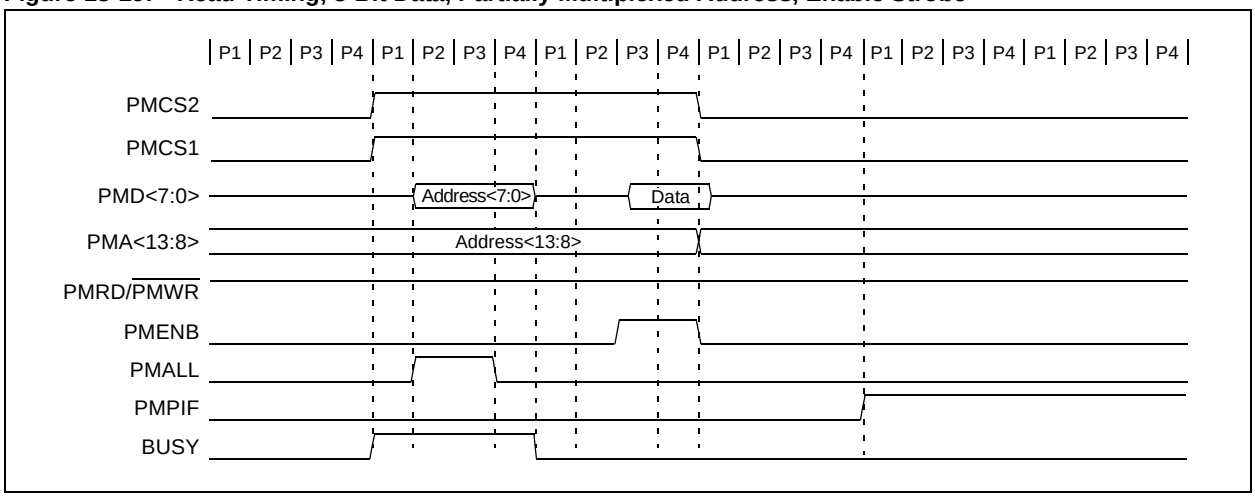


Figure 13-20: Write Timing, 8-Bit Data, Partially Multiplexed Address, Enable Strobe

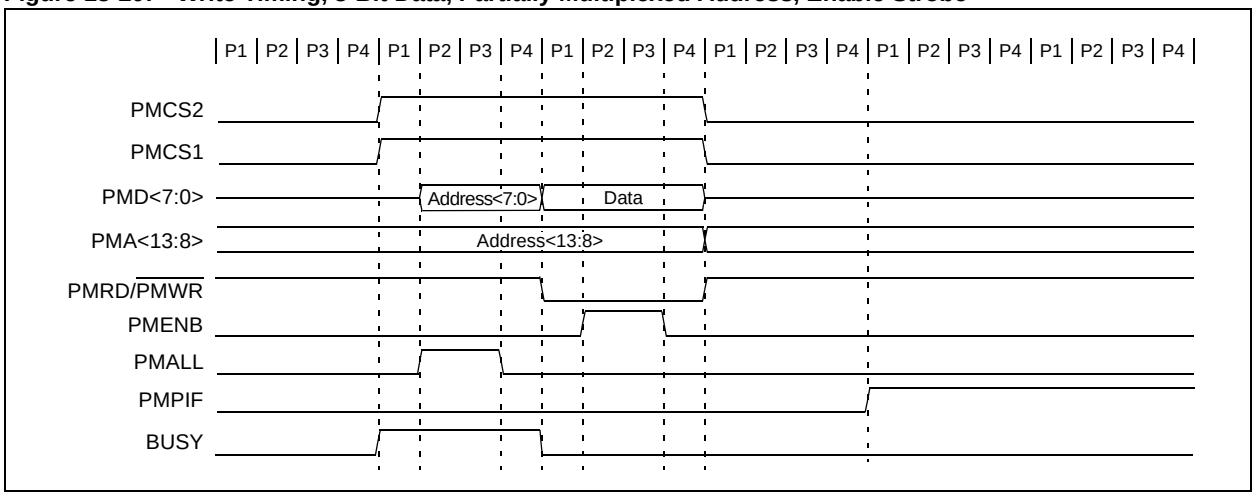


Figure 13-21: Read Timing, 8-Bit Data, Fully Multiplexed 16-Bit Address

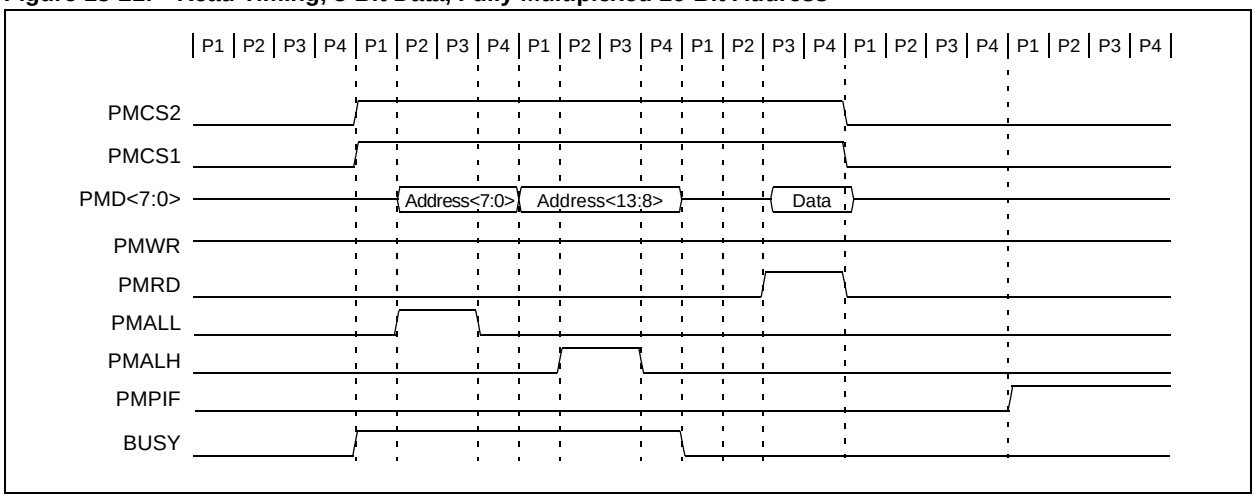


Figure 13-22: Write Timing, 8-Bit Data, Fully Multiplexed 16-Bit Address

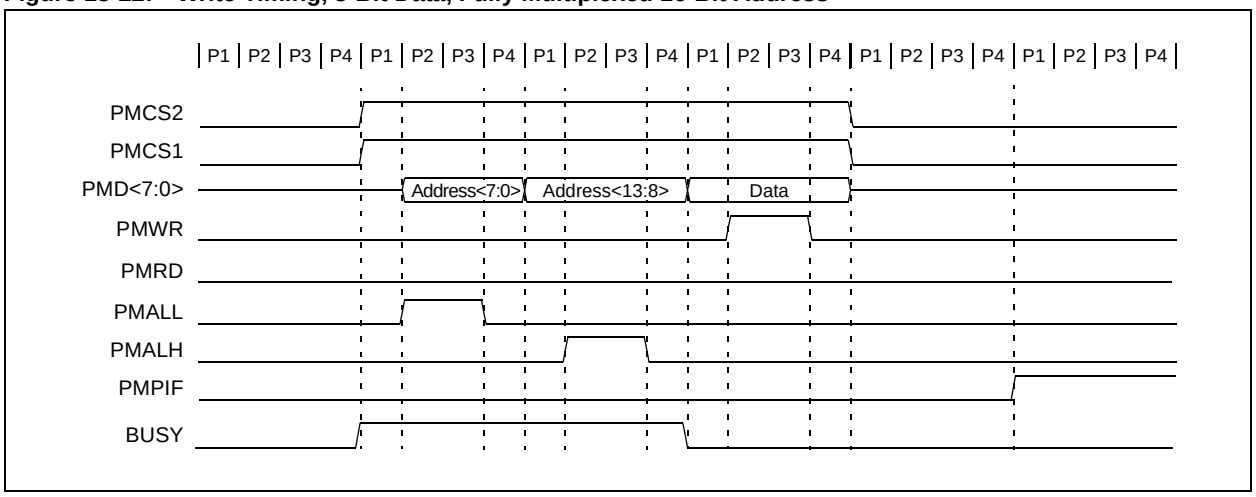


Figure 13-23: Read Timing, 16-Bit Data, Demultiplexed Address

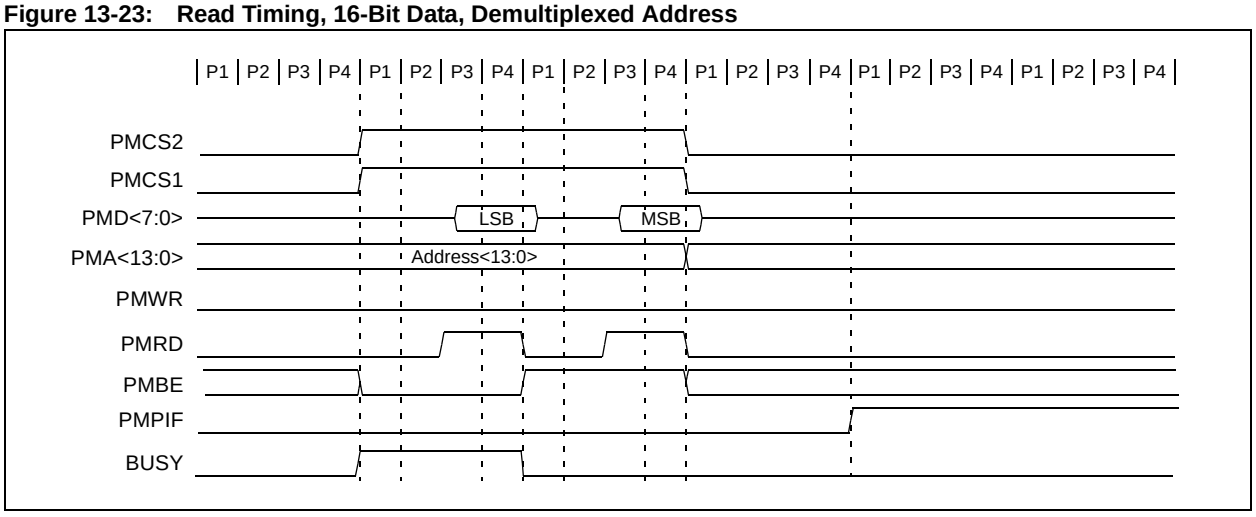


Figure 13-24: Write Timing, 16-Bit Data, Demultiplexed Address

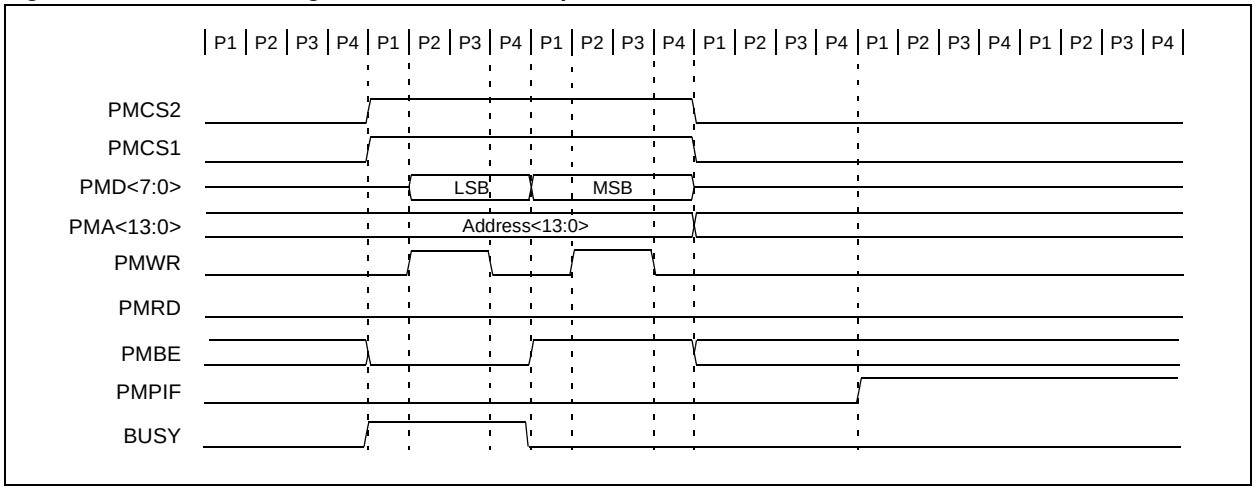


Figure 13-25: Read Timing, 16-Bit Multiplexed Data, Partially Multiplexed Address

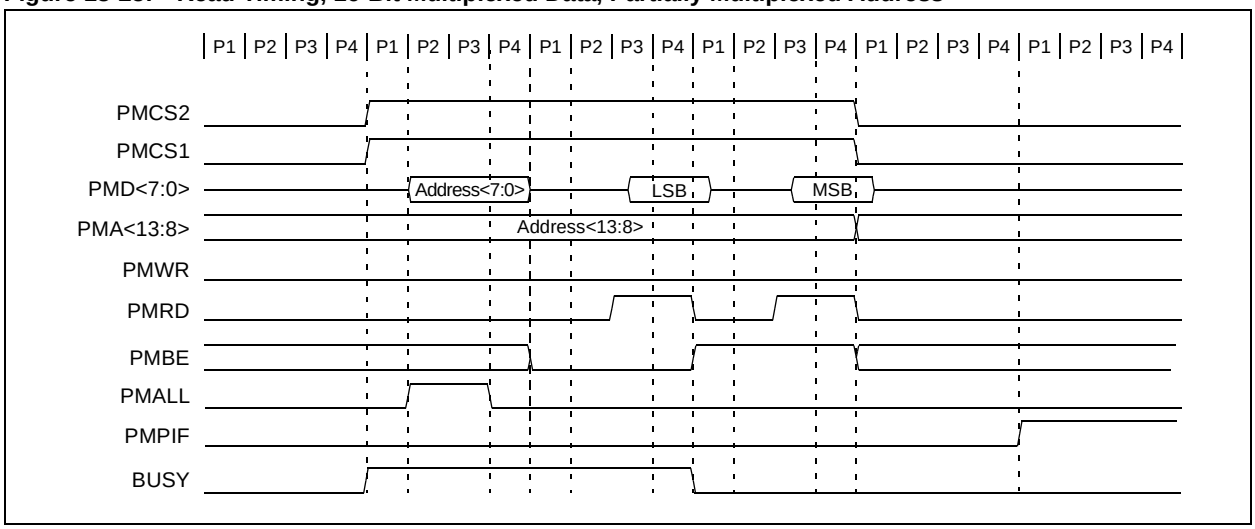


Figure 13-26: Write Timing, 16-Bit Multiplexed Data, Partially Multiplexed Address

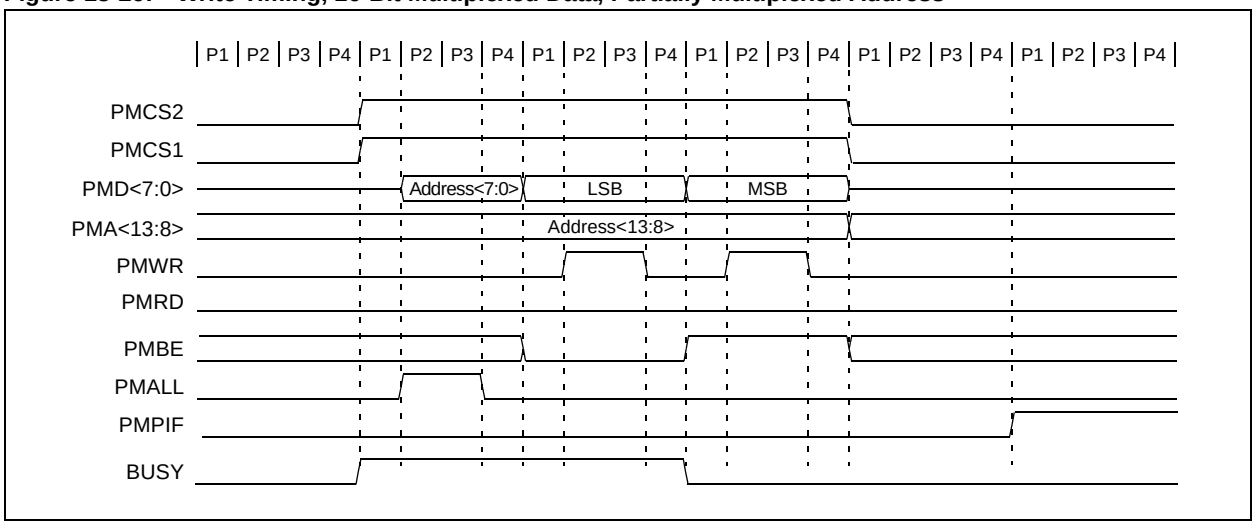


Figure 13-27: Read Timing, 16-Bit Multiplexed Data, Fully Multiplexed 16-Bit Address

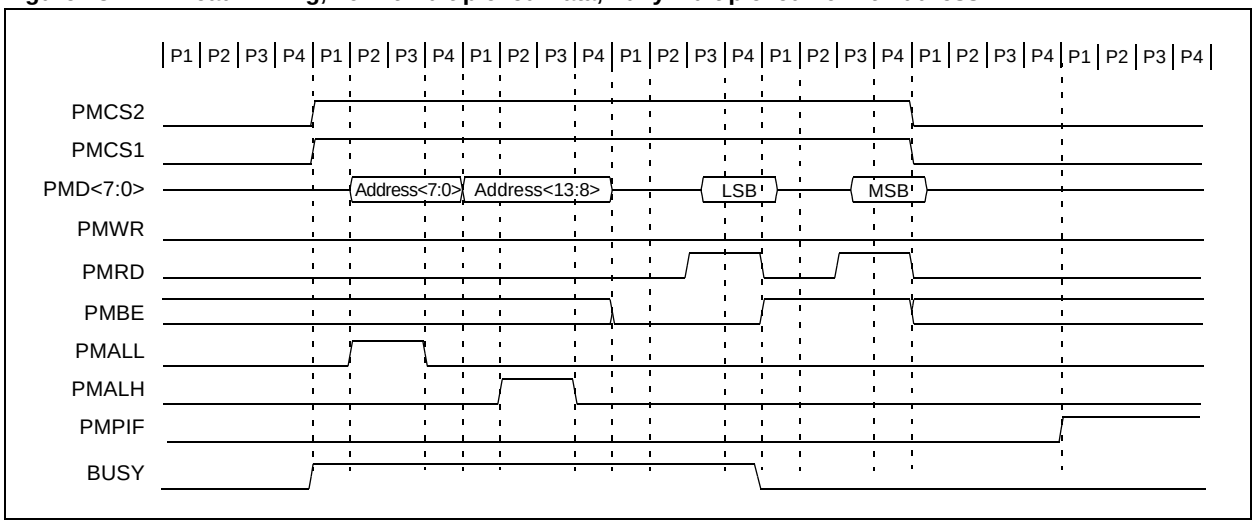
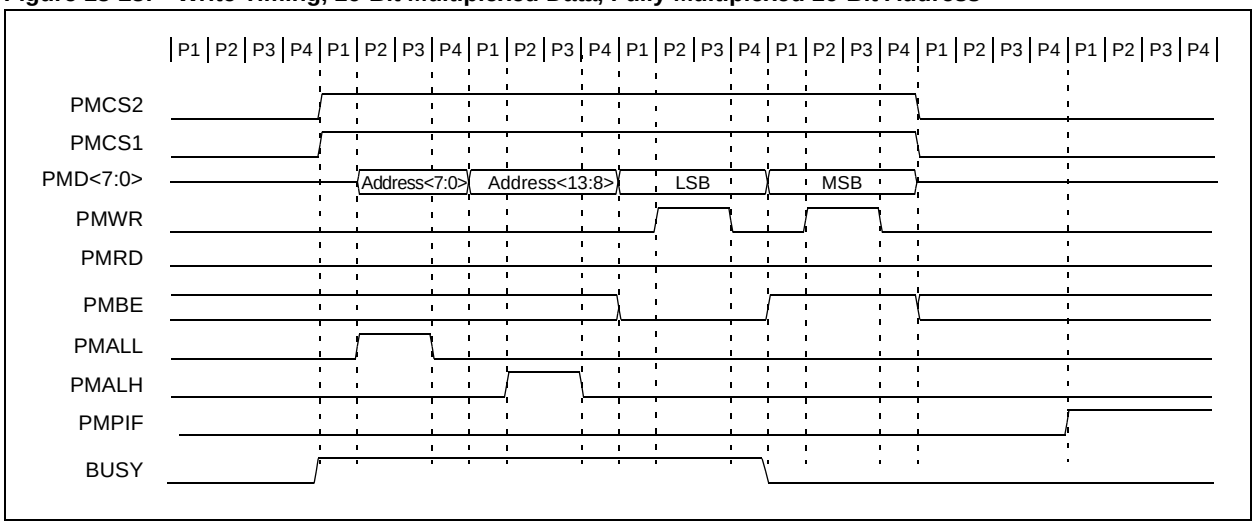


Figure 13-28: Write Timing, 16-Bit Multiplexed Data, Fully Multiplexed 16-Bit Address



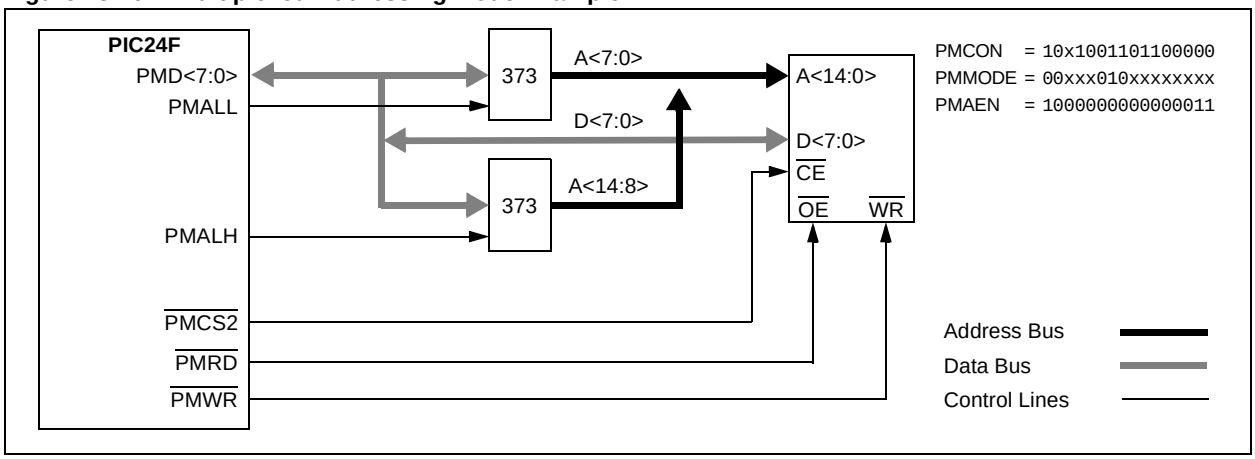
13.5 APPLICATION EXAMPLES

This section introduces some potential applications for the PMP module.

13.5.1 Multiplexed Memory or Peripheral

Figure 13-29 demonstrates the hook up of a memory or another addressable peripheral in Full Multiplex mode. Consequently, this mode achieves the best pin saving from the microcontroller perspective. However, for this configuration, there needs to be some external latches to maintain the address.

Figure 13-29: Multiplexed Addressing Mode Example



13.5.2 Partially Multiplexed Memory or Peripheral

Partial multiplexing implies using more pins; however, for a few extra pins, some extra performance can be achieved. Figure 13-30 shows an example of a memory or peripheral that is partially multiplexed with an external latch. If the peripheral has internal latches, then no extra circuitry is required except for the peripheral itself (as shown in Figure 13-31).

Figure 13-30: Partially Multiplexed Addressing Mode Example

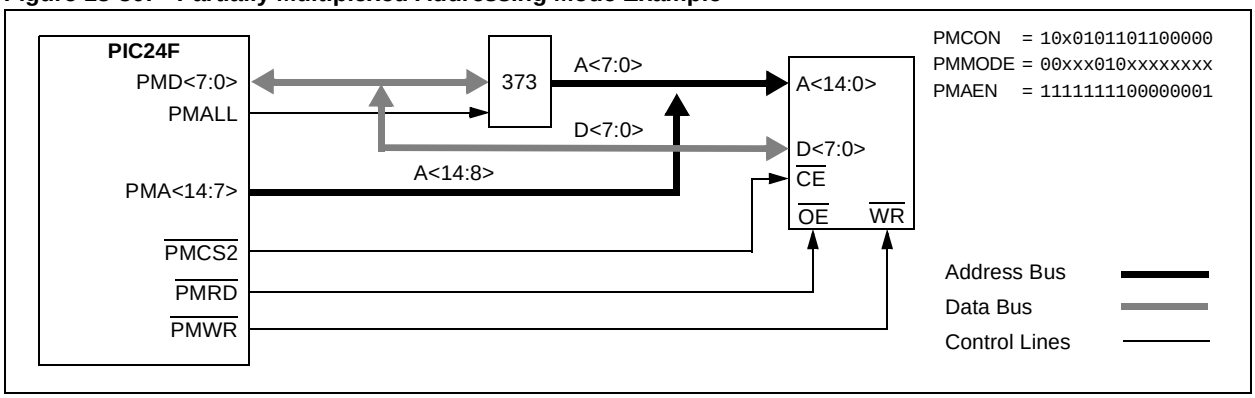
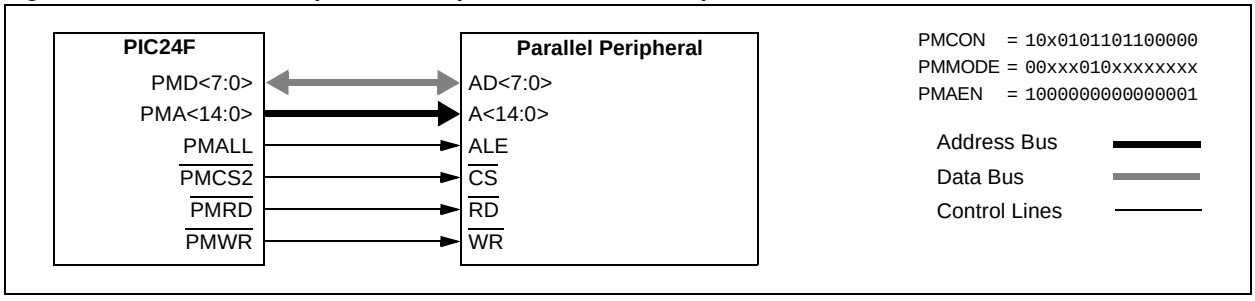


Figure 13-31: Parallel Peripheral Example with 8-Bit Demultiplexed Address and Data



13.5.3 Parallel Flash/EEPROM Examples

Figure 13-32 shows an example of connecting parallel Flash/EEPROM to the PMP. Figure 13-33 shows a slight variation to this, configuring the connection for 16-bit data from a single byte addressable Flash/EEPROM. Figure 13-34 also demonstrates the interface with a 16-bit device but without using byte select logic.

Figure 13-32: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 8-Bit Data

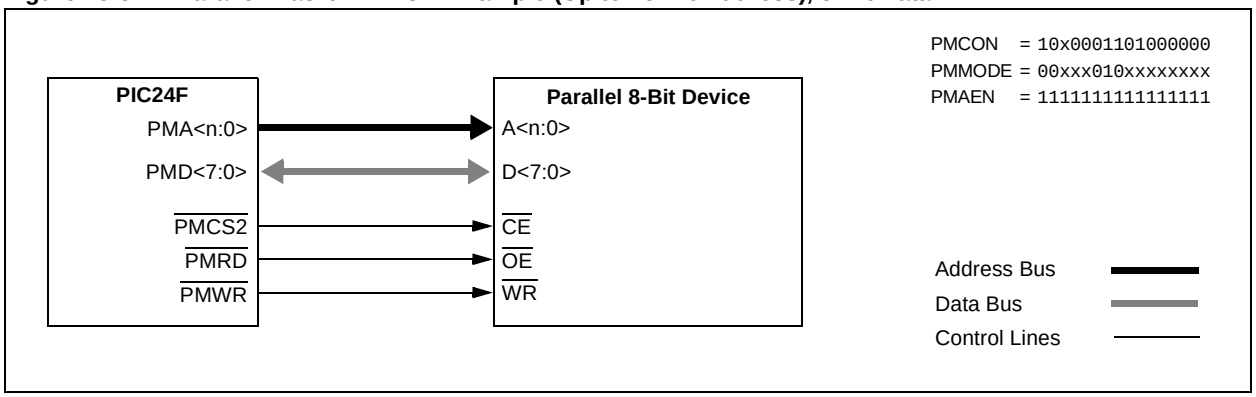


Figure 13-33: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 16-Bit Data (Byte Select Mode)

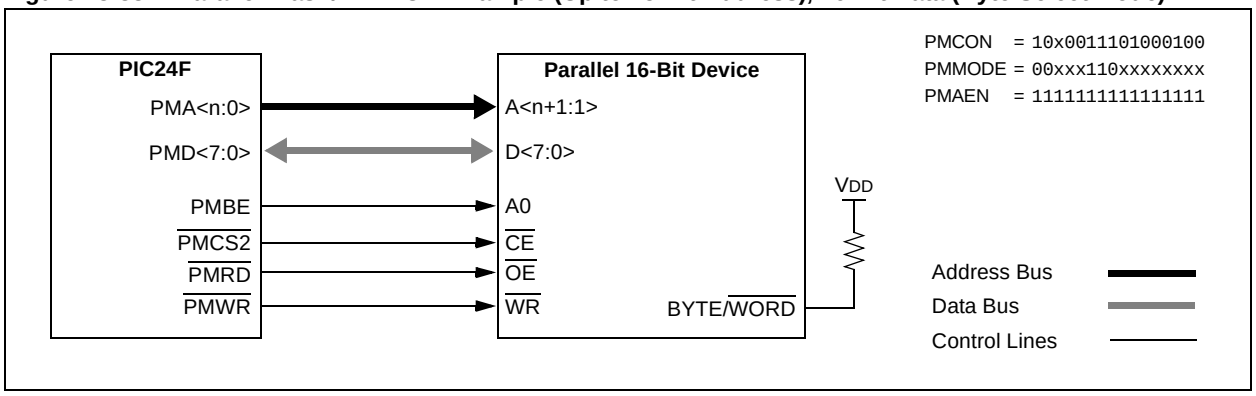
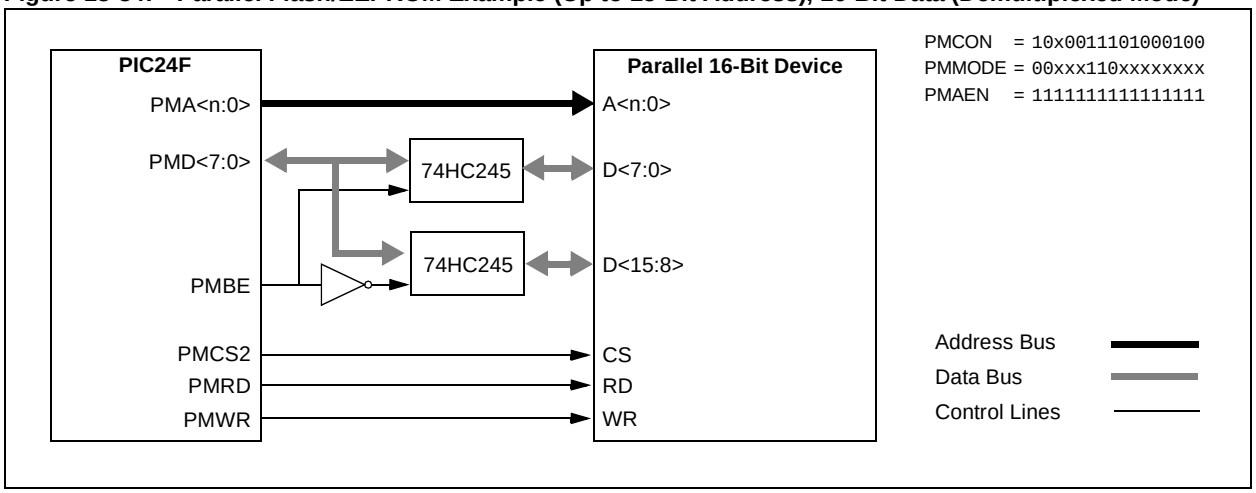


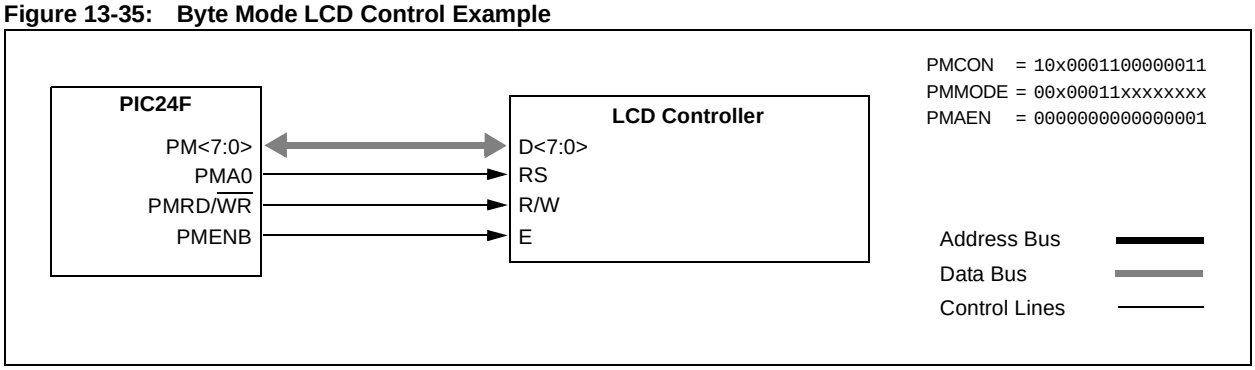
Figure 13-34: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 16-Bit Data (Demultiplexed Mode)



13.5.4 LCD Controller Example

The PMP module can be configured to connect to a typical LCD controller interface, as shown in Figure 13-35. In this case, the PMP module is configured for active-high control signals since common LCD displays require active-high control.

Figure 13-35: Byte Mode LCD Control Example



13.6 OPERATION IN POWER SAVE MODES

The PIC24F family of devices has three power modes: the Normal Operational (Full-Power) mode, and the two Power-Saving modes, invoked by the PWRSAV instruction. Depending on the mode selected, entering a Power-Saving mode may also affect the operation of the module.

13.6.1 Sleep Mode

When the device enters Sleep mode, the system clock is disabled. The consequences of Sleep mode depend on which mode the module is configured in at the time that Sleep mode is invoked.

13.6.1.1 MASTER MODE OPERATION

If the microcontroller enters Sleep mode while the module is operating in Master mode, PMP operation will be suspended in its current state until clock execution resumes. As this may cause unexpected control pin timings, users should avoid invoking Sleep mode when continuous use of the module is needed.

13.6.1.2 SLAVE MODE OPERATION

While the module is inactive, but enabled for any Slave mode operation, any read or write operations occurring at that time will be able to complete without the use of the microcontroller clock. Once the operation is completed, the module will issue an interrupt according to the setting of the IRQMx bits. This interrupt can wake the device from Sleep mode.

13.6.2 Idle Mode

When the device enters Idle mode, the system clock sources remain functional. The PSIDL bit (PMCON<13>) selects whether the module will stop or continue functioning on Idle. If PSIDL = 1, the module will behave the same way as it does in Sleep mode (i.e., slave reception is still possible even though the module clocks are not available and Master mode is suspended).

If PSIDL = 0 (default), the module will continue operation in Idle mode. The current transaction in both Master and Slave modes will complete and issue an interrupt.

13.7 AC ELECTRICAL SPECIFICATIONS

Figure 13-36: Parallel Slave Port Timing

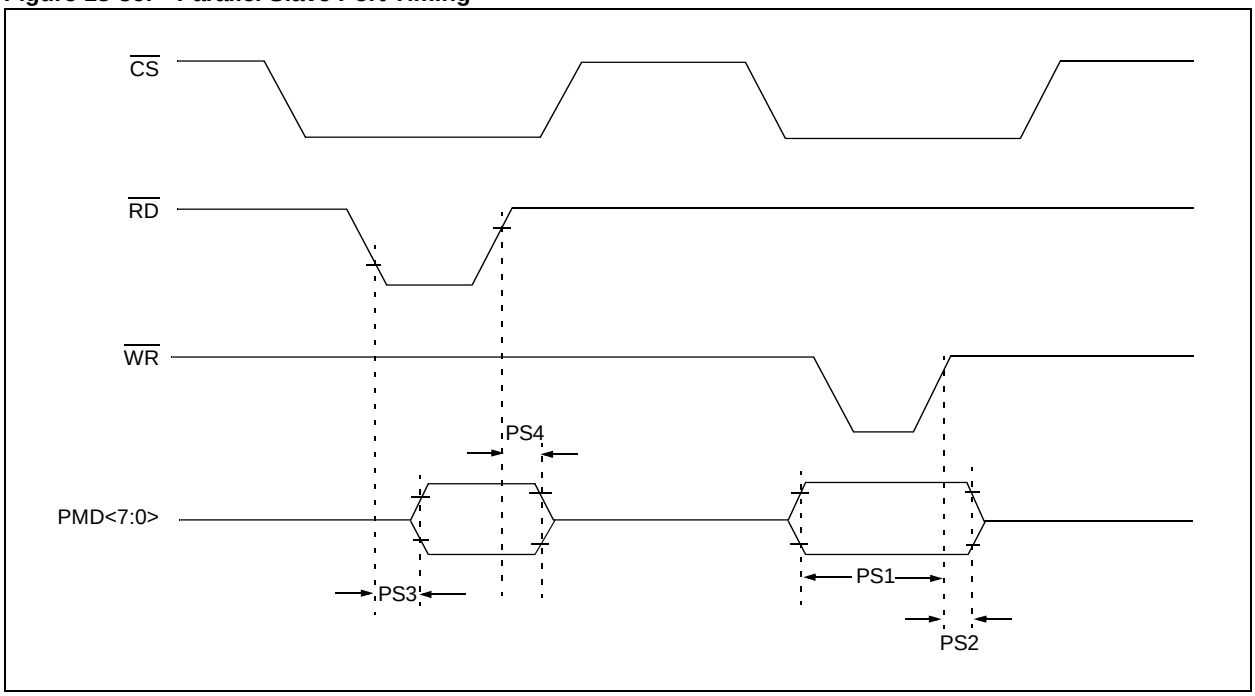


Table 13-4: Parallel Slave Port Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data–In Invalid (hold time)	20	—	—	ns	
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data–Out Valid	—	—	80	ns	
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data–Out Invalid	10	—	30	ns	

Figure 13-37: Parallel Master Port Read Timing Diagram

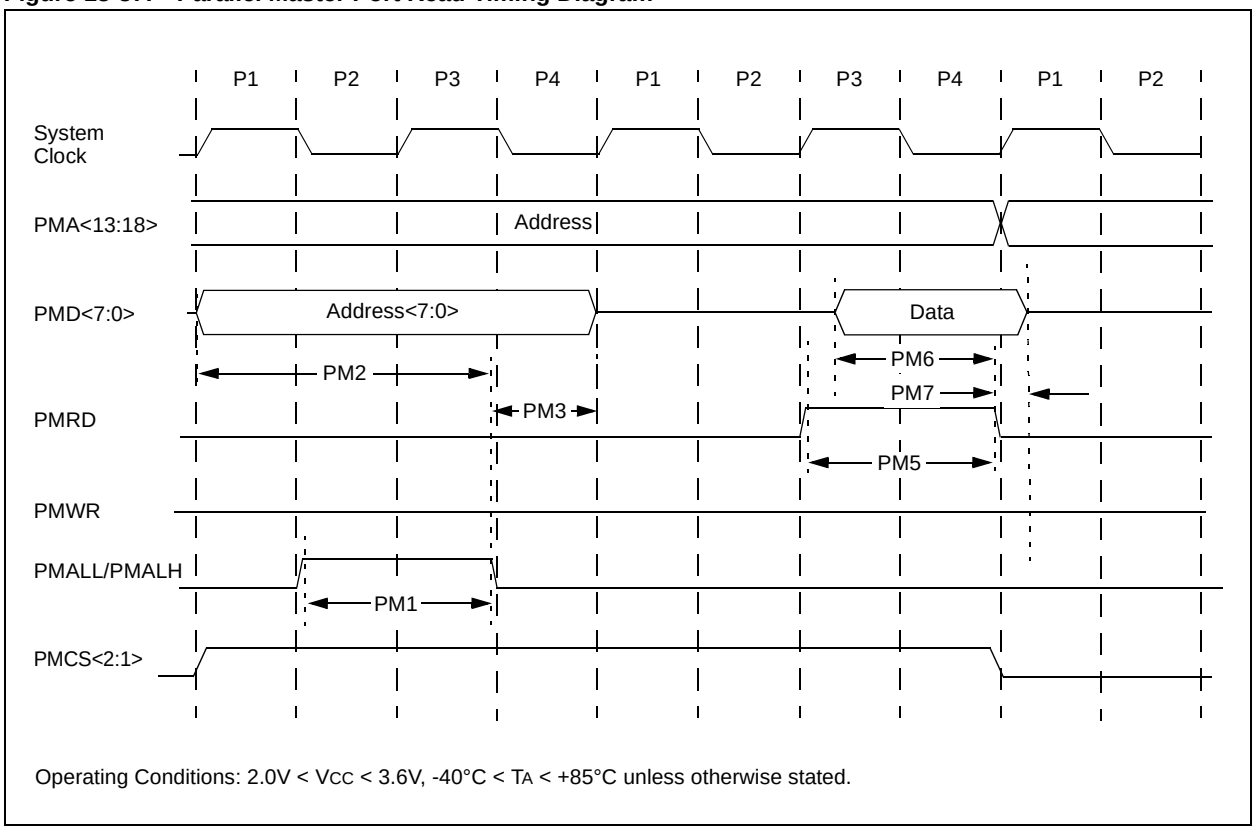


Table 13-5: Parallel Master Port Read Timing Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No	**Symbol**	**Characteristics(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
PM1		PMALL/PMALH Pulse Width	—	0.5 TCY	—	ns	
PM2		Address Out Valid to PMALL/PMALH Invalid (address setup time)(2)	—	0.75 TCY	—	ns	
PM3		PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	0.25 TCY	—	ns	
PM5		PMRD Pulse Width	—	0.5 TCY	—	ns	
PM6		Data In to PMRD or PMENB Inactive state	150	—	—	ns	
PM7		PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	5	ns	

Note 1: Wait states disabled for all cases.

2: The setup time for the LSB and the MSB of the address are not the same; the setup time for the LSB is 0.5 TCY and for the MSB is 0.75 TCY.

Figure 13-38: Parallel Master Port Write Timing Diagram

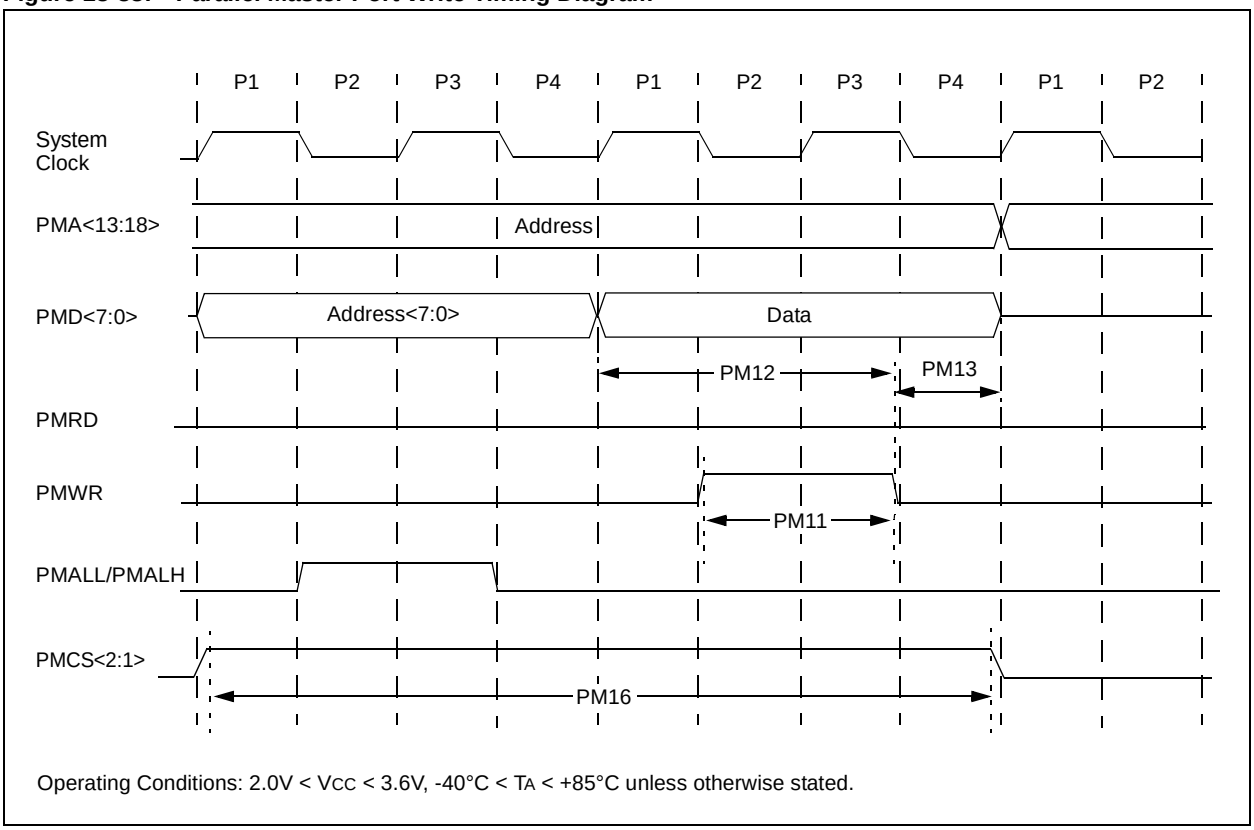


Table 13-6: Parallel Master Port Write Timing Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No	**Symbol**	**Characteristics(1)**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
PM11		PMWR Pulse Width	—	0.5 TCY	—	ns	
PM12		Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	0.75 TCY	—	ns	
PM13		PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	0.25 TCY	—	ns	
PM16		PMCSx Pulse Width	TCY – 5	—	—	ns	

Note 1: Wait states disabled for all cases.

13.8 REGISTER MAPS

A summary of the registers associated with the PMP module is provided in Table 13-7.

Table 13-7: Parallel Master/Slave Port Register Map(1)

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP	0000
PMMODE	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000
PMADDR(2)	CS2	CS1	Parallel Port Address (ADDR<13:0>)														0000
PMAEN	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMSTAT	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008Fh
PMDIN1	Parallel Port Data In Register 1 (Buffers Level 0 and 1)																0000
PMDIN2	Parallel Port Data In Register 2 (Buffers Level 2 and 3)																0000
PMDOUT1(2)	Parallel Port Data Out Register 1 (Buffers Level 0 and 1)																0000
PMDOUT2	Parallel Port Data Out Register 2 (Buffers Level 2 and 3)																0000
PADCFG1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSECSEL	PMPTTL	0000
PMD3	—	—	—	—	—	CMPMD	RTCCMD	PMPMD	CRCPMD	—	—	—	—	—	I2CMD	—	0000

Legend: – = unimplemented, read as '0'. Shaded bits are not used in the operation of the Parallel Master Port module.

Note 1: Refer to the product device data sheet for specific Core register map details.

2: PMADDR and PMDOUT1 are the same physical register, but are defined differently depending on the module's operating mode.

13.9 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Parallel Master Port (PMP) module are:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

13.10 REVISION HISTORY

Revision A (September 2006)

This is the initial released revision of this document.

Revision B (May 2008)

Updated Wait state operation in **Section 13.4.1.8 “Wait States”**; added **Section 13.4.1.9 “Pin Functions Based on Operating Mode”** and Table 13-2 and Table 13-3 to clarify Master mode pin functions; updated and added timing diagrams in **Section 13.4.5 “Master Mode Timing”**; updated electrical specifications in **Section 13.7 “AC Electrical Specifications”**; other minor typographical corrections throughout.

