Section 12. I/O Ports

HIGHLIGHTS

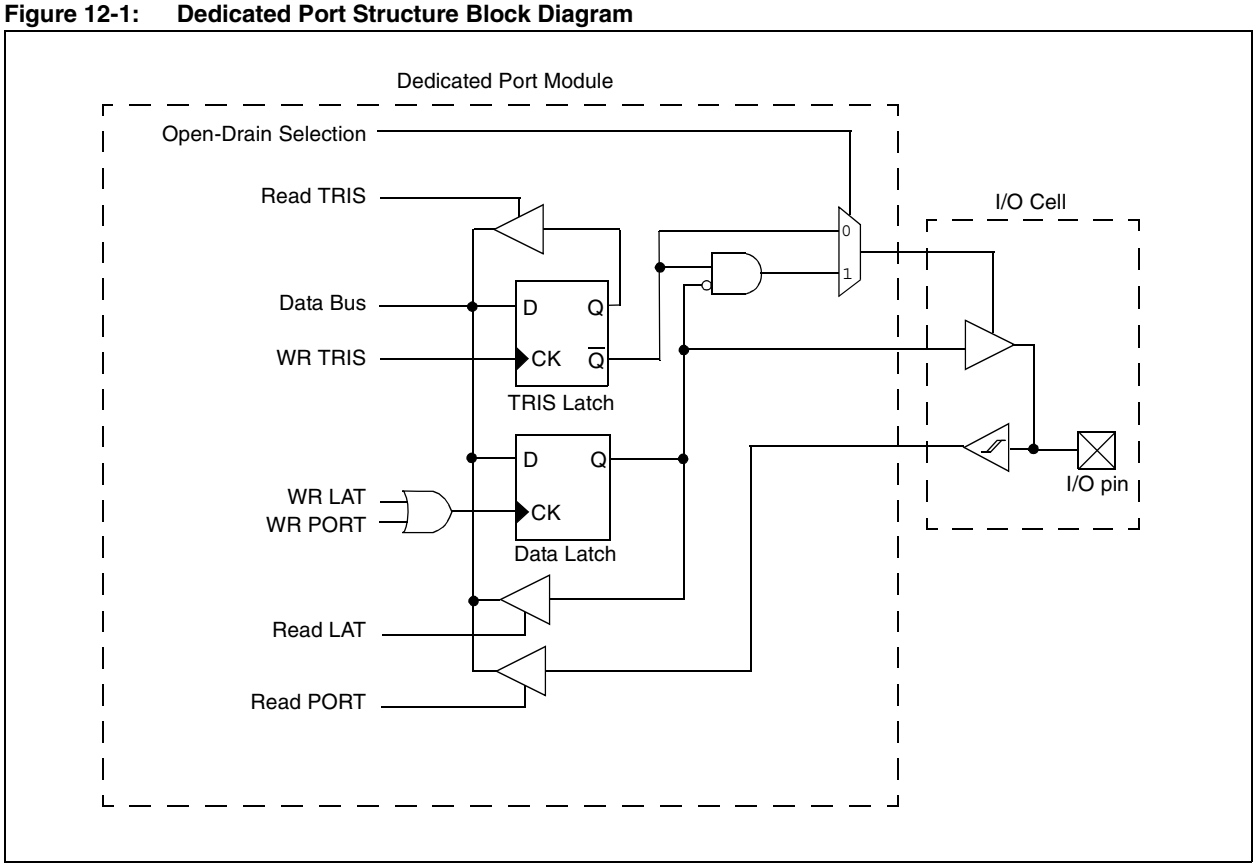
This section of the manual contains the following topics:

12.1 INTRODUCTION

The general purpose I/O pins can be considered the simplest of peripherals. They allow the PICmicro® MCU to monitor and control other devices. To add flexibility and functionality to a device, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Figure 12-1 shows a block diagram of a typical I/O port. This block diagram does not take into account peripheral functions that may be multiplexed onto the I/O pin.

Figure 12-1: Dedicated Port Structure Block Diagram



12.2 I/O PORT CONTROL REGISTERS

All I/O ports have four registers directly associated with the operation of the port, where 'x' is a letter that denotes the particular I/O port:

- TRISx: Data Direction register
- PORTx: I/O Port register
- LATx: I/O Latch register
- ODCx: I/O Open-Drain Control register

Each I/O pin on the device has an associated bit in the TRIS, PORT, LAT and ODC registers.

Note:	The total number of ports and available I/O pins will depend on the device variant. In a given device, all of the bits in a port control register may not be implemented. Refer to the specific device data sheet for further details.

12.2.1 TRIS Registers

The TRISx register control bits determine whether each pin associated with the I/O port is an input or an output. If the TRIS bit for an I/O pin is a '1', then the pin is an input. If the TRIS bit for an I/O pin is a '0', then the pin is configured for an output. An easy way to remember this is that a '1' looks like an I (input) and a '0' looks like an O (output). All port pins are defined as inputs after a Reset.

12.2.2 PORT Registers

Data on an I/O pin is accessed via a PORTx register. A read of the PORTx register reads the value of the I/O pin, while a write to the PORTx register writes the value to the port data latch.

Many instructions, such as BSET and BCLR, are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch. Care should be taken when read-modify-write commands are used on the PORTx registers when some I/O pins associated with the port are configured as inputs. If an I/O pin configured as an input is changed to an output, at some later time, an unexpected value may be output on the I/O pin. This effect occurs because the read-modify-write instruction reads the instantaneous value on the input pin and loads that value into the port data latch.

12.2.3 LAT Registers

The LATx register associated with an I/O pin eliminates the problems that could occur with read-modify-write instructions. A read of the LATx register returns the values held in the port output latches instead of the values on the I/O pins. A read-modify-write operation on the LAT register, associated with an I/O port, avoids the possibility of writing the input pin values into the port latches. A write to the LATx register has the same effect as a write to the PORTx register.

The differences between the PORT and LAT registers can be summarized as follows:

- A write to the PORTx register writes the data value to the port latch.
- A write to the LATx register writes the data value to the port latch.
- A read of the PORTx register reads the data value on the I/O pin.
- A read of the LATx register reads the data value held in the port latch.

Any bit and its associated data and control registers that is not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin, will read as zeros.

12.2.4 ODC Registers

Each I/O pin can be individually configured for either normal digital output or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each I/O pin. If the ODC bit for an I/O pin is a '1', then the pin acts as an open-drain output. If the ODC bit for an I/O pin is a '0', then the pin is configured for a normal digital output (ODC bit is valid only for output pins). After a Reset, the status of all the bits of the ODCx register is set to '0'.

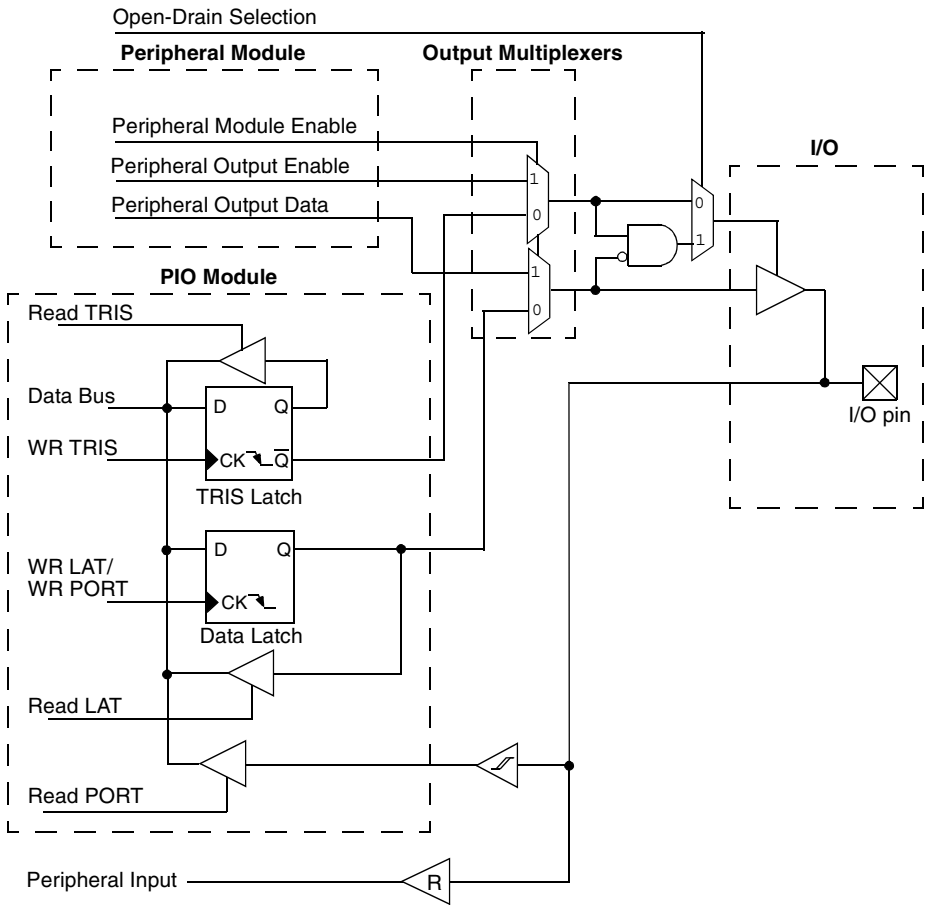
The open-drain feature allows the generation of outputs higher than V_{DD} on any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification. The ODC register setting takes effect in all the I/O modes, allowing the output to behave as an open-drain even if a peripheral is controlling the pin. Although the user could achieve the same effect by manipulating the corresponding LAT and TRIS bits, this procedure will not allow the peripheral to operate in Open-Drain mode (except for the default operation of the I^2C™ pins). Since I^2C pins are already open-drain pins, the ODCx settings do not affect the I^2C pins. Also, the ODCx settings do not affect the JTAG output characteristics as the JTAG scan cells are inserted between the ODCx logic and the I/O.

12.3 PERIPHERAL MULTIPLEXING

Pins can also be configured as digital inputs or outputs, and analog inputs or outputs. When configured as digital inputs, they are either TTL buffers or Schmitt Triggers. When configured as digital outputs, they are either CMOS drivers or open-drain outputs.

Many pins also support one or more peripheral modules. When configured to operate with a peripheral, a pin may not be used for general input or output. In many cases, a pin must still be configured for input or output, although some peripherals override the TRIS configuration. Figure 12-2 shows how ports are shared with other peripherals, and the associated I/O pin to which they are connected. For some PIC24F devices, multiple peripheral functions may be multiplexed on each I/O pin. The priority of the peripheral function depends on the order of the pin description in the pin diagram of the specific product data sheet.

Figure 12-2: Shared Port Structure Block Diagram



Legend: R = Input buffer type depends on the peripheral. For more information, refer to the specific product data sheet.

12.3.1 Multiplexing Digital Input Peripheral

- Peripheral does not control the TRISx register.
- PORTx register can read pin value.
- PORTx data input path is unaffected.
- Peripheral input path is independent of IO input path with a special input buffer.

12.3.2 Multiplexing Digital Output Peripheral

- Peripheral controls output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type is selected by peripheral (e.g., drive strength, slow rate, etc.).
- User needs to configure the pin as an output by clearing the associated TRISx bit.
- If an output has an automatic tri-state feature (e.g., PWM outputs), the peripheral has the ability to tri-state the pin.

12.3.3 Multiplexing Digital Bidirectional Peripheral

- Peripheral can automatically configure the pin as an output but not as an input. User needs to configure the pin as an input by setting the associated TRISx bit.
- Peripherals control output data and PORTx register has no effect.
- PORTx register can read pin value.
- Pad output driver type could be affected by peripheral (e.g., drive strength, slow rate, etc.).

12.3.4 Multiplexing Analog Input Peripheral

- All digital port input buffers are disabled and PORTx registers read '0' to prevent crowbar current.

12.3.5 Multiplexing Analog Output Peripheral

- All digital port input buffers are disabled and PORTx registers read '0' to prevent crowbar current.
- Analog output is driven onto the pin independent of the associated TRISx setting.

Note:	In order to use pins multiplexed with the A/D for digital I/O, the corresponding bits in the AD1PCFG register must be set to '1', even if the A/D module is turned off.

12.3.6 Software Input Pin Control

Some of the functions assigned to an I/O pin may be input functions that do not take control of the pin output driver. An example of one such peripheral is the input capture module. If the I/O pin associated with the input capture is configured as an output, using the appropriate TRIS control bit, the user can manually affect the state of the input capture pin through its corresponding PORT register. This behavior can be useful in some situations, especially for testing purposes, when no external signal is connected to the input pin.

Referring to Figure 12-2, the organization of the peripheral multiplexers will determine if the peripheral input pin can be manipulated in software using the PORT register. The conceptual peripherals shown in this figure disconnect the PORT data from the I/O pin when the peripheral function is enabled.

In general, the following peripherals allow their input pins to be controlled manually through the PORT registers:

- External Interrupt pins
- Timer Clock Input pins
- Input Capture pins
- PWM Fault pins

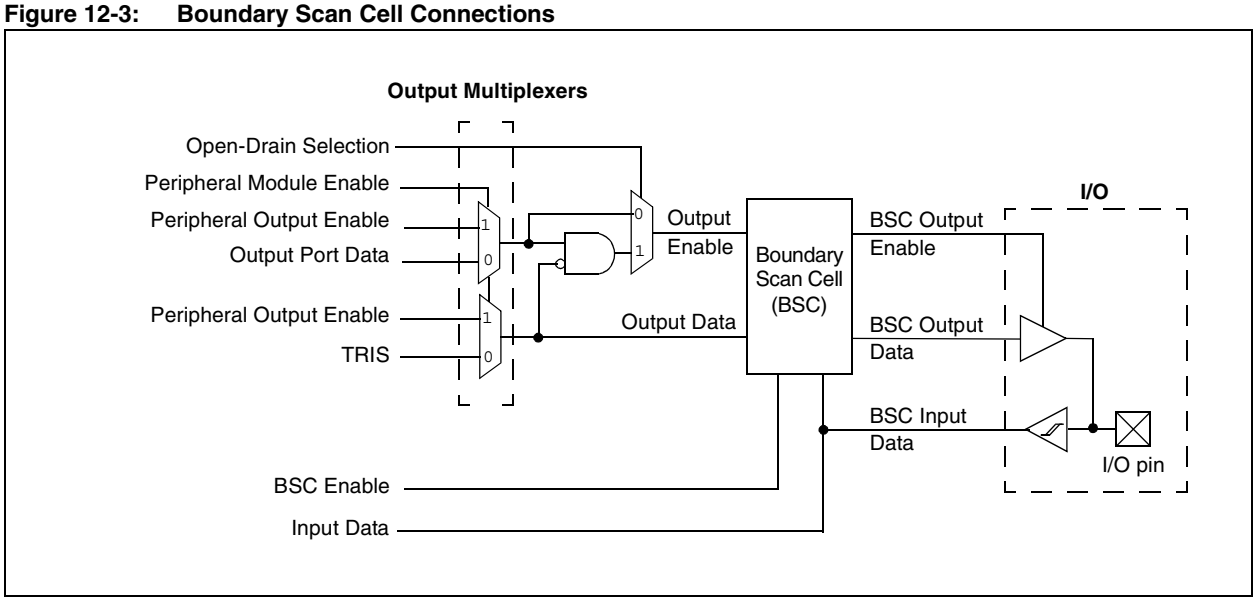
Most serial communication peripherals, when enabled, take full control of the I/O pin so that the input pins associated with the peripheral cannot be affected through the corresponding PORT registers. These peripherals include the following:

- SPI
- I^2C™
- DCI
- UART
- CAN

12.4 BOUNDARY SCAN CELL CONNECTIONS

The PIC24F device supports JTAG boundary scan. A Boundary Scan Cell (BSC) is inserted between the internal I/O logic circuit and the I/O pin, as shown in Figure 12-3. All the I/O pads have boundary scan cells. For normal I/O operation, the BSC is disabled and hence bypassed: The output enable input of the BSC is directly connected to the BSC output enable and the output data input of the BSC is directly connected to the BSC output data. The pads that do not have Boundary Scan Cells are the power supply pads (VDD, VSS and VCAP/VDDCORE) and the JTAG pads (TCK, TDI, TDO and TMS).

Figure 12-3: Boundary Scan Cell Connections



12.5 PORT DESCRIPTIONS

Refer to the specific device data sheet for a description of the available I/O ports and peripheral multiplexing details.

12.6 CHANGE NOTIFICATION (CN) PINS

The Change Notification (CN) pins provide PIC24F devices the ability to generate interrupt requests to the processor in response to a change of state on selected input pins. Up to 24 input pins may be selected (enabled) for generating CN interrupts. The total number of available CN inputs is dependent on the selected PIC24F device. Refer to the specific device data sheet for further details.

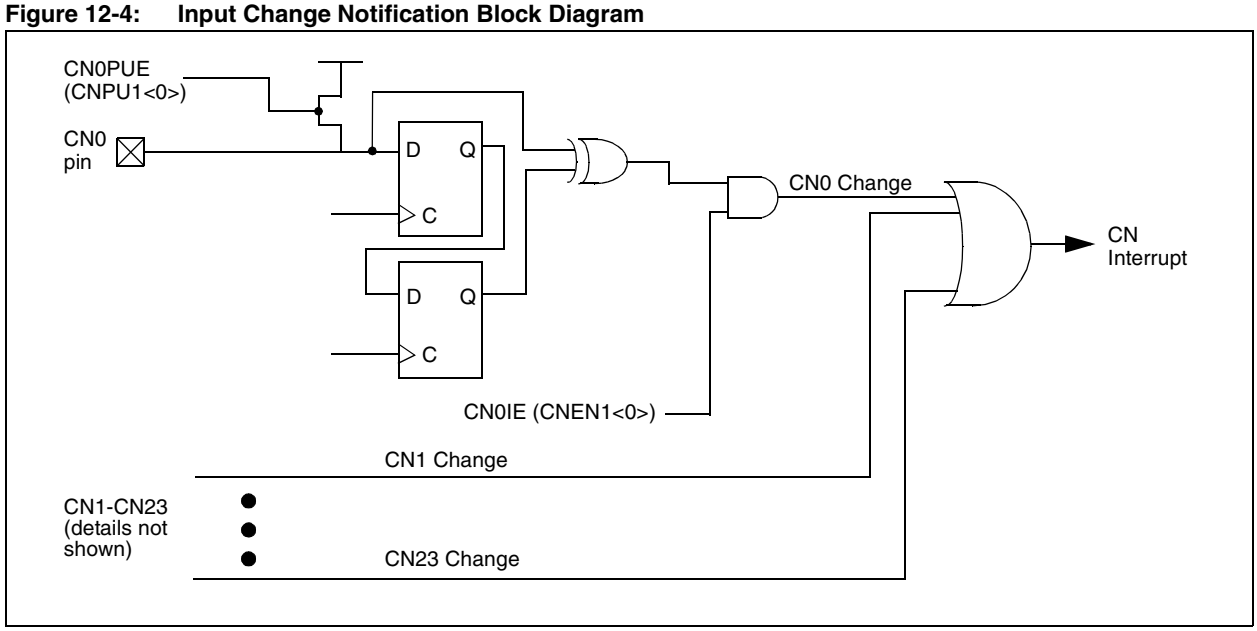
Figure 12-4 shows the basic function of the CN hardware.

12.6.1 CN Control Registers

There are four control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the CNxIE control bits, where 'x' denotes the number of the CN input pin. The CNxIE bit must be set for a CN input pin to interrupt the CPU.

The CNPU1 and CNPU2 registers contain the CNxPUE control bits. Each CN pin has a weak pull-up device connected to the pin which can be enabled or disabled using the CNxPUE control bits. The weak pull-up devices act as a current source that is connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for CN pull-up device current specifications.

Figure 12-4: Input Change Notification Block Diagram



12.6.2 CN Configuration and Operation

The CN pins are configured as follows:

1. Ensure that the CN pin is configured as a digital input by setting the associated bit in the TRISx register.
2. Enable interrupts for the selected CN pins by setting the appropriate bits in the CNEN1 and CNEN2 registers.
3. Turn on the weak pull-up devices (if desired) for the selected CN pins by setting the appropriate bits in the CNPU1 and CNPU2 registers.
4. Clear the CNIF (IFS1<3>) interrupt flag.
5. Select the desired interrupt priority for CN interrupts using the CNIP<2:0> control bits (IPC4<14:12>).
6. Enable CN interrupts using the CNIE (IEC1<3>) control bit.

When a CN interrupt occurs, the user should read the PORT register associated with the CN pin(s). This will clear the mismatch condition and set up the CN logic to detect the next pin change. The current PORT value can be compared to the PORT read value obtained at the last CN interrupt to determine the pin that changed.

The CN pins have a minimum input pulse-width specification. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for further details.

12.6.3 CN Operation in Sleep and Idle Modes

The CN module continues to operate during Sleep or Idle mode. If one of the enabled CN pins changes states, the CNIF (IFS1<3>) status bit will be set. If the CNIE bit (IEC1<3>) is set, the device will wake from Sleep or Idle mode and resume operation.

If the assigned priority level of the CN interrupt is equal to, or less than, the current CPU priority level, device execution will continue from the instruction immediately following the `SLEEP` or `IDLE` instruction.

If the assigned priority level of the CN interrupt is greater than the current CPU priority level, device execution will continue from the CN interrupt vector address.

Register 12-1: CNEN1: Input Change Notification Interrupt Enable Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNxIE:** Input Change Notification Interrupt Enable bits
1 = Enable interrupt on input change
0 = Disable interrupt on input change

Register 12-2: CNEN2: Input Change Notification Interrupt Enable Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **CNxIE:** Input Change Notification Interrupt Enable bits
1 = Enable interrupt on input change
0 = Disable interrupt on input change

Register 12-3: CNPU1: Input Change Notification Pull-up Enable Register 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNxPUE:** Input Change Notification Pull-up Enable bits
1 = Enable pull-up on input change
0 = Disable pull-up on input change

Register 12-4: CNPU2: Input Change Notification Pull-up Enable Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **CNxPUE:** Input Change Notification Pull-up Enable bits
1 = Enable pull-up on input change
0 = Disable pull-up on input change

12.7 REGISTER MAPS

A summary of the registers associated with the PIC24F I/O ports is provided in Table 12-1 and Table 12-2.

Table 12-1: Special Function Registers Associated with I/O Ports

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISx	PORTx Data Direction Control Register																FFFF
LATx	PORTx Data Latch Register																xxxx
PORTx	Rx15	Rx14	Rx13	Rx12	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0	xxxx
ODCx	PORTx Open-Drain Control Register																0000

Note 1: Refer to the specific device data sheet for I/O Ports register map details.

Table 12-2: Special Function Registers Associated with Change Notification Pins

Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	CN15IE	CN14IE	CN13IE	CN12IE	CN11IE	CN10IE	CN9IE	CN8IE	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	—	—	—	—	—	—	—	—	CN23IE	CN22IE	CN21IE	CN20IE	CN19IE	CN18IE	CN17IE	CN16IE	0000
CNPU1	CN15PUE	CN14PUE	CN13PUE	CN12PUE	CN11PUE	CN10PUE	CN9PUE	CN8PUE	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	—	—	—	—	—	—	—	—	CN23PUE	CN22PUE	CN21PUE	CN20PUE	CN19PUE	CN18PUE	CN17PUE	CN16PUE	0000

Legend: — = unimplemented, read as '0'.
Note: Refer to the specific device data sheet for I/O Ports register map details.

12.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the I/O Ports are:

Title	Application Note #
Implementing Wake-up on Key Stroke	AN552

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

12.9 REVISION HISTORY

Revision A (August 2006)

This is the initial released revision of this document.

NOTES:

